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DN 6000365-B

TECHNICAL MANUAL
MODEL 501V-20 SERIES
BIT SYNCHRONIZER

Acroamatics, Inc.
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May 2, 2006

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TECHNICAL MANUAL
MODEL 501V-20 SERIES
BIT SYNCHRONIZER

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TECHNICAL MANUAL
MODEL 501V-20 SERIES
BIT SYNCHRONIZER

SECTION 1
INTRODUCTION

1.1 DESCRIPTION

The Model 501V-20 series PCM Bit Synchronizer (BSYN) is a stand-alone, VME-compatible, 6U card that synchronizes to and recovers data from PCM input signals. The card contains five selectable input sources, AGC and DC restoration circuitry, and programmable filtering for optimum data recovery. Sophisticated phase-lock-loop (PLL) circuitry synchronizes a clock to the incoming signal to extract digital data from the PCM input. This circuitry produces NRZ-L Data and Clock outputs for use by a PCM format decommutator or similar equipment. The programmability of both the PLL and the input filters allows you to optimize bit synchronizer performance in high-noise environments. The PLL circuitry synchronizes to the data transitions of the incoming signal. The programmable loopwidth of the PLL enables the bit synchronizer to quickly acquire and maintain synchronization on signals contaminated by random noise, DC offsets, or amplitude/frequency modulation. The BSYN is tunable from 8bps to 20Mbps (NRZ codes) and provides encoded PCM output for analog tape recording. The unit also provides a soft bit decision output of four bits, and is optionally capable of decoding rate 1/2 convolutionally encoded data. The on-card processor provides status of input amplitude, offset, and synchronization to the VME Host interface.

1.2 ENHANCEMENTS

The 501V-20 series BSYN features an upgradable logic module with an optional data source selector (DSS), as well as a built-in bit error rate test (BERT) option. The logic module is reprogrammable and replaceable in the field without any special tools, thus minimizing down time when an upgrade becomes necessary. These unique capabilities allow you to have the module reprogrammed to respond quickly to evolving application requirements such as:

a) Recovering data from newly defined or application specific coding schemes;

b) Monitoring data streams for frame synchronization to resolve ambiguities or polarity inversions typical with many modulation schemes;

c) Creating canned formats for recovering data from concatenated or layered codes.

The BERT option includes a pseudo-random number (PN) pattern generator with forced error injection, an auto-correlating pattern synchronizer, and a bit error counter with a programmable length sample period. This allows basic BER probability data to be compiled without requiring an external link analyzer.

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1.3 OPTIONAL FEATURES

The following options are available on the 501V-20 series Bit Synchronizer. All options include the basic 20 MHz PCM Bit Synchronizer.

6051256-01	*Viterbi Decoder*
6051256-02	*Atlas DSS (Data Source Selector)*
6051256-03	*Built-in BERT (Bit-Error-Rate Tester)*
6051256-04	*Both Atlas DSS & Viterbi capabilities*
6051256-05	*Atlas DSS, Viterbi, & BERT capabilities*

1.4 DOCUMENT CONVENTIONS

In this document, register addresses and address offsets are hexadecimal numbers. Where it is necessary to refer to a hexadecimal number in the text, we use the C programming convention 0xNN to refer to hexadecimal number NN. Bits in a register are numbered in decimal. The term Device n refers to an address destination on the TDP system A-Bus.

1.5 WARRANTY INFORMATION

The BSYN is guaranteed as shown in the following warranty.

ACROAMATICS, INC. PRODUCT WARRANTY

Acroamatics, Inc. warrants all equipment manufactured by it to be free from defects in design, materials, and workmanship for a period of twelve months from the date of acceptance by the Customer. Acroamatics, Inc. will repair without charge all parts of said products that are returned to the factory within the warranty period, provided that the equipment is returned prepaid to the factory within twelve months after the date of acceptance, or that the defect is reported, in writing, within twelve months after the date of acceptance, and provided that inspection by Acroamatics, Inc. discloses that the defects are as above specified. Equipment found to be defective will, at Acroamatics, Inc.'s option, be replaced or repaired, and returned via surface transportation, prepaid. With the exception of the twelve-month warranty set forth above, Acroamatics, Inc. makes no express warranties, no warranties of merchantability, and no warranties that extend beyond the description on the face hereof. In no event will Acroamatics, Inc. be liable for consequential damages of any kind. For products sold to the United States Government, under procurements governed by the Federal Acquisition Regulations (FAR), any part of this PRODUCT WARRANTY that conflicts with an applicable FAR clause, incorporated actually or by reference in the purchase contract, shall be supplanted by the FAR clause.

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1.6 SHIPPING AND HANDLING PRECAUTIONS

CAUTION: Failure to follow standard ESD protection procedures may result in damage to equipment.

Use ESD protection when handling the card. Make sure you are well grounded. Handle the card by its ears or edges only. Place the card in an ESD protection bag when it is not in the unit. Ship the card in its original shipping materials. If original shipping materials are not available, wrap the bag-enclosed card in antistatic foam and place it in a sturdy close-fitting box. Seal the shipping package with reinforced tape and mark it "FRAGILE."

1.7 STORAGE DATA

The Model 501V-20 PCM Bit Synchronizer (BSYN) requires no special storage. Keep the card in an ESD protection bag when it is not in the unit. For long-term storage, pack the card as for shipping above. Do not expose the card to high humidity or extreme temperatures.

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SECTION 2
INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 501V-20 series PCM Bit Synchronizer. The card part number is 6011501-2x, with x being 0, 1, 2, etc., depending on the version.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the antistatic bag. Retain the container, antistatic bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification/update you want. Pack the card for shipment by placing it in the antistatic bag. Then place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Mark it "FRAGILE". Provide the name and phone number of a technical contact we can talk to regarding the card failure.

Call Acroamatics at (805) 967-9909 and get an RMA number before returning any equipment to the factory. Include the RMA number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

The BSYN card mounts in a standard VMEbus chassis. Mounting dimensions are shown in the assembly drawing in Section 6.

CAUTION: Installing or removing a card by pressing or pulling on the card itself, rather than the ears, may damage the card.

Slide the card into one of your system VME chassis slots and seat the card firmly by pressing against the ears, then tighten the screws within the ears. Make the front panel cable connections appropriate to your system. To remove the card, loosen the screws within the ears, press outward on the ears so that their cam-like action pulls the card from the connector, and remove the card by pulling on the ears.

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2.5 2.5 CONNECTORS

The following tables contain information on all the connections into and out of the BSYN card.

> Note:
> An asterisk (*) indicates that the pin or connector has more than one use or configuration, based upon on-card jumpers or software setup. See Table 5-1 and the schematics for further information.

TABLE 2-1. MATING CONNECTOR LIST FOR MODEL 501V-20

CONN.	FUNCTION	MATING CONNECTOR
P01	VMEbus	603-2-IEC-C096
***P02**	VMEbus	603-2-IEC-C096
J01	CLOCK OUTPUT	SMB 903-285P-51S
J02	DATA OUTPUT	SMB 903-285P-51S
J03	TAPE OUTPUT	SMB 903-285P-51S
***J04**	X2 CLOCK OUTPUT	SMB 903-285P-51S
***J05**	CODE OUTPUT	SMB 903-285P-51S
***J06**	RNRZ OUTPUT	SMB 903-285P-51S
J07	RS-232	MODULAR
***J08**	INPUT 1	SMB 903-285P-51S
***J09**	INPUT 2	SMB 903-285P-51S
***J10**	INPUT 3	SMB 903-285P-51S
***J11**	DIFFERENTIAL INPUT 4	PL75-1

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TABLE 2-2. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P01-ROW-A

NOTE: ALL ($) SIGNALS NOT USED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED00	Data Bus 00
02	4VMED01	Data Bus 01
03	4VMED02	Data Bus 02
04	4VMED03	Data Bus 03
05	4VMED04	Data Bus 04
06	4VMED05	Data Bus 05
07	4VMED06	Data Bus 06
08	4VMED07	Data Bus 07
09	GND	Ground
10	4VMECLK ($)	System Clock
11	GND	Ground
12	9VMEDS1	Data Strobe 1
13	9VMEDS0	Data Strobe 0
14	9VMEWRT	Write
15	GND	Ground
16	9VMDACK	Data Transfer Acknowledge
17	GND	Ground
18	9VMASTB	Address Strobe
19	GND	Ground
20	9VMIACK	Interrupt Acknowledge
21	9VMIAIN	Interrupt Acknowledge IN
22	9VMIAOT	Interrupt Acknowledge OUT
23	4VMAM04	Address Modifier 4
24	4VMEA07	Address Bus 07
25	4VMEA06	Address Bus 06
26	4VMEA05	Address Bus 05
27	4VMEA04	Address Bus 04
28	4VMEA03	Address Bus 03
29	4VMEA02	Address Bus 02
30	4VMEA01	Address Bus 01
31	-12 VDC ($)	-12 Volts DC
32	+5 VDC	+5 Volts DC

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TABLE 2-3. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P01-ROW-B

NOTE: ALL ($) SIGNALS NOT USED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	9VMBSBY	Bus Busy
02	9VMBCLR	Bus Clear
03	ACFAIL ($)	AC Power Fail
04	9VMBGI0	Bus Grant 0 IN
05	9VMBGO0	Bus Grant 0 OUT
06	9VMBGI1	Bus Grant 1 IN
07	9VMBGO1	Bus Grant 1 OUT
08	9VMBGI2	Bus Grant 2 IN
09	9VMBGO2	Bus Grant 2 OUT
10	9VMBGI3	Bus Grant 3 IN
11	9VMBGO3	Bus Grant 3 OUT
12	9VMBRQ0	Bus Request 0
13	9VMBRQ1	Bus Request 1
14	9VMBRQ2	Bus Request 2
15	9VMBRQ3	Bus Request 3
16	4VMAM00	Address Modifier 0
17	4VMAM01	Address Modifier 1
18	4VMAM02	Address Modifier 2
19	4VMAM03	Address Modifier 3
20	GND	Ground
21	SERCLK ($)	Serial Clock
22	SERDAT ($)	Serial Data
23	GND	Ground
24	9VMIRQ7	Interrupt Request 7
25	9VMIRQ6	Interrupt Request 6
26	9VMIRQ5	Interrupt Request 5
27	9VMIRQ4	Interrupt Request 4
28	9VMIRQ3	Interrupt Request 3
29	9VMIRQ2	Interrupt Request 2
30	9VMIRQ1	Interrupt Request 1
31	+5 VSTDBY ($)	Stand-by +5 Volts DC
32	+5 VDC	+5 Volts DC

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TABLE 2-4. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P01-ROW-C

NOTE: ALL ($) SIGNALS NOT USED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED08	Data Bus 08
02	4VMED09	Data Bus 09
03	4VMED10	Data Bus 10
04	4VMED11	Data Bus 11
05	4VMED12	Data Bus 12
06	4VMED13	Data Bus 13
07	4VMED14	Data Bus 14
08	4VMED15	Data Bus 15
09	GND	Ground
10	SYSFAIL ($)	System Failure
11	9VMBERR	Bus Error
12	9VMPRST	System Reset
13	9VMELWD	Long Word
14	4VMAM05	Address Modifier 5
15	4VMEA23	Address Bus 23
16	4VMEA22	Address Bus 22
17	4VMEA21	Address Bus 21
18	4VMEA20	Address Bus 20
19	4VMEA19	Address Bus 19
20	4VMEA18	Address Bus 18
21	4VMEA17	Address Bus 17
22	4VMEA16	Address Bus 16
23	4VMEA15	Address Bus 15
24	4VMEA14	Address Bus 14
25	4VMEA13	Address Bus 13
26	4VMEA12	Address Bus 12
27	4VMEA11	Address Bus 11
28	4VMEA10	Address Bus 10
29	4VMEA09	Address Bus 09
30	4VMEA08	Address Bus 08
31	+12 VDC ($)	+12 Volts DC
32	+5 VDC	+5 Volts DC

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Note:
An asterisk (*) indicates that the pin or connector has more than one use or configuration, based upon on-card jumpers or software setup. See Table 5-1 and the schematics for further information.

TABLE 2-5. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P02-ROW-A

PIN	SIGNAL	FUNCTION
01	9SRCH02	ACRO Search Status Output 2-
***02**	9SRCH04	ACRO Search Status Output 4-
***03**	9EXTDAT	External Data Input -
***04**	9EXTCLK	External Clock Input -
***05**	9LOCK01	ACRO Lock Status Output 1-
***06**	9LOCK03	ACRO Lock Status Output 3-
07	4SBDCLK	Soft Bit Decision Clock Output
08	4SBD002	Soft Bit Decision Output
09	4SBD000	Soft Bit Decision Output (LSB)
***10**	9TAPOUT	Tape Output -
***11**	GND	ACRO GND
***12**	9CLCKX2	X2 Clock Output -
***13**	9DATNRZ	NRZ Data Output -
***14**	9CLK000	0° Clock - Output
***15**	9CLK090	90° Clock - Output
***16**	9CLK180	180° Clock - Output
***17**	9CLK270	270° Clock - Output
18	GND	ACRO GND
***19**	9CLKRTN	Clock Return (GND)
***20**	9DIF1IN	Differential Input 1-
***21**	9DIF2IN	Differential Input 2-
***22**	9DIF3IN	Differential Input 3-
***23**	9INPUT4	Input 4-
***24**	9SRCLED	Search LED
***25**	9LEDRTN	LED Return (GND)
***26**	4CLKTP	Clock Out Test Point
***27**	9TSTRTN	Test Return
***28**	4SIMIN1	ACRO Simulator Code 1 Input
***29**	4SIMIN2	ACRO Simulator Code 2 Input
***30**	4SIMIN3	ACRO Simulator Code 3 Input
***31**	4SIMIN4	ACRO Simulator Code 4 Input
32	9RNRZDT	Randomizer Output -

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TABLE 2-6. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P02-ROW-B

NOTE: ALL ($) SIGNALS NOT USED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	+5 VDC	+5 Volts DC
02	GND	Ground
03	RESERVED ($)	
04	4VMEA24($)	Address Bus 24
05	4VMEA25($)	Address Bus 25
06	4VMEA26($)	Address Bus 26
07	4VMEA27($)	Address Bus 27
08	4VMEA28($)	Address Bus 28
09	4VMEA29($)	Address Bus 29
10	4VMEA30($)	Address Bus 30
11	4VMEA31($)	Address Bus 31
12	GND	Ground
13	+5 VDC	+5 Volts DC
14	4VMED16($)	Data Bus 16
15	4VMED17($)	Data Bus 17
16	4VMED18($)	Data Bus 18
17	4VMED19($)	Data Bus 19
18	4VMED20($)	Data Bus 20
19	4VMED21($)	Data Bus 21
20	4VMED22($)	Data Bus 22
21	4VMED23($)	Data Bus 23
22	GND	Ground
23	4VMED24($)	Data Bus 24
24	4VMED25($)	Data Bus 25
25	4VMED26($)	Data Bus 26
26	4VMED27($)	Data Bus 27
27	4VMED28($)	Data Bus 28
28	4VMED29($)	Data Bus 29
29	4VMED30($)	Data Bus 30
30	4VMED31($)	Data Bus 31
31	GND	Ground
32	+5 VDC	+5 Volts DC

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Note:
An asterisk (*) indicates that the pin or connector has more than one use or configuration, based upon on-card jumpers or software setup. See Section 5, Table 5-1 and the schematics for further information.

TABLE 2-7. CONNECTOR LIST

MODEL 501V-20 BACKPLANE CONNECTOR P02-ROW-C

PIN	SIGNAL	FUNCTION
*01	9SRCH01	ACRO Search Status Output 1-
*02	9SRCH03	ACRO Search Status Output 3-
*03	4EXTDAT	External Data Input +
*04	4EXTCLK	External Clock Input +
*05	GNDSTS	Status Ground
*06	9LOCK02	ACRO Lock Status Output 2-
*07	9LOCK04	ACRO Lock Status Output 4-
08	4SBD003	Soft Bit Decision Output (MSB)
09	4SBD001	Soft Bit Decision Output
*10	4TAPOUT	Tape Output +
*11	TP1GND	ACRO Ground
*12	4CLCKX2	X2 Clock Output +
*13	4DATNRZ	NRZ Data Output +
*14	4CLK000	0° Clock Output +
*15	4CLK090	90° Clock Output +
*16	4CLK180	180° Clock Output +
*17	4CLK270	270° Clock Output +
*18	4NRZOUT	NRZ Output +
*19	4CLKOUT	Clock Output +
*20	4DIF1IN	Differential Input 1+
*21	4DIF2IN	Differential Input 2+
*22	4DIF3IN	Differential Input 3+
*23	4INPUT4	Input 4+
*24	4LOCLED	Lock LED
*25	9LOSRTN	Loss LED
*26	4DATATP	Data Out Test Point
27	4INPUTP	Input Test Point
28	GND	ACRO Ground
29	GND	ACRO Ground
30	GND	ACRO Ground
31	GND	ACRO Ground
32	4RNRZDT	Randomizer Output +

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TABLE 2-8. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J01

PIN	SIGNAL	FUNCTION
01	4BSCLCK	Clock Output +
02	GND	Ground

TABLE 2-9. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J02

PIN	SIGNAL	FUNCTION
01	4NRZDAT	Data Output +
02	GND	Ground

TABLE 2-10. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J03

PIN	SIGNAL	FUNCTION
01	2TAPOUT	Tape Output +
02	GND	Ground

TABLE 2-11. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J04

PIN	SIGNAL	ENCODER MODE	FUNCTION
01	4CLOKX2 4VTENCK	PCM Viterbi	X2 Clock Output Viterbi Encoder Clock
02	GND		Ground

TABLE 2-12. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J05

PIN	SIGNAL	ENCODER MODE	FUNCTION
01	4CODE 4VTENC0	PCM Viterbi	X2 Code Output Viterbi Encoder Symbol C0
02	GND		Ground

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TABLE 2-20. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J06

PIN	SIGNAL	ENCODER MODE	FUNCTION
01	4RNRZXX 4VTENC1	PCM Viterbi	X2 RNRZ Output Viterbi Encoder Symbol C1
02	GND		Ground

TABLE 2-14. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J07

PIN	SIGNAL	FUNCTION
01	GND	Ground
02	4RECDAT	RS-232 Receive Data
03		Not Used
04	GND	Ground
05	4TRXDAT	RS-232 Transmit Data

TABLE 2-15. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J08

PIN	SIGNAL	FUNCTION
01	4BSINP1	Input 1
02	GND	Ground

TABLE 2-16. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J09

PIN	SIGNAL	FUNCTION
01	4BSINP2	Input 2
02	GND	Ground

TABLE 2-17. CONNECTOR LIST
MODEL 501V-20 FRONT PANEL CONNECTOR J10

PIN	SIGNAL	FUNCTION
01	4BSINP3	Input 3
02	GND	Ground

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TABLE 2-18. CONNECTOR LIST

MODEL 501V-20 FRONT PANEL CONNECTOR J11

PIN	SIGNAL	FUNCTION
01	4BSINP4	Diff. Input 4+
02	9BSINP4	Diff. Input 4-
03	GND	Ground

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SECTION 3
OPERATION

3.1 GENERAL

This section describes operation of the Model 501V-20 PCM Bit Synchronizer card (BSYN). Extensive user instructions are also provided in the manual for the chassis-level bit synchronizer unit. The BSYN is configured from the VME host computer by ASCII setup commands that are compiled and transmitted to the command/status registers located on the card. They are accessed through nonprivileged or supervisory A16/D16 memory instructions. The location of the registers is mapped in the VME A16 Utility Address Space on a switch-selectable 64-byte boundary. The following paragraphs describe allocation of the A16 Utility Space and contain a description of the registers.

TABLE 3-1. A16 UTILITY SPACE

Address	Function	Mode
1E	Mask/Pattern - MS Byte	R/W
1C	Mask/Pattern - Next Byte	R/W
1A	Mask/Pattern - LS Byte	R/W
18	Frame Length - Bits per Frame	R/W
16	Bit Error Rate/Test Pattern Control	R/W
14	Clock Generator	R/W
12	Viterbi Control	R/W
10	Randomizer/Derandomizer Control	R/W
E	PLL Loopwidth/Tracking Control	R/W
C	Code Processing Control	R/W
A	Bit Rate Exponent, Source & Filter Control	R/W
8	Bit Rate Mantissa	R/W
6	Frequency Deviation & Status	Read
4	Input Amplitude & Offset/Special Codes	Read
2	Bit Errors/Firmware Options	Read
0	Signature(Read)/Soft Reset(Write)	R/W

3.2 STARTUP & SHUTDOWN PROCEDURES

The BSYN starts up and shuts down automatically upon startup and shutdown of the chassis-level bit synchronizer unit. No separate procedures are required. There are no emergency shutdown procedures. Setup program edits must be saved prior to shutdown, or they will be lost. If the default setup program is selected as the startup setup, the BSYN will power up with a bit rate setting of zero (idle).

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3.3 VME REGISTER DESCRIPTIONS

3.3.1 Signature Register (Address 0)

The *Signature Register* identifies your BSYN for system configuration purposes. Reading this register returns 6501_{hex} on the VMEbus when your BSYN has the Viterbi logic installed, and 5501_{hex} when not installed. Writing to this register generates a soft reset that reinitializes the on-card microcomputer.

3.3.2 Bit Errors/Firmware Options (Address 2)

This double-use register will contain two different data sets, depending upon the status of bit 7 in register E. If bits 7 & 13 of register E are set to **1**, register/address 2 contains data on the *Firmware Options* installed on your BSYN. Each bit that is set to **1** indicates the presence of that feature as shown in TABLE 3-2(A) below.

TABLE 3-2(A). FIRMWARE OPTIONS Mode (Bits 7 & 13 of Register E set to 1)

Bits	Option
15	CODE/CKX2 Programmability
14-9	Reserved
8	BERT (Bit Error Rate Test) option
7-1	Reserved
0	Frame Synchronizer / Data Source Selection

If bit 7 of register E is set to **0**, register/address 2 is in Signal Status Mode and reports the most recent BER Test Status and Error Count (if the BERT option is installed on your board and the BER test is enabled). A BER Test is enabled when bit 2 of the Code Processing Control Register (Address C) is set to **1**. BER Test parameters are configured in the Bit Error Rate/Test Pattern Control Register (Address 16).

TABLE 3-2(B). SIGNAL STATUS Mode (BERT OPTION ENABLED) (Bit 7 of Register E set to 0, bit 13 n/a)

Bits	Status
15	Sync loss during most recent sample period
14	Error count updated
13	Error count overflow (continuous mode only)
12-3	Error count mantissa
2-0	Error count exponent

The bit error count can range from zero to 9.99 billion. The count is formed by multiplying the hexadecimal mantissa in bits 12-3 by 10eN, with N in bits 2-0. For example, if bits 12-3 were 1B7H and bits 2-0 were 4, the error count would

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be 439x10e4 or 4,390,000. The mantissa range is 0 to 3e7H and the exponent range is 0 to 7. To calculate the bit error rate, divide the error count by the sample period.

Bits 15-13 are status flags for the error counter. These flags as well as the error count are cleared to 0 when this register is read. Bit 15 set to 1 indicates that the test pattern synchronizer temporarily lost synchronization during the most recently completed sample period. During a loss of synchronization, both the sample period counter and error counter are disabled, thus extending the time it takes to complete a sample period. A continuously updated version of this flag is available in Address 6. See Frequency Deviation & Status Register (Address 6). Bit 14 set to 1 indicates an updated error count value is stored in bits 12-0 of this register. When continuously accumulating errors, this flag will set to 1 on the first bit period in which the test pattern synchronizer becomes synchronized with the tested data. Otherwise, the flag sets to 1 upon the completion of each sample period. Bit 13 indicates that the error counter overflowed by exceeding 10 billion errors. This can only occur in the continuous accumulate mode since the maximum sample period length is 1 billion bit periods.

3.3.3 Input Amplitude & Offset/Special Codes Register (Address 4)

This double-use register, like register 2 above, will also contain two different data sets, depending upon the status of bits 7 & 13 in register E.

If bits 7 & 13 of register E are set to **1**, register/address 4 reports the special codes your BSYN supports. Each bit that is set to **1** indicates support for an optional special input code, as shown in TABLE 3-3(B) below. The codes (15-1) are defined in the appendices.

TABLE 3-3(B). SPECIAL CODES Mode (Bits 7 & 13 of Register E set to 1)

Bits	Special Code
15-1	15-1
0	Viterbi

If bit 7 of register E is set to **0**, register/address 4 provides input amplitude and offset status to the VME Host. The least significant byte of this register contains the input peak amplitude, expressed as an unsigned binary number. Actual peak amplitude (in volts) is computed by dividing the count by 10. The most significant byte contains the input DC offset. The 2's complement value range is ± 100. Actual input offset (in volts) is computed by dividing the count by 10.

TABLE 3-3(A). INPUT AMPLITUDE & STATUS Mode (Bit 7 of Register E set to 0, bit 13 n/a)

Bits	Function
15-8	Input Signal Offset
7-0	Input Signal Amplitude

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3.3.4 Frequency Deviation & Status Register (Address 6)

This register provides frequency and synchronization status to the VME host.

TABLE 3-4. FREQUENCY DEVIATION & STATUS REGISTER

Bits	Function
15	Search/Lock Status
14	Bit Rate = 0 (not set)
13	μcomputer Not Ready
12	Servo Error
11	BER Test Synchronization Lost
10	Reserved
9	μcomputer Acknowledge
8	Signal Loss
0-7	Frequency Error

Bits 0-7, the least significant byte, contains the input data stream frequency deviation from the programmed rate. The 2's complement value ranges ± 127 counts, with each count corresponding to a 0.1% resolution in error from the programmed rate. For example, if the programmed bit rate is 2000 bps and the count value is 13 decimal (a + 1.3% error), the actual input rate is determined to be 2026 Hz.

Bit 8 set to **1** indicates that the signal is below 0.2V p-p, the minimum input level.

Bit 9 is used by the μcomputer to acknowledge completion of VME host request. The VME host makes requests by setting bits 7 & 13 in register E to 1. The μcomputer acknowledges completion of the request by toggling the value of bit 9.

Bit 10 is reserved.

Bit 11 set to **1** indicates that the BER Test Pattern Synchronizer lost sync during the time interval since this bit was last queried. If the unit was in lock during the entire interval, this bit is set to **0**.

Bit 12 set to **1** indicates that the Mcomputer failed to servo the PLL to the programmed rate.

Bit 13 set to **1** indicates that the μcomputer has not completed initialization after being powered up or reset.

Bit 14 set to **1** indicates that the bit rate is set to zero or the bit sync is in idle state.

Bit 15 is set to **1** if the unit ever lost rate sync during the time interval since this bit was last queried. If the unit was in lock during the entire interval, this bit is set to **0**.

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3.3.5 Bit Rate Mantissa Register (Address 8)

This register contains the mantissa value of the bit rate as expressed in scientific notation format. The rate ranges from 1.000 to 9.999, and is programmed in binary form scaled by a factor of 1000. For example, the programmed value for a 1KHz bit rate would be $3e8_{hex.}$ Note that the bit rate multiplier in bits 0-2 of Register Address A has to be set to 3 (multiplier of 1000) to generate 1kHz.

TABLE 3-5. BIT RATE MANTISSA REGISTER

Bits	Function
15-0	Bit Rate Mantissa

3.3.6 Bit Rate Exponent, Source & Filter Control Register (Address A)

This register contains the exponent value of the bit rate, the high and low pass filter controls, the input termination, and the input source selection. When the VME host writes to this register, a *rate interrupt* is sent to the embedded processor. The processor in turn reads the bit rate mantissa register (Address 8) to obtain the mantissa of the bit rate.

TABLE 3-6. BIT RATE EXPONENT, SOURCE & FILTER REGISTER

Bits	Function
15	Encode External Clock & Data
14-12	Input Source Selection
11-8	Input Termination Selection
7-6	External Clock Control
5-4	Low Pass Filter Control
3	High Pass Filter Enable
2-0	Bit Rate Exponent

Bits 0-2 contain the power of 10 exponent for the bit rate, ranging from 0 to 7.

Bit 3 set to **1** enables the high pass filter for bi-phase codes.

Bits 4 & 5 control the low pass filter (01 = narrow, 10 = wide, and 11 = over-filtered data recovery).

Bits 6 & 7 control the external clock input: Bit 7 is set to **1** to indicate that the external clock is twice the bit rate, and set to **0** when external clock is at the bit rate. Bit 6 set to **1** inverts the external clock.

Bits 8-11 select the terminations for inputs 1 through 4 respectively. 0 = low, 1 = high impedance.

Bits 12-14 perform a one-of-eight decode to select the input source: 0 selects a TTL-compatible PCM input from the P2 connector; 1 through 4 select one of four full-range analog inputs; 5 selects the external clock and data to the PCM decoder; 6 is reserved; and 7 disables all inputs.

Bit 15 set to **1** selects the external clock and data to the PCM encoder. If the input source = 5 and bit 15 = 1, the decoded external clock and data are routed

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to the encoder.

Bit 15 set to **0** selects the bit synchronizer clock and data as the input to the PCM encoder.

3.3.7 Code Processing Control Register (Address C)

This register contains bits controlling input and output code type, enable signals for special code decoding, convolutional encoding, derandomizing, randomizing, BER testing, encoding the internal pattern generator, input polarity, and direction control. When the VME host writes to this register, a *code interrupt* is sent to the embedded processor. Upon receipt of this interrupt the processor reads the information stored at addresses 10 to 1F.

TABLE 3-7. CODE TYPE & CONTROL REGISTER

Bits	Function
0	Playback Direction
1	Invert Data Out
2	Enable BERT
3	Encode Test Pattern Generator
4	Encode Randomized Data
5	Enable Derandomizer
6	Enable Convolutional Encoder
7	Enable Special Codes Decoder
8-11	Output Code Type
12-15	Input Code Type

Bit 0 set to **1** enables the derandomizing of data received in the reverse direction.

Bit 1 set to **1** inverts the NRZ data out of the decoder.

Bit 2 set to **1** enables the BERT counter. Refer to the Bit Error Rate Test Control Register (Address 16).

Bit 3 set to **1** selects the PN test pattern generator as the data source to the encoder. This bit overrides the input selected by Register A bit 15.

Bit 4 set to **1** directs the randomized output to both the PCM and convolutional encoders. Bit 4 set to **0** directs the unrandomized data to both the PCM and convolutional encoders. Refer to the Randomizer/Derandomizer Control Register (Address 10).

Bit 5 set to **1** directs decoded data through the derandomizer. See Randomizer/Derandomizer Control Register (Address 10).

Bit 6 set to **1** enables the convolutional encoder. The convolutional encoder outputs G1 and G2 are routed to the BSYN front panel connectors *CODE* (J5) and *RNRZ* (J6). Refer to the Viterbi Control Register (Address 12) description.

Bit 6 set to **0** directs the PCM encoder output to the *CODE* connector and the randomizer output to the *RNRZ* connector.

Bit 7 set to **1** enables the optional Special Codes decoder. Refer to the Viterbi

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Control Register (Address 12), the Input Amplitude & Offset/Special Codes Register (Address 4), and the Special Codes appendices.

Bits 12-15 and 8-11 select the input and output code types, respectively, as shown in TABLE 3-8.

TABLE 3-8. INPUT & OUTPUT CODE TYPES

* = Transition codes

Bits 15-12	Input Code	Bits 11-8	Output Code
0	NRZ-L	0	NRZ-L
1	NRZ-M	1	NRZ-M
2	NRZ-S	2	NRZ-S
3	RZ	3	RZ
4	Reserved	4	Reserved
5	Reserved	5	Reserved
6	Reserved	6	Reserved
7	BPH-L*	7	BPH-L*
8	DBPH-S*	8	DBPH-S*
9	DBPH-M*	9	DBPH-M*
A	BPH-M*	A	BPH-M*
B	BPH-S*	B	BPH-S*
C	DM-M*	C	DM-M*
D	DM-S*	D	DM-S*
E	M2-M*	E	M2-M*
F	M2-S*	F	M2-S*

3.3.8 PLL Loopwidth/Tracking Control Register (Address E)

This register selects the phase of the output data clock as well as the loopwidth and tracking range of the phase-lock-loop circuitry. When the VME host writes to this register, a *loopwidth interrupt* is sent to the embedded processor.

TABLE 3-9. PLL LOOPWIDTH CONTROL REGISTER

Bits	Function
15-14	Output Clock Phase
13	Request μcomputer Acknowledge
12-8	Loop Width
7	Readback Mode
6-0	Loop Tracking Limit

Bits 15-14 select the phase of the data clock output as follows: 00 = 0°, 01 = 90°, 10 = 180°, 11 = 270°.

Bit 13 allows the VME host to check the responsiveness of the μcomputer. Each time the VME host writes this register with bit 13 set to **1**, the μcomputer will

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toggle the *Acknowledge* bit, bit 9 in the Register at Address 6.

Bits 12-8 contain the loopwidth setting of the PLL. The PLL has 32 possible settings, ranging from 3.2% to 0.1%. The PLL's widest setting, 3.2%, allows the unit to quickly capture and track off-frequency signals. The narrowest setting is 0.1%, and enables the unit to recover data from extremely noisy input.

Bit 7 controls the two *Readback Modes* for Registers 2 and 4. When bit 7 is set to **0**, registers 2 and 4 will report *BER Test Status* and *Input Amplitude Status* values, respectively. When bit 7 is set to **1**, the *Firmware Options & Special Codes* supported by your BSYN card are reported in registers 2 and 4 respectively. Bit 13 of register E (as well as bit 7) must also be set to **1** for this mode to take effect.

Bits 6-0 are set to limit the PLL's maximum offset tracking range. This tracking range is programmed by a binary count from 1 to 99. The count represents a tracking range from 0.1% to 9.9% of the programmed bit rate. For example, a setting of 99 allows the unit to track input signals with a frequency deviation of ±9.9% without losing synchronization. The PLL circuitry resets to the programmed bit rate if the PLL drifts beyond the programmed loop-tracking limit. A setting of zero disables the tracking limits, thus allowing the PLL to track the incoming bit rate to its maximum ability (generally in excess of ±12%).

3.3.9 Randomizer/Derandomizer Control Register (Address 10)

This register selects the modulus for both the input derandomizer and output randomizer, and also configures the Encoder Data Polarity, CODE output, and CKX2 output. The register is set up prior to loading either the *randomizer* or *derandomizer enable* bit into address C.

TABLE 3-10. RANDOMIZER/DERANDOMIZER CONTROL REGISTERS

Bits 3 2 1 0	Randomizer	Bits 7 6 5 4	Derandomizer
0 0 0 0	bypass	0 0 0 0	passthrough
0 0 0 1	RNRZ-9	0 0 0 1	RNRZ-9
0 0 1 0	RNRZ-11	0 0 1 0	RNRZ-11
0 0 1 1	RNRZ-15	0 0 1 1	RNRZ-15
0 1 0 0	RNRZ-17	0 1 0 0	RNRZ-17
0 1 0 1	RNRZ-23	0 1 0 1	RNRZ-23

Bits 0 - 3 select the output randomizer modulus.

Bits 4 - 7 select the input derandomizer modulus. The selections are the same as for the randomizer.

Bits 8 - 11 are reserved.

Bits 12 - 15 configure the encoder data polarity, CODE output, and CKX2 output as follows.

Bit 12 set to **1** inverts the encoder data source prior to being encoded.

Bit 13 set to **1** passes the unencoded data source directly to the CODE output, unless the convolutional encoder is enabled. Refer to the Code Processing Control Register (Address C).

Bit 14 set to **1** inverts the encoder clock provided at the CKX2 output.

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Bit 15 set to **1** provides a X1 clock at the CKX2 output when the encoder source is clocked by the BSYN-recovered clock. If the encoder source is externally clocked, the CKX2 output is always X1.

3.3.10 Viterbi Control Register (Address 12)

This control register configures both the *convolutional encoder* and *Viterbi decoder*. The Viterbi Control register is set up prior to loading either of the associated enable bits into register C.

TABLE 3-11. VITERBI CONTROL REGISTER

Bits	Function
15	Decode Parallel Input
14	Master Mode
13	Decode OQPSK
12	Reverse G1/G2 Symbols
11	Hard Bit Decision
10	Differential Decoder Enable
9-8	Descrambler Mode
7-6	Reserved
5	Encode OQPSK
4	Reverse G1/G2 Symbols
3	Encode Parallel Output
2	Differential Encoder Enable
1-0	Scrambler Mode

Bits 15-8 configure the BSYN for decoding k=7, rate 1/2, convolutionally encoded data.

Bit 15 set to **1** configures the BSYN for *parallel* operation; set to **0** selects *serial* operation. When configured for serial operation, bit 14 should be set to **1**. In order to use an external convolutional decoder to decode the soft bits, set bits 14 and 15 to 1. Parallel operation requires two 501V-20 cards. You must set bit 14 to 1 on the BSYN you want to be the master, and to 0 on the one to be the slave. As a master, the BSYN recovers symbols from either the I or the Q channel of a QPSK demodulator. As a slave, the BSYN recovers symbols from the remaining channel of the QPSK demodulator. The slave's soft bit decisions are forwarded via the P2 connector back to the master. The Viterbi decoder on the master reconstructs the original data from the soft bit decisions.

Bit 13 set to **1** configures the Viterbi decoder for processing data transmitted on an Offset QPSK link.

Bit 12 set to **1** configures the Viterbi decoder for recovering serially transmitted symbols in which the G2 symbol precedes the G1 symbol.

Bit 11 set to **1** configures the Viterbi decoder to process the data with just the polarity bit of the soft bit decision. The magnitude bits are ignored, which reduces the coding gain of the Viterbi decoder.

Bit 10 set to **1** selects differential coding as the output of the Viterbi decoder, and is set to **0** to accept NRZ-L data.

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Bits 9 & 8 configure the Viterbi data descrambler as follows. 00 = off, 01 = CCITT V.35 algorithm, 10 = INTELSAT specified algorithm, and 11 = G2 invert.

Bits 7-6 are reserved and should be set to **0**.

Bit 5 set to **1** sets the convolutional encoder to output the G1/G2 symbols in a *staggered* format, in which the G1 symbol precedes the G2 symbol by one half of a symbol period. This capability applies in *parallel* format, for generating OQPSK data.

Bit 4 set to **1** sets the convolutional encoder to reverse the position of the G1 and G2 symbols. In the parallel format, G2 will be output on front panel connector J5, and G1 on connector J6. In the serial format, the G2 symbol will precede the G1 symbol at front panel connector J5, while front panel connector J6 will provide standard randomized data. Refer to Randomizer/Derandomizer Control Register (Address 10) for more.

Bits 3 & 2 configure the k=7 rate 1/2 convolutional encoder.

Bit 3 set to **1** configures the BSYN to output the data symbols in the parallel format: G1 is available at front panel connector J5, and G2 is available at J6.

Bit 3 set to **0** configures the BSYN to output G1 and G2 serially, with G1 output first. The composite signal is available at connector J5.

Bit 2 set to **1** enables you to differentially encode data prior to loading into the convolutional encoder.

Bits 1 & 0 configure the scrambler as follows: 00 = off, 01 = CCITT V.35 algorithm, 10 = INTELSAT specified algorithm, and 11 = G2 invert.

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3.3.11 Clock Generator (Address 14)

This register configures the clock rate generator that the *internal test pattern generator* uses, and is setup prior to loading the *Encode Test Generator* bit into address C.

Bit 15 set to **1** enables the clock rate generator as the clock source to the test pattern generator and encoder. This bit overrides bit 15 of Register A. See Address A description, paragraph 3.3.6

Bits 14-12 control the base 10 exponent of the clock rate, and bits 11-10 control the mantissa of the clock rate.

Bits 9-0 are reserved.

TABLE 3-12. RATE GENERATOR REGISTER

BITS						DESCR	BITS					DESCR
15	**14**	**13**	**12**	**11**	**10**	**Clock Rate**	**14**	**13**	**12**	**11**	**10**	**Clock Rate**
1	0	0	0	0	0	**na**	1	0	0	0	0	**1.0e4**
1	0	0	0	0	1	**na**	1	0	0	0	1	**1.25e4**
1	0	0	0	1	0	**na**	1	0	0	1	0	**2.5e4**
1	0	0	0	1	1	**na**	1	0	0	1	1	**5.0e4**
1	0	0	1	0	0	**1.0e1**	1	0	1	0	0	**1.0e5**
1	0	0	1	0	1	**1.25e1**	1	0	1	0	1	**1.25e5**
1	0	0	1	1	0	**2.5e1**	1	0	1	1	0	**2.5e5**
1	0	0	1	1	1	**5.0e1**	1	0	1	1	1	**5.0e5**
1	0	1	0	0	0	**1.0e2**	1	1	0	0	0	**1.0e6**
1	0	1	0	0	1	**1.25e2**	1	1	0	0	1	**1.25e6**
1	0	1	0	1	0	**2.5e2**	1	1	0	1	0	**2.5e6**
1	0	1	0	1	1	**5.0e2**	1	1	0	1	1	**5.0e6**
1	0	1	1	0	0	**1.0e3**	1	1	1	0	0	**1.0e7**
1	0	1	1	0	1	**1.25e3**	1	1	1	0	1	**2.0e7**
1	0	1	1	1	0	**2.5e3**	1	1	1	1	0	**na**
1	0	1	1	1	1	**5.0e3**	1	1	1	1	1	**na**

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3.3.12 Bit Error Rate/Test Pattern Control (Address 16)

This register configures the test pattern synchronizer, error counter, and pseudo-random number (PN) test pattern generator.

Bit 15 set to **1** enables the test pattern synchronizer. This synchronizer time-aligns a self-generated test pattern to the data being measured, thereby providing a reference for the bit error counter.

Bits 14-12 configure the sample period over which the bit error count is to be measured. The sample ranges are one thousand to one billion bits, and a continuous accumulation of errors mode. The measured error count is stored in address 2. Refer to Bit Errors/Firmware Options Register (Address 2).

TABLE 3-13. BER SAMPLE PERIOD

BITS 14	BITS 13	BITS 12	SAMPLE PERIOD
0	0	0	Continuous Accumulate
0	0	1	1,000 bits
0	1	0	10,000 bits
0	1	1	100,000 bits
1	0	0	1,000,000 bits
1	0	1	10,000,000 bits
1	1	0	100,000,000 bits
1	1	1	1,000,000,000 bits

Bits 11-10 select the Frame Sync or BERT source as follows.

TABLE 3-14. BERT SOURCE SELECT

BITS 11	BITS 10	SOURCE
0	0	Decoder
0	1	XDAT
1	0	Test Generator

Bit 9 set to **1** Selects Frame Sync Auto Polarity

Bit 8 set to **1** forces an error in each iteration of a pattern generated by either the internal PN test pattern generator or the frame format. This forced error will produce a known error count for any length sample period.

Bits 7-6 are not used.

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Bits 5-4 determine Test Generator Blanking as follows.

TABLE 3-15. TEST GENERATOR BLANKING

BITS 5	BITS 4	BLANKING
0	0	OFF
0	1	64 Blanks
1	0	128 Blanks
1	1	256 Blanks

Bits 3-0 determine Test Pattern Format as follows.

TABLE 3-16. TEST PATTERN FORMAT

BITS 3	BITS 2	BITS 1	BITS 0	PATTERN FORMAT
0	0	0	0	PN11F
0	0	0	1	PN9F
0	0	1	0	PN7F
0	0	1	1	PN15F
X	1	X	X	FRAME PATTERN
1	0	0	0	PN11R
1	0	0	1	PN9R
1	0	1	0	PN7R
1	0	1	1	PN15R

3.3.13 Format Frame Length (Address 18)

This register defines the number of bits in a complete frame when using the frame synchronizer. Bits 15-0 equal the number of bits in the frame minus one i.e. /1F equals 32 bits per frame. The minimum value is /17.

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3.3.14 Mask/Pattern LS Byte (Address 1A)

This register contains the Least Significant Byte of the mask and the pattern of the frame.

LEAST SIGNIFICANT BYTE																
MASK BITS								PATTERN BITS								MODE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**R/W**

3.3.15 Mask/Pattern Next Byte (Address 1C)

This register contains the Next Byte of the mask and the pattern of the frame.

NEXT BYTE																
MASK BITS								PATTERN BITS								MODE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**R/W**

3.3.16 Mask/Pattern MS Byte (Address 1E)

This register contains the Most Significant Byte of the mask and the pattern of the frame.

MOST SIGNIFICANT BYTE																
MASK BITS								PATTERN BITS								MODE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**R/W**

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3.4 VME SOFTWARE DESCRIPTION

The setup software for the Model 501V-20 BSYN is written in the C language and is portable to many platforms. The syntax language is compatible with that used in the Acroamatics 2000 series of Telemetry Data Processors.

At the beginning of a setup, the compiler first reads the current values of all the parameters associated with the specified BSYN and builds a simple table of setup parameters (bit rate, loop width, input source, code type, etc). The compiler then processes the setup text for the BSYN, replacing any old parameter values with the newly assigned ones. At the end of this input, the new table is transmitted to the bit synchronizer - essentially intact and without modification. Any parameters that are not explicitly assigned new values remain unchanged.

The following sections discuss the setup syntax for the Model 501V-20 BSYN.

3.4.1 Multiple Bit Synchronizers

The general form of a BSYN setup program is

```
BITS n
  .
  .
  .
commands
  .
  .
  .
END
```

where *n* is the unit number of the BSYN you are setting up. If n is omitted, BSYN one is assumed. There are 16 addresses available for BSYNs, which are assigned according to the configuration of the system.

3.4.2 Bit Rate

The bit rate is set by the following command:

BR=*rate*

where *rate* is 0 Hz or the range 8 Hz to *MaxRate*. *MaxRate* is 2.000E7 Hz for NRZ and bi-phase codes and 1.000E7 for all others. The rate can be expressed in several ways. For example, if you wish to set the rate to 12.34 MHz, any of the following commands will work:

```
BR=12340000
BR=12340K
BR=12.34M
BR=1.234E7
```

The BSYN remains in the IDLE state until a bit rate is entered. Once a bit rate has been entered, the BSYN will go into SEARCH mode and begin processing input signals. Entering a rate of zero will return the BSYN to the IDLE state, disabling the inputs and turning off the bit sync status LEDs.

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3.4.3 Source Selection

To select the input source, use the command

SRC=*n [termination]*

where *n* may be 0, 1, 2, 3 or 4. Source 0 is a TTL input compatible with the Model 500V PCM Simulator. Sources 1, 2, 3 & 4 are full-range analog inputs compatible with most other PCM input sources. If you are selecting input sources 1, 2, 3, or 4, you can also specify the termination as LO or HI impedance. Analog inputs are jumper-configurable to accept single-ended or differential inputs.

3.4.4 Source Termination

To select the input source termination, you can use the command

TERM *input_1_Z_value input_2_Z_value input_3_Z_value input_4_Z_value*

Valid Z values are LO or HI, which signify 75 Ω and 10k Ω terminations, respectively, when the input is configured as single ended. They signify 125 Ω and 10k Ω terminations, respectively, when the input is configured as differential. Each of the Z values must be given.

3.4.5 Loop Width

Loop width expresses the effective size of the "window" in which the bit sync can lock onto and track a signal. The larger the window, the more quickly lock is achieved, but also the more susceptible the device is to signal perturbations. The larger the numeric value given as the loop width parameter, the larger the window. The command

LW=*n.n%*

sets the loop width. The Model 501V-20 Bit Sync provides 32 loop widths from 0.1% to 3.2%.

3.4.6 Loop Tracking

Loop tracking sets the maximum allowable PLL frequency deviation from the programmed bit rate. The larger the numeric value of the loop tracking parameter, the larger the range. Setting the loop tracking to 0.0% allows the loop to track over its maximum range. The command

TRK=*n.n%*

sets the loop tracking. The PLL is momentarily reset when the output frequency drifts beyond the +/-n.n% value. The Model 501V-20 BSYN provides 100 settings from 0.0% to 9.9%.

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3.4.7 Polarity

The following two polarity commands are available:

NOR	This command selects NORMAL polarity for output data.
INV	This command selects INVERTED polarity for output data.

3.4.8 Playback Tape Direction

You select the playback direction of tape recorded data with two commands:

FOR
REV

Use the FOR command with forward direction data, and the REV command for data received in the reverse direction. You can decode NRZ and Bi-phase codes in reverse.

3.4.9 Filter Selection

The following filtering functions are available:

NLF	Selects the narrow bandwidth for the low-pass filter
WLF	Selects the wide bandwidth for the low-pass filter
EHF	Enables the high-pass filter
DHF	Disables the high-pass filter
OFD	Enables over-filtered data recovery

Generally speaking, the low-pass filter removes noise and perturbations above the BSYN's frequency setting, and the high-pass filter removes signal content below the frequency setting. Using the filters does not necessarily result in better data output, and you should experiment with the filters on noisy signals or tapes. Try the OFD command when your data has been severely over-filtered. This command modifies the AGC routine to compensate for the varying amplitude levels of overfiltered signals. Also, the detection circuitry monitors the data peaks rather than the zero crossings on bit rates above 100kbps. This allows you to recover extremely over-filtered data.

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3.4.10 Input Code Types

Specify the input code type you are going to process by entering the mnemonic as shown below under *Command*.

IRIG Code	Command	Code Definition
NRZ-L	**NZL**	Non-Return-to-Zero Level
NRZ-M	**NZM**	Non-Return-to-Zero Mark
NRZ-S	**NZS**	Non-Return-to-Zero Space
BiP-L	**BPL**	Bi-phase Level (Split Phase)
BiP-M	**BPM**	Bi-phase Mark
BiP-S	**BPS**	Bi-phase Space
DBiP-M	**DBI-M**	Differential Bi-phase Mark
DBiP-S	**DBI-S**	Differential Bi-phase Space
DM-M	**DMM**	Delay Modulation Mark (Miller)
DM-S	**DMS**	Delay Modulation Space (Miller)
M2-M	**M2M**	Modified Delay Modulation Mark (Miller)
M2-S	**M2S**	Modified Delay Modulation Space (Miller)
RZ	**RZ**	Return-to-Zero
NRZ-L	**RNZ-n**	Randomized Non-Return-to-Zero Level

You can apply an IRIG derandomizer to the data after the input code conversion. The run length of the derandomizer is specified on the code line following the input code, as follows:

code [n]

Specify *code* by using the command from the codes listed above. Run length values for n are 9, 11, 15, 17, or 23. You need to specify the run length only if you have a randomized code. If you do not specify a derandomizer length, the derandomizer is disabled. The RNZ-n command is applicable only for randomized NRZ-L data.

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3.4.11 Viterbi Input Decoding (Optional)

The BSYN card, equipped with any of the above options, decodes data that has been encoded with a K = 7, rate 1/2 convolutional, forward error correcting device. Rate 1/2 convolutional encoding applies two separate polynomials to seven consecutive bits of data, then forwards the output as two symbols, each symbol being the result of one of the polynomials. The symbol rate is therefore twice the input data rate. The symbols may be transmitted serially using time division multiplexing techniques, or in parallel, using two links (such as a QPSK modulator). Using a history of previous symbols and a maximum-likelihood decoding algorithm, the decoder recombines and processes the symbols to reproduce the original data. The Viterbi decoder is enabled by the following command line:

VIT *[type] [decision] [code] [descrambler]*

The input type can be serial, with the two symbols alternating in time, or parallel. Decoding parallel inputs with the symbols simultaneously processed requires two BSYNs. One BSYN, designated the slave, produces a soft bit decision and sends it to the other BSYN, designated the master. The Viterbi decoder on the master BSYN takes the soft bit decisions for the two symbols and combines them to reproduce the original data. If type is not specified, serial is assumed. Type is selected by:

SER	serial
MAS	master
SLA	slave

In a soft bit decision, the decoder is given an 8-level value that expresses not only the binary value of the bit, but also a level of confidence to which the binary value is considered known. Because the decoder receives more information in a soft bit decision, you get better decoding performance. If decision type is not specified, soft bit decision is assumed. Specify *decision* by

HBD	hard bit decision
SBD	soft bit decision

The input code can be normal (NRZ-L) or differential, indicating an edge transition code (NRZ-M). If it is not specified, normal is assumed. Specify *code* as

NOR	normal
DIF	differential

In order to increase the number of binary transitions in a convolutionally encoded data stream, the data may be enhanced with a scrambling algorithm. The BSYN supports three scrambling algorithms commonly used with convolutionally encoded data. These are the CCITT V.35 algorithm, the INTELSAT algorithm, and *G2 inversion*, which simply inverts the G2 symbol generated by the convolutional encoder. Specify scrambler by:

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ITT CCITT V.35
INT Intelsat
G2 Invert G2

The BSYN also allows you to control the orientation of the G1 and G2 symbols. Specifying REV reverses the orientation of G1 and G2. For serial input, this means that G2 precedes G1 in time. For parallel input, this means that the relationship between the G1, G2 symbols and the master, slave bit synchronizers is reversed. Further, for parallel input the two input symbols may be staggered a half bit period. This is known as *offset QPSK*, and can be decoded by specifying OQ.

3.4.12 Output Clock Phase

The NRZ data at front panel connector J2 is accompanied by a synchronous clock at connector J1. The phase relationship between this clock and the output data is selectable with the following command:

CLK *n*

where *n* is 0, 90, 180, or 270, expressing the phase shift in degrees between the positive transition of the output clock with respect to the start of the bit period.

3.4.13 Controlling the Output Encoder

3.4.13.1 Encoder Source

The encoder can use either the clock and data recovered from the bit synchronized PCM signal, or an external clock and data source connected via the P2 user input pins. The default source for the output encoder is the recovered clock and data. You can select the external clock and data to be encoded with the command

XDAT *[+/-n]*

where *n* is either 1 or 2, indicating that the external clock is the bit rate or twice the bit rate, respectively. The sign, - or +, expresses whether the external clock is to be inverted or non-inverted, respectively. If the rising edges of the clock coincide with the transitions of the data, the sign must be +. If the falling edges of the clock coincide with the transitions of the data, the sign must be -. If you do not give the +/-n parameter, the setting will be + for a non-inverted "times-one" clock. To explicitly select the bit synchronizer decoded output as the source for the encoder, use the command

IDAT

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3.4.13.2 Encoder Output

The PCM encoder output is provided as a bipolar analog signal at the Bit Synchronizer's TAPE connector. The output code from the encoder is specified by the command

OUT *code [n]*

or the command

TAPE *code [n]*

Select *code* from the IRIG Code list in Section 3.4.10, Input Code Types. You can randomize the data prior to encoding. The run length *n* of the randomizer is specified after *code*. Specifying a run length here causes two things to happen. First, it selects the randomizer output to be encoded. Second, it sets the run length for the randomizer. Run lengths for n are 9, 11, 15, 17, or 23. The RNZ-n command is applicable only for randomized NRZ-L data. You must specify the run length if you want to randomize the data prior to encoding. The **RAN** command (see section 3.4.13.3) can also be used to specify the randomizer's run length, but this command does not affect the randomizer's path to the encoder.

3.4.13.3 Randomizer Output

You can randomize the data source you have selected into the PCM encoder. To specify the randomizer run length, use the following command:

RAN *n*

where *n* defines the randomizer run length. Valid values are 0 (pass through), 9, 11, 15, 17, or 23. The randomizer output is provided at the RNRZ connector unless the convolutional encoder is enabled. The RNRZ connector then provides the convolutionally encoded data. Also, there is only one randomizer; therefore, if you have selected a randomized output code (see Section 3.4.13.2, Encoder Output), you should not change the randomizer length with this command.

3.4.13.4 CODE Output

The data at the CODE connector is either a TTL version of the data at the TAPE connector, a "pass-through" of the encoder's data source, or convolutionally encoded data. When not convolutional encoding, the CODE connector is set up using the command

CODE *mode*

where *mode* is specified as either TAPE or DATA. If you specify TAPE, the CODE connector will provide a TTL version of the PCM encoded provided at the TAPE output. If you specify DATA, the CODE connector will provide a TTL version of the encoder source. See Section 3.4.13.1, Encoder Source, for a description of how to set the encoder source. By default, the CODE output is a TTL version of the TAPE output.

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3.4.13.5 CKX2 Output

The CKX2 connector provides a programmable clock output. Program it using the command

CKX2 *multiplier*

where *multiplier* specifies the multiplier and polarity of the CKX2 output clock relative to the encoder's output data. *Multiplier* may take on the values +2, -2, +1, or -1. The + or - specifies that either the rising or falling edges of the clock are coincident with the data bit boundries. The 2 or 1 specifies the rate multiplier relative to the encoder's input data rate. Use the command described in section 3.4.10, Input Code Types, to set up the encoder input.

3.4.13.6 Viterbi Encoding (Optional)

The BSYN, with any of the above options, provides convolutional (Viterbi) encoding. The convolutionally encoded data is provided at the CODE and RNRZ connectors. The encoder is set up by the following two commands. The first command enables the encoder, the second disables it.

VENC *[type] [code] [scrambling]*
VENC OFF

The output type can be serial (with the two symbols alternating in time) or parallel, with the G1 and G2 symbols output simultaneously. Serial data is provided at the CODE connector, while parallel data is provided with the G1 symbol at the CODE connector and the G2 symbol at the RNRZ connector. If type is not specified, serial is assumed. The commands that define type are:

SER	for serial output
PAR	for parallel output

The input code can be normal (NRZ-L) or differential (NRZ-M). If code is not specified, normal is assumed. Specify code as:

NOR	normal
DIF	differential

In order to increase the number of transitions in a convolutionally encoded data stream, you can use a scrambling algorithm. You can use the CCITT V.35 algorithm, the INTELSAT algorithm, or G2 inversion which simply inverts the G2 symbol generated by the convolutional encoder. The BSYN supports all of the scrambler options, i.e. ITT, INT and G2. The BSYN also allows you to control the orientation of the G1 and G2 symbols. Specifying **REV** reverses the orientation of G1 and G2. For serial output, this means that G2 precedes G1 in time. For parallel output, this means that G1 is provided at the RNRZ connector, while G2 is provided at the CODE connector. For parallel output, you can also specify **OQ** which causes the two symbols to be staggered by one half a bit period. This is known as offset QPSK.

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3.4.14 Default Values

To revert to default values for all parameters, use the following command:

INIT

The parameter default values are listed below.

```
Source Select            0
Source Termination       LO for all inputs
Input Code               NRZ-L
Derandomizer             Off
Playback Tape Direction  FORward
Bit Rate         0
Loop Width               0.3%
Loop Tracking            0.0% (disabled)
Hi Pass Filter           DHF (disabled)
Low Pass Filter          NLF (narrow)
Decoder Clock Phase      0°
Decoder Data Polarity    NORmal
Output Clock Phase       0°
Encoder Source           IDAT (decoder data)
External Clock           +1 (0° at bit rate)
Randomizer               0 (pass through)
Encoder Output Code      BiP-L
CODE Output              TAPE (encoder output)
CKX2 Output              +2 (0° at 2x bit rate)
Convolutional Encoding   Off
```

3.4.15 Typical Setup

An example of a typical BSYN setup is shown below.

```
BITS 1           | BEGIN BIT SYNC #1 SETUP
BR=1.2E7                | SET BIT RATE TO 12MHz
BPL                     | SET INPUT CODE TO BIPHASE-L
SOURCE=1                | SELECT INPUT SOURCE 1
LW=1.5%          | SET LOOP WIDTH TO 1.5%
NOR                     | SELECT NORMAL POLARITY
FOR                     | SELECT FORWARD TAPE DIRECTION
NLF                     | SELECT LOW PASS FILTER
OUT DMM          | TAPE OUT SET FOR DELAY MILLER MARK
END                     | END OF SETUP
```


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3.5 Specifications

Specifications of the BSYN are presented in the following table.

501V-20 PCM BIT SYNCHRONIZER SPECIFICATIONS	
INPUT	**CHARACTERISTICS**
Source	Program selectable, one of five inputs
Impedance	Program selectable, 10K or 75 ohms input impedance Four single-ended/differential, one TTL-compatible
Polarity	Program selectable, normal or invert polarity
Amplitude	0.2 to 20 Vpp single-ended, 0.2 to 10 Vpp differential
DC Offset	No degradation for DC offsets up to 10 Volts Peak signal+offset shall not exceed +/-15V
Offset Variation	Tracks baseline variations equal to signal amplitude at 0.1% of bit rate without data loss
Bit Rate Range	8bps-20Mbps NRZ, Bi codes; 8bps-10Mbps Miller, RZ, Viterbi codes
Tuning Resolution	0.1% of bit rate
PCM Input Codes	13 selectable input codes: NRZ-L/M/S, Bi-L/M/S, DBi-M/S, DM-M/S, MDM-M/S, RZ
Derandomizer	RNRZ-9, 11, 15, 17, 23
Viterbi	K=7, rate 1/2
SYNCHRONIZATION	
Loop Bandwidth	Programmable, 0.1% to 3.2% of bit rate, 0.1% increments
Capture Range	+/-5% of bit rate at 3.2% loopwidth, minimum
Tracking Range	+/-12% maximum typical
Sync Acquisition	Acquires synchronization to signals as low as 0dB SNR for NRZ and Bi codes, and 3dB SNR for DM and RZ codes
Acquisition Time	Acquires sync in less than 32 bit periods with 50% transition density, typical
Sync Retention	Maintains sync on signals with 50% transition density through a minimum of 128 consecutive missing bits per 1024 bits
Bit Error Rate	Performance to 1dB of theoretical curve
Bi-Phase Ambiguity	Automatic correction for Bi, DBi, DM, or MDM codes
OUTPUT	
Clock	Programmable: 0, 90, 180, 270 - TTL-compatible
Data	NRZ-L Data, TTL-compatible
Tape Output	+/-2 Volts, balanced output
Output Code Type	Programmable, same as input codes
Randomizer	RNRZ-9, 11, 15, 17, 23
Convolutional Encoding	K=7, rate 1/2
REQUIREMENTS	
Power	+5VDC at 1.1 Amp, +12VDC at 900 mA, -12VDC at 700 mA
Temperature	Operating 0 to +40 C, non-operating -40 to +86 C
Relative Humidity	Up to 90% non-condensing
Cooling	30 linear FPM
Shock	Operating 6G, non-operating 50G
Vibration	Operating 0.5G, 5 to 2000 Hz, non-operating 1.2G, 5 to 500 Hz

Specifications are subject to change without notice.

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SECTION 4
THEORY OF OPERATION

4.1 DESCRIPTION

This chapter contains a block diagram of the 501V-20 BSYN card and its signal routing.

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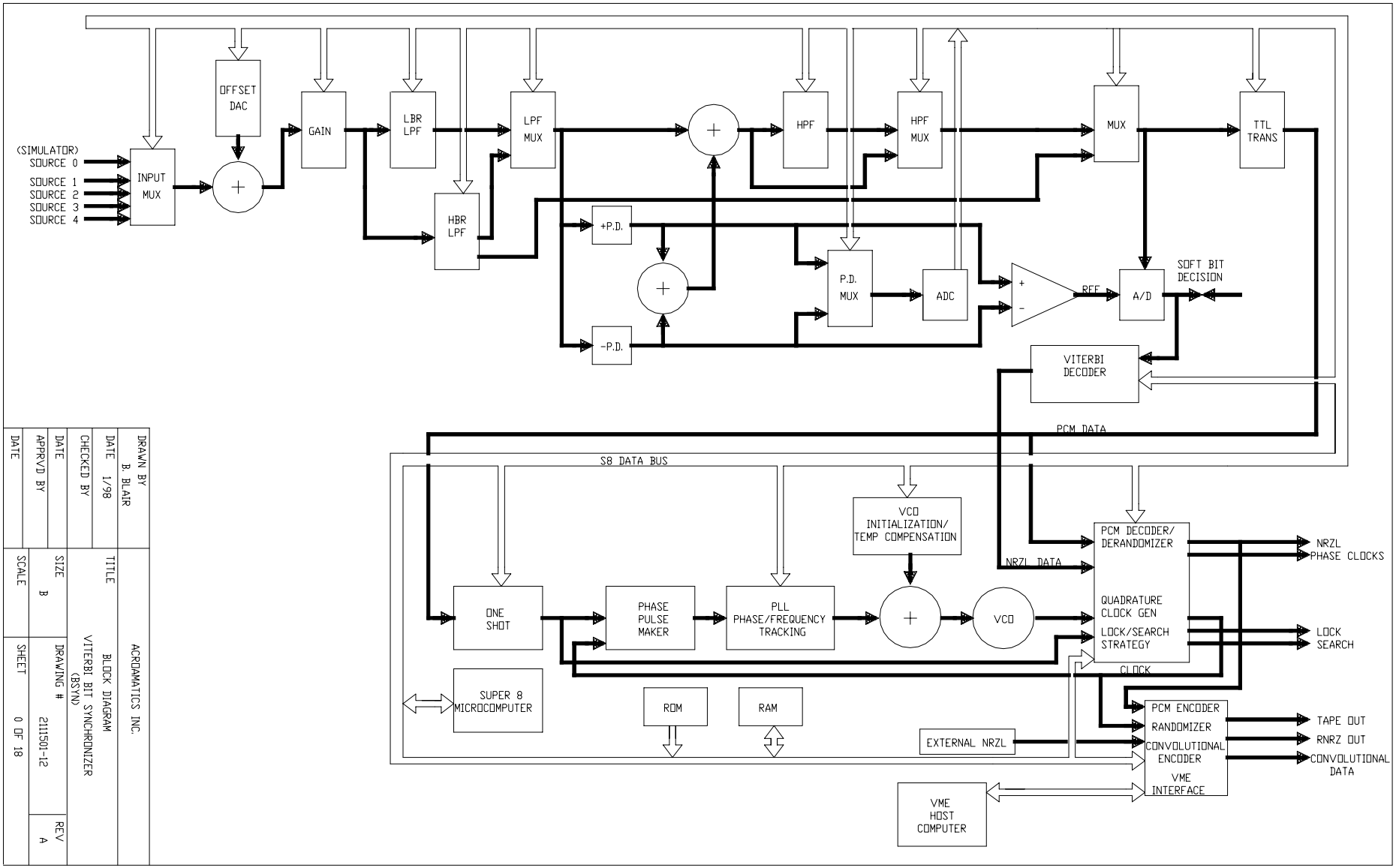


Figure 4-1. 501VA-20 Series BSYN Block Diagram.

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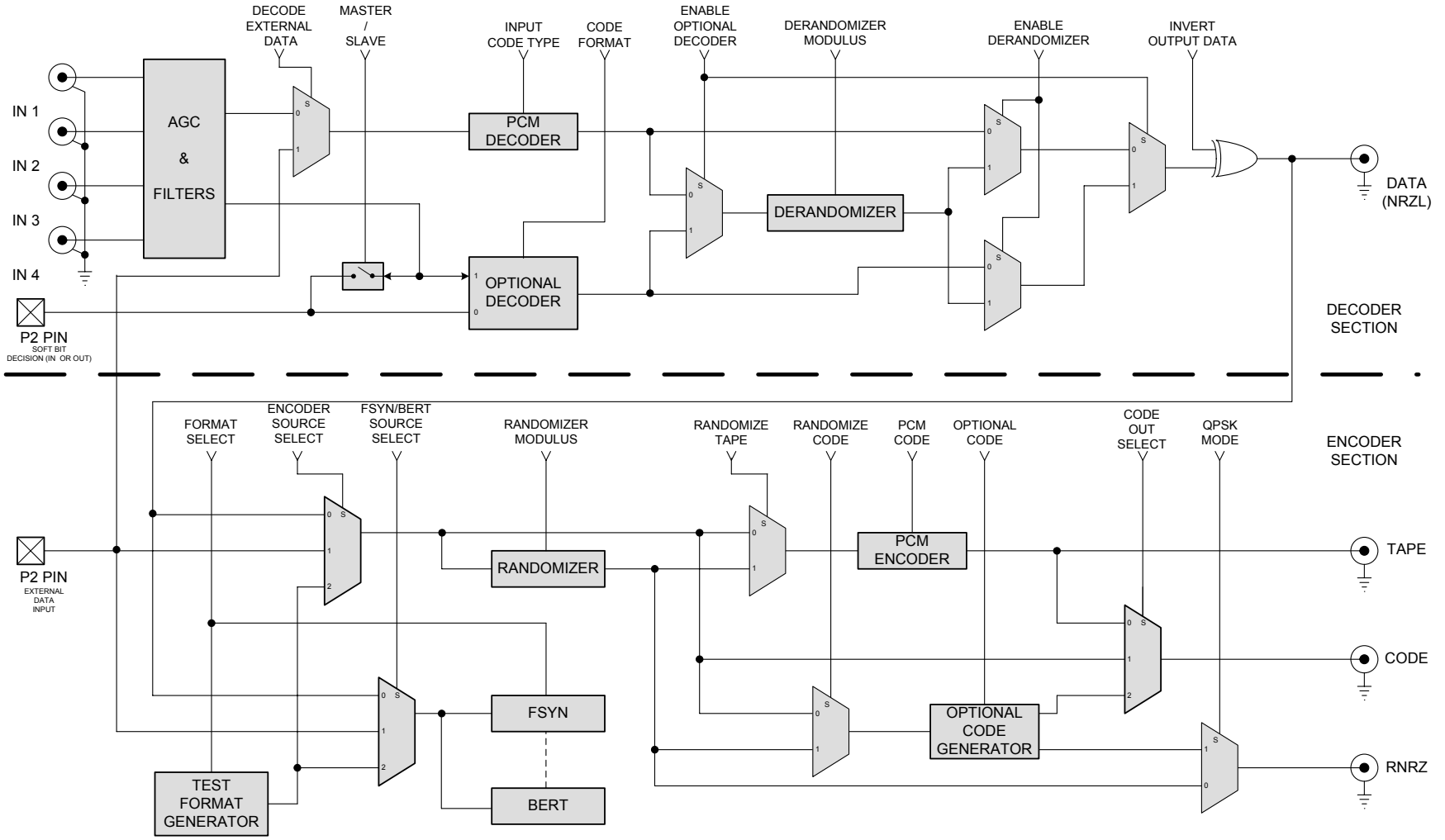


Figure 4-2. Viterbi - Bit Synchronizer Decoder/Encoder Routing

DIAG. 7000140 PG.1 REV. E

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SECTION 5
ADJUSTABLE SWITCH & JUMPER SETTINGS

5.1 DESCRIPTION

This section describes the selections available on your 501V-2x BSYN card.

5.1.1 ADDRESS SELECT

The switches U3 and U4 select the base of the 64-byte block of bit synchronizer registers in the A16:D16 address space A6 through A15. Switch U3 positions 1-8 select the eight MSBs and Switch U4 positions 1-2 select the two LSBs.

5.2 FACTORY TEST MODE

JP1 is a factory test function and must be empty for normal operation.

5.3 QUALITY WORD STATUS

Jumpers JP8, JP12, JP14, JP16, JP18, JP19, JP22, and JP24 direct the BSYN's Search and Lock status lines to P2 connector pins. You can use these TTL signals directly, or you can jumper them across the backplane to a pair of P2 connector pins on a corresponding PCM frame synchronizer. When connected across the backplane, the bit synchronizer status will be presented in the Quality Word of the frame synchronizer and on the front panel status display (if your Telemetry Data Processor has one). The BSYN and associated frame synchronizer card must be set to the same physical stream selection. Do this by matching the bit synchronizer physical stream selection with the frame synchronizer selection. See Section 2, Connector PO2, Rows A and C, as well as DN6000329 (Model 1502V PCMD) for the specific pin numbers.

5.4 SIMULATOR INPUT SELECTION

JP68 to JP71 select which one of the four format simulator outputs the BSYN board will accept as a test input from the user P2 connector. Loading considerations require that each of the four simulator outputs drive no more than two BSYN inputs.

5.5 SINGLE-ENDED/DIFFERENTIAL INPUT SELECTION

Card jumpers let you select either single-ended or differential configurations for Inputs 1 through 4. You can then select the impedance for either type of input via menu entry or software setup.

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5.5 SINGLE-ENDED/DIFFERENTIAL INPUT SELECTION

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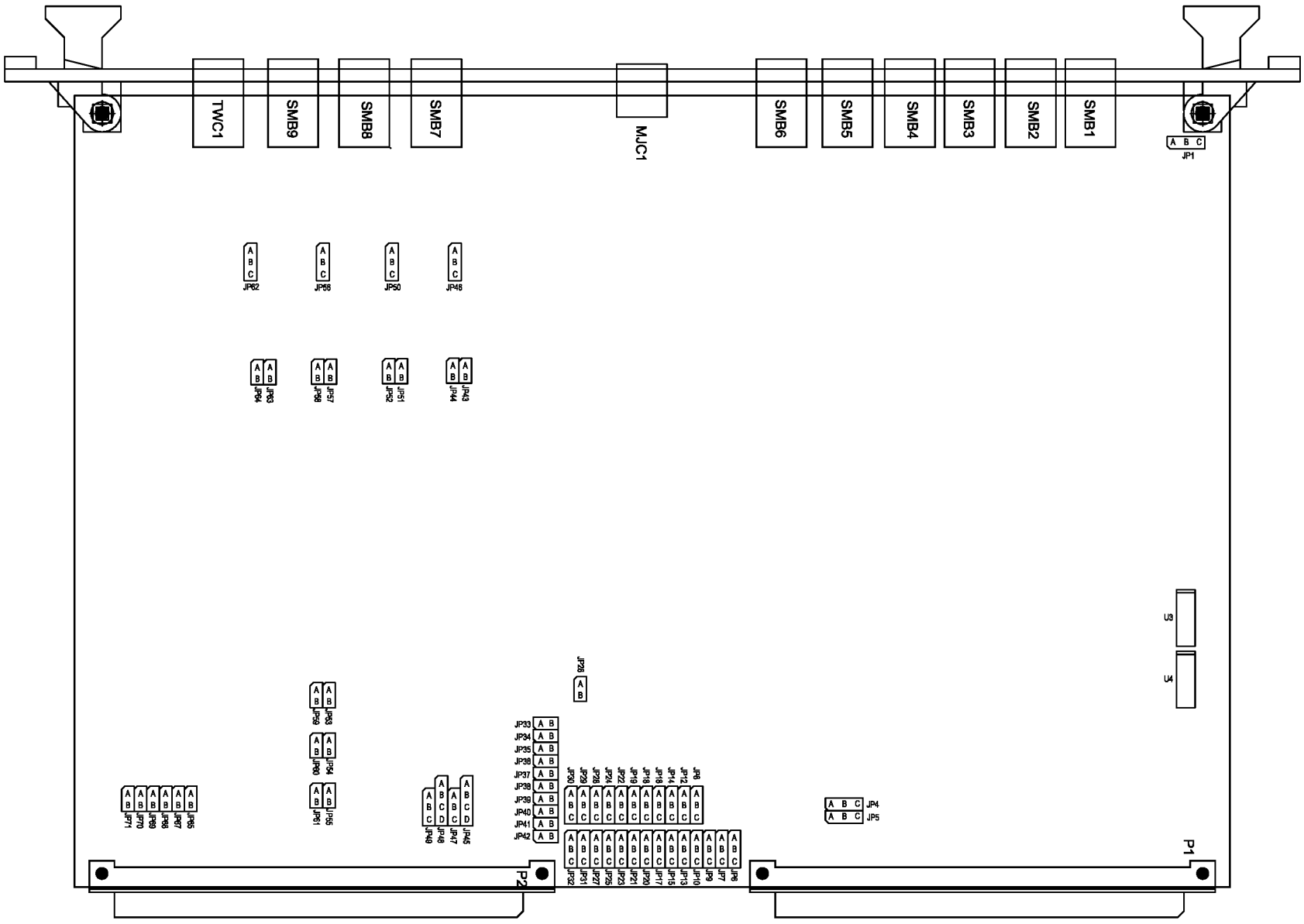
5.6 FACTORY SETTINGS

Figure 5-1 shows jumper and switch locations on the BSYN. Figure 5-2 provides a record of the factory settings when the board was shipped. Table 5-1 indicates the functions of all the possible switch and jumper selections.

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ACROAMATICS INC.

DN6000365



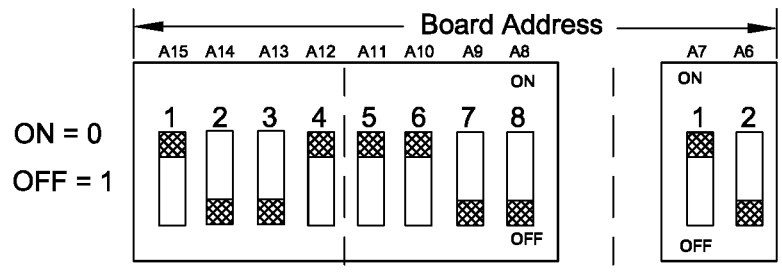
Factory Jumper Settings

	A	B	B	C
JP1			*	
JP4				
JP5				
JP6				
JP7				
JP8				
JP9				
JP10				
JP11				
JP12				
JP13				
JP14				
JP15				
JP16				
JP17				
JP18				
JP19				
JP20				
JP21				
JP22				

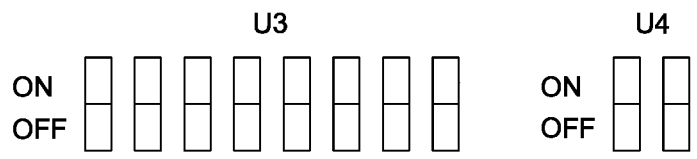
	A	B	B	C
JP23				
JP24				
JP25				
JP26				
JP27				
JP28				
JP29				
JP30				
JP31				
JP32				
JP33				
JP34				
JP35				
JP36				
JP37				
JP38				
JP39				
JP40				
JP41				
JP42				
JP43				
JP44				

	A	B	B	C	
JP45					
JP46					(1)
JP47					
JP48					
JP49					
JP50					(2)
JP51					
JP52					
JP53					
JP54					
JP55					
JP56					(3)
JP57					
JP58					
JP59					
JP60					
JP61					
JP62					(4)
JP63					
JP64					
JP65					
JP67					
JP68					(5)
JP69					(5)
JP70					(5)
JP71					(5)

DIP SWITCHES



Address 634X Shown
(Note that third nibble varies by 2 MSB's only)



* No Jumper should ever be installed here.

(1) When JP46 is at A-B (Single-ended input for channel 1) JP43, JP44 and JP59 are off.
When JP46 is at B-C (Differential input for channel 1) JP43, JP44 and JP59 are on.

(2) When JP50 is at A-B (Single-ended input for channel 2) JP51, JP52 and JP60 are off.
When JP50 is at B-C (Differential input for channel 2) JP51, JP52 and JP60 are on.

(3) When JP56 is at A-B (Single-ended input for channel 3) JP57, JP58 and JP61 are off.
When JP56 is at B-C (Differential input for channel 3) JP57, JP58 and JP61 are on.

(4) When JP62 is at A-B (Single-ended input for channel 4) JP63, JP64 are on and JP67, JP68 are off.
When JP62 is at B-C (Differential input for channel 4) JP63, JP64 are off and JP67, JP68 are on.

(5) Only one of these 4 jumpers may be installed.

SHIPPED ADDRESS _____

CARD 6011501- _____

SERIAL# / REV. _____

CUSTOMER JOB#

CONFIGURED BY DATE

QC CHECK BY DATE

DIAG. 7000407 PG.1 REV. A

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TABLE 5-1

SINGLE-ENDED CLOCK AND DATA OUTPUT CONFIGURATION

DESCRIPTION	LOCATION	INSTALLED JUMPER
NRZL DATA OR NC	P2-C18 (+)	JP33 OR NONE
BIT SYNC CLK* OR NC	P2-C19 (+)	JP34 OR NONE
NRZL DATA OR NC	P2-C26 (+)	JP35 OR NONE
BIT SYNC CLK* OR NC	P2-A26 (+)	JP36 OR NONE
GROUND OR NC	P2-A19	JP37 OR NONE
GROUND OR NC	P2-A25	JP38 OR NONE
GROUND OR NC	P2-A27	JP39 OR NONE

*NOTE, CLOCK PHASE IS CONFIGURED THROUGH SOFTWARE

RS-422 CLOCK AND DATA OUTPUT CONFIGURATION

DESCRIPTION	LOCATION	INSTALLED JUMPER
TAPE OUT	P2 - A10/C10 (+/-)	JP4 A-B / JP6 A-B / JP7 A-B
CODE	P2 - A10/C10 (+/-)	JP4 B-C / JP6 A-B / JP7 A-B
CLOCK X2	P2 - C12/A12 (+/-)	JP5 A-B / JP9 A-B / JP10 A-B
CODE CLOCK	P2 - C12/A12 (+/-)	JP5 B-C / JP9 A-B / JP10 A-B
NRZL DATA	P2 - C13/A13 (+/-)	JP21 A-B / JP22 A-B
0 DEG. CLOCK	P2 - C14/A14 (+/-)	JP23 A-B / JP24 A-B
90 DEG CLOCK	P2 - C15/A15 (+/-)	JP25 A-B / JP26 A-B
180 DEG. CLOCK	P2 - C16/A16 (+/-)	JP28 A-B / JP27 A-B
270 DEG. CLOCK	P2 - C17/A17 (+/-)	JP30 A-B / JP29 A-B

*NOTE, JP28 IS INSTALLED TO ENABLE DRIVERS FOR THESE SIGNALS. THE ABOVE CONFIFURATION IS FOR RS-422 (TWISTED PAIR). FOR SINGLE-ENDED DRIVE ANY P2 PIN MAY BECOME GROUND BY MOVING THE SHORTING PLUG TO B-C. FOR EXAMPLLE, P2-A14 BECOMES GROUND WHEN JP20 B-C IS SHORTED.

STATUS OUTPUT CONFIGURATION

DESCRIPTION	LOCATION	INSTALLED JUMPER
SEARCH1 (-)* OR FRAME SYNC	P2-C1	JP8 A-B OR JP8 B-C
SEARCH2 (-)* OR NC	P2-A1	JP12 A-B OR JP12 B-C
SEARCH3 (-)* OR GND	P2-C2	JP14 A-B OR JP14 B-C
SEARCH4 (-)* OR GND	P2-A2	JP16 A-B OR JP16 B-C
LOCK1 (-)* OR LOCK (-)	P2-A5	JP18 A-B OR JP18 B-C
LOCK2 (-)* OR SEARCH (-)	P2-C6	JP19 A-B OR JP19 B-C
LOCK3 (-)* OR LOSS (-)	P2-A6	JP22 A-B OR JP22 B-C
LOCK4 (-)* OR GND	P2-C7	JP24 A-B OR JP24 B-C
NC OR GROUND	P2-C11	JP26 A-B OR JP26 B-C
NC OR GROUND	P2-A11	JP29 A-B OR JP29 B-C
NC OR GROUND	P2-C5	JP30 A-B OR JP30 B-C
LOCK LED DRIVE (-)	P2-C24	JP40
SEARCH LED DRIVE (-)	P2-A24	JP41
LOSS LED DRIVE (-)	P2-C25	JP42

*NOTE, DEPENDING ON STREAM ASSIGNMENT, ONLY ONE SEARCH AND LOCK WILL BE SELECTED. THE DUAL STREAM BIT SYNC BOX JUMPERING IS INDICATED BY A DOTTED BORDER

SIGNAL INPUT CONFIGURATION

CHAN.	TYPE	LOCATION	IMPEDANCE	JUMPERS	
				INSTALLED JUMPER	NOT INSTALLED
		FRONT PANEL	SOFTWARE CONTROLLED (LOW IMP. IS DEFAULT)		
1	SINGLE-ENDED	SMB (J8)	75 OHM / 10K OHM	JP46 A-B	JP43, JP44, JP53, JP59
2	SINGLE-ENDED	SMB (J9)	75 OHM / 10K OHM	JP50 A-B	JP51, JP52, JP54, JP60
3	SINGLE-ENDED	SMB (J10)	75 OHM / 10K OHM	JP56 A-B	JP55, JP57, JP58, JP61
4	DIFFERENTIAL	TWINAX (J11)	125 OHM / 10K OHM	JP63, JP64, JP62 B-C	N/A
		VME 96 PIN P2			
1	DIFFERENTIAL	P2-C20/A20 (+/-)	125 OHM / 10K OHM	JP43,JP44,JP46 B-C,JP59	JP53
2	DIFFERENTIAL	P2-C21/A21 (+/-)	125 OHM / 10K OHM	JP51,JP52,JP50 B-C,JP60	JP54
3	DIFFERENTIAL	P2-C22/A22 (+/-)	125 OHM / 10K OHM	JP55,JP57,JP61,JP56 B-C	JP55
4	SINGLE-ENDED	P2-C23/A23 (A23 IS GND)	75 OHM / 10K OHM	JP62 B-C, JP67, JP68	JP63, JP64
1*	SINGLE-ENDED	P2-C20/A20 (+/GND)	125 OHM / 10K OHM	JP43,JP46 B-C,JP53,JP59	JP44
2*	SINGLE-ENDED	P2-C21/A21 (+/GND)	125 OHM / 10K OHM	JP51,JP59 B-C,JP54,JP60	JP52
3*	SINGLE-ENDED	P2-C22/A22 (+/GND)	125 OHM / 10K OHM	JP55,JP57,JP61,JP56 B-C	JP58
			(JUMPER CONFIGURED)		
EXT DATA	SINGLE-ENDED	P2-C3/A3 (+/GND)	75 OHM	JP47 B-C, JP45 A-B, C-D	
EXT DATA	SINGLE-ENDED	P2-C3/A3 (+/GND)	120 OHM	JP47 A-B, JP45 A-B, C-D	
EXT DATA	DIFFERENTIAL	P2-C3/A3 (+/-)	120 OHM	JP47 A-B, JP45 B-C	
EXT CLOCK	SINGLE-ENDED	P2-C3/A3 (+/GND)	75 OHM	JP49 B-C, JP48 A-B, C-D	
EXT CLOCK	SINGLE-ENDED	P2-C3/A3 (+/GND)	120 OHM	JP49 A-B, JP48 A-B, C-D	
EXT CLOCK	DIFFERENTIAL	P2-C3/A3 (+/-)	120 OHM	JP49 A-B, JP48 B-C	
			(FIXED)		
SIM INPUT 1	TLL/GND	P2-A28/C28	120 OHM	JP68	JP69, JP70, JP71
SIM INPUT 2	TLL/GND	P2-A29/C29	120 OHM	JP69	JP68, JP70, JP71
SIM INPUT 3	TLL/GND	P2-A30/C30	120 OHM	JP70	JP68, JP69, JP71
SIM INPUT 4	TLL/GND	P2-A31/C31	120 OHM	JP71	JP68, JP69, JP70

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SECTION 6
DRAWINGS

6.1 DESCRIPTION

This section contains the Assembly and Bill Of Materials drawings for your 501-20 BSYN, keyed to your specific serial numbered card.

Because the VME card includes so many programmed parts (PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc.), it is unlikely that you will be able to perform any repair in the field. Therefore, return all failed VME cards to the factory for repair.

See Section 2, INSTALLATION, for card removal and factory return procedures, including ESD precautions.

Call Acroamatics at (805) 967-9909 to get an RMA number before returning any equipment to the factory, and include the RMA number in any correspondence or shipments to Acroamatics.

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REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASED ECR 5075		BL		03/06
B	RELEASED ECR 5090		BL		05/06

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

LIST OF MATERIALS 6011501-21

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

PC CARD 1290250

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

SCHEMATICS 2111501-21

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

DR	I.E. STEELE	05/06
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

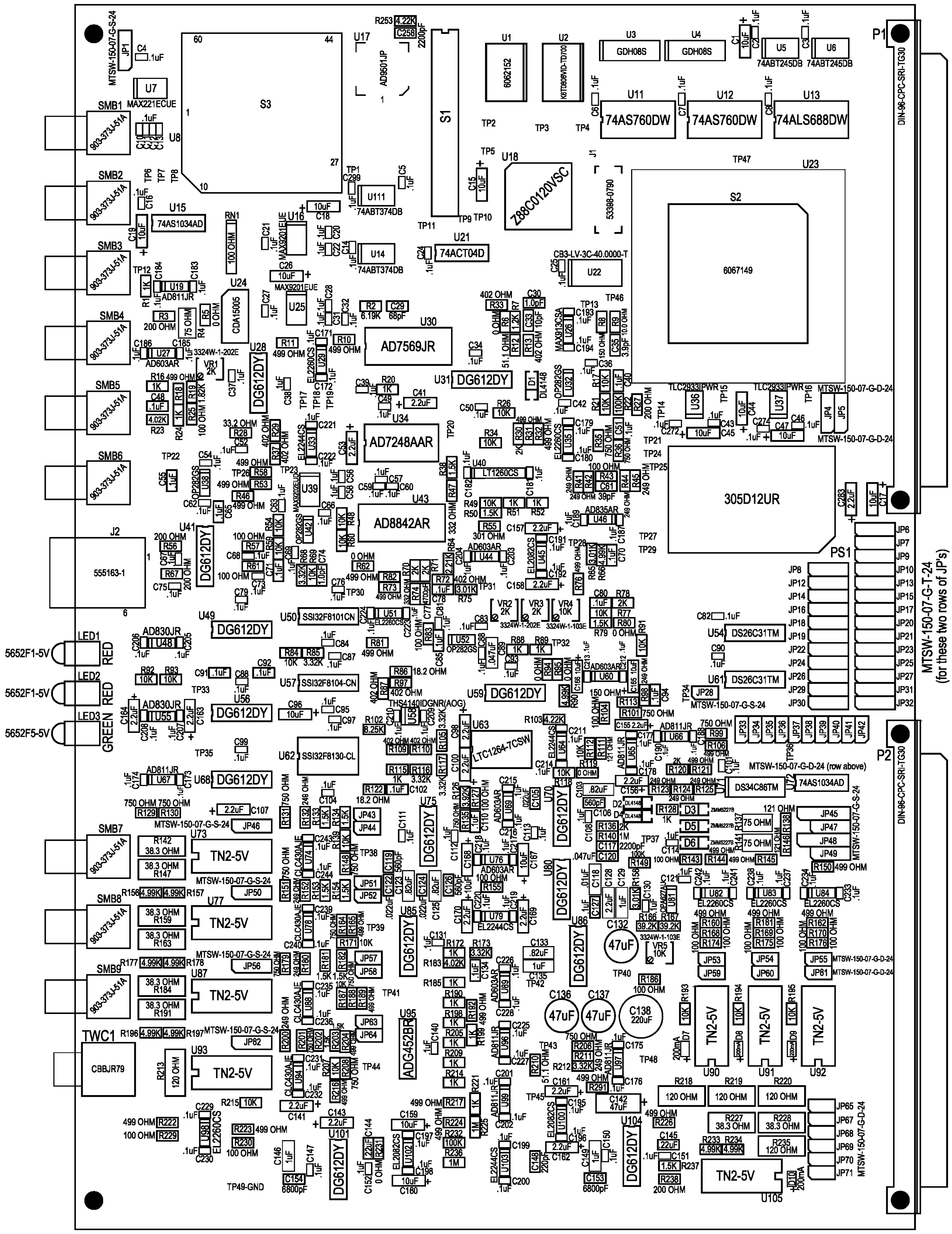
ASSEMBLY, CIRCUIT CARD

VME VITERBI BIT SYNCHRONIZER

SIZE	SCALE	DWG NO.	REV
B	NTS	6011501-21	B

SHEET 1 OF 3

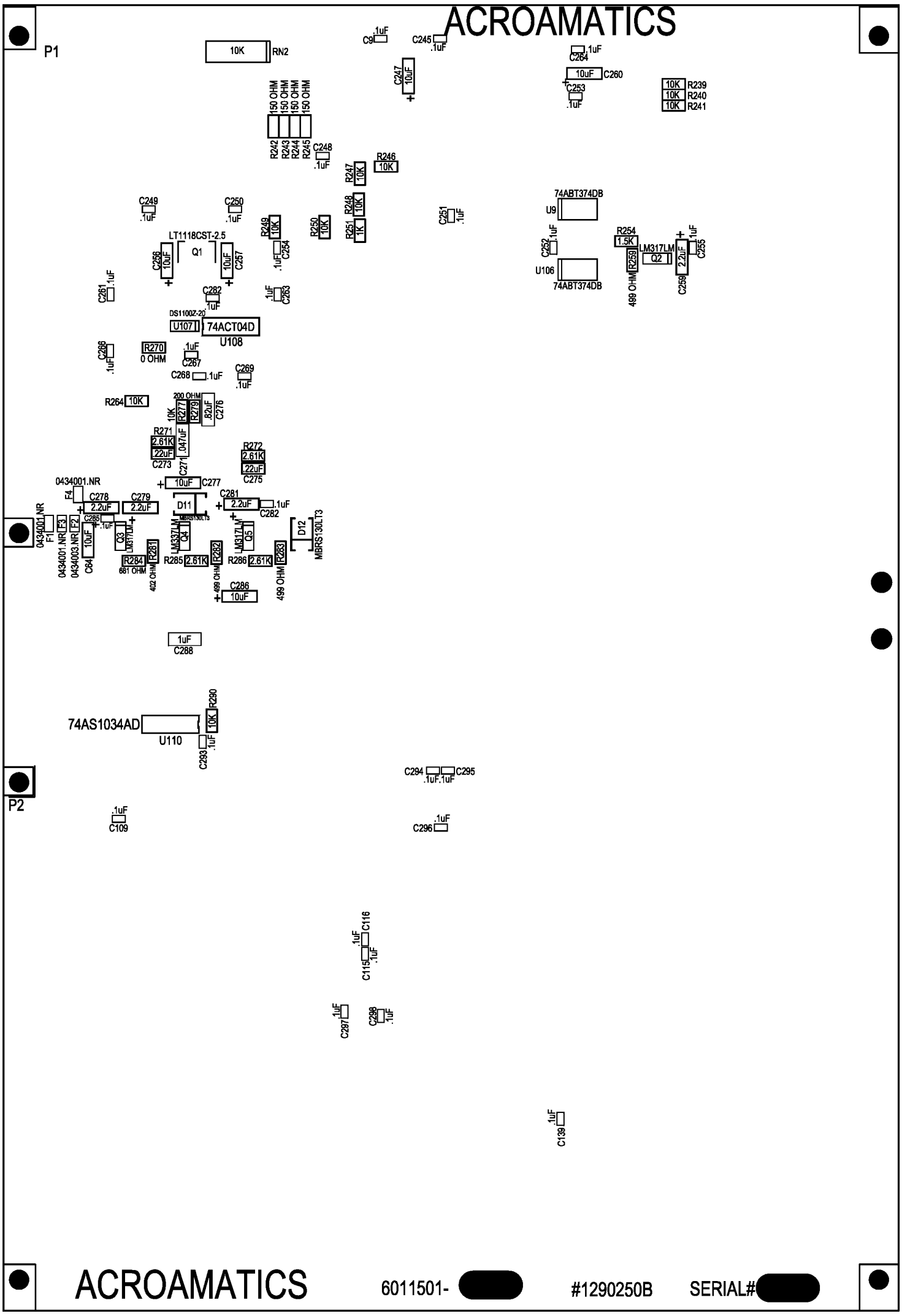
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COMPONENT SIDE

DR	I.E. STEELE	06/06	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK			
APPD			ASSEMBLY, CIRCUIT CARD VME VITERBI BIT SYNCHRONIZER
NEXT ASSY	USED ON		SIZE: B · SCALE: NTS · DWG NO. 6011501-21
APPLICATION			SHEET 2 OF 3 · REV B

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ACROAMATICS 6011501- [redacted] #1290250B SERIAL# [redacted]

SOLDER SIDE

DR I.E. STEELE	06/06	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK		ASSEMBLY, CIRCUIT CARD VME VITERBI BIT SYNCHRONIZER
APPD		SIZE B / SCALE NTS / DWG NO. 6011501-21
NEXT ASSY / USED ON		SHEET 3 OF 3 / REV B
APPLICATION		

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TELEMETRY SYSTEMS

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Drawing 6011501-21 Last Used Type Engineering

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
1	1290250	1	EACH	PCB VME VITERBI BIT SYNC	*		1290250	ACROAMATICS	
2	1903068	1	EACH	CAP X7R 4700pF 10% 50V SMT	*		ECU-V1H472KBG	PANASONIC	C77
3	1903069	17	EACH	CAP X7R .1UF 5% 50V SMT-0805	*		C0805C104J5RAC	KEMET	C40,C48,C51,C55,C65,C70,C71, C78,C80,C85,C91,C92,C94,C102, C110,C127,C134
4	1903071	3	EACH	CAP X7R 560pF 10% 50V SMT-805	*		08052R561K9B20D	YAGEO	C106,C119,C126
	1903071A	**Acceptable Substitute**					ECU-V1H561KBN	PANASONIC	
5	1903072	2	EACH	CAP X7R 2200pF 10% 50V SMT	*		ECU-V1H222KBN	PANASONIC	C117,C258
6	1903073	3	EACH	CAP X7R .047uF 10% 50V SMT	*		ECU-V1H473KBW	PANASONIC	C89,C120,C271
7	1903074	5	EACH	CAP X7R .82uF 10% 16V SMT	*		C1206C824K4RAC	KEMET	C103,C123,C125,C133,C276
8	1903075	4	EACH	CAP X7R .22uF 10% 16V SMT-805	*		ECJ-2VBIC224K	PANASONIC	C144,C145,C273,C275
9	1903076	3	EACH	CAP X7R .022uF 10% 50V SMT	*		C0805C223K5RAC	KEMET	C105,C122,C124
10	1903077	1	EACH	CAP X7R .01uF 10% 50V SMT-805	*		C0805C103K5RAC	KEMET	C118
11	1903078	2	EACH	CAP X7R 6800pF 10% 50V SMT-805	*		C0805C682K5RAC	KEMET	C153,C154
12	1903080	1	EACH	CAP X7R 2.2uF 10% 16V SMT-1206	*		ECJ-3YB1C225K	PANASONIC	C128
13	1903081	183	EACH	CAP .1uF 16V SMT-0402	*		ECJ-OEFIC104Z	PANASONIC	C2-C14,C16,C20-C22,C24,C25, C27,C28,C31,C32,C34,C36-C39, C42,C43,C46,C49,C50,C52,C54, C56-C60,C62,C63,C66-C69, C73-C76,C79,C81-C84,C86-C88, C90,C93,C95,C97,C99,C101, C104,C108,C109,C111-C116, C121,C130,C131,C139,C140, C147,C150-C152,C171-C245, C248-C255,C261-C264, C266-C269,C272,C274,C282, C285,C293-C299
14	1903086	4	EACH	CAP X7R 1UF 10% 16V SMT	*		C1206C105K4RACTU	KEMET	C129,C135,C146,C149
15	1904001	1	EACH	CAP NPO 220pF 100V 5% SMT	*		0805N221J101N	NOVACAP	C148
16	1904002	1	EACH	CAP NPO 68pF 100V 5% SMT	*		0805N680J101N	NOVACAP	C29
17	1904003	1	EACH	CAP NPO 3.9pF 100V 5% SMT	*		0805N3R9D101N	NOVACAP	C35
18	1904005	2	EACH	CAP NPO 1.0pF 100V 5% SMT	*		0805N1R0D101N	NOVACAP	C30,C74
19	1904103	1	EACH	CAP NPO 39pF 5% 50V SMT	*		ECU-V1H390JCG	PANASONIC	C61
20	1904105	1	EACH	CAP NPO 10pF 5% 50V SMT	*		ECUV1H100DCN	PANASONIC	C33
21	1904106		EACH	CAP NPO 100pF 5% 50V SMT	*		ECU-V1H101JCV	PANASONIC	
22	1916027	1	EACH	CAP NP-LYTIC 220uF 6.3v LO-PRO	*		USP0J221MCA	NICHICON	C138
23	1916028	3	EACH	CAP NP-LYTIC 47uF 6.3v LO-PRO	*		UMP0J470MDA	NICHICON	C132,C136,C137
24	1922646	22	EACH	CAP TA 2.2uF 10% 16V SMT	*		T491A225K016AS	KEMET	C41,C53,C98,C100,C107,C141, C143,C155-C158,C161-C164, C169,C170,C259,C278,C279, C281,C283
25	1922650	1	EACH	CAP TA 47uF 10% 6V SMT	*		267E6301476K-720	MATSUO	C142
	1922650A	**Acceptable Substitute**					T491C476K006AS	KEMET	

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TELEMETRY SYSTEMS

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Drawing 6011501-21 Last Used Type Engineering

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
26	1922658	23	EACH	CAP TA 10uF 10% 10V SMT	*		491A106K010AS	KEMET	C1,C15,C17-C19,C26,C44,C45, C47,C64,C96,C159,C160, C165-C168,C247,C256,C257, C260,C277,C286
27					*				
28	2796057	9	EACH	CONN PC SMB RTANGLE 1P	*		903-373J-51A	AMPHENOL	SMB1-SMB9
29	2796061	2	EACH	CONN PC 96P SDR RTANGL	*		DIN-96-CPC-SRI-TG30	3M	P1,P2
	2796061A	**Acceptable Substitute**					7296-50C2TH	3M	
30	2796064	1	EACH	CONN PC TWC RTANGLE	*		CBBJR79	TROMPETER	TWC1
31	2796083	1	EACH	CONN PC RTANGL TELEPHONE JACK	*		555163-1	AMP	J2
32	2796104	1	EACH	CONN PC 7PIN 1.25 HEADER SMT	*		53398-0790	MOLEX	J1
33	3290013	1	EACH	IC DIGITAL DELAY LINE 20ns	*		DS1100Z-20	DALLAS	U107
34	3290014	1	EACH	IC ANALOG 15ns DELAY LINE	*		CDA15005	ELMEC	U24
35	3570017	2	EACH	INDICATOR LED RED CUR LIM	*		5652F1-5V	IDI	LED1,LED2
36	3570019	1	EACH	INDICATOR LED GREEN CUR LIM	*		5652F5-5V	IDI	LED3
37	3574023	3	EACH	DIODE ZENER 3.6V 500mW SMT	*		ZMM5227B	VISHAY	D3,D5,D6
38	3573821	4	EACH	DIODE SCHOTTKY SMT 200mA	*		MA2SD10	PANASONIC	D7-D10
39	4600094	3	EACH	FUSE 1A 0603 SMT (H)	*		0434001.NR	LITTELFUSE	F1,F3,F4
40	4600096	1	EACH	FUSE 3A 0603 SMT (P)	*		0434003.NR	LITTELFUSE	F2
41					*				
42	5300002-37		EACH	IC QUAD 2 INPUT NOR GATE SMT	*		74AS02DR	TI	
43	5300004-63	2	EACH	IC HEX INVERTER SMT	*		74ACT04D	TI	U21,U108
44	5300034-37	3	EACH	IC HEX DRIVER +-48ma SMT	*		74AS1034AD	GENERIC	U15,U72,U110
45	5300245-91	2	EACH	IC OCT BUS XCVR NI TS SMT	*		74ABT245DB	GENERIC	U5,U6
46	5300374-91	4	EACH	IC OCT D-F/F EDGE-TRIG SMT	*		74ABT374CMSA	NATIONAL	U9,U14,U106,U111
	5300374-91A	**Acceptable Substitute**					74ABT374DB	TI	
47					*				
48	5300688-32	1	EACH	IC 8-BIT MAG COMP SMT	*		74ALS688DW	GENERIC	U13
49	5300760-37	2	EACH	IC OCTAL BUFFER OC NI SMT	*		74AS760DW	TI	U11,U12
50					*				
51	5301244-01	4	EACH	IC DUAL OP AMP 325v/us SMT	*		EL2244CS	ELANTEC	U33,U64,U79,U103
52	5301260	7	EACH	IC OP AMP DUAL CFB SMT	*		EL2260CS	ELANTEC	U29,U35,U51,U82-U84,U98
53	5301261	1	EACH	IC OP AMP 3x CFB W/DISABL SMT	*		LT1260CS	LINEAR-TECH	U40
54	5301282	4	EACH	IC DUAL OP AMP 9v/us SMT	*		OP282GS	ANALOG-DEVICES	U32,U38,U42,U52
55	5301612-01	14	EACH	IC QUAD SWITCH 30ohm SMT	*		DG612DY	SILICONIX	U28,U31,U41,U49,U56,U59, U68,U70,U75,U80,U85,U86, U101,U104
56	5301627-01	1	EACH	IC OP AMP 55v/us SMT	*		OPA627AU	BURR-BROWN	U81
57	5301810-01	4	EACH	IC OP AMP CFB W/DISABLE SMT	*		CLC430AJE	NATIONAL	U74,U78,U88,U94
	5301810-01A	**Acceptable Substitute**					AD810AR	ANALOG-DEVI	
58	5301811-01	7	EACH	IC OP AMP CFB 2000V/uS SMT	*		AD811JR	ANALOG-DEVICES	U19,U65-U67,U96,U97,U99
59	5301830-01	2	EACH	IC DIFF OP AMP 450/us SMT	*		AD830JR	ANALOG-DEVICES	U48,U55
60	5301913-01	1	EACH	IC VOLT COMPARATOR 10ns SMT	*		MAX913CSA	MAXIM	U26
61	5301914	2	EACH	IC VOLT COMPARATOR 7ns SMT	*		MAX9201EUE	MAXIM	U16,U25
62	5301915	1	EACH	IC VOLT COMPARATOR 7ns SMT	*		MAX9202EUD	MAXIM	U39

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No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
63	5301452	1	EACH	IC QUAD ANALOG SWITCH SMT	*		ADG452BR	ANALOG-DEVICES	U95
64	5301933	2	EACH	IC HI SPEED PLL SMT	*		TLC2933IPWR	TI	U36,U37
65	5302631-01	2	EACH	IC QUAD DIFF LN DRV SMT	*		DS26C31TM	NATIONAL	U54,U61
66	5302967	1	EACH	IC HIGH SPEED DIFF AMP	*		THS4140IDGNR(AOG)	TI	U58
67	5304126-01	1	EACH	IC 200kHz LOWPASS FILTER SMT	*		LTC1264-7CSW	LIN-TECH	U63
68	5304603	6	EACH	IC VARIABLE GAIN -10-30dB SMT	*		AD603AR	ANALOG-DEVICES	U27,U44,U60,U69,U76,U89
69	5304835	1	EACH	IC 4 QUAD MLTPLR SMT	*		AD835AR	ANALOG-DEVICES	U46
70	5304811	1	EACH	IC PRGMBLE FLTR 9M-27M SMT	*		SSI32F8101CN	SILICON-SYS	U50
71	5304815	1	EACH	IC PRGMBLE FLTR 200K-2.2M SMT	*		SSI32F8130-CL	SILICON-SYS	U62
72	5304816	1	EACH	IC PRGMBLE FLTR 3M-9M SMT	*		SSI32F8104-CN	SILICON-SYS	U57
73	5308082-01	3	EACH	IC TWO QDRNT MLTPLR SMT	*		EL2082CS	INTERSIL/QTL	U45,U100,U102
74	5308124	1	EACH	IC QUAD CMOS LINE RECEIVER	*		DS34C86TM	NATIONAL	U71
75	5308221	1	EACH	IC SNGL RS-232 XCVR SMT	*		MAX221ECUE	MAXIM	U7
76	5336622-70	1	EACH	IC 32Kx8 CMOS SRAM 70ns SMT	*		K6T0808VID-TD700	SAMSUNG	U2
	5336622-70A	**Acceptable Substitute**					KM62V256DLTGI-7	SAMSUNG	
	5336622-70B	**Acceptable Substitute**					KM62V256DLTGE-7	SAMSUNG	
77	5470011	1	EACH	JUMPER PINS SINGLE ROW 50POS	*		MTSW-150-07-G-S-24	SAMTEC	JP1,JP28,JP45-JP50,JP56,JP62
78	5470012	1	EACH	JUMPER PINS DOUBLE ROW 50POS	*		MTSW-150-07-G-D-24	SAMTEC	JP4,JP5,JP33-JP44,JP51-JP55, JP57-JP61,JP63-JP65,JP67-JP71
79	5470013	1	EACH	JUMPER PINS TRIPLE ROW 50POS	*		MTSW-150-07-G-T-24	SAMTEC	JP6-JP10,JP12-JP27,JP29-JP32
80	5400017-01	1	EACH	IC 8-BIT DAC/ADC SMT	*		AD7569JR	ANALOG DEVICES	U30
81	5400018-01	1	EACH	IC 12-BIT DAC, SMT	*		AD7248AAR	ANALOG DEVICES	U34
82	5400024-01	1	EACH	OCTAL 8 BIT SER DAC V/OUT SMT	*		AD8842AR	ANALOG DEVICES	U43
83					*				
84					*				
85	5352258	1	EACH	IC 32Kx8 OTB EPROM 70ns SMT	*		AT27LV256A-70TC	ATMEL	U1, 6062152 Rev P program prior to installation
	5352258A	**Acceptable Substitute**					AT27C256A-70TC	ATMEL	
86	6067147	1	EACH	VME BIT SYNC CONTROLLER	*	STD	5354027-REV.A	ACROAMATICS	U23
87	6128801	1	EACH	IC SPR-8 MCU 44PLCC 20MHz	*		Z88C0120VSC	ZILOG	U18
88	6250002-01	1	EACH	IC PGRM DELAY 2.5ns/10uS SMT	*		AD9501JP	ANALOG DEVICES	U17
89	6250003		EACH	IC PGMBLE DELAY 10-138 NS SMT	*		DS1021S-50	MAXIM	
90	6350057	1	EACH	OSCIL. XTAL 40.000MHZ SMT	*		CB3-LV-3C-40.0000-T	CTS	U22
91	7093060	3	EACH	4MM TRIM POT 2K 13 TURN SMT	*		3324W-1-202E	BOURNS	VR1-VR3
92	7093061	2	EACH	4MM TRIM POT 10K 13 TURN SMT	*		3324W-1-103E	BOURNS	VR4,VR5
93	7130082	1	EACH	PWR SUP 12V TO +-5V 250ma	*		305D12UR	CONVERSION-DEV.	PS1
	7130082A	**Acceptable Substitute**					BWR-5/250-D12	DATEL	
94	7555001	3	EACH	RECTIFIER HIGH SPEED SW SMT	*		DL4148	MICROSEMI	D1,D2,D4
95	7555002	2	EACH	RECTIFIER SCHOTTKY 30V 1A SMT	*		MBRS130LT3(1BL3)	MOTOROLA	D11,D12
96	7580017-01	3	EACH	REGULATOR ADJUSTABLE POS SMT	*		LM317LM	NATIONAL	Q2,Q3,Q5
97	7580018-01	1	EACH	REGULATOR ADJUSTABLE NEG SMT	*		LM337LM	NATIONAL	Q4
98	7580041	1	EACH	REGULATOR +2.5V 800ma SMT	*		LT1118CST-2.5	LINEAR	Q1
99					*				
100	7610014	8	EACH	IC DIP RELAY 5v DPST	*		TN2-5V	AROMAT	U73,U77,U87,U90-U93,U105
101	7672755	3	EACH	RES 75 OHM 1/4W 5% SMT	*		ERJ-14YJ750	PANASONIC	R4,R137,R141

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Engineer Bryan L.

Drawing 6011501-21 Last Used Type Engineering

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
102	7680909	34	EACH	RES 499 OHM .1W 1% SMT-0805	*		ERJ-6ENF499	PANASONIC	R10,R11,R18,R31,R32,R46, R53,R58,R73,R76,R81,R82, R106,R121,R144,R145,R150, R160-R162,R165,R189,R192, R204,R216,R217,R222,R223, R224,R226,R259,R282,R283, R291
103	7680911	2	EACH	RES 4.02K .1W 1% SMT-0805	*		ERJ-6ENF4.02K	PANASONIC	R23,R183
104	7680913	18	EACH	RES 100 OHM .1W 1% SMT-0805	*		ERJ-6ENF100	PANASONIC	R25,R43,R57,R61,R83,R104, R127,R143,R155,R168,R169, R170,R74-R176,R186,R229, R230
105	7680914	6	EACH	RES 150 OHM .1W 1% SMT-0805	*		ERJ-6ENF150	PANASONIC	R8,R113,R242-R245
106	7680915	16	EACH	RES 750 OHM .1W 1% SMT-0805	*		ERJ-6ENF750	PANASONIC	R35,R36,R99,R101, R129-R131,R135,R148,R151, R164,R179,R188,R201,R206, R208
107	7680916	1	EACH	RES 1.21K .1W 1% SMT-0805	*		ERJ-6ENF1.21K	PANASONIC	R7
108	7680917	2	EACH	RES 332 OHM .1W 1% SMT-0805	*		ERJ-6ENF332	PANASONIC	R47,R74
109	7680921	1	EACH	RES 2.21K .1W 1% SMT-0805	*		ERJ-6ENF2.21K	PANASONIC	R64
110	7680922	3	EACH	RES 3.01K .1W 1% SMT-0805	*		ERJ-6ENF3.01K	PANASONIC	R65,R75,R158
111	7680923	1	EACH	RES 3.92K .1W 1% SMT-0805	*		ERJ-6ENF3.92K	PANASONIC	R126
112	7680924	2	EACH	RES 4.22K .1W 1% SMT-0805	*		ERJ-6ENF4.22K	PANASONIC	R103,R253
113	7680925	1	EACH	RES 6.19K .1W 1% SMT-0805	*		ERJ-6ENF6.19K	PANASONIC	R2
114	7680926	1	EACH	RES 8.25K .1W 1% SMT-0805	*		ERJ-6ENF8.25K	PANASONIC	R102
115	7680927	3	EACH	RES 1M .1W 1% SMT-0805	*		ERJ-6ENF1M	PANASONIC	R140,R225,R236
116	7680928	13	EACH	RES 249 OHM .1W 1% SMT-0805	*		ERJ-6ENF249	PANASONIC	R41,R42,R44,R45,R98, R123-R125,R132,R152,R180, R200,R211
117	7680929	10	EACH	RES 402 OHM .1W 1% SMT-0805	*		ERJ-6ENF402	PANASONIC	R13,R29,R33,R37,R72,R87, R97,R109,R110,R281
118	7680930	2	EACH	RES 51.1 OHM .1W 1% SMT-0805	*		ERJ-6ENF51.1	PANASONIC	R12,R210
119	7680931	10	EACH	RES 4.99K .1W 1% SMT-0805	*		ERJ-6ENF4.99K	PANASONIC	R66,R90,R156,R157,R177,R178, R196,R197,R233,R234
120	7680969	2	EACH	RES 18.2 OHM .1W 1% SMT-0805	*		ERJ-6ENF18.2	PANASONIC	R86,R122
121	7680974	3	EACH	RES 121 OHM .1W 1% SMT-0805	*		ERJ-6ENF121	PANASONIC	R111,R138,R146
122	7680976	1	EACH	RES 10.0 OHM .1W 1% SMT-0805	*		ERJ-6ENF10.0	PANASONIC	R9
123	7680977	2	EACH	RES 39.2K .1W 1% SMT-0805	*		ERJ-6ENF39.2K	PANASONIC	R166,R167
124	7680979	20	EACH	RES 1K .1W 1% SMT-0805	*		ERJ-6ENF1.00K	PANASONIC	R1,R16,R20,R24,R51,R52,R88, R89,R115,R128,R172,R185, R190,R198,R199,R205,R209, R214,R221,R251
125	7680980	1	EACH	RES 33.2 OHM .1W 1% SMT-0805	*		ERJ-6ENF33.2	PANASONIC	R28

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ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011501-21 Last Used Type Engineering

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
126	7680981	36	EACH	RES 10K .1W 1% SMT-0805	*		ERJ-6ENF10.0K	PANASONIC	R17,R21,R26,R34,R39,R48, R49,R54,R59,R60,R69,R84, R91-R93,R107,R112,R118, R139,R171,R187,R193-R195, R207,R215,R239-R241, R246-R250,R252,R255,R264, R277,R290
127	7680982	7	EACH	RES 3.32K .1W 1% SMT-0805	*		ERJ-6ENF3.32K	PANASONIC	R68,R85,R105,R116,R117,R173, R212
128	7680983	3	EACH	RES 100K .1W 1% SMT-0805	*		ERJ-6ENF100K	PANASONIC	R22,R149,R232
129	7680984	6	EACH	RES 200 OHM .1W 1% SMT-0805	*		ERJ-6ENF200	PANASONIC	R3,R27,R56,R67,R238,R279
130	7680986	1	EACH	RES 681 OHM .1W 1% SMT-0805	*		ERJ-6ENF681	PANASONIC	R284
131	7680987	13	EACH	RES 1.5K .1W 1% SMT-0805	*		ERJ-6ENF1501	PANASONIC	R38,R50,R79,R133,R134,R153, R154,R181,R182,R202,R203, R237,R254
132	7680989	1	EACH	RES 1.82K .1W 1% SMT-0805	*		ERJ-6ENF1.82K	PANASONIC	R19
133	7680990	5	EACH	RES 2K .1W 1% SMT-0805	*		ERJ-6ENF2.00K	PANASONIC	R70,R71,R78,R120,R136
134	7680991	4	EACH	RES 2.61K .1W 1% SMT-0805	*		ERJ-6ENF2.61K	PANASONIC	R271,R272,R285,R286
135	7680996	1	EACH	RES 301 OHM .1W 1% SMT-0805	*		ERJ-6ENF301	PANASONIC	R55
136	7680999	6	EACH	RES 0 OHM .1W SMT-0805	*		ERJ-6GEY0R00	PANASONIC	R6,R62,R94,R119,R231,R270
137					*				
138	7690103	1	EACH	RES DIP 10K OHM 15R 16P SMT	*		4816P-T02-103	BOURNS	RN2
139	7690108	1	EACH	RES DIP 100 OHM 8R 16P SMT	*		766163101G	CTS	RN1
140	7710012	8	EACH	RES PWR 38.3 OHM 1W 5% SMT	*	STD	ERJ-1TYJ39OU	PANASONIC	R142,R147,R159,R163,R184, R191,R227,R228
141	7710015	5	EACH	RES PWR 120 OHM 1W 5% SMT-2512	*		ERJ-1TYJ121U	PANASONIC	R213,R218-R220,R235
142					*				
143	8542083	1	EACH	SOCKET 28-PIN DIP LOPRO .3W	*		115-93-328-41-0003	PRECI-DIP	S1
144	8542104	1	EACH	SOCKET 208 PIN SMT	*		IC198-208-2101	YAMAICHI	S2
145	8542068	1	EACH	SOCKET 68P CHIP CARRIER	*		540-99-068-24-000	PRECI-DIP	S3, U8
146	9070015	2	EACH	DIP SWITCH 8-POS SLIDE SMT	*		218-8LPST	CTS	U3,U4
	9070015A	**Acceptable Substitute**					GDH08S	AUGAT	
147					*				
148	5951112	1	EACH	MOD VME FR PNL VITERBI BS	*		6730092	ACROAMATICS	
149	8071177	1	EACH	SILKSCN-FP BS VITERBI	*		6730092	ACROAMATICS	

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