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# Series ACPC8625 Industrial I/O Pack
# CompactPCI Bus Non-Intelligent Carrier Board

# USER'S MANUAL

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**8500-622-E02A006**

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**IMPORTANT SAFETY CONSIDERATIONS**

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

## 1.0 GENERAL INFORMATION

The ACPC8625 card is a personal computer Compact Peripheral Component Interconnect (CompactPCI) bus card and a carrier for the Industrial I/O Pack (IP) mezzanine board field I/O modules. The carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. IP modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with IP modules may replace several dedicated function CompactPCI bus boards. The ACPC8625 non-intelligent carrier board provides impressive functionality at low cost.

Model is available in one standard CompactPCI bus 6U size. With support for up to four IP modules.

| MODEL | CompactPCI Board Size | Supported IP Slots | Operating Temperature Range |
|---|---|---|---|
| ACPC8625 | 6U | 4(A,B,C,D) | 0 to +70°C |
| ACPC8625E | 6U | 4(A,B,C,D) | -40 TO +85°C |

**KEY ACPC8625 FEATURES**

- **PCI Specification Version 2.1 and PICMG 2.0, R2.1 Compliant Slave Carrier** - Provides a CompactPCI bus interface to control and communicate with industry standard IP modules.
- **Interface for Four IP Modules** - Provides an electrical and mechanical interface for up to four industry standard IP modules. IP Modules are available from Acromag and other vendors in a wide variety of Input/Output configurations to meet the needs of varied applications.
- **Plug-And-Play CompactPCI bus Carrier** - The carrier card contains standard CompactPCI bus configuration memory.



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Upon power-up the system auto-configuration process assigns the carrier's base address in memory space.

- **Plug-And-Play Interrupt Support** - The personal computer system software will allocate one interrupt line to the carrier. The carrier's interrupt pending register can be used to quickly identify IP module pending interrupts.
- **Supports Two Interrupt Channels per IP** - Up to two interrupt requests are supported for each IP. Additional registers are associated with each interrupt request for control and status monitoring.
- **Full IP Register Access** - Makes maximum use of logically organized programmable registers on the carrier boards to provide for easy configuration and control of IP modules. Supports accesses to IP input/output, interrupt, and ID ROM data spaces. No hardware jumper settings are required on the carrier board.
- **IP Module Access Time Out** - Allows access to empty IP slots without system failure. If the IP module accessed does not respond within 32u seconds the bus access is terminated without system failure. This allows each IP slot to be probed to determine if an IP is installed. A control register bit will be set and/or issue of an interrupt request to indicate IP module time out access has occurred.
- **LED Indicators Simplify Debugging** - Front panel LED's are dedicated to each IP module to give a visual indication of successful IP accesses
- **Rear Backplane Connectors Access I/O** - Rear backplane connectors P4 and P5 access to field I/O signals mapped per the IP on CompactPCI Specification (PICMG 2.4, R1.0). A transition module (Acromag Model TRANS-C200) routes the field I/O signals from P4 and P5 to the rear of the cage system with separate SCSI-2 connectors for each IP module. All SCSI-2 connectors can be connected with a standard SCSI-2 cable from the transition module without interference from boards in adjacent slots. Spring latch hardware on the transition module provides for excellent connection integrity and easy cable removal.
- **Optional Screw Termination Panel** - Model supports field connection via screw terminals using the optional DIN rail mount termination panel (Model 5028-182).
- **Supervisory Circuit for Reset Generation** - A microprocessor supervisor circuit provides power-on, power-off, and low power detection reset signals to the IP modules per the IP specification.
- **Individually Filtered Power** - Filtered +5V, +12V, and -12V DC power is provided to the IP modules via passive filters present on each supply line serving each IP. This provides optimum filtering and isolation between the IP modules and the carrier board and allows analog signals to be accurately measured or reproduced on IP modules without signal degradation from the carrier board logic signals.
- **Individually Fused Power** - Fused +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each IP module.
- **ESD Strip on ACPC8625 Board** - The ACPC8625 board has been designed to provide electrostatic discharge (ESD) capability by using an ESD strip on the board per ANSI/VITA 1.1-1997 and IEEE1101.10.
- **Injector/Ejector Handles** - The ACPC8625 uses modern injector/ejector handles, which push the board into the rack during installation and have a positive self-locking mechanism so they cannot be unlocked accidentally. These handles are fully IEEE 1101.10 compliant and are needed to give leverage to install and remove the board.
- **EMC Front Panel** - The ACPC8625 uses the preferred EMC front panel per IEEE 1101.10 specification.
- **5 Volt CompactPCI Keying** - The ACPC8625 implements a keying mechanism to differentiate 5V or 3.3V signaling operation. This board uses 5V signaling operation. The key is inserted into the J1 connector. (Key Color: Brilliant Blue)
- **OLE Control Software is Available** - Acromag provides Object Linking and Embedding (OLE) controls software for Windows 95/98/NT™. This software (Model IPSW-OLE-PCI, MSDOS format) provides individual drivers that allow IP modules and Acromag personal computer carriers to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, Borland Delphi™, Microsoft® Office 97® applications, and others.

**CompactPCI BUS INTERFACE FEATURES**

- **Slave Module**- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.
- **Immediate Disconnect on Read** - The CompactPCI bus will immediately disconnect after a read. The read data is then stored in a read FIFO. Data in the read FIFO is then accessed by the CompactPCI bus when the read cycle is retried. This allows the CompactPCI bus to be free for other system operations while the read data is moved to the read FIFO.
- **Interrupt Support** - CompactPCI bus INTA# interrupt request is supported. All IP module interrupts are mapped to INTA#. Carrier board software programmable registers are utilized as interrupt request control and status monitors.

**SIGNAL INTERFACE PRODUCTS**

(See Appendix for more information on compatible products)

This IP carrier board will mate directly to all industry standard 8 MHz IP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board and transition module which passes them to the individual IP modules):

**Cables:**

Model 5028-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting ACPC8625 with the TRANS-C200, or other compatible carrier boards, to Model 5025-552 termination panels.

**Termination Panel:**

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag ACPC8625 with the TRANS-C200, or other compatible carrier boards, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

**CompactPCI Transition Module:**

Model TRANS-C200: This module plugs into the rear backplane directly behind the carrier board. The field I/O connections are made through the backplane to J4 and J5 connectors of the carrier board and then routed to four SCSI-2 connectors on the transition module (marked IP module slots "A through D") for rear exit from the card cage. It is available for use in CompactPCI bus card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the CompactPCI Specification (PICMG 2.0, R2.1-1997) and IEEE Standard (1101.11-1998), with a printed circuit board depth of 80mm, which is a standard transition module depth. The transition module connects to



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Acromag Termination Panel (Model 5025-552) using SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187) to the rear of the card cage, and to ACPC8625 boards within the card cage.

**IP MODULE OLE CONTROL SOFTWARE**

Acromag provides a software product (sold separately) consisting of IP module OLE (Object Linking and Embedding) drivers for Windows 95/98 and Windows NT compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow Acromag IP modules and our personal computer carriers to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, Borland Delphi™, Microsoft® Office 97® applications, and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag PCI or CompactPCI carrier and consist of a carrier OLE control, and an OLE control for each Acromag IP module as well as a generic OLE control for non-Acromag IP modules.

## 2.0 PREPARATION FOR USE

**UNPACKING AND INSPECTION**

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.




This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

**CARD CAGE CONSIDERATIONS**

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis is a cause for some concern. The dense packing of the IP modules to the carrier board alone results in elevated IP module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

**BOARD CONFIGURATION**

The carrier board is plug-and-play compatible and, as such, its board addresses are automatically assigned by the system auto-configuration routine upon power-up. The base address of the carrier board's configuration registers in memory space and I/O space is assigned. In addition, the base address of the IP modules and carrier board registers are assigned in 32-bit memory space.

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-789 and your IP module documentation for specific configuration and assembly instructions.

**Interrupt Configuration**

No hardware jumper configuration is required. All interrupt enabling, and status are configured via programmable registers on the carrier board (see Section 3 for programming details). The carrier board passes interrupt requests from the IP modules to the PCI bus. Refer to the IP modules for their specific configuration requirements.

**CONNECTORS**

Connectors of the ACPC8625 carrier consist of four carrier IP module field I/O connectors, four IP module logic connectors, and one CompactPCI bus interface connector. These interface connectors are discussed in the following sections.

**Carrier Field I/O Connectors (IP modules A through D)**

Field I/O connections are made through the rear via transition module (TRANS-C200) connectors A, B, C, and D for IP modules in positions A through D, respectively. IP module assignment is marked on the transition module for easy identification (see location drawing 4501-788 for physical locations of the IP modules). SCSI-2 Round cable assemblies and Acromag termination panels (or user defined terminations) can be quickly mated to the transition module connectors. Pin assignments are defined by the IP I/O Mapping to CompactPCI Specification (PICMG 2.4, R1.0).

Connectors A through D are 50-pin SCSI-2 right angle (female) connectors (AMP). Connectors are high-density, and there is one connector for each IP module marked with A, B, C, & D on the transition module panel. These connectors include spring latch hardware and 30 microns of gold in the mating area for excellent connection.

**IP Field I/O Connectors (IP modules A through D)**

The field side connectors of IP modules A through D mate to connectors P1, P3, P5, and P7, respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.



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P1, P3, P5, and P7 are 50-pin male plug header connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-788 & 789 for assembly details).

Pin assignments for these connectors are made by the specific IP model used and correspond identically to the pin numbers of the transition module panel connectors.

**IP Logic Interface Connectors (IP modules A through D)**

The logic interface sides of IP modules A through D mate to connectors P2, P4, P6, and P8 respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

P2, P4, P6, and P8 are 50-pin male plug header connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-789 for assembly details).

Pin assignments for these connectors are defined by the IP module specification and are shown in Table 2.1:

**Table 2.1: Standard IP Logic Interface Connections (P2,4,6,8)**

| Pin Description | Number | Pin Description | Number |
|---|---|---|---|
| GND | 1 | GND | 26 |
| CLK | 2 | +5V | 27 |
| Reset* | 3 | R/W* | 28 |
| D00 | 4 | IDSEL* | 29 |
| D01 | 5 | ***DMAReq0**** | 30 |
| D02 | 6 | ***MEMSEL**** | 31 |
| D03 | 7 | ***DMAReq1**** | 32 |
| D04 | 8 | IntSel* | 33 |
| D05 | 9 | ***DMAck0**** | 34 |
| D06 | 10 | IOSEL* | 35 |
| D07 | 11 | ***RESERVED*** | 36 |
| D08 | 12 | A1 | 37 |
| D09 | 13 | ***DMAEnd**** | 38 |
| D10 | 14 | A2 | 39 |
| D11 | 15 | ERROR* | 40 |
| D12 | 16 | A3 | 41 |
| D13 | 17 | INTReq0* | 42 |
| D14 | 18 | A4 | 43 |
| D15 | 19 | INTReq1* | 44 |
| BS0* | 20 | A5 | 45 |
| BS1* | 21 | STROBE* | 46 |
| -12V | 22 | A6 | 47 |
| +12V | 23 | ACK* | 48 |
| +5V | 24 | ***RESERVED*** | 49 |
| GND | 25 | GND | 50 |

Asterisk (*) is used to indicate an active-low signal.
***BOLD ITALIC*** Logic Lines are NOT USED by the carrier board.

**CompactPCI Bus Connections for J1**

Table 2.2 indicates the pin assignments for the CompactPCI bus signals at the J1 connector. The J1 connector is the lower rear connector on the ACPC8625 board, as viewed from the front. The connector consists of 25 rows of six pins labeled A, B, C, D, E and F. Pin A1 is located at the lower right hand corner of the connector if the board is viewed from the front component side.

Refer to the CompactPCI bus specification for additional information on the CompactPCI bus signals.

**TABLE 2.2: CompactPCI bus J1 CONNECTIONS**

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 1 | +5V | -12v | ***TRST#*** | +12V | +5V | GND |
| 2 | ***TCK*** | +5V | ***TMS*** | TDO | TDI | GND |
| 3 | INTA# | ***INTB#*** | ***INTC#*** | +5V | ***INTD#*** | GND |
| 4 | ***BR*A4*** | GND | V(I/0) | ***INTP*** | ***INTS*** | GND |
| 5 | ***BR*A5*** | ***BR*B5*** | RST# | GND | ***GNT#*** | GND |
| 6 | ***REQ#*** | GND | +3.3V | CLK | AD[31] | GND |
| 7 | AD[30] | AD[29] | AD[28] | GND | AD[27] | GND |
| 8 | AD[26] | GND | V(I/O) | AD[25] | AD[24] | GND |
| 9 | C/BE[3]# | IDSEL | AD[23] | GND | AD[22] | GND |
| 10 | AD[21] | GND | +3.3V | AD[20] | AD[19] | GND |
| 11 | AD[18] | AD[17] | AD[16] | GND | C/BE[2]# | GND |
| 12 | **KEY AREA** | | | | | GND |
| 13 | | | | | | GND |
| 14 | | | | | | GND |
| 15 | +3.3V | FRAME# | IRDY# | GND | TRDY# | GND |
| 16 | DEVSEL# | GND | V(I/O) | STOP# | LOCK# | GND |
| 17 | +3.3V | ***SDONE*** | ***SBO#*** | GND | PERR# | GND |
| 18 | SERR# | GND | +3.3V | PAR | C/BE[1]# | GND |
| 19 | +3.3V | AD[15] | AD[14] | GND | AD[13] | GND |
| 20 | AD[12] | GND | V(I/O) | AD[11] | AD[10] | GND |
| 21 | +3.3V | AD[9] | AD[8] | ***M66EN*** | C/BE[0]# | GND |
| 22 | AD[7] | GND | +3.3V | AD[6] | AD[5] | GND |
| 23 | +3.3V | AD[4] | AD[3] | +5V | AD[2] | GND |
| 24 | AD[1] | +5V | V(I/O) | AD[0] | ***ACK64#*** | GND |
| 25 | +5V | ***REQ64#*** | ***ENUM#*** | +3.3V | +5V | GND |

Pound (#) is used to indicate an active-low signal.
***BOLD ITALIC*** Logic Lines are NOT USED by the carrier board.



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**CompactPCI I/O Signals Connections for J4**

Table 2.3 indicates the pin assignments for the CompactPCI I/O signal mapping at the J4 connector. The J4 connector is the second connector from the upper rear corner on the ACPC8625 board, as viewed from the front. The connector consists of 25 rows of six pins labeled A, B, C, D, E and F. Pin A1 is located near the center of the board, viewed from the front component side. J4 is used to route IP Modules A & B field signals from the carrier to the backplane.

**TABLE 2.3: CompactPCI I/O Signals J4 CONNECTIONS**

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 1 | ***+3.3V*** | ***+3.3V*** | ***+3.3V*** | ***+5V*** | ***+5V*** | GND |
| 2 | A46 | A47 | A48 | A49 | A50 | GND |
| 3 | A41 | A42 | A43 | A44 | A45 | GND |
| 4 | A36 | A37 | A38 | A39 | A40 | GND |
| 5 | A31 | A32 | A33 | A34 | A35 | GND |
| 6 | A26 | A27 | A28 | A29 | A30 | GND |
| 7 | A21 | A22 | A23 | A24 | A25 | GND |
| 8 | A16 | A17 | A18 | A19 | A20 | GND |
| 9 | A11 | A12 | A13 | A14 | A15 | GND |
| 10 | A6 | A7 | A8 | A9 | A10 | GND |
| 11 | A1 | A2 | A3 | A4 | A5 | GND |
| 12 | | | | | | GND |
| 13 | | | **KEY AREA** | | | GND |
| 14 | | | | | | GND |
| 15 | ***+3.3V*** | ***+3.3V*** | ***+3.3V*** | ***+5V*** | ***+5V*** | GND |
| 16 | B46 | B47 | B48 | B49 | B50 | GND |
| 17 | B41 | B42 | B43 | B44 | B45 | GND |
| 18 | B36 | B37 | B38 | B39 | B40 | GND |
| 19 | B31 | B32 | B33 | B34 | B35 | GND |
| 20 | B26 | B27 | B28 | B29 | B30 | GND |
| 21 | B21 | B22 | B23 | B24 | B25 | GND |
| 22 | B16 | B17 | B18 | B19 | B20 | GND |
| 23 | B11 | B12 | B13 | B14 | B15 | GND |
| 24 | B6 | B7 | B8 | B9 | B10 | GND |
| 25 | B1 | B2 | B3 | B4 | B5 | GND |

Note: The letter in front of the number indentifies the IP Module Slot. The number indentifies the I/O pin number of that IP Module.

Example: A46 A = IP Module in Slot "A"
46 = I/O Pin number "46"
(This pin on the IP Module connects to J4, Pin 2, Row A.)

***BOLD ITALIC*** Power Lines are NOT USED by the carrier board.

The I/O signals for the J4 connector are mapped per the IP Module I/O to CompactPCI Specification (PICMG 2.4, R1.0).

**CompactPCI I/O Signals Connections for J5**

Table 2.4 indicates the pin assignments for the CompactPCI I/O signal mapping at the J5 connector. The J5 connector is the first connector from the upper rear corner on the ACPC8625 board, as viewed from the front. The connector consists of 22 rows of six pins labeled A, B, C, D, E and F. Pin A22 is located at the upper left hand corner of the connector if the board is viewed from the front component side. J5 is used to route IP Modules C & D field signals from the carrier to the backplane.

**TABLE 2.4: CompactPCI I/O Signals J5 CONNECTIONS**

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 1 | ***+3.3V*** | ***+3.3V*** | ***+3.3V*** | ***+5V*** | ***+5V*** | GND |
| 2 | C46 | C47 | C48 | C49 | C50 | GND |
| 3 | C41 | C42 | C43 | C44 | C45 | GND |
| 4 | C36 | C37 | C38 | C39 | C40 | GND |
| 5 | C31 | C32 | C33 | C34 | C35 | GND |
| 6 | C26 | C27 | C28 | C29 | C30 | GND |
| 7 | C21 | C22 | C23 | C24 | C25 | GND |
| 8 | C16 | C17 | C18 | C19 | C20 | GND |
| 9 | C11 | C12 | C13 | C14 | C15 | GND |
| 10 | C6 | C7 | C8 | C9 | C10 | GND |
| 11 | C1 | C2 | C3 | C4 | C5 | GND |
| 12 | ***+3.3V*** | ***+3.3V*** | ***+3.3V*** | ***+5V*** | ***+5V*** | GND |
| 13 | D46 | D47 | D48 | D49 | D50 | GND |
| 14 | D41 | D42 | D43 | D44 | D45 | GND |
| 15 | D36 | D37 | D38 | D39 | D40 | GND |
| 16 | D31 | D32 | D33 | D34 | D35 | GND |
| 17 | D26 | D27 | D28 | D29 | D30 | GND |
| 18 | D21 | D22 | D23 | D24 | D25 | GND |
| 19 | D16 | D17 | D18 | D19 | D20 | GND |
| 20 | D11 | D12 | D13 | D14 | D15 | GND |
| 21 | D6 | D7 | D8 | D9 | D10 | GND |
| 22 | D1 | D2 | D3 | D4 | D5 | GND |

Note: The letter in front of the number indentifies the IP Module Slot. The number indentifies the I/O pin number of that IP Module.

Example: C46 C = IP Module in Slot "C"
46 = I/O Pin number "46"
(This pin on the IP Module connects to J5, Pin 2, Row A.)

***BOLD ITALIC*** Power Lines are NOT USED by the carrier board.

The I/O signals for the J5 connector are mapped per the IP Module I/O to CompactPCI Specification (PICMG 2.4, R1.0).

**DATA TRANSFER TIMING**

All CompactPCI bus read or write cycles to the ACPC8625 are typically implemented within 150n seconds (FRAME# active to TRDY# active). After 150n seconds the CompactPCI bus is available to the system for other CompactPCI bus activity. As the CompactPCI bus is released, the ACPC8625 completes the read or write cycle to the targeted IP module or carrier register within the access times given in Table 2.5.

**TABLE 2.5: ACPC8625 Write and Read Complete Time**

| Register | Data Transfer Time |
|---|---|
| Carrier Registers Write | 650nS, Typical[1] |
| 8 and 16-bit IP Write | 750nS, Typical[1,2] |
| 32-bit IP Write | 1250nS, Typical[1,3] |
| Carrier Register Read | 500nS, Typical[1] |
| 8 and 16-bit IP Read | 650nS, Typical[1,2] |
| 32-bit IP Read | 1100nS, Typical[1,3] |

**Notes (Table 2.5):**

1. The data transfer times given in table 2.5 are measured from the falling edge of FRAME# to the falling edge of LRDYi#. The CompactPCI bus starts a data transfer cycle by driving FRAME# low. The ACPC8625 signals the completion of a read or write cycle by driving LRDYi# low.
2. This access time assumes zero IP module wait states. For each IP module wait state 125n seconds must be added to this value.



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3. This access time assumes zero IP module wait states. For each IP module wait state 250n seconds must be added to this value.

**FIELD GROUNDING CONSIDERATIONS**

Carrier boards are designed with passive filters on each supply line to each IP module. This provides maximum filtering and signal decoupling between the IP modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the CompactPCI bus and the IP grounds. Therefore, unless isolation is provided on the IP module itself, the field I/O connections are not isolated from the CompactPCI bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP input/output modules.

## 3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the ACPC8625 non-intelligent carrier board.

This Acromag ACPC8625 complies with PCI Specification Version 2.1 and CompactPCI Specification PICMG 2.0 R2.1. It is a CompactPCI bus slave carrier board for Industrial I/O Pack mezzanine (IP) modules. The carrier connects a CompactPCI host bus to the IP module's 16-bit data bus per the Industrial I/O Pack logic interface specification on the mezzanine (IP) modules which are installed on the carrier.

The CompactPCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. **The IP modules can be accessed via the CompactPCI bus memory space only.**

The CompactPCI card's configuration registers are initialized by system software at power-up to configure the card. The CompactPCI carrier is a Plug-and-Play card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A CompactPCI bus configuration access is used to access a CompactPCI card's configuration registers.

**CompactPCI Configuration Address Space**

When the computer is first powered-up, the computer's system configuration software scans the CompactPCI bus to determine what CompactPCI devices are present. The software also determines the configuration requirements of the CompactPCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the carrier requires. It then programs the carrier's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the CompactPCI carrier requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the CompactPCI carrier.

Since this CompactPCI carrier is relocatable and not hardwired in address space, this carrier's mapping and IRQ information is stored in the carrier's Configuration Space registers.

**Configuration Transactions**

The CompactPCI bus is designed to recognize certain I/O accesses initiated by the host processor as a configuration access. Configuration uses two 32-bit I/O ports located at addresses 0CF8 and 0CFC hex. These two ports are:

- 32-bit configuration address port, occupying I/O addresses 0CF8 through 0CFB hex.
- 32-bit configuration data port, occupying I/O addresses 0CFC through 0CFF hex.

Configuration space is accessed by writing a 32-bit long-word into the configuration address port that specifies the CompactPCI bus, the carrier board on the bus, and the configuration register on the carrier being accessed. A read or write to the configuration data port will then cause the configuration address value to be translated to the requested configuration cycle on the CompactPCI bus. Accesses to the configuration data port determine the size of the access to the configuration register addressed and can be an 8, 16, or 32-bit operation.

Any access to the Configuration address port that is not a 32-bit access is treated like a normal computer I/O access. Thus, computer I/O devices using 8 or 16-bit registers are not affected because they will be accessed as expected.

**Table 3.1: Configuration Address Port**

| BIT | FUNCTION |
|---|---|
| 31 | Enables accesses to Configuration Data to be translated to configuration cycles on the CompactPCI bus. |
| 30-24 | Reserved, Return 0 when read. |
| 23-16 | Bus Number<br>Choose a specific CompactPCI bus in the system. |
| 15-11 | Device Number<br>Choose a specific device/CompactPCI board on the bus. |
| 10-8 | Function Number<br>Choose a specific function in a device. Function number is zero for the ACPC8625. |
| 7-2 | Register Number<br>Used to indicate which CompactPCI Configuration Register to access. The Configuration Registers and their corresponding register numbers are given in Table 3.2. |
| 1-0 | Read Only bits that return 0. |

**Configuration Registers**

The CompactPCI specification requires software driven initialization and configuration via the Configuration Address space. This CompactPCI carrier provides 256 bytes of configuration registers for this purpose as shown in Table 3.2, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the carrier and the interrupt request line that goes active on a carrier interrupt request.



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**Table 3.2 Configuration Registers**

| Reg. Num. | D31 D24 | D23 D16 | D15 D8 | D7 D0 |
|---|---|---|---|---|
| 0 | Device ID=1024 | | Vendor ID= 10B5 | |
| 1 | Status | | Command | |
| 2 | Class Code | | | Rev ID |
| 3 | BIST | Header | Latency | Cache |
| 4 | Base Addr. Memory Mapped Configuration Registers | | | |
| 5 | Base Address for I/O Mapped Configuration Registers | | | |
| 6 | 32-bit Memory Base Address for ACPC8625 | | | |
| 7 : 10 | Not Used | | | |
| 11 | Subsystem ID | | Subsystem Vendor ID | |
| 12 | Not Used | | | |
| 13 | Reserved | | | |
| 14 | Reserved | | | |
| 15 | Max_Lat | Min_Gnt | Inter. Pin | Inter. Line |

**MEMORY MAP**

The 1K byte of memory consumed by the board is composed of blocks of memory for the ID, I/O and INT spaces corresponding to four IP modules. In addition, a small portion of the 1K byte address space contains registers specific to the function of the carrier board.

The carrier is configured to map this 1K byte block of memory into 32-bit memory space. The system configuration software will allocate space by writing the assigned address into the corresponding Base Address register of the Configuration Registers. The memory map for ACPC8625 is shown in Tables 3.3.

**Table 3.3: ACPC8625 Carrier Bd Memory Map**

| Base Address + (Hex) | High Byte D15 D08 | Low Byte D07 D00 | Base Address + (Hex) |
|---|---|---|---|
| 0001 | Bit-8 Software Reset | Carrier Board Status/Control | 0000 |
| 0003 | IP Interrupt Pending Register | | 0002 |
| 0005 | IP A Interrupt 0 Select Space | | 0004 |
| 0007 | IP A Interrupt 1 Select Space | | 0006 |
| 0009 | IP B Interrupt 0 Select Space | | 0008 |
| 000B | IP B Interrupt 1 Select Space | | 000A |
| 000D | IP C Interrupt 0 Select Space | | 000C |
| 000F | IP C Interrupt 1 Select Space | | 000E |
| 0011 | IP D Interrupt 0 Select Space | | 0010 |
| 0013 | IP D Interrupt 1 Select Space | | 0012 |
| 0015 | Not Used | | 0014 |
| 0017 | Not Used | | 0016 |
| 0019 ↓ 003F | Not Used | Not Used | 0018 ↓ 003E |
| 0041 ↓ 007F | IP A ID Space | IP A ID Space | 0040 ↓ 007E |
| 0081 ↓ 00BF | IP B ID Space | IP B ID Space | 0080 ↓ 00BE |
| 00C1 ↓ 00FF | IP C ID Space | IP C ID Space | 00C0 ↓ 00FE |
| 0101 ↓ 013F | IP D ID Space | IP D ID Space | 0100 ↓ 013E |
| 0141 ↓ 017F | Not Used | Not Used | 0140 ↓ 017E |
| 0181 ↓ 01FF | IP A I/O Space | IP A I/O Space | 0180 ↓ 01FE |
| 0201 ↓ 027F | IP B I/O Space | IP B I/O Space | 0200 ↓ 027E |
| 0281 ↓ 02FF | IP C I/O Space | IP C I/O Space | 0280 ↓ 02FE |
| 0301 ↓ 037F | IP D I/O Space | IP D I/O Space | 0300 ↓ 037E |
| 0381 ↓ 03FF | Not Used | Not Used | 0380 ↓ 03FE |

The ACPC8625 base address is determined through the CompactPCI Configuration Registers. The addresses given in Table 3.3 are relative to the base address of the ACPC8625 carrier. The addresses within each IP's own space are specific to that IP module. Refer to the IP module's User Manual for information relating to the IP specific registers.

The Carrier registers, IP Identification (ID) spaces, IP Input/Output (IO), and IP Interrupt spaces are accessible via the CompactPCI bus space as given in Table 3.3. A 32-bit CompactPCI bus access will result in two 16-bit accesses to the IP module. A 16-bit or 8-bit CompactPCI bus access results in a single 16-bit or 8-bit access to the IP module, respectively.

**Carrier Status/Control Register - (Read/Write, Base + 00H)**

The Carrier Board Status Register reflects and controls functions globally on the carrier board.

| BIT | FUNCTION |
|---|---|
| 15-09 | Not Used |
| 08 Write Only | Software Reset<br>Writing a "1" to this bit causes a software reset. Writing a "0" or reading this bit has no effect. When set, the software reset pulse will have a duration of 1u second. |
| 07-06 | Not Used |
| 05 Read and Write | IP Module Access Time Out Interrupt Pending<br>This bit will be "1" when there is an IP Module Access Time Out interrupt pending. This bit will be "0" when there is no interrupt pending. Reset condition: Set to "0". Writing a "1" to this bit will release the pending interrupt. |
| 04 Read Only | IP Module Access Time Out Status<br>Status bit to indicate that the last IP module access has timed out. This bit only reflects the last IP module access.<br>"0" if last IP module access did not time out.<br>"1" if last IP module access did time out. |
| 03 Read and | Time Out Interrupt Enable<br>When set to "1", this bit will enable the carrier board to generate an interrupt upon time out of an |



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| BIT | FUNCTION |
|---|---|
| Write | IP module access. The default setting or reset condition is “0” (interrupt generation upon time out disabled). The interrupt service routine, in responding to the Time Out Access interrupt, will need to set this bit to 0 to clear the pending interrupt request. |
| 02 Read and Write | IP Module Interrupt Enable<br>When set to “1”, this bit will enable the generation of IP module interrupts. The default setting or reset condition is “0” (IP module interrupt generation disabled). Interrupts must also be supported and configured at the IPs. |
| 01 Read Only | IP Module Interrupt Pending<br>This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the IP Module's pending interrupt status, even if the IP Module Interrupt Enable bit is set to "0". Reset condition: Set to "0". |
| 00 Read Only | IP Module Error<br>This bit will be "1" when there is an active IP Module Error signal. This bit will be "0" when all IP module Error signals are inactive. This bit allows the user to monitor the Error signals of IP modules A through D. The Industrial I/O Pack specification states that the error signals indicate a non-recoverable error from the IP (such as a component failure or hard-wired configuration error). Refer to your IP specific documentation to see if the error signal is supported and what it indicates. Reset condition: Set to "0". |

**IP Interrupt Pending Register - (Read, Base + 02H)**

The IP Interrupt Pending Register is used to individually identify pending IP interrupts or a pending carrier generated interrupt as a result of IP module time out access. If multiple IP interrupts are pending, software must determine the order in which they are serviced.

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| IP D Int1 Pend | IP D Int0 Pend | IP C Int1 Pend | IP C Int0 Pend | IP B Int1 Pend | IP B Int0 Pend | IP A Int1 Pend | IP A Int0 Pend |

| MSB D15 | D14 | D13 | D12 | D11 | D10 | D9 | LSB D8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | | Time Out Interrupt Pend | Not Used | Not Used |

Where:

| | |
|---|---|
| All Bits IP Interrupt Pending (Read) | A bit will be a “1” when the corresponding interrupt is pending. A bit will be a “0” when its corresponding interrupt is not pending. Polling this bit will reflect the IP module's pending interrupt status, even if the IP interrupt enable bit is set to “0”. Reset Condition: Set to "0". An IP module pending interrupt bit will be cleared if its corresponding interrupt request signal is inactive. |

**IP Module Interrupt Space - (Read Only)**

The Interrupt space for each IP module is fixed at two 16-bit words. Interrupt 0 select space is read, typically by an interrupt service routine, to respond to an interrupt request via the IP Module's INTREQ0* signal. Likewise interrupt 1 select space is read to respond to an interrupt request via the IP Module's INTREQ1* signal. An access to an interrupt select space results in the IP module serving up an interrupt vector. In addition, access to the interrupt space will cause some IP modules to release their interrupt request. See each IP module's User Manual for details.

**IP Module ID Space - (Read Only)**

Each IP contains identification (ID) information that resides in the ID space per the IP specification. This area of memory contains either 32 bytes (Format I ID) or 64 bytes (Format II ID) of information, at most. Format I requires read of only the least significant byte. Format II requires read of a 16-bit value. The carrier will implement 16-bit reads to the ID space to allow support for either Format I or Format II. Both fixed and variable information may be present within the ID ROM. Variable information may include unique information required for the module. The identification Section for each IP module is located in the carrier board memory map per Table 3.3. Refer to the documentation of your IP module for specific information about each IP module's ID Space contents.

**IP Module I/O Space - (Read/Write Only, 256-Byte Addresses)**

The I/O space on each IP module is fixed at 128, 16-bit words (256 bytes). The four IP module I/O spaces are accessible at fixed offsets for the ACPC8625's Base Address. IP modules may not fully decode their I/O space and may use byte or word only accesses. See each IP module's User Manual for details.

**GENERATING INTERRUPTS**

Interrupt requests originate from the carrier board in the case of an access time out and from the IP modules. Each IP may support 0, 1, or 2 interrupt requests. Upon an IP module interrupt request the carrier passes the interrupt request on to the host, provided that the carrier board is enabled for interrupts within the Carrier Board Status Register.

**Sequence of Events For an Interrupt**

1. Clear the interrupt enable bits in the Carrier Board Status Register by writing a "0" to bit 2/bit 3.
2. Write interrupt vector to the location specified on the IP and perform any other IP specific configuration required - do for each supported IP interrupt request.
3. Determine the IRQ line assigned to the carrier during system configuration (within the configuration register).
4. Set up the CPU's interrupt vector for the appropriate interrupt.
5. Unmask the IRQ on the CPU's 8259 (or equivalent) interrupt controller.
6. The IP asserts an interrupt request to the carrier board (asserts interrupt request line IntReq0* or IntReq1*).
7. The carrier drives PCI bus interrupt request signal INTA# active.
8. CPU drives the IRQ line assigned to the active carrier.
9. The interrupt service routine pointed to by the vector set up in step 4 starts.
10. Interrupt service routine determines which IP module caused the interrupt by reading the carrier interrupt pending register. If multiple interrupts are pending the interrupt service routine



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software determines which IP module to service first. In a CompactPCI System interrupts are shared and can be from any slot on the backplane. The routine must first check that the interrupt came from the CompactPCI carrier by reading the carrier interrupt pending register.

11. The interrupt service routine accesses the interrupt space of the IP module selected to be serviced. Note that the interrupt space accessed must correspond to the interrupt request signal driven by the IP module.
12. The carrier board will assert the INTSEL* signal to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*; A1 high corresponds to INTREQ1*).
13. The IP module receives an active INTSEL* signal from the carrier and supplies its interrupt vector to the host system during this interrupt acknowledge cycle. An IP module designed to release its interrupt request on acknowledge will release its request upon receiving an active INTSEL* signal from the carrier. If the IP module is designed to release its interrupt request on register access the interrupt service routine must access the required register to clear the interrupt request.
14. Write "End-Of-Interrupt" command to CPU's 8259 (or equivalent).
15. If the IP interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board negates its interrupt request INTA#).

## 4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the carrier board. Refer to the Block Diagram shown in the Drawing 4501-790 as you review this material.

### CARRIER BOARD OVERVIEW

The carrier board is a CompactPCI bus slave/target board providing up to four industry standard IP module interfaces. The carrier board's CompactPCI bus interface allows an intelligent single board computer (CompactPCI bus Master) to control and communicate with IP modules that are present on the CompactPCI bus carrier. IP module field I/O connections link to the field I/O connections of the carrier which in turn are used to connect field electronic hardware to the carrier board via SCSI-2 cable and TRANS-C200 transition module.

The CompactPCI bus and IP module logic commons have a direct electrical connection (i.e., they are not electrically isolated). However, the field I/O connections can be isolated from the PCI bus if an IP module that provides this isolation (between the logic and field side) is utilized. A wide variety of IP modules are currently available (from Acromag and other vendors) that allow interface to many external devices for digital I/O, analog I/O, and communication applications.

### CompactPCI Bus Interface

The carrier board's CompactPCI bus interface is used to program and monitor carrier board registers for configuration and control of the board's documented modes of operation (see section 3). In addition, the CompactPCI bus interface is also used to communicate with and control external devices that are connected to an IP module's field I/O signals (assuming an IP module is present on the carrier board).

The CompactPCI bus interface is implemented in the logic of the carrier board's CompactPCI bus target interface chip. The CompactPCI bus interface chip implements PCI Specification Version 2.1 and CompactPCI Specifications PICMG 2.0 R2.1 as an interrupting slave including 8-bit and 16-bit data transfers to the IP modules.

The carrier board's CompactPCI bus data transfer rates are shown in Table 2.5.

### Carrier Board Registers

The carrier board registers (presented in section 3) are implemented in the logic of the carrier board's Field Programmable Gate Array (FPGA). An outline of the functions provided by the carrier board registers includes:

- Monitoring the error signal received from each IP module is possible via the **IP Error Bit**.
- Enabling of CompactPCI bus interrupt requests from each IP module is possible via the **IP Module Interrupt Enable Bit**.
- Enabling of interrupt generation upon an IP module access time out is implemented via the **Time Out Interrupt Enable Bit.**
- Monitoring an IP module access time out is possible via the **IP Module Access Time Out Status Bit.**
- Identify pending interrupts via the carrier's **IP Module Interrupt Pending Bit**.
- Lastly, pending interrupts can be individually monitored via the **IP Module Interrupt Pending register**.

### IP Logic Interface

The IP logic interface is also implemented in the logic of the carrier board's FPGA. The carrier board implements ANSI/VITA 4 1995 Industrial I/O Pack logic interface specification and includes four IP logic interfaces. The CompactPCI bus address and data lines are linked to the address and data of the IP logic interface. This link is implemented and controlled by the carrier board's FPGA.

The CompactPCI bus to IP logic interface link allows a CompactPCI bus master to:

- Access up to 64 ID Space bytes for IP module identification via 8-bit or 16-bit data transfers using CompactPCI bus.
- Access up to 128 I/O Space bytes of IP data via 8-bit or 16-bit data transfers.
- Access IP module interrupt space via 8-bit or 16-bit CompactPCI bus data transfers.
- Respond to two IP module interrupt requests per IP module.

### Carrier Board Clock Circuitry

A 16MHz clock is divided down by a clock driver to obtain the IP module 8MHz clock signals. Separate IP clocks are driven to each IP module. All clock lines include series damping resistors to reduce clock overshoot and undershoot.

When an IP module places data on the bus, for all data read cycles, any undriven data lines are read by the CompactPCI bus as high because of pull-up resisters on the carrier board's data bus.

### CompactPCI Interrupter

Interrupts are initiated from an interrupting IP module. However, the carrier board will only pass an interrupt generated by an IP module to the CompactPCI bus if the carrier board has been first enabled for interrupts. Each IP module can initiate two interrupts which can be individually monitored on the carrier board. After interrupts are enabled on the carrier board via the Interrupt Enable Bits (see section 3 for programming details), an IP generated



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interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register.

A carrier board pending interrupt will cause the board to pass the interrupt to the CompactPCI bus provided the Interrupt Enable bits of the carrier's Status Register have been enabled (see section 3 for programming details). The PC interrupt request line assigned by the system configuration software will then be asserted. The CPU will respond to the asserted interrupt line by executing the interrupt service routine corresponding to the interrupt line asserted. The interrupt service routine is executed only if the IRQ on the CPU's 8259 interrupt controller has been previously unmasked (see section 3 for programming details).

The interrupt service routine should respond to an interrupt by accessing IP Interrupt Select (INTSEL*) space. The interrupt service routine should also conclude the interrupt routine by writing the "End-Of-Interrupt" command to the CPU's 8259 interrupt controller (see section 3 for more details).

**Power Failure Monitor**

The carrier board contains a 5 volt undervoltage monitoring circuit which provides a reset to the IP modules when the 5 volt power drops below 4.27 volts typical / 4.15 volts minimum. This circuitry is implemented per the Industrial I/O Pack specification.

**Power Supply Fuses**

The +5V, supply lines to each of the IP modules are individually fused with a current limit of 2 amp imposed by the fuses. In addition, the +12, and -12 supply lines to each of the IP modules are individually fused with a current limit of 1 amp imposed by the fuses. A blown fuse can be identified by visible inspection or by use of an ohm meter. The fuses are located under each IP slot near the "logic connectors" (see figure 4501-788).

**Power Supply Filters**

Power line filters are dedicated to each IP module for filtering of the +5, +12, and -12 volt supplies. The power line filters are a "T" type filter circuit comprising ferrite bead inductors and a feed-through capacitor. The filters provide improved noise performance as is required on precision analog IP modules.

## 5.0 SERVICE AND REPAIR

**SERVICE AND REPAIR ASSISTANCE**

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

**PRELIMINARY SERVICE PROCEDURE**

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

## 6.0 SPECIFICATIONS

**PHYSICAL**

Physical Configuration.....CompactPCI 5 V Board
Length.....9.187 inches (233.3 mm)
Width.....6.299 inches (160.0 mm)
Board Thickness.....0.062 inches (1.59 mm)
Max Component Height.....0.550 inches (13.97 mm)
Max Component
Height Under IP Modules.....0.180 inches (4.57 mm)
Recommended Card Spacing.....0.800 inches (20.32 mm)

Connectors:

J1 (CompactPCI Bus).....PCI Specification Version 2.1 & CompactPCI Specification PICMG 2.0 R2.1 5 V Board. Type "A" right-angle female connector, 110 contacts with upper shield.

**Note:** A 5 volt coding key is inserted into J1 connector to allow this card to be plugged into a 5 volt backplane system only. (Key Color: Brilliant Blue)

J4, J5 (CompactPCI Field I/O).....CompactPCI Specification PICMG 2.4 R1.0. IP field I/O mapping to CompactPCI field I/O. Type "B" right-angle female connector, 110 contacts with upper shield.

**Note: J4 and J5 are <u>not</u> compliant with Computer Telephony Specification. (H.110 and Telephony I/O)**

P1,3,5, 7 (IP Field I/O).....50-pin male plug header (AMP 173280-3 or equivalent).
P2,4,6, 8 (IP Logic).....50-pin male plug header (AMP 173280-3 or equivalent).

Power:

Board power requirements are a function of the installed IP modules. This specification lists currents for the carrier board only. The carrier board provides +5V, +12V and -12V power to each IP from the CompactPCI bus. Each IP module supply line is individually filtered and fused.

Fuses: +5 volts, 2 amp per slot
±12 volts, 1 amp per slot



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The power failure monitor circuit provides a reset to IP modules when the 5 volt power drops below 4.27 volts typically / 4.15 volts minimum.

Currents specified are for the carrier board only, add the IP module currents for the total current required from each supply.

+5 Volts (±5%)..... 180mA, Typical
250mA, Maximum.
+12 Volts (±5%)..... 0mA (Not Used)
-12 Volts (±5%)..... 0mA (Not Used)

**CompactPCI BUS COMPLIANCE**

Specification..... This device meets or exceeds all written PCI Specification Version 2.1 & CompactPCI Specification PICMG 2.0 R2.1.
Data Transfer Bus.....Slave with 32-bit, 16-bit, and 8-bit data transfer operation. 32-bit read or write accesses are implemented as two 16 bit transfers to the IP modules.
CompactPCI bus Write Cycle Time.....150nS typical measured from falling edge of FRAME# to the falling edge of TRDY#.
CompactPCI bus Read Cycle Time.....150nS typical; The carrier issues a RETRY which frees the CompactPCI bus while the read request is completed. The CompactPCI bus will repeat the same read request until it completes with the requested data.
ACPC8625 Write Complete Time..... Time from FRAME# active until LRDYi# active. 650nS typical carrier register; 750nS typical 8-bit and 16-bit IP module write assuming 0 IP module wait states). 1250nS typical 32-bit IP module write (assuming 0 IP module wait states).
ACPC8625 Read Complete Time.....Time from FRAME# active until LRDYi# active. 500nS typical carrier register; 650nS typical 8-bit and 16-bit IP module read (assuming 0 IP module wait states). 1100nS typical 32-bit IP module read (assuming 0 IP module wait states).
Interrupts.....CompactPCIbus INTA# interrupt signal. Up to two requests sourced from each IP mapped to INTA#. Interrupt vectors come from IP modules via access to IP module INT space.
32-bit Memory Space..... Upon power-up the system auto-configuration process (plug & play) maps the carrier's base address (for a 1K byte block of memory) into the PCI bus 32-bit Memory Space.

**INDUSTRIAL I/O PACK COMPLIANCE**

Specification.....This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 (For 8MHz operation only) and IP I/O Mapping to CompactPCI (PICMG 2.4 R1.0).
Electrical/Mechanical Interface....Carrier supports four single-size IP modules (A-D), or two double-size IP module. 32-bit IP modules are not supported.
I/O Space.....16-bit and 8-bit: Supports 128 byte values per IP module.
ID Space..... A16/D08(O); supports 32 bytes per IP (consecutive odd-byte addresses) ID Data Format I. D16 is also supported with pull-ups on the carrier board holding the upper 8-bits high.
Memory Space..... Not Supported.
Interrupts..... Supports two interrupt requests per IP and interrupt acknowledge cycles via access to IP INT space.
Access LED (Illuminate duration)..... 0.125 second, typical

**ENVIRONMENTAL**

Operating Temperature.....0 to +70°C; -40 to +85°C (E Versions) Note that visual LED performance may be degraded below -20°C.
Relative Humidity..... 5-95% non-condensing
Storage Temperature..... -55 to +100°C.
Non-Isolated.....CompactPCI bus and IP module logic commons have a direct electrical connection. As such, unless the IP module provides isolation between the logic and field side, the field I/O connections are not isolated from the CompactPCI bus.
Radiated Field Immunity (RFI)..... Designed to comply with IEC1000-4-3 Level 3 (10V/m at frequencies 27MHz to 500MHz) and European Norm EN50082-1.
Electromagnetic Interference Immunity (EMI)..... No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Electrostatic Discharge Immunity (ESD)..... Complies with IEC1000-4-2 Level 1 (2KV direct contact discharge) at field input/output terminals and European Norm EN50082-1.
Electric Fast Transient Immunity EFT..... Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.



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Radiated Emissions..... Meets or exceeds European Norm EN50081-1 for class A equipment.

## APPENDIX

**CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)**

Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the TRANS-C200 Transition Module. The transition module then connects to all four IP module slots to the rear of the ACPC8625 (Slots A-D).
Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other length. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware. (Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a "D Shell" and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.'s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

**TERMINATION PANEL: MODEL 5025-552**

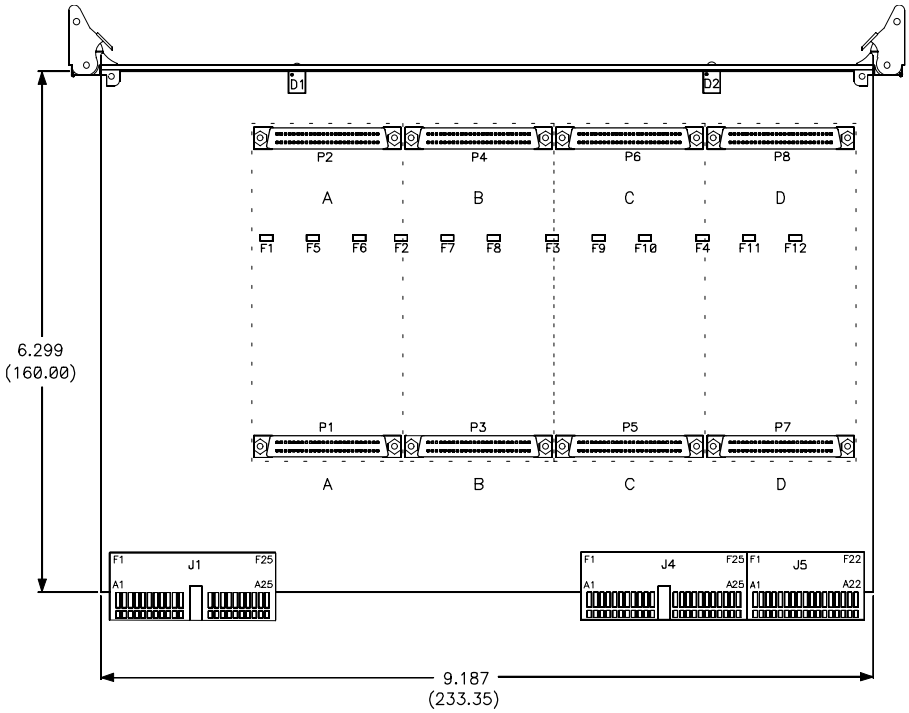
Type: Termination Panel For Carrier Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the TRANS-C200 transition module via a cable (Model 5028-187). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to TRANS-C200 Transition Module: P1, 50-pin male header with strain relief ejectors. Use Acromag 5028-187 cable to connect panel to TRANS-C200 transition module. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packed.

**CompactPCI TRANSITION MODULE: MODEL TRANS-C200**

Type: Transition module for ACPC8625 board.
Application: To repeat field I/O signals of IP modules A through D for rear exit from CompactPCI card cages. This module is available for use in card cages which provide rear exit for I/O connections via 80 mm wide transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the CompactPCI bus mechanical dimensions and IEEE Standard (1101.11-1998), for 80 mm depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to ACPC8625 boards within card cage, via connectors P4 and P5.
Schematic and Physical Attributes: See Drawing 4501-791.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.'s).
Field Wiring: Four SCSI-2, 50-pin female connectors (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via round shielded cable (Model 5028-187).
Connections to ACPC8625: Connections are made though the PC board connectors P4 and P5 (right-angle female connector, 110 contacts with upper shield. The transition module plugs directly behind the ACPC8625 board into the CompactPCI bus backplane within the card cage system.
Mounting: Transition module is inserted into a 6U-size, 80 mm width slot at the rear of the CompactPCI bus card cage. (Directly behind ACPC8625 board)
Printed Circuit Board: Eight-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.

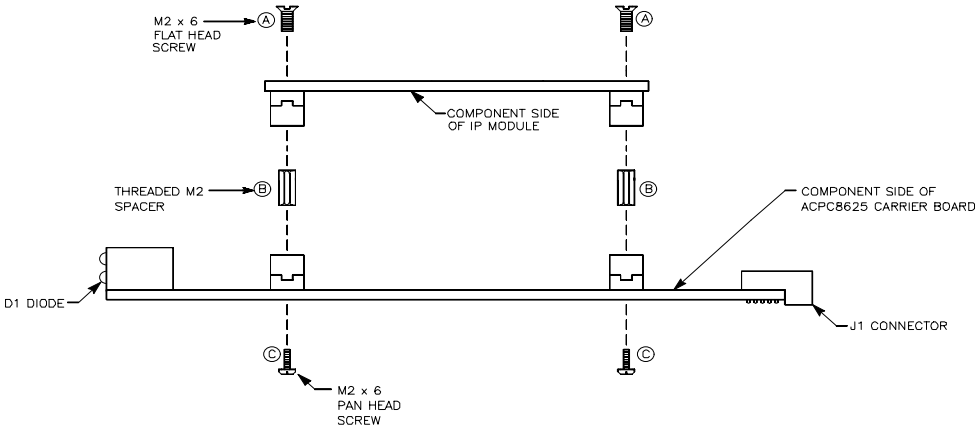


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NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

ACPC8625 IP LOCATIONS 4501–788A




ASSEMBLY PROCEDURE:

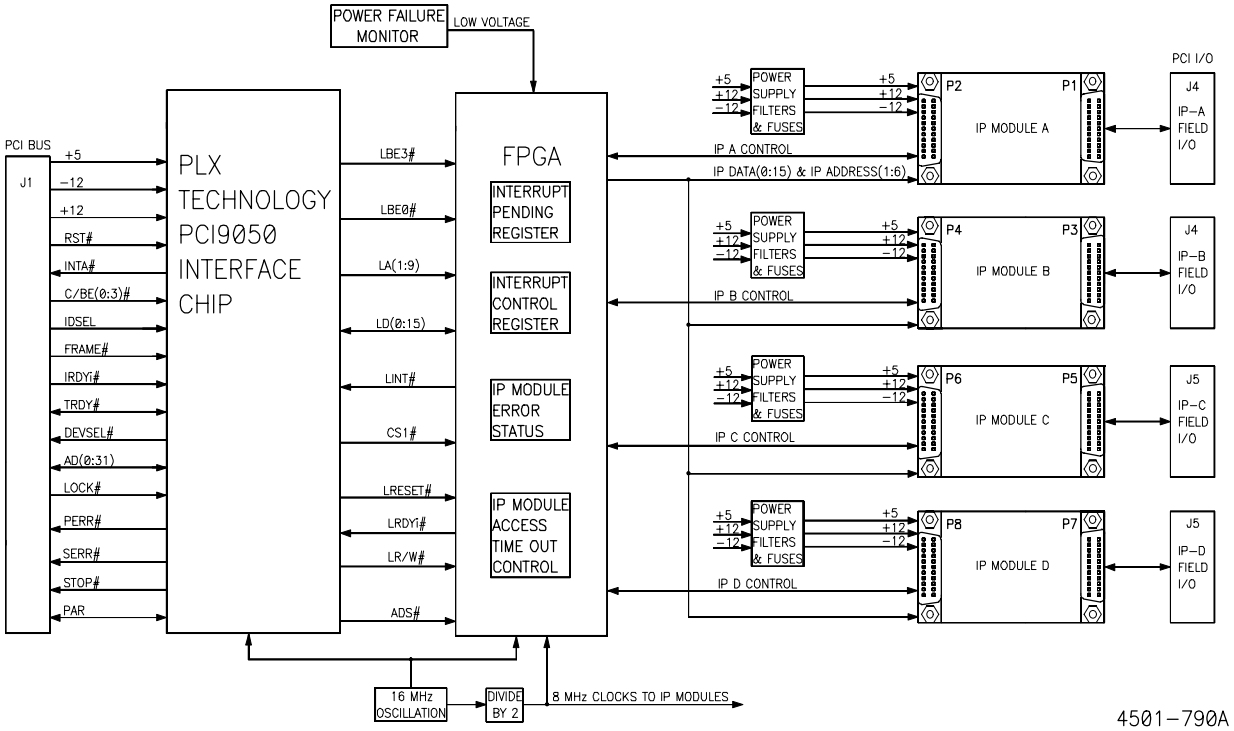
1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH ACPC8625 CARRIER BOARD (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO ACPC8625 CARRIER BOARD MECHANICAL ASSEMBLY 4501–789A

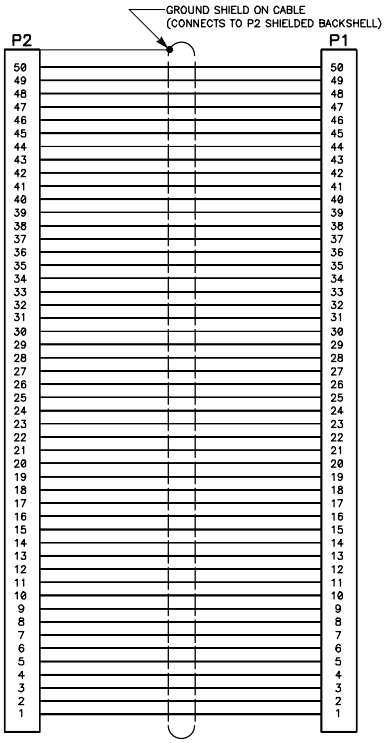


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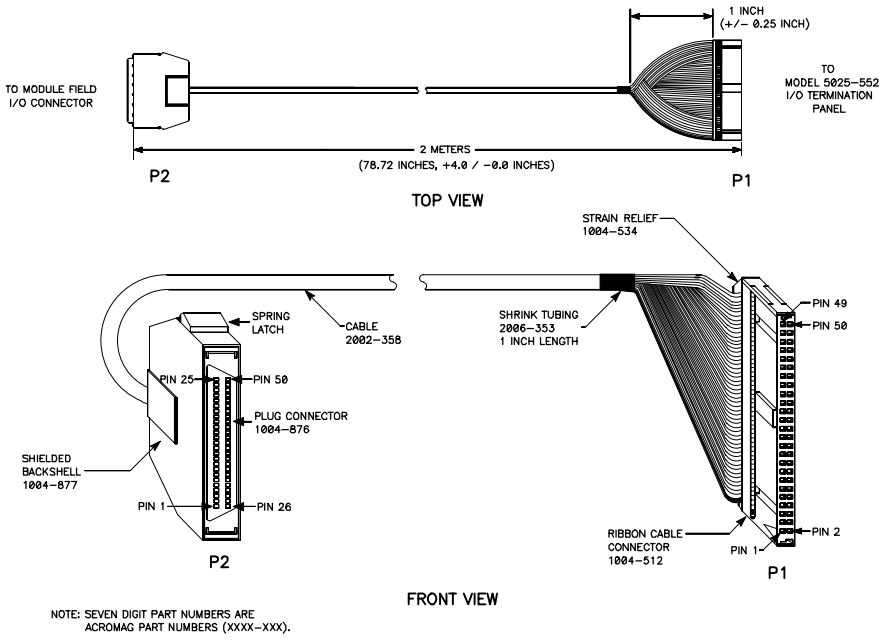
## ACPC8625 BLOCK DIAGRAM




4501−790A




SCHEMATIC

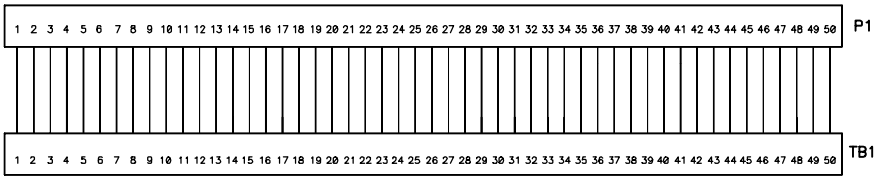



MODEL 5028−187, SCSI−2 TO FLAT RIBBON CABLE, SHIELDED

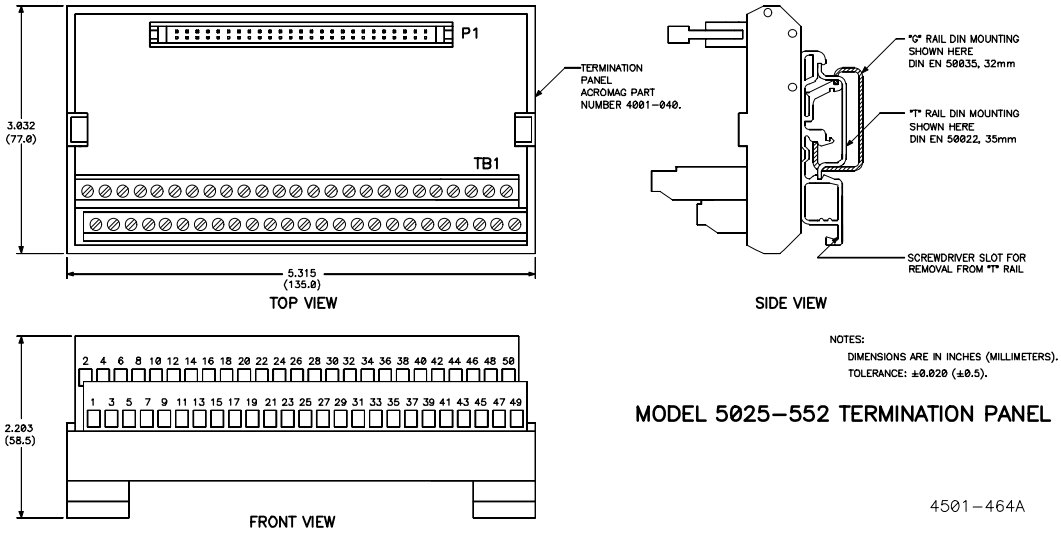
4501−758B



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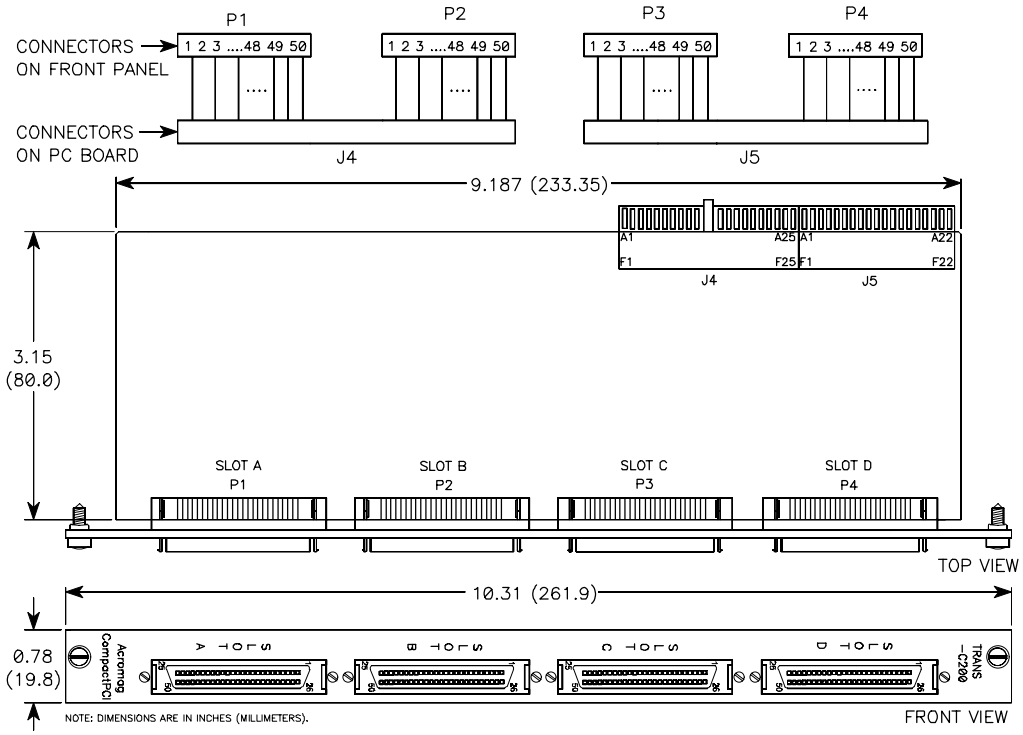

MODEL 5025-552 TERMINATION PANEL SCHEMATIC




NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

4501-464A




TRANS-C200 MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

4501-791B



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# TRANSITION MODULE: MODEL TRANS-C200

Type: Transition Module For ACPC8625 Boards

The TRANS-C200 transition module plugs into the rear backplane directly behind the carrier board. The field I/O connections are made through the backplane to J4 and J5 connectors of the carrier board and then routed to four SCSI-2 connectors on the transition module (marked IP module slots “A through D”) for rear exit from the card cage. It is available for use in CompactPCI bus card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the CompactPCI mechanical dimensions and IEEE Standard (1101.11-1998), with a printed circuit board depth of 80mm, which is a standard transition module depth. The transition module connects to Acromag Termination Panel (Model 5025-552) using SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187) to the rear of the card cage, and to ACPC8625 boards within the card cage.

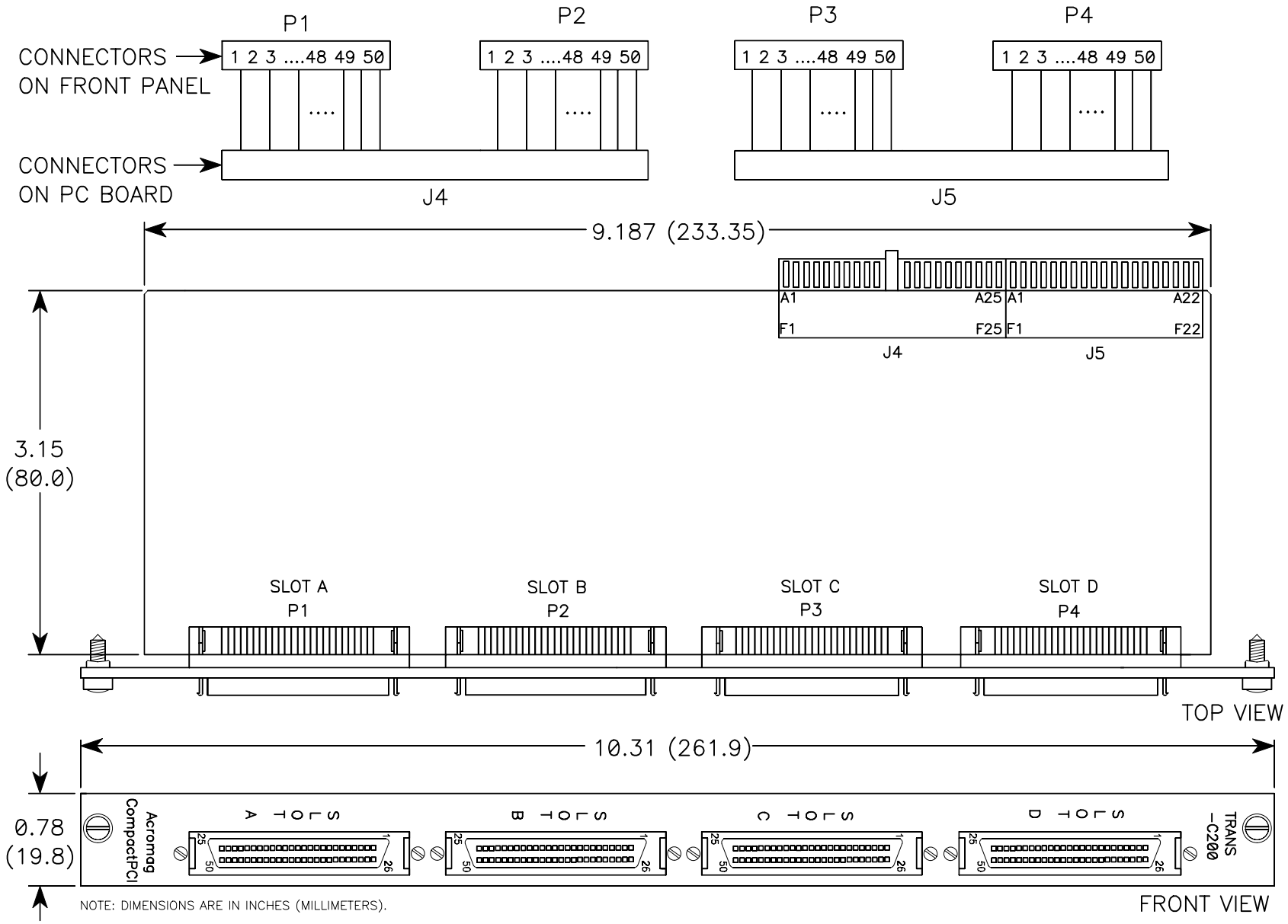
| | |
|---|---|
| Application | To repeat field I/O signals of IP modules A through D for rear exit from CompactPCI card cages. |
| Schematic and Physical Attributes | See Drawing 4501-791 (Over). |
| Electrical Specifications | 30 VAC per UL and CSA (SCSI-2 connector spec.’s).<br>1 Amp maximum at 50% energized (SCSI-2 connector spec.’s). |
| Field Wiring | Four SCSI-2, 50-pin female connectors (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via round shielded cable (Model 5028-187). |
| Connections to ACPC8625 | Connections are made though the PC board connectors J4 (110 signals, female right angle with upper ground shield-keyed) and J5 (110 signals, female right angle with upper ground shield). The transition module plugs directly behind the ACPC8625 board into the CompactPCI bus backplane within the card cage system. |
| Mounting | Transition module is inserted into a 6U-size, 80 mm width slot at the rear of the CompactPCI bus card cage.<br>(Directly behind ACPC8625 board) |
| Printed Circuit Board | Eight-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick. |
| Operating Temperature | -40°C to +85°C. |
| Storage Temperature | -40°C to +85°C. |
| Shipping Weight | 1.25 pounds (0.6Kg) packed. |

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TRANS–C200 MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

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