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Acromag®

Series APC730, Multifunction Board PCI Bus

USER'S MANUAL

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Table of Contents **Page**

1.0 GENERAL INFORMATION..... 3
KEY APC730 ADC FEATURES..... 3
KEY APC730 DAC FEATURES..... 4
KEY APC730 COUNTER/TIMER FEATURES..... 4
KEY APC730 DIGITAL INPUT/OUTPUT FEATURES... 4
PCI BUS INTERFACE FEATURES..... 4
SIGNAL INTERFACE PRODUCTS..... 5
APC730 DLL CONTROL SOFTWARE..... 5
APC730 VxWORKS SOFTWARE..... 5
APC730 QNX SOFTWARE..... 5
2.0 PREPARATION FOR USE..... 5
UNPACKING AND INSPECTION..... 5
CARD CAGE CONSIDERATIONS..... 5
BOARD CONFIGURATION..... 5
Default Hardware Jumper/DIP Switch Configuration. 6
Analog Input Range Hardware Configuration..... 6
CONNECTORS..... 6
Front Panel Field I/O Connector 6
Non-Isolation Considerations..... 7
PCI Bus Connector P1..... 7
3.0 PROGRAMMING INFORMATION..... 8
PCI Configuration Address Space..... 8
Configuration Registers..... 8
MEMORY MAP..... 8
Interrupt Register..... 9
Analog Input & Corresponding Digital Codes..... 10
ADC MODES OF CONVERSION..... 10
ADC Uniform Continuous Mode..... 10
ADC Uniform Single Mode..... 10
ADC Burst Continuous Mode..... 10
ADC Burst Single Mode..... 11
ADC Convert On External Trigger Only Mode..... 11
ADC Control/Status Register..... 12
ADC Start Channel Value Register..... 13
ADC End Channel Value Register..... 13
ADC Prescaler Register..... 13
ADC Conversion Timer Register..... 13
ADC Memory Threshold Register..... 14
ADC Start Convert Register..... 14
ADC Memory Buffer..... 14
Uncalibrated ADC Performance..... 15
Calibrated ADC Performance..... 15
DAC MODES OF CONVERSION..... 16
DAC Single Conversion Mode..... 16
DAC Continuous New Data Conversion Mode..... 16
DAC Recycle Same Data Conversion Mode..... 16
DAC Control/Status Register..... 17
DAC Conversion Timer Register..... 17
DAC FIFO Interrupt Threshold..... 18
DAC Start Convert Register..... 18
DAC FIFO Write Port..... 18
DAC Uncalibration Data..... 18
DAC Calibration Performance..... 19
Digital Input/Output Registers..... 20
Digital Direction Control Register..... 20
Digital Interrupt Enable Registers..... 20
Digital Interrupt Status Registers..... 20
Interrupt Type (COS or H/L) Configuration Register 20
Interrupt Polarity Register..... 20
Debounce Duration Select and Enable Register..... 21
COUNTER TIMER MODES OF OPERATION..... 22
Pulse Width Modulation..... 22
Watchdog Timer Operation..... 22
Event Counting Operation..... 22
Input Pulse Width Measurement..... 23
Input Period Measurement..... 23
One-Shot Pulse 23
Counter Control Register..... 25
Counter Readback Register..... 26
Counter Constant 1 Register..... 26
Counter Constant 2 Register..... 26
Counter Trigger Control Register..... 26
Calibration Access Register..... 27
Calibration Read Data/Status Register..... 27
4.0 THEORY OF OPERATION..... 28
LOGIC/POWER INTERFACE..... 28
PCI INTERFACE LOGIC..... 28
ADC CONVERSION CONTROL LOGIC..... 28
FIELD ANALOG INPUT..... 28
DAC CONVERSION CONTROL LOGIC..... 30
COUNTER TIMER CONTROL LOGIC..... 31
DIGITAL INPUT/OUTPUT LOGIC..... 31
APC Software..... 31
5.0 SERVICE AND REPAIR..... 32
SERVICE AND REPAIR ASSISTANCE..... 32
PRELIMINARY SERVICE PROCEDURE..... 32
6.0 SPECIFICATIONS..... 33
PHYSICAL..... 33
ENVIRONMENTAL..... 33
ANALOG INPUT..... 34
ANALOG OUTPUT..... 35
DIGITAL INPUT/OUTPUT..... 36
COUNTER TIMER..... 36
PCI Local Bus Interface..... 36

APPENDIX..... 37
CABLE, SCSI-3 to SCSI-3 (Shielded):
MODEL 5028-432..... 37
TERMINATION PANEL: MODEL 5025-288..... 37

DRAWINGS **Page**
4501-946 APC730 ANALOG SWITCH LOCATION..... 38
4501-947 APC730 ANALOG INPUT CONNECTION..... 39
4501-948 APC730 BLOCK DIAGRAM..... 40
4501-919 CABLE 5028-432 (SHEILDED)..... 41
4501-920 TERMINATION PANEL 5025-288..... 42

REVISION HISTORY..... 44

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

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1.0 GENERAL INFORMATION

The APC730 board is a precision, short size PCI board with the capability to monitor 16 differential or 32 single-ended analog input channels to 16-bit resolution. In addition, eight 16-bit analog output voltage channels and 16 digital input/output channels are provided. Lastly, one independent multifunction 32-bit counter/timer is available.

The analog voltage input channels share a single 16-bit Analog to Digital Converter (ADC). The channel conversion rate is controlled by a user programmable delay counter. All analog input channels share two generous 512-sample memory buffers, from which digitized values are read. Since all channels share the same memory buffer, data tagging is implemented for easy identification of corresponding channel data. To minimize CPU interaction, an interrupt can be generated upon reaching a programmable memory full threshold condition.

The eight analog output voltage channels each have a dedicated register from which digital values are transferred to their corresponding Digital-to-Analog-Converter (DAC). The eight analog output voltage channels share a 1024-sample First-In-First-Out (FIFO) buffer. Digital samples are moved from the FIFO to the individual DAC registers. The digital values are then simultaneously converted to analog at the rate set by a user programmable delay counter. Interrupt generation is provided for a FIFO almost empty condition, to minimize CPU interaction.

The 16 digital input/output channels can be programmed as input or output on a byte basis. All input channels can be enabled for change of state, low, or high level transition interrupts.

One independent 32-bit multifunction counter/timer is also provided. The counter can be configured for pulse width modulated output, one shot pulse output, event counter, pulse width measurement, period measurement, or watchdog timer.

The APC730 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial and scientific applications that require, high-performance analog input and output.

The APC730 board is available in standard and extended temperature ranges as follows:

MODEL	OPERATING TEMPERATURE RANGE
APC730	0 to +70°C
APC730E	-40°C to +85°C

KEY APC730 ADC FEATURES

- **16-Bit ADC Resolution** – 16 differential or 32 single-ended analog input channels multiplexed to a single 16-bit ADC. Acquisition mode and channels are selected via programmable control registers.
- **ADC 10μsec Conversion Time** - A maximum ADC conversion rate of 100KHz is supported.
- **Differential or Single Ended** – Monitors up to 16 differential or 32 single ended analog input signals. The acquisition mode and channels are selected via programmable control registers.
- **Two 512 Sample Memory Buffers –** Two 512 sample deep memory buffers are available for ADC operation to reduce CPU interactions. While new digitized data is written to one memory buffer, data can be read from the other at burst data rates. This allows the external processor to service more tasks within a given time. Data tagging is also implemented for easy channel data identification.
- **ADC Memory Buffers Switch Condition –** When the number of new data samples exceed a programmable threshold value the input buffer switches to the data read buffer which allows reading of the new data. The old read buffer will simultaneously switch from the data read to the data input buffer.
- **User Scan Modes –** The scan modes: Uniform Continuous, Uniform Single, Burst Continuous, Burst Single, and External Trigger Only can be selected via a programmable control register.
- **Interrupt Upon Reaching a Memory Threshold Condition –** An interrupt can be generated when the number of new data samples reaches a programmable threshold condition. This feature can be used to minimize CPU interaction.
- **User Programmable Conversion Timer** - A programmable conversion timer is available to control the time between conversion of each channel when Uniform-Continuous or Single Scan modes are selected. If Burst-Continuous is selected, the conversion timer controls the delay after a group of channels are converted before conversion is initiated on the group again.
- **External Trigger Input or Output** - The external trigger is available through the digital input/output channels. This external trigger may be configured as an input, output, or disabled. As an output this signal provides a means to synchronize other boards to a single APC730 timer reference. As an input the signal will trigger the APC730 hardware to initiate data conversions.
- **Precision On Board Calibration Voltages** - Calibration autozero and autospan precision voltages are available to permit host computer correction of conversion errors. The calibration voltages can be converted and then compared to the expected value stored in on board memory. Calibration voltages include: 0V (local analog ground), and precision 9.87, 4.93, 2.46, and 1.23 volt references.
- **Fault Protected Input Channels** - Analog input overvoltage protection to ±25V with power on and ±40V with power off.

KEY APC730 DAC FEATURES

- **16-Bit DAC Resolution** – 16-bit differential DAC with ±10V bipolar voltage output range.
- **12.375µsec Conversion Time –** A maximum recommended conversion rate of 80.8KHz is supported.
- **1024 Sample FIFO Buffer –** A single FIFO buffer is provided to store analog output channel samples. Each sample must have a tag to identify the corresponding channel to be updated. Samples are read from the FIFO and moved to the channel corresponding to its tag until an end of sample flag is detected. The end of sample flag makes it possible to update only one channel or up to all channels for each output conversion cycle. Those channels not updated by the FIFO will maintain and output the last sample read for the new conversion cycle.
- **Interrupt Upon Reaching FIFO Threshold Level –** An interrupt can be generated when the number of remaining FIFO samples reaches a programmable threshold level. This feature can be used to minimize CPU interaction.
- **Continuous New Data Conversion Mode –** Data must be written to the 1024 sample FIFO from the PCI bus at a rate that prevents the FIFO from reaching empty status. Maintenance of new data in the FIFO is important since sample data is continually read from the FIFO at the rate set by a conversion timer.
- **Recycle Same Data Conversion Mode –** This mode allows continuous recycling of the same FIFO samples starting with the first sample written after a reset and ending at the location of the last sample written to the FIFO.
- **User Programmable Conversion Timer –** A user programmable conversion timer is provided to control the delay between conversions. During the period of each conversion interval, new digital values are read from FIFO memory and then all channels are simultaneously converted. This feature supports a minimum interval of 12.375µsec and a maximum interval of 2.09 seconds.
- **Single Conversion Mode –** Output channels can be individually updated. Other channels not updated maintain their previous analog output value. Analog output can be triggered for update via software or external trigger.
- **External Trigger Scan Mode –** All channels simultaneously implement a new conversion with each external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Input or Output –** An external trigger signal is available through the digital input/output channels. This signal can be used to synchronize operation with other boards when used as an output. As an input the signal can be used to initiate new conversions.
- **Reliable Software Calibration –** Calibration coefficients stored in on board memory provide a means for accurate software calibration for both gain and offset correction for all eight analog output channels.
- **Reset is Failsafe for Analog Output –** The analog output channels are reset to 0 volts upon power up or issue of a software or hardware reset.

KEY APC730 COUNTER/TIMER FEATURES

- **32-Bit Counter/Timer** – A multifunction 32-bit counter is provided for implementation of: waveform generation, event counting, watchdog timing, pulse-width measurement, or period measurement.
- **Output Waveform Generation** – The counter can be programmed for pulse width modulation, and square wave generation. A one-shot pulse waveform may also be generated.
- **Event Counter** – The counter can be configured to count input pulses or events. A gate-off signal is provided to control count-up upon each event or countdown with each event. Interrupt generation upon programmed count condition is available.
- **Watchdog Timer** – The counter can be configured as a countdown timer for implementation as a watchdog timer. A gate-off signal is available for use to stop the count down operation. Interrupt generation upon a countdown to zero condition is available.
- **Pulse-Width or Period Measurement –** The counter can be configured to measure pulse-width or waveform period. In addition, an interrupt can be generated upon measurement complete.
- **Programmable Interface Polarity-** The polarities of the counter's external trigger, input, and output pins are programmable for active high or low operation. These counter control signals are available through the digital input/output channels.
- **Internal or External Triggering –** A software or hardware trigger is selectable to initiate waveform generation, watchdog countdown, event counting, pulse-width measurement, or period measurement.

KEY APC730 DIGITAL INPUT/OUTPUT FEATURES

- **16 Digital Input/Output Channels** – Interface with up to 16 input/output channels which can be configured as input or output in groups of eight channels.
- **TTL Compatible Thresholds –** Input and output thresholds are at TTL levels. Buffer input channels include hysteresis for increased noise immunity.
- **Programmable Change of State/Level Interupts –** Interrupts are software programmable for any bit Change-Of-State or level on all 16 channels.
- **Power Up and System Reset is Failsafe –** For safety, the digital channels are configured for input upon power-up.

PCI BUS INTERFACE FEATURES

- **Slave Module**- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.
- **Immediate Disconnect on Read** - The PCI bus will immediately disconnect after a read. The read data is then stored in a read FIFO. Data in the read FIFO is then accessed by the PCI bus when the read cycle is retried. This allows the PCI bus to be free for other system operations while the read data is moved to the read FIFO.
- **Interrupt Support** - PCI bus INTA# interrupt request is supported. All board interrupts are mapped to INTA#. The APC730 board software programmable registers are utilized as interrupt request control and status monitors.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

The APC730 field I/O is accessed from a SCSI-2 (68-pin) front panel connector. This board only supports front I/O access.

The cable and termination panel, described in the following paragraphs, are also available. For optimum performance with the APC730 analog input board, use of the shortest possible length of shielded input cable is recommended.

Cables:

Model 5028-432: A 2-meter, round 68 conductor shielded cable with a male SCSI-3 connector at both ends and 34 twisted pairs. The cable is used for connecting the APC730 board to Model 5025-288 termination panels.

Termination Panel:

Model 5025-288: DIN-rail mountable panel provides 68 screw terminals for universal field I/O termination. Connects to Acromag APC730, via SCSI-3 to twisted pair cable, Model 5028-432.

APC730 DLL CONTROL SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/NT4/2000/XP®) applications accessing Acromag PMC I/O module products, PCI I/O Cards, and CompactPCI I/O Cards. This software (Model PCISW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments including Visual C++™, Visual Basic®, Borland C++ Builder® and others. The DLL functions provide a high-level interface to PMC modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

APC730 VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of APC730 VxWorks® library. This software (Model PMCSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag PCI boards. The software is implemented as a library of “C" functions which link with existing user code to make possible simple control of all Acromag PCI boards (APC products use the corresponding PMC Module software).

APC730 QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of APC730 QNX® library. This software (Model PCISW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag PCI boards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag PCI boards (APC products use the corresponding PMC Module software).

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION



Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the APC730 board to within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible analog input ranges are configured by DIP switch settings (SW1) which will be discussed in the following sections. The DIP switch location is shown in Drawing 4501-946.

Remove power from the APC730 board when configuring hardware jumpers, cables, termination panels, and field wiring.

Default Hardware Jumper/DIP Switch Configuration

When the board is shipped from the factory, it is configured as follows:

- Analog input range is configured for a bipolar input with a 20 volt span (i.e. an ADC input range of ±10 volts).
- J3 is open. Plus 3.3 volts is provided from an on board regulator.
- SW1 – Position 10 is used for providing a 4.7K open drain pull-up for the counter/timer output signal. Default switch position is "ON" (pulled up). The DIP switch location is shown in Drawing 4501-946.
- The default configuration of the programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired configuration before starting data input or output operation.

Analog Input Range Hardware Configuration

The ADC input range is programmed via hardware DIP switches. The DIP switches control the input voltage span and the selection of unipolar or bipolar input ranges. The configuration of the DIP switch for the different ranges is shown in Table 2.1. A switch selected as "ON" would be positioned to the side of the DIP labeled "ON". The DIP switch location is shown in Drawing 4501-946.

Table 2.1: Analog Input Range Selections/DIP Switch Settings – SW1

Desired ADC Input Range (VDC)	Required Input Span (Volts)	Required Input Type	Switch Settings ON	Switch Settings OFF
$+3.\overline{3}$ to $-3.\overline{3}$ [2]	$6.\overline{6}$ [2]	Bipolar	2,4,6,9	1,3,5,7,8
-5 to +5	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 to +10[1]	20	Bipolar	2,5,6,9	1,3,4,7,8
0 to +5	5	Unipolar	1,3,5,8	2,4,6,7,9
0 to +10	10	Unipolar	1,3,4,7	2,5,6,8,9

Notes (Table 2.1):

1. The APC730 board is shipped from the factory for the ADC input range of ±10 volts.
2. A 'bar' above a number indicates a repeating digit (e.g. $3.\overline{3} = 3.333...$).

CONNECTORS

Connectors of the APC730 boards consist of one 68-pin front panel SCSI-3 field I/O connector, and a PCI Bus connector P1. These interface connectors are discussed in the following sections.

Front Panel Field I/O Connector

The front panel connector provides the field I/O interface connections. It is a SCSI-3 68-pin female connector (AMP 787082-7 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-288 from the front panel via round shielded cable (Model 5028-432).

IMPORTANT: All unused analog input pins should be tied to analog ground. Floating unused inputs can drift outside the input range causing temporary saturation of the input analog circuits. Recovery from saturation is slow and affects the reading of the desired channels.

Table 2.2: APC730 Field I/O Pin Connections

Pin Description	Pin	Pin Description	Pin
Counter Output	1	COMMON	35
Dig CH0/ ADC Trigger In	2	Dig CH8/ ADC Trig Out	36
Dig CH1/ DAC Trigger In	3	Dig CH9/ DAC Trig Out	37
Dig CH2/ Counter Input	4	Digital CH10 Counter Output	38
Dig CH3/ Counter Trig In	5	Digital CH11	39
Dig CH4/ Counter Ext Clk	6	Digital CH12	40
Dig CH5/ Counter Gate off	7	Digital CH13	41
Digital CH6	8	Digital CH14	42
Digital CH7	9	Digital CH15	43
COMMON	10	Analog Out CH4	44
COMMON	11	Analog Out CH5	45
Analog Out CH0	12	COMMON	46
Analog Out CH1	13	COMMON	47
Analog Out CH2	14	COMMON	48
Analog Out CH3	15	COMMON	49
COMMON	16	Analog Out CH6	50
COMMON	17	Analog Out CH7	51
COMMON	18	SENSE	52
Analog In S15/D15+	19	Analog In S31/D15–	53
Analog In S14/D14+	20	Analog In S30/D14–	54
Analog In S13/D13+	21	Analog In S29/D13–	55
Analog In S12/D12+	22	Analog In S28/D12–	56
Analog In S11/D11+	23	Analog In S27/D11–	57
Analog In S10/D10+	24	Analog In S26/D10–	58
Analog In S9/D9+	25	Analog In S25/D9–	59
Analog In S8/D8+	26	Analog In S24/D8–	60
Analog In S7/D7+	27	Analog In S23/D7–	61
Analog In S6/D6+	28	Analog In S22/D6–	62
Analog In S5/D5+	29	Analog In S21/D5–	63
Analog In S4/D4+	30	Analog In S20/D4–	64
Analog In S3/D3+	31	Analog In S19/D3–	65
Analog In S2/D2+	32	Analog In S18/D2–	66
Analog In S1/D1+	33	Analog In S17/D1–	67
Analog In S0/D0+	34	Analog In S16/D0–	68

Front panel connector pin assignments are shown in Table 2.2. When reading Table 2.2, note that channel designations are abbreviated to save space.

The SENSE line (pin 52), as shown in the single ended voltage input connection diagram at the end of this manual, must be connected to analog common when operating in single ended mode. With differential mode, the SENSE line is not used but it is

recommended that this input be grounded to avoid a floating input. In this case connect the SENSE line (pin 52 to pin 18).

Non-Isolation Considerations

The APC730 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the APC730 board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs and outputs when a high level of accuracy/resolution is needed.

PCI Bus Connector P1

Table 2.3 indicates the pin assignments for the PCI bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. "B" is on the component side of the carrier board while "A" is on the solder side. Connector "gold finger" numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI bus specification for additional information on the PCI bus signals.

TABLE 2.3: PCI Bus P1 CONNECTIONS

Bracket End ↑

Signal	Pin	Pin	Signal
-12V	B01	A01	***TRST#***
TCK	B02	A02	+12V
Ground	B03	A03	***TMS***
TDO	B04	A04	TDI
+5V	B05	A05	+5V
+5V	B06	A06	INTA#
INTB#	B07	A07	***INTC#***
INTD#	B08	A08	+5V
PRSNT1#	B09	A09	***Reserved***
Reserved	B10	A10	***+VIO***
PRSNT2#	B11	A11	***Reserved***
+3.3V KEYWAY			+3.3V KEYWAY
+3.3V KEYWAY			+3.3V KEYWAY
Reserved	B14	A14	***3.2Vaux***
Ground	B15	A15	RST#
CLK	B16	A16	***+VIO***
Ground	B17	A17	***GNT#***
REQ#	B18	A18	Ground
+VIO	B19	A19	***PME#***
AD[31]	B20	A20	AD[30]
AD[29]	B21	A21	***+3.3V***
Ground	B22	A22	AD[28]
AD[27]	B23	A23	AD[26]
AD[25]	B24	A24	Ground
+3.3V	B25	A25	AD[24]
C/BE[3]#	B26	A26	IDSEL
AD[23]	B27	A27	***+3.3V***
Ground	B28	A28	AD[22]
AD[21]	B29	A29	AD[20]
AD[19]	B30	A30	Ground
+3.3V	B31	A31	AD[18]
AD[17]	B32	A32	AD[16]
C/BE[2]#	B33	A33	***+3.3V***
Ground	B34	A34	FRAME#
IRDY#	B35	A35	Ground
+3.3V	B36	A36	TRDY#
DEVSEL#	B37	A37	Ground
PCIXCAP	B38	A38	STOP#
LOCK#	B39	A39	***+3.3V***
PERR#	B40	A40	***SMBCLK***
+3.3V	B41	A41	***SMBDAT***
SERR#	B42	A42	Ground
+3.3V	B43	A43	PAR
C/BE[1]#	B44	A44	AD[15]
AD[14]	B45	A45	***+3.3V***
Ground	B46	A46	AD[13]
AD[12]	B47	A47	AD[11]
AD[10]	B48	A48	Ground
M66EN/GND	B49	A49	AD[09]
5V KEYWAY			5V KEYWAY
5V KEYWAY			5V KEYWAY
AD[08]	B52	A52	C/BE[0]#
AD[07]	B53	A53	***+3.3V***
+3.3V	B54	A54	AD[06]
AD[05]	B55	A55	AD[04]
AD[03]	B56	A56	Ground
Ground	B57	A57	AD[02]
AD[01]	B58	A58	AD[00]
+VIO	B59	A59	***+VIO***
ACK64#	B60	A60	***REQ64#***
+5V	B61	A61	+5V
+5V	B62	A62	+5V

(#) s used to indicate an active-low signal.

BOLD ITALIC Logic Lines are NOT USED by this board.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the APC730 board.

This Acromag APC730 board complies with PCI Specification Version 2.2. It is a PCI bus slave board.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. This APC730 board can be accessed via the PCI bus memory space and configuration spaces only.

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PCI board is a Plug-and-Play PCI card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to read/write a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the carrier requires. It then programs the boards configuration registers with the unique memory base address.

The configuration registers are also used to indicate that the PCI board requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PCI board.

Since this PCI board is relocatable and not fixed in address space, this board's device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space and which interrupt line will be used.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This PCI board provides 256 bytes of configuration registers for this purpose. The APC730 contains the configuration registers, shown in Table 3.1, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the APC730 and the interrupt request line that goes active on a APC730 interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=4457		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for APC730 4K-Byte Block			
5 : 10	Not Used			
11	Subsystem ID=0000		Subsystem Vendor ID=0000	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCI bus memory space to control the multiple functions of this board. Three types of information are stored in the memory space: control, status, and data.

The memory space address map for the APC730 is shown in Table 3.2. Note that the base address for the APC730 in memory space must be added to the addresses shown to properly access the APC730 registers. Register accesses as 32, 16, and 8-bit in memory space are permitted.

Table 3.2: APC730 Memory Map

Base Addr +	D31 D16	D15 D00	Base Addr +
03	Not Used[1]	Interrupt Register	00
07	Not Used[1]	ADC Control/Status Register	04
0B	Not Used[1]	ADC Start and End Channel Values	08
0F	ADC Conversion Timer	Not Used[1] / Prescaler	0C
13	Not Used[1]	ADC Memory Threshold Register	10
17	Not Used Bits-31 to 01	ADC Start Convert Bit-0	14
1B	Not Used[1]		18
1F	Not Used[1]		1C
23	Not Used[1]	DAC Control/Status Register	20
27	Not Used[1]	DAC Conversion Timer	24
2B	Not Used[1]	DAC FIFO Interrupt Threshold	28
2F	Not Used Bits-31 to 01	DAC Start Convert Bit-0	2C
33	DAC FIFO Write Port Not Used (31:20), Flag bit(19), Tag bits(18:16), Data(15:0)		30
37	Not Used[1]		34
3B	Not Used[1]	16-bit Digital I/O Register	38
3F	Not Used[1]	Digital I/O Direction Control Register	3C
43	Digital I/O Interrupt Status Register	Digital I/O Interrupt Enable Register	40
47	Digital I/O Interrupt Polarity Register	Digital I/O Interrupt Type Register	44
4B	Debounce Duration Select and Enable Register Channels 0 to 7		48
4F	Debounce Duration Select and Enable Register Channels 8 to 15		4C
53	Not Used[1]	Counter Control Register	50
57	Counter Read Back Register		54
5B	Counter Constant 1 Register		58
5F	Counter Constant 2 Register		5C
63	Not Used Bits 31 to 1	Counter Trigger Bit-0	60
67	Not Used[1]	Calibration Access Register	64
6B	Not Used[1]	Calibration Read Data & Status	68
6F	Not Used[1]	Calibration Write Enable Code[2]	6C
73	Not Used[1]		70
↓	↓		↓
7FF	Not Used[1]		7FC
803	1st Memory Location Not Used(31:21), Tag bits(20:16), Data(15:0)		800
↓	↓		↓
FFF	512th Memory Location Not Used(31:21), Tag bits(20:16), Data(15:0)		FFC

Notes (Table 3.2):

1. The APC730 will return 0 for all addresses that are "Not Used".
2. This byte is reserved for use at the factory to enable writing of the reference voltage. Write only byte value = “A3”.

This memory map reflects byte accesses using the “Little Endian” byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses “Little Endian” byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Interrupt Register, (Read/Write) - (Base + 00H)

This read/write register is used to enable APC730 interrupt operation, determine the pending status of interrupts, and release pending interrupts.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.3: Interrupt Register

BIT	FUNCTION
0	Board Interrupt Enable Bit. (Read/Write Bit) 0 = Disable Interrupt 1 = Enable Interrupt If enabled via this bit an interrupt request from the board will be issued to the system upon any of the APC730 interrupt conditions. The interrupt request will remain active until the interrupt release bit is set, or by disabling interrupts via this bit.
1	Board Interrupt Pending Status Bit. (Read Only Bit) 0 = Interrupt Not Pending 1 = Interrupt Pending This bit can be read to determine the interrupt pending status of the APC730. When this bit is logic “1” an interrupt is pending, and will cause an interrupt request if bit-0 of the register is set. When this bit is a logic “0” an interrupt is not being requested. Once the bit is in the pending status it will remain until the pending interrupt is removed via the source of the interrupt. This bit will remain active even if interrupts are disabled via bit-0. When this bit is set, the pending interrupt can originate from the ADC, DAC, Digital I/O, or Counter Functions. To identify the source of the pending interrupt the following register bits must be read. • Bit-12 of the ADC Control/Status Register. • Bit-12 of the DAC Control/Status Register. • Bits-15 to 0 of the Digital Interrupt Status Reg • Bit-12 of the Counter Control Register.
13 to 2	Not Used[1]
14	Software Reset: The APC730 board is reset.
15	Not Used[1]

Notes (Table 3.3):

1. All bits labeled “Not Used” bit when set will read back as logic “1”.

Analog Input Ranges and Corresponding Digital Output Codes

Selection of an analog input range is implemented via the DIP switch settings given in Table 2.1. The ideal input voltage corresponding to each of the supported input ranges is given in Table 3.4. In Table 3.5 the digital output code corresponding to each of the given ideal analog input values is given in both binary two's complement and straight binary formats.

Table 3.4: Supported Full-Scale Ranges and Ideal Analog Input

DESCRIP.	ANALOG INPUT				
Input Range	±10V	0 - 10V	±5V	0 to 5V	$\pm 3.\overline{3}$ Volt
LSB (Least Significant Bit) Weight	305μV	153μV	153μV	76μV	102μV
+ Full Scale Minus One LSB	9.999695 Volts	9.999847 Volts	4.999847 Volts	4.999924 Volts	$+3.\overline{3}$ Volt
Midscale	0V	5V	0V	2.5V	0V
One LSB Below Midscale	-305μV	4.999847 Volts	-153μV	2.499924 Volts	-102μV
- Full Scale	-10V	0V	-5V	0V	$-3.\overline{3}$ Volt

The digital output format is controlled by bit-0 of the Control register. The two formats supported are Binary Two's Complement and Straight Binary. The hex codes corresponding to these two data formats are depicted in Table 3.5.

Table 3.5: Digital Output Codes and Input Voltages

	DIGITAL OUTPUT	
DESCRIPTION	**Binary 2's Comp** (Hex Code)	**Straight Binary** (Hex Code)
+ Full Scale - 1 LSB	7FFF	FFFF
Midscale	0000	8000
1 LSB Below Midscale	FFFF	7FFF
- Full Scale	8000	0000

ADC MODES OF CONVERSION

The APC730 provides five different modes of analog input acquisition to give the user maximum flexibility for each application. These modes of operation include: uniform continuous, uniform single, burst continuous, burst single, and convert on external trigger only. In all modes, a single channel or a sequence of channels may be converted. The following sections describe the features of each and how to best use them.

ADC Uniform Continuous-Mode

In uniform continuous mode of operation, conversions are performed continuously (in sequential order) for all channels enabled (via the ADC Start/End Channel Value registers). The interval between conversions is controlled by the ADC Conversion Timer register. The ADC conversion timer must be used in this mode of operation.

After software selection of the uniform continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the ADC Control register must be set to "01" to accept the external trigger as an input signal.

Stopping the execution of uniform continuous conversions is possible by writing 000 to the Scan Mode bits (10-8) of the ADC Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

Interrupts can be enabled to go active when the Memory buffer contains more samples than the set threshold value. The interrupt condition will remain set until interrupts are disabled or ADC data is read from the Memory.

ADC Uniform Single-Mode

In uniform single mode of operation, conversions are performed once (in sequential order) for all channels enabled via the ADC Start/End Channel Value registers. The interval between conversions is controlled by the ADC Conversion Timer. The ADC Conversion Timer must be used in this mode of operation.

After software selection of the uniform single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to "01" to accept the external trigger as an input signal.

Interrupts can be enabled to go active when the Memory buffer contains more samples than the set threshold value. The interrupt condition will remain set until interrupts are disabled or ADC data is read from the Memory.

ADC Burst Continuous-Mode

In burst continuous mode of operation, conversions are continuously performed in sequential order for all channels enabled via the ADC Start/End Channel Value registers. The interval between conversion for all enabled channels will be fixed at 15μ seconds. However, the interval after conversion of a group of channels can be controlled by the ADC Conversion Timer register. The timer can be disabled via bit-6 of the ADC control

register. If disabled, the interval between conversions will be fixed at 15μ seconds.

Burst modes can be used to provide pseudo-simultaneous sampling for many low to medium speed applications requiring simultaneous channel acquisition. The 15μ seconds between conversions of each channel can essentially be considered simultaneous sampling for low to medium frequency applications.

After software selection of the burst continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

Stopping the execution of burst continuous conversions is accomplished by writing 000 to the Scan Mode bits (10-8) of the ADC Control register. See the ADC Control register section for additional information on the Scan Mode control bits and the ADC Control register board address location.

Interrupts can be enabled to go active when the Memory buffer contains more samples than the set threshold value. The interrupt condition will remain set until interrupts are disabled or ADC data is read from the Memory.

ADC Burst Single-Mode

In burst single mode of operation conversions are performed once for all channels (in sequential order) for all channels enabled via the ADC Start/End Channel Value registers. The interval between conversions of each channel is fixed at 15μ seconds. The ADC Conversion Timer has no functionality in this mode of operation.

After software selection of the burst single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

Interrupts can be enabled to go active when the Memory buffer contains more samples than the set threshold value. The interrupt condition will remain set until interrupts are disabled or ADC data is read from the Memory.

ADC Convert On External Trigger Only-Mode

In convert on External Trigger Only Mode of operation each conversion is initiated by an external trigger (falling edge of a logic low pulse) input to the APC730 on pin 2 (Digital Channel 0) signal of the field I/O connector. Conversions are performed for all channels enabled via the ADC Start/End Channel Value registers in sequential order. The interval between conversions is controlled by the period between external triggers. The ADC Conversion Timer has no functionality in this mode of operation.

The external trigger signal must be configured as an input for this mode of operation. The external trigger can be configured as an input by setting bits 2 and 1 of the Control register to “01”.

At least 10μ seconds of data acquire time should be provided (via software) after programming the ADC Control register, and ADC Start/End Channel Value registers before the first external trigger is issued. These configuration registers control the APC730 on board multiplexers which control the channel selected for the input to the converter.

In the external trigger, only mode, it is important to understand the sequence in which converted data is transferred from the ADC to the Memory buffer. Upon an external trigger the selected analog signal is converted but remains at the ADC while the previous digitized value is output from the ADC to the Memory buffer. Thus, with this sequence the Memory is consistently updated with the previous cycle’s converted data. In other words, new data in the Memory buffer is one cycle behind the ADC. With this sequence, at the end of data conversions, one additional external trigger is required to move the data from the ADC to the Memory buffer. At the start of data conversion, with the first external trigger signal (given the Start Convert Bit is set), data is not input to the Memory buffer since the data in the ADC buffer is old convert data.

ADC Control/Status Register, (Read/Write) - (Base + 04H)

This read/write register is used to select the output data format, select the external trigger signal as an input or output, select acquisition input mode, select scan mode, enable/disable interrupts, monitor the interrupt pending status, and monitor memory status.

The function of each of the control register bits is described in Table 3.6. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.6: ADC Control/Status Register

BIT	FUNCTION
0	Output Data Format 0 = Binary Two's Complement 1 = Straight Binary See Tables 3.4 and 3.5 for a description of these two data formats.
2,1	External Trigger 00, 11 = Disabled 01 = Input (Active Low) 10 = Output (Active Low) It is possible to synchronize the data acquisition of multiple boards. A single master board must be selected to output an external trigger signal while all other boards are selected to input the external trigger signal. When enabled as an input, the external trigger signal is provided via pin 2 (Digital Channel 0). When enabled as an output, the external trigger signal is provided via pin 36 (Digital Channel 8). Thus Digital Channel 0 or 8, if selected, will not be available as a general digital I/O channel. When enabled here as an input, digital channels (0 to 7) must be selected as input via the Digital I/O Direction Control register. When enabled as an output, digital channels (8 to 15) will all be forced to be output. If External Trigger input or output is not required, the External Trigger should be configured as Disabled.
5,4,3	Acquisition Input Mode 000 = All Channels Differential Input 001 = All Channels Single Ended Input 010 = Not Used 011 = 9.88v Calibration Voltage Input 100 = 4.94v Calibration Voltage Input 101 = 2.47v Calibration Voltage Input 110 = 1.23v Calibration Voltage Input 111 = Auto Zero Calibration Voltage Input
6	Timer Enable 0 = Disable (0nly in External Trigger Only, or Burst modes). 1 = Enable (Continuous and Burst modes).
7	Not Used[1]
10,9,8	Scan Mode 000 = Disable 001 = Uniform Continuous 010 = Uniform Single 011 = Burst Continuous 100 = Burst Single 101 = Convert on External Trigger Only 110 = Not Used 111 = Not Used See the Modes of Operation section for a description of each of these scan modes.
11	0 = Disable Interrupt 1 = Enable Interrupt If enabled via this bit an interrupt request from the board will be issued to the system if the Memory contains more than the threshold number of bytes selected via the threshold register. The interrupt request will remain active until released via a read of the Analog Data Memory buffer, or by disabling interrupts via this bit.
12	Interrupt Pending/Interrupt Release Bit. **Read** of this bit reflects the interrupt pending status of the ADC logic. 0 = Interrupt Not Pending 1 = Interrupt Pending **Write** a logic "1" to this bit to release an ADC pending interrupt. A pending interrupt can also be released by disabling interrupts via bit-11 of this register.
13 (Read/ Write Bit)	0 = Enable Continued Analog Input 1 = Disable Conversions on Memory Bank Switch If the system cannot read all valid data values available in the memory buffer before the rate of new input data acquisition causes the buffers to switch, then the automatic disabling of analog input acquisition upon memory bank switching can be selected via this control register bit. If this bit is set to 1, analog input will be disabled upon a memory bank switch. Also, bits 8, 9, and 10 of this register will be set to 000 to reflect the disabled analog input mode.
14	0 = Enable Reset of Memory Write Pointer on issue of a software or external trigger. 1 = Disable reset of Memory Write Pointer on software or external trigger.
15 (Read Only Bit)	Transition Status Bit 0 = Waiting for New Valid Data in Memory 1 = Valid Data in Memory This transition status bit can be polled to insure the Memory buffer data is valid. The transition status bit will be set when the memory buffer switches causing new valid data to be available in the read memory buffer. The transition status bit is cleared upon the first read of the memory buffer and will not be set again until new valid data is available.

Notes (Table 3.6):

1. All bits labeled "Not Used" bit when set will read back as logic "1".

ADC Start Channel Value Register (Read/Write, 08H)

The Start Channel Value register must be written to set the first channel that is to be converted once conversions have been triggered. All channels from the start to the end channel value are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The Start Channel Value register can be read or written with 8-bit data transfers. In addition, the Start Channel Value register can be simultaneously accessed with the End Channel Value via a 32-bit or 16-bit data transfer. The unused bits are zero when read. The register contents are cleared upon reset.

Start Channel Value Register							
Unused			Start Channel Value				
07	06	05	04	03	02	01	00

After data conversions are halted, the internal hardware pointers are reinitialized to the start channel value. Thus when conversions are started again, the first channel converted is defined by the Start Channel Value register.

ADC End Channel Value Register (Read/Write, 09H)

The End Channel Value register must be written to indicate the last channel in a sequence to be converted. When scanning, all channels between and including the start and end channels are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The End Channel Value register can be read or written with 8-bit data transfers. In addition, the End Channel Value register can be simultaneously accessed with the Start Channel Value with a 32-bit or 16-bit data transfer. The unused data bits are zero when read. The register contents are cleared upon reset.

End Channel Value Register							
Unused			End Channel Value				
15	14	13	12	11	10	09	08

ADC Prescaler Register (Read/Write, 0CH)

The ADC Prescaler and Conversion Timer registers control the interval time between conversions. This 8 bit register controls the interval time between conversions of all enabled channels along with the Conversion Timer.

Timer Prescaler Register							
MSB							LSB
07	06	05	04	03	02	01	00

This 8-bit number divides an 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 50 hex or 80 decimal. A Timer Prescaler value of less then 80 (decimal) will result in erroneous operation. This minimum value corresponds to a conversion interval of 10μ seconds which translates to the maximum conversion rate of 100KHz.

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. The Timer Prescaler register contents are cleared upon reset.

ADC Conversion Timer Register (Read/Write, 0EH)

The Conversion Timer Register can be written to control the interval time between conversions. Reading or writing to this register is possible with either 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Conversion Timer Register															
MSB								LSB							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

This 16-bit number is the second divisor of an 8MHz. clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by an 8MHz. clock signal. The output of this clock is input to the second counter, the Conversion Timer, and the output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{8} = \text{T in } \mu\text{seconds}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 80 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval which can be programmed to occur is (80 * 1) ÷ 8 = 10μ seconds.

The 10μ seconds maximum sample rate corresponds to a maximum sample frequency of 100KHz. The maximum analog input frequency should be band limited to one half the sample frequency. An anti-aliasing filter should be added to remove unwanted signals above 1/2 the sample frequency in the input signal for critical applications.

Reading or writing the ADC Conversion Timer register is possible with 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

ADC Memory Threshold Register (Read/Write, 10H)

The Memory Threshold register is a 9-bit register that is used to control transition between two 512 deep memory banks. One memory bank is used to store converted analog input data while the other is accessible for reading of converted analog input data. When the analog input memory buffer contains more samples than the Memory Threshold value the memory banks will switch. This allows software to read new converted analog input data. The new data must be read before the memory banks switch again. If the system cannot keep up by reading the memory buffer before they switch, then the automatic disabling of analog input upon memory bank switching can be selected via the control register bit-13.

The number of valid analog input data samples available in the memory buffer will be one more than the value set in the Memory Threshold register. Thus, if the memory threshold value is 33 then 34 valid data entries will be present in memory when the memory buffer switch occurs. The Memory Threshold register value can be any value between 1 and 511.

An interrupt can also be issued upon exceeding the specified threshold level, if enabled via bit-0 of the interrupt register and bit-11 of the ADC Control register. This interrupt indicates that new data is available in the memory buffer. The interrupt request can also be disabled by setting bit-0 of the Interrupt register to a logic zero or bit-11 of the ADC Control register to logic 0. The interrupt request will remain active until released via a read of the Analog Data Memory buffer.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. This register's contents are set to 1FF hex (511 decimal) upon reset.

ADC Start Convert Register (Write Only, 14H)

The ADC Start Convert register is write-only and is used to trigger ADC conversions by setting data bit-0 to a logic one. The first conversion is initiated in hardware 10μs after this software start convert is set. This method of starting conversions is most useful for its simplicity and for when precise time of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The ADC Control, Channel Enable, and Conversion Timer register must first be configured before the Start Convert bit is set.

This register can be written via 32-bit, 16-bit or 8-bit data transfer. Data bit-0 must be a logic one to initiate data conversions.

Start Convert Register			
Not Used			Start Convert
31	• • •	01	00

ADC Memory Buffer (Read Only, 800H to FFCH)

In order to support burst data reading of ADC data, two 512-sample memory buffers are used. While one buffer functions to acquire new digitized data, the other functions as a read buffer. Data can be read at burst rates via the PCI bus to obtain new converted data. When the number of new input digitized data samples exceeds the Memory Threshold value, the two memory buffers switch functions.

Since all channels share the same memory, channel data tagging is implemented. The tag value identifies the channel to which the data corresponds. The hardware tags each memory location with a channel number, so the data can easily be matched with its source channel.

The Memory samples are 21-bit data values. The least significant bits, 15 to 0, represent the digitized data while bits 20 to 16 represent the channel tag.

Care should be taken when reading data from the memory buffer. To insure the memory buffer data is valid, the Transition Status bit (bit-15 of the Control Register) can be polled. The Transition Status bit will be set when valid data is available in the memory buffer. The Transition Status bit is cleared upon the first read of the memory buffer and will not be set again until the memory buffers switch, based upon the Threshold register value. Alternatively, an interrupt upon threshold met condition can be used to start reading of valid data.

Reading of the Memory is possible via 32-bit, 16-bit, or 8-bit data transfers.

Uncalibrated ADC Performance

The uncalibrated ADC performance is affected by two primary error sources. These are the instrumentation amplifier and the Analog to Digital Converter (ADC). The untrimmed instrumentation amplifier and ADC have offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated ADC Performance

Very accurate calibration of the ADC digitized values can be accomplished by using calibration reference voltages present on the board. The four voltages and the analog ground reference are used to determine two points of a straight line which defines the analog input characteristic. The exact value of the four reference voltages are stored in on board memory to provide the most accurate calibration. See Table 3.14 and the Calibration Access Register section for details regarding read of calibration coefficients.

The calibration voltages are used with the auto zero signal to find two points that determine the straight line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in Table 3.7.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected_Count} = \left[\frac{65536 * m}{\text{Ideal_Volt_Span}}\right] * \left[\text{Count_Actual} + \frac{\text{Volt}_{\text{CALLO}} - \text{Ideal_Zero}}{m} - \text{Count}_{\text{CALLO}}\right] \quad (1)$$

where, "**m**" represents the actual slope of the transfer characteristic as defined in equation 2:

$$m = \left[\frac{\text{Volt}_{\text{CALHI}} - \text{Volt}_{\text{CALLO}}}{\text{Count}_{\text{CALHI}} - \text{Count}_{\text{CALLO}}}\right] \quad (2)$$

$\text{Volt}_{\text{CALHI}}$ = High Calibration Voltage (See Table 3.7)

$\text{Volt}_{\text{CALLO}}$ = Low Calibration Voltage (See Table 3.7)

$\text{Count}_{\text{CALHI}}$ = Actual ADC Data Read with High Calibration Voltage Applied

$\text{Count}_{\text{CALLO}}$ = Actual ADC Data Read with Low Calibration Voltage Applied

Ideal_Volt_Span = Ideal ADC Voltage Span (See Table 3.8)

Count_Actual = Actual Uncorrected ADC Data for Input Being Measured

Ideal_Zero = Ideal ADC Input For "Zero" (See Table 3.8)

Table 3.7: Recommended Calib. Voltages For Input Ranges

ADC Range (Volts)	Rec. Low Calib. Voltage "$\text{Volt}_{\text{CALLO}}$" (Volts)	Rec. High Calib. Voltage "$\text{Volt}_{\text{CALHI}}$" (Volts)
-3.3 to +3.3	0.0000 (Auto Zero)	2.47
-5 to +5	0.0000 (Auto Zero)	4.94
-10 to +10	0.0000 (Auto Zero)	9.88
0 to+5	1.23	4.94
0 to +10	1.23	9.88

Table 3.8: Ideal Voltage Span and Zero For Input Ranges

ADC Range (Volts)	"Ideal_Volt _Span" (Volts)	"Ideal_ Zero" (Volts)
-3.33 to +3.33	6.6666	-3.333333
-5 to +5	10.0000	-5.0000
-10 to +10	20.0000	-10.0000
0 to +5	5.0000	0.0000
0 to +10	10.0000	0.0000

The calibration parameters ($\text{Count}_{\text{CALHI}}$ and $\text{Count}_{\text{CALLO}}$) for each active input range should not be determined immediately after startup but after the board has reached a stable temperature and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 512) of the calibration count parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

DAC MODES OF CONVERSION

The APC730 provides four methods of analog output operation for maximum flexibility with different applications. The following sections describe the features of each method and how to best use them.

DAC Single Conversion Mode

In Single Conversion mode of operation, sample data is written to the DAC FIFO buffer with channel tag values. The tag value is a 3-bit value present on bits 18 to 16. This mode can be used to update a single DAC channel or any number, up to all DAC channels, with new analog output voltage. The end of sample flag (bit-19) is utilized to identify the last channel to be converted in this single conversion cycle. With a conversion trigger initiated by software (via the DAC Start Convert register) or external trigger, the digital values are moved to their corresponding converter for update of their analog output signal. It is possible to keep a given channel's analog voltage unchanged by simply not updating the corresponding DAC channel. Only those channels with updated digital values will result in different analog output voltages.

To select this mode of operation bits 1 and 0 of the DAC Control register must be set to digital code "01". Then, issuing a software start convert or external trigger will initiate the update of the DAC channels. The DAC Conversion Timer register is not used in this mode of operation.

DAC Continuous New Data Conversion Mode

In the Continuous New Data Conversion mode of operation, the hardware controls the continuous shifting of digital data from the FIFO buffer to the DAC channels. Each sample must have a tag to identify the corresponding channel to be updated. The tag value is a 3-bit value present on bits 18 to 16. Samples are read from the FIFO and moved to the channel corresponding to their tag until an end of sample flag is detected. The end of sample flag (bit-19) makes it possible to update only one channel or up to all channels for each output conversion cycle. Those channels not updated in the given cycle will use their last valid sample in the new conversion cycle. Digital data is output to the converter at the rate specified by the DAC Conversion Timer. This mode of operation is ideal for aperiodic waveform generation.

To select this mode of operation bits 1 and 0 of the DAC Channel Control register must be set to digital code "10". Then, issuing a software start convert or external trigger will initiate the continuous update of the DAC channels.

The interrupt capability of the APC730 can be employed as a means to indicate to the system that the 1024 sample FIFO has fewer samples than the set threshold and must be loaded with additional values.

Alternatively, a polling method could be used. The FIFO empty, full, and Less Samples than set Threshold status flags are available on bits 13 and 14, respectively. These bits can be polled and when set the FIFO can be reloaded with new data.

DAC Recycle Same Data Conversions Mode

Recycle Same Data Conversion Mode allows continuous recycling through FIFO memory. In this mode, a continuous recycling of the FIFO data starting with the first value written to the FIFO after a reset and ending at the last value written to the FIFO. The output data is continuously recycled in an unending loop. This mode is useful when it is necessary to generate periodic waveforms. Writing data to the FIFO, while this mode is active, will cause erroneous operation. The FIFO should be preloaded before this mode of operation is triggered.

This mode also utilizes the tag and end of sample flag. Each sample must have a tag to identify the corresponding channel to be updated. The tag value is a 3-bit value present on bits 18 to 16. Samples are read from the FIFO and moved to the channel corresponding to their tag until an end of sample flag is detected. The end of sample flag (bit-19) makes it possible to update only one channel or up to all channels for each output conversion cycle. Those channels not updated by the FIFO in a new cycle will maintain and output the last sample read. DAC conversions, are implemented at the rate specified by the DAC Conversion Timer or External Trigger rate.

To select this mode of operation bits 1 and 0 of the DAC Channel Control register must be set to digital code "11". Then, issuing a software start convert or external trigger will start the data output cycles.

DAC Control/Status Register, (Read/Write) – (Base + 20H)

This read/write register is used to enable single, continuous, or recycle mode conversions, control external trigger mode, enable/disable DAC generated interrupts, and monitor FIFO status.

The function of each of the control register bits is described in Table 3.9. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.9: DAC Control/Status Register

BIT	FUNCTION
1, 0	00 = Disable Conversions. 01 = Enable Single Conversion Mode. (A software start convert or external trigger is required for each conversion.) 10 = Enable Continuous New Data Conversions 11 = Enable Recycle Same Data Conversions Conversion are initiated via software start convert or external trigger. In the Single Conversion mode of operation, sample data is provided from the FIFO. With each trigger, the conversion of all eight DAC channels is possible. Only those channels with new sample data will change. All channels not updated with new sample data will maintain their last analog output voltage. For Continuous New Data Conversion mode, conversions (once triggered) continue at the frequency set by the DAC Conversion timer register. In Continuous New Data Conversion mode data is supplied from the FIFO. If the FIFO becomes empty the last valid value output will remain unchanged. For Recycle Same Data Conversion Mode sample data is provided from the FIFO. A Recycling of the FIFO data starts with the first value written to the FIFO after a reset and ending with the last value written to the FIFO. The output data is Recycled in an unending loop. Writing to the FIFO while this mode is actively running will result in unpredictable DAC output voltage control. The FIFO must be preloaded before this mode of operation is triggered.
3, 2	External Trigger 00, 11 = Disabled 01 = Input (Active Low) 10 = Output It is possible to synchronize the DAC output of multiple boards. A single master board must be selected to output an external trigger signal while all other boards are selected to input the external trigger signal. When enabled as an input, the external trigger signal is provided via pin 3 (Digital Channel 1). When enabled as an output, the external trigger signal is provided via pin 37 (Digital Channel 9). Thus, Digital Channel 1 or 9 if selected will not be available as a general digital I/O channel. When enabled here as an input, digital channels (0 to 7) must all be selected as input. When enabled as an output, digital channels (8 to 15) must be selected as output. If External Trigger input or output is not required, the External Trigger should be configured as Disabled.
4	0 = Disable Interrupt 1 = Enable Interrupt If enabled via this bit an interrupt request from the board will be issued to the system if the FIFO contains less than the threshold number of bytes selected via the threshold register. The interrupt request will remain active until the interrupt condition is removed, or by disabling interrupts via this bit. The interrupt condition can be removed by writing more data to the FIFO buffer (thus extending the number of samples above the set threshold). Interrupts should not be enabled if Enable Recycle Same Data Conversion mode is selected.
5	FIFO Pointer Reset This bit must be set prior to writing data to the DAC FIFO when Recycle Same Data mode is used. Typical sequence is: 1) Select Recycle Same Data mode and set this bit 2) Write all data to be cycled to DAC FIFO, 3) Start Recycle Same Data mode.
6-11	Not Used
12	0 = Interrupt Not Pending 1 = Interrupt Pending A pending interrupt will remain active until the number of samples in Memory is more than the set threshold, or until DAC interrupts are disabled via bit-4 of this register.
13 Status	0 = FIFO Empty 1 = FIFO Not Empty
14 Status	0 = FIFO has ≥ samples than set threshold 1 = FIFO has less samples than set threshold.
15 Status	0 = FIFO Not Full 1 = FIFO Full

DAC Conversion Timer Register (Read/Write) - (Base + 24H)

DAC conversion control has its own dedicated Conversion Timer register. The value stored in the Conversion Timer Register controls the interval time between conversions. Read or writing the Conversion Timer register is possible with either 32-bit, 16-bit, or 8-bit data transfers. This register's contents are cleared upon reset.

The DAC Conversion Timer value/number is divided by an 8MHz clock signal. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions. The time period between trigger pulses is described by the following equation:

$$\frac{\text{DAC Conversion Timer Value} + 3}{8{,}000{,}000 Hz} = \text{T in seconds}$$

Where: **T** = time period between trigger pulses in seconds.
DAC Conversion Timer can be any value between 96 and 16,777,212 decimal.

The maximum period of time which can be programmed to occur between conversions is (16,777,212 + 3) ÷ 8Mhz = 2.0971 seconds. The minimum time interval which can be programmed to occur is (96 + 3) ÷ 8 = 12.375μ seconds. This minimum of

12.375μ seconds is defined by the minimum conversion time of the hardware.

The following equation can be used to calculate the DAC Conversion Timer value. Note, this gives the value in decimal. It must still be converted to hex before it is written to the DAC Conversion Timer register.

$$\text{DAC Conversion Timer Value} = (\text{T seconds} \times 8{,}000{,}000\text{Hz}) - 3$$

Where:
T = the desired time period between trigger pulses in seconds. The DAC Conversion Timer value can be a minimum of 96 decimal.

DAC FIFO Interrupt Threshold (Read/Write) - (Base + 28H)

The DAC FIFO Interrupt Threshold register is a 10-bit register that is used to set a threshold upon which an interrupt will be generated. When the FIFO contains less samples than the FIFO Interrupt Threshold value an interrupt will be issued. This register allows selection of any FIFO depth level. This interrupt indicates that new data should be written to the FIFO.

An interrupt request will remain asserted to the system as long as the FIFO contains less data than the set threshold and interrupts are enabled. The interrupt request can be removed by 1) disabling interrupts on the board or 2) writing data to the FIFO until it has more samples than that set by the Threshold register. Note, interrupts must first be enabled in the Interrupt Enable register (bit-0) and the DAC Control register (bit-4).

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. This register's contents are set to zero upon reset.

DAC Start Convert Register (Write Only) - (Base + 2CH)

The DAC Start Convert register is write-only and is used to trigger DAC conversions by setting data bit-0 to a logic one. This method of starting conversions is most useful for its simplicity and for when precise time of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The DAC Control, Conversion Timer, and FIFO threshold register must first be configured before the Start Convert bit is set. Data must also be present in FIFO memory before the Start Convert bit is set for conversion modes.

This register can be written via 32-bit, 16-bit or 8-bit data transfer. Data bit-0 must be a logic one to initiate data conversions.

DAC FIFO Write Port (Write Only) - (Base + 30H)

DAC operations have a dedicated 1024 sample deep FIFO buffer. The FIFO samples are 20-bit data values. The least significant bits, 15 to 0, represent the digitized data, bits 18 to 16 represent the channel tag, and bit-19 is the end of sample flag bit. Writing to the FIFO is possible via 32-bit data transfers only.

A new set of digitized values are read from the FIFO and written to the DAC upon each new conversion cycle. A new set of digitized values can be any number of samples from one up to all eight channels. The sample flag bit is used to mark the end of a set of new digitized values. For example, if only channels 1 and 3 are to be updated on the first conversion cycle and channels 1-3, and 7 are to be updated on the next conversion cycle, then the FIFO will contain the data shown in the following table. Notice the placement of the sample flag bit and that each digitized data value must have a corresponding tag to identify the channel to be updated. The sample flag bit must be set to a logic one to identify the last value data sample of the present conversion cycle. Also, notice that the first value written to the FIFO is shown in the last row of this table. Likewise, the second value written is shown in the second from the last row.

Example DAC FIFO Data

Sample Flag	Tag Bits	DAC Data
Bit-19	Bit-18 to 16	Bit-15 down to 0
1	7	A030
0	3	3FFF
0	2	003F
0	1	0000
1	3	7FFF
0	1	8000 (First Value Read)

Care should be taken when writing data to the FIFO buffer to insure the FIFO is not full when a new write is initiated. The FIFO Full flag bit (Control register bit-15) can be read prior to writing the FIFO to avoid this error. Data is not stored in the FIFO once it becomes full.

New FIFO locations are available after data transfers to the DAC are initiated. In addition, the FIFO can be cleared by implementing a software or hardware reset or by setting bit-5 of the DAC control register to a logic high.

DAC Uncalibrated Data

The DAC data must be written in straight binary format. The ideal digital input value for a given output voltage can be calculated using equation (3).

Equation (3):

$$\text{Ideal DigVal} = \left(\frac{65536}{20} \times \text{Vout} \right) + 32768$$

For example, a Vout of –5 volts results in an Ideal Digital Input value of 16,384 decimal. The corresponding hexadecimal code of 4000 hex must be written on data bits 15 to 0. This equation does not correct the offset and gain errors (see following section). This will be acceptable for some applications.

DAC Calibrated Performance

Accurate calibration of the APC730 DAC output signals can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in memory for each channel as shown in Table 3.14. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channels to accurately generate the desired output voltage. See the specification chapter for details regarding maximum calibrated error.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal Digital Input value into a Corrected Digital Input value. This is accomplished by using equation (4).

Equation (4):

$$CorrectDigVal = ((Vout + 10) \times Gain_Correct) - Offset_Correct$$

where,

Gain_Correct = ((Stored_Gain_Error / 1,000,000)+1) x 3276.75
Offset_Correct = Stored_Offset_Error / 100

Ideal Digital Input is determined from equation (3) given above. Stored_Gain_Error and Stored_Offset_Error are written at the factory and are obtained from memory on the APC730 on a per channel basis. The Stored_Gain_Error and Stored_Offset_Error are stored in memory as two's complement numbers. Refer to the "Calibration Access Register" section for details on how to read the coefficients from memory.

Using equation (4), you can determine the corrected digital input. For the previous example, equation (3) returned a result 16,384 for the Ideal Digital Input to produce an output of -5 Volts. Assuming that a gain error of 836 and an offset error of 200 are read from memory on the APC730 for the desired channel, substitution into equation (4) yields:

$$Gain_Correct = \left\{ \left[\frac{836}{1{,}000{,}000} \right] + 1 \right\} x\ 3276.75 = 3279.4893$$

$$CorrectDigVal = \left[(-5 + 10) \times Gain_Correct \right] - \frac{200}{100} = 16{,}395.4$$

If the hexadecimal value 400B (rounded to 16,395 decimal) is used to program the DAC output, the output value will approach -5 Volts to within the calibrated error (see the specification chapter for details regarding maximum calibrated error).

It is recommended that interrupts be enabled upon a FIFO threshold condition. Upon this interrupt no more than 1024 samples minus the threshold value should be written to the FIFO. A software or hardware reset will clear the FIFO contents.

Digital Input/Output Registers (Read/Write) - (Base + 38H)

Sixteen possible input/output channels numbered 0 through 15 may be individually accessed via these registers. The Input/Output Digital register is used to monitor/read or set/write channels 0 through 15. Channels 7 to 0 are accessed at the carrier base address +38H via data bits 7 to 0. Channels 15 to 8 are accessed at the carrier base address +38H via data bits 15 to 8.

Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs on a power-on or software reset. The unused upper 16 bits of this register are "Not Used" and will always read low (0's).

Digital Direction Control Register (Read/Write) - (Base + 3CH)

The data direction (input or output) of the 16 digital channels is selected via bit-0 and bit-1 of this register. The data direction of channels 0 to 7 are set/controlled via bit-0 while the data direction for bits 8 to 15 are controlled via bit-1. Setting a bit high configures the corresponding channel data direction for output. Setting the control bit low configures the corresponding channel data direction for input.

The ADC and DAC trigger signals can be enabled to use Digital Port bits 0 and 1 as input and Digital bits 8 and 9 as output. If a trigger signal is enabled for input at either the ADC or DAC control register the data Direction Control Register must also be set as input for channels 0 to 7. If a trigger signal is enabled for output at either the ADC or DAC control register the data Direction Control Register must also be set as output for channels 8 to 15.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs on system reset or power-up. The unused upper bits of this register are "Not Used" and will always read low (0's). Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Digital Interrupt Enable Registers (Read/Write) - (Base + 40H)

The Interrupt Enable Registers provide a mask bit for each of the 16 channels. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding channel to generate an interrupt.

The Interrupt Enable register at the base address + offset 40H is used to control channels 0 through 15 via data bits 0 to 15. For example, channel 0 is controlled via data bit-0.

All input channel interrupts are disabled (set to "0") following a power-on or software reset. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Digital Interrupt Status Registers (Read/Write) - (Base + 42H)

The Interrupt Status Register reflects the status of each of the interrupting channels. A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register). In addition, an interrupt will be generated if any of the channels enabled for interrupt have an interrupt pending (i.e. one that has not been cleared). Writing "0" to a bit location has no effect; that is, a pending interrupt will remain pending.

The Interrupt Status register at the base address + offset 42H is used to control channels 0 through 15 via data bits 31 to 16. For example, channel 0 is controlled via data bit-16.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Interrupt Type (COS or H/L) Configuration Registers (Read/Write) - (Base + 44H)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 16 possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at base address + offset 44H is used to control channels 0 through 15. For example, channel 0 is controlled via data bit-0. All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Channel read or write operations use 8-bit, 16-bit, or 32-bit data transfers. Note that interrupts will not occur unless they are enabled.

The Interrupt Status register at the carrier's base address + offset 42H is used to monitor pending interrupts corresponding to channels 0 through 15. For example, channel 0 is monitored via data bit-0.

Interrupt Polarity Registers (Read/Write) - (Base + 46H)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the digital input channel data register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

If debounce is enabled and an Interrupt Polarity bit is set low the corresponding active low signal will be debounced. Likewise, with debounce enabled and the Interrupt Polarity bit set high the active high signal is debounced.

The Interrupt Polarity register at the carrier's base address + offset 46H is used to control channels 0 through 15. For example, channel 0 is controlled via data bit-16.

All bits are set to “0” following a reset which means that the inputs will cause interrupts when they are below TTL threshold (provided they are enabled for interrupt on level).

Debounce Duration Select and Enable Register (Read/Write) - (Base + 48H and 4CH)

This register controls debounce enable and duration selection for each of the 16 digital channels. The long word at base + 48hex controls debounce for the digital I/O signals 0 to 7. The long word at base + 4C hex controls debounce for the digital I/O signals 8 to 15.

Table 3.10A: Debounce Duration Select and Enable Register (Base + 48H)

BIT	FUNCTION
2,1,0[2]	Channel 0 Debounce Control (See Table 3.11)
3	Not Used[1]
6,5,4[2]	Channel 1 Debounce Control (See Table 3.11)
7	Not Used[1]
10,9,8[2]	Channel 2 Debounce Control (See Table 3.11)
11	Not Used[1]
14,13,12[2]	Channel 3 Debounce Control (See Table 3.11)
15	Not Used[1]
18,17,16[2]	Channel 4 Debounce Control (See Table 3.11)
19	Not Used[1]
22,21,20[2]	Channel 5 Debounce Control (See Table 3.11)
23	Not Used[1]
26,25,24	Channel 6 Debounce Control (See Table 3.11)
27	Not Used[1]
30,29,28	Channel 7 Debounce Control (See Table 3.11)
31	Not Used[1]

Table 3.10B: Debounce Duration Select and Enable Register (Base + 4CH)

BIT	FUNCTION
2,1,0[2]	Channel 8 Debounce Control (See Table 3.11)
3	Not Used[1]
6,5,4[2]	Channel 9 Debounce Control (See Table 3.11)
7	Not Used[1]
10,9,8[2]	Channel 10 Debounce Control (See Table 3.11)
11	Not Used[1]
14,13,12[2]	Channel 11 Debounce Control (See Table 3.11)
15	Not Used[1]
18,17,16[2]	Channel 12 Debounce Control (See Table 3.11)
19	Not Used[1]
22,21,20[2]	Channel 13 Debounce Control (See Table 3.11)
23	Not Used[1]
26,25,24[2]	Channel 14 Debounce Control (See Table 3.11)
27	Not Used[1]
30,29,28[2]	Channel 15 Debounce Control (See Table 3.11)
31	Not Used[1]

Notes (Table 3.10):

1. All bits labeled “Not Used” bit when set will read back as logic “1”.
2. These bits must be set as shown in the Debounce Duration Select Table 3.11.

Table 3.11: Debounce Duration Select

Bit Setting	Time
000	Debounce Disabled
001	4μ second Debounce
010	64μ second Debounce
011	1m second Debounce
100	8m second Debounce
101, 110, 111	Reserved

All bits are set to “0” following a reset. Thus, on reset and power-up debounce will be disabled by default. These registers are read/write registers that can be accessed with 8-bit, 16-bit, or 32-bit data transfers.

COUNTER TIMER MODES OF OPERATION

The 32-bit counter timer function of the APC730 provides six modes of operation: pulse width modulation, watchdog timer, event counting, pulse width measurement, period measurement, and one-shot pulse mode. The following sections describe the features of each method of operation and how to best use them.

Pulse Width Modulation

Pulse width modulated waveforms may be generated at the counter timer output (field connector pin-1). Waveforms are generated continuously. Waveform generation is configured via the Counter Control Register. The time until the pulse is generated is controlled via the Counter Constant 1 register. The duration of the pulse high or low is set via the Counter Constant 2 register. Note that a high pulse will be generated if active high output is selected while a low pulse will be generated if active low output is selected.

The counter goes through a full countdown sequence for each Counter Constant value. When the 0 count is detected, on the next rising-edge of the clock, the output toggles to the opposite state, and the second Counter Constant value is loaded into the counter, and countdown resumes, decrementing by one each clock cycle. For example, a counter constant value of 3 will provide a pulse duration of 4 clock cycles, since the counter will count down from 3 to 0.

Due to the rise/fall time delay of the output mosfet driver, a fixed delay of 1 to 2μs will be added to the pulse duration programmed into the counter constant registers. Waveform generation may be triggered externally via the Trigger input, or internally via the Trigger Control Register, according to the state of the trigger source bit 7 in the Counter Control Register. An initial trigger, software or external, causes the pulse width modulated signal to be generated with no additional triggers required.

If the Interrupt Enable bit of the Counter Control Register is set (bit 8) and bit-0 of the Interrupt register is set, an interrupt is generated when the pulse transitions from low to high and also when the pulse transitions from high to low.

Watchdog Timer Operation

The watchdog operation will countdown from a programmed (Counter Constant 1) value until it reaches 0. While counting, the counter output will be in its active state (the output polarity is programmable). Upon time-out, the counter output will return to its inactive state, and an optional interrupt may be generated. A watchdog timer that has timed-out will not re-cycle until it is re-triggered following a load of the Counter Constant 1 register (Counter Control Register bit 11=0). The counter can also be re-cycled by generating an input pulse (140ns minimum) at the input pin 4 (Digital Channel 2). Note that auto-loading must be inhibited via Counter Control Register bit 11=1.

Failure to cause a reload would generate an automatic time-out upon re-triggering, since the counter register will contain the 0 it has counted down to. The reload is implemented by either writing the Counter Constant 1 register or by setting bit-11 to logic high “1” and input of a load signal on pin 4 (Digital Channel 2).

The watchdog timer may be triggered internally (via the Trigger Control Register), or externally (via the Trigger input signal pin 5, Digital Channel 3). When triggered, the counter/timer contents are decremented by one each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. The current contents of the counter/timer can be read from the Counter Readback Register. The timer may be clocked via the internal 1MHz, 4MHz, or 8MHz clock, or by an external clock up to 3.5MHz at the counter clock pin. Due to the asynchronous relationship between the trigger and the selected clock, the time-out may occur within (1/selected clock frequency) from the programmed time selected. Upon time-out, the counter output pin returns to its inactive state and an interrupt can be optionally generated.

The Gate-Off signal, when active and enabled via bits 13 and 14 of the Counter Control register, can be used to stop the counter in watchdog mode. The Gate-Off signal is input via Digital I/O pin-7.

Upon detection of a count value equal to 0, the APC730 will issue an interrupt, if enabled via bit-8 of the Counter Control Register and bit-0 of the Interrupt register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized. The interrupt will remain pending until the watchdog timer is reinitialized and the interrupt is released by setting bit-12 of the count control register (offset 50H).

Event Counting Operation

Positive or negative polarity events may be tallied, as selected via the input polarity bit of the Counter Control Register (bits 4 and 5). In this mode, input pulses or events occurring at the input pin of the counter may be counted up to a programmed count limit. Upon reaching the count limit, the counter output will generate an output pulse, an optional interrupt can be generated, and the internal event counter register is then cleared. Alternatively, events occurring at the input pin can be selected to count down with use of the Gate-Off signal present on Digital I/O pin 7. When the Gate-Off signal is active the counter is in the count down mode (when inactive the counter counts up).

The Counter Constant 1 Register holds the count-to value (constant). Reading the Counter Readback Register will return the current count (variable). In event counter mode, the input event serves as an enable to count an event. A minimum event pulse width of 140ns is required for correct pulse detection with input debounce disabled. With debounce enabled, a minimum event pulse width is defined by that selected via the Debounce Duration Select and Enable register. Internal or external clock selection has no effect for event counters. Event counting may be initially triggered internally (via the Trigger Control Register), or externally (via the Trigger input signal pin 5 Digital Channel 3). To prevent missing events, the counter will continuously wrap around when in up counting mode and resume counting up from zero, without requiring a new trigger each time the count limit is reached. Upon reaching the count limit, an output pulse will be generated at the counter output pin, and an optional interrupt may be generated.

If the Interrupt Enable bit of the Counter Control Register is set (bit 8) and bit-0 of the Interrupt register is set, an interrupt is generated when the number of input pulse events is equal to the constant value stored in the Counter Constant 1 Register. The internal counter register is then cleared and will continue counting events until the counter constant value is again reached and a

new interrupt generated. An interrupt will remain pending until released via bit-12 of the counter control register (offset 50H).

Input Pulse Width Measurement

The Counter/Timer may also be used to accomplish input pulse-width measurement for pulses occurring at the counter input pin (Digital I/O pin 4). Pulse-width measurement may be triggered internally via the corresponding Counter Trigger Control register, or externally via the counter Trigger input signal. Bits 0 to 2 of the Counter Control Register are used to configure the channel for pulse-width measurement. An internal 1MHz, 4MHz, 8MHz clock, or an external clock (up to 3.5MHz) is used to set the pulse measurement resolution. The polarity of the pulse is configured via input polarity bits 4 and 5 of the Counter Control Register.

For pulse-width measurement, the pulse-width being measured serves as an enable control for an up-counter whose value can be read from the Counter Readback Register. When triggered, the counter increments by one for each clock pulse while the input signal level remains in the active state (high or low according to the programmed polarity). The up-counter may use an internal clock, or an external clock at the counter's clock pin (up to 3.5MHz). The resultant pulse-width is equivalent to the count value read from the Counter Readback Register, multiplied by the clock rate. An output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured pulse width may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFFFFFF, for a 32-bit counter, indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon read of this overflow value you must select a slower clock frequency and re-measure.

An interrupt can be generated upon completion of a given pulse width measurement (the pulse has returned to the opposite polarity), if enabled via the interrupt enable bit of the Counter Control Register (bit 8) and bit-0 of the Interrupt register. The interrupt will remain pending until released via bit-12 of the counter control register (offset 50H).

Input Period Measurement

The counter/timer may be used to measure the period of an input signal at the counter input pin (Digital I/O pin-4). Bits 0 to 2 of the Counter Control Register are used to configure the channel for periodic-rate measurement. Period measurement is accomplished the same way as described above for pulse-width measurement, except that the Counter Readback Register holds the period of the input signal (in number of clock cycles), not just the width of the high or low pulse. Note that the measured period may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFFFFFF, for a 32-bit counter, indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon read of this overflow value you must select a slower clock frequency and re-measure.

An interrupt can be generated upon completion of a given period measurement, if enabled via the interrupt enable bit of the Counter Control Register (bit 8) and bit-0 of the Interrupt register. The interrupt will remain pending until released via bit-12 of the counter control register (offset 50H).

One-Shot Pulse Mode

One-Shot pulse mode provides an output pulse that is asserted active after the time defined by the Counter Constant 1 register. The duration of the active pulse is defined by the Counter Constant 2 register. The one shot pulse waveform will be generated one time and repeated each time it is re-triggered.

Due to the rise/fall time delay of the output mosfet driver, a fixed delay of 1 to 2μs will be added to the pulse duration programmed into the counter constant registers.

One-Shot generation may be triggered externally via the Trigger input, or internally via the Counter Trigger Control Register, according to the state of the trigger source bit 7 in the Counter Control Register. An initial trigger, software or external, causes the count-down sequence to begin.

An interrupt can be generated upon pulse generation, if the interrupt enable bit 8 of the Counter Control Register is set and interrupt enable bit-0 of the Interrupt register is set. The interrupt will remain pending until released via bit-12 of the Counter Control register or disabled via bit-8 of the Counter Control register.

Table 3.12: Counter Timer Modes Overview

Description	PWM	Watchdog	Event Count	Pulse Meas.	Period Meas	One Shot
[1]Counter Input (Dig Ch 2 or Pin 4)		Used to cause reload of counter. Bit-11 must be high.	Event input	Input Pulse to be Measured.	Input Period to be Measured.	
[1]Clocks (External Clock Dig Ch 4 or Pin 6)	1MHz, 4MHz, 8MHz, and external.	1MHz, 4MHz, 8MHz, and external.	Fixed in Hardware not Selectable	1MHz, 4MHz, 8MHz, and external.	1MHz, 4MHz, 8MHz, and external.	1MHz, 4MHz, 8MHz, and external.
[1]Gate Off (Dig Ch5 or Pin7)		When active stops the counter.	When active causes count down mode on events.			
[1]External Trig. (Dig Ch 3 or Pin 5)	Starts PWM	Starts Count Down	Start Event Counting	Next complete pulse after trigger is measured.	Next complete period after trigger is measured.	Starts One Shot Generation.
Internal Software Trig	Starts PWM	Starts Count Down	Start Event Counting	Next complete pulse after trigger is measured.	Next complete period after trigger is measured.	Starts One Shot Generation.
Counter Timer Output	Output Waveform	Output is active from trigger until terminal count.	4us pulse is output upon reaching the count limit.	4us pulse is output upon end of pulse measurement	4us pulse is output upon end of period measurement	Pulse Output
Constant 1 Reg	Count down from value loaded.	Counts down from value loaded. Must always load before trigger. Note that the Counter input can be used to reload.	Count Limit. Input events are counted up to the count limit then a 1us pulse is output.			Count down value until pulse generated.
Constant 2 Reg	Count down from value loaded.					Count down value for Pulse Duration.
Counter Readback Reg		Gives the Count value at the time of the read.	Gives the Count value at the time of the read.	Gives count value reflecting pulse measured.	Gives count value reflecting period measured.	
Interrupt	On Edge Transitions	On Terminal Count of 0	Upon reach of count limit	Upon end of pulse measurement	Upon end of period measurement	On Edge Transitions

Notes (Table 3.12):

1. Debounce Available Through Digital I/O Control Register.

Counter Control Register (Read/Write) - (Base + 50H)

This register is used to configure counter/timer functionality for the 32-bit timer. This register defines the counter mode, output polarity, input polarity, external trigger polarity, trigger source, interrupt enable, clock source, internal or external counter load selection, gate-off enable and polarity.

Table 3.13: Counter Control Register

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	0	000	Disabled (Default)
	1	001	Disabled
	2	010	Pulse Width Modulation
	3	011	Watchdog Function
	4	100	Input Pulse Event Counter
	5	101	Input Pulse Width Measurement
	6	110	Input Period Measurement
	7	111	One-Shot Pulse Mode
3	Output Polarity (Output Pin ACTIVE Level):		
	0		Active LOW (Default)[1]
	1		Active HIGH
5, 4	Input/Event Polarity (Pin 4 Digital Channel 2):		
	00		Disabled (Default)
	01		Active LOW
	10		Active HIGH
	11		Disabled
6	External Trigger Polarity (When Bit-7 Set to 1)		
	0		High-to-Low (Default)
	1		Low-to-High
7	Trigger Source		
	0		Software Generated via Counter Trigger Control Register
	1		External input on Pin 5 (Digital Channel 3) with a 250ns minimum Trigger pulse required.
8	Interrupt Enable		
	0		Disable Interrupt Service (Default)
	1		Enable Interrupt Service
10,9	Clock Source		
	00		Internal @ 1MHz (Default)
	01		Internal @ 4MHz
	10		Internal @ 8MHz
	11		External Clock (Up to 3.4MHz) (Pin 6 Digital Channel 4)
11	Watchdog Timer Counter Internal or External Register Load Selection:		
	0		Load via write to Counter Constant 1 Register
	1		Externally Triggered Load of Counter via pulse at Input pin (Pin 4 Digital Channel 2). Bits 4 and 5 of this register must be enabled when using external load.
12	Interrupt Pending/Interrupt Release Bit. **Read** of this bit reflects the interrupt pending status of the counter timer logic. 0 = Interrupt Not Pending 1 = Interrupt Pending **Write** a logic "1" to this bit to release a counter timer pending interrupt. A counter timer pending interrupt can also be released by disabling interrupts via bit-8 of this register.		
14, 13	Gate-Off Source: If enabled the Gate-Off signal must be input on pin 7 (Digital Channel 5). Gate-Off, when active, causes event counter to count down and the watchdog counter to stop.		
	00		Disabled: Gate-Off not used
	01		Enable Gate-Off Active Low
	10		Enable Gate-Off Active High
	11		Disabled: Gate-Off not used
15	Counter Output Control		
	0		Output Available on Pin as driven by MOSFET.
	1		Output Available on Pin as driven by MOSFET. Output is also available on pin 38 (Digital Channel 10). Digital I/O Direction register for channels 8 to 15 must also be selected for output.

Notes (Counter Control Register):

1. The default state of the output pin is high (output has pullup installed and the drain supply jumper is present). Bit 3 specifies the active output polarity when the output is driven.

Bit 11 can be used to select whether the watchdog timer counter is to be loaded from the Counter Constant Register via an external input pulse (250ns minimum pulse width, on pin 4 digital channel 2), or automatically upon writing to the Counter Constant Register. In any mode, except watchdog, when you write to the Counter Constant Register the internal counter register will be written with the same value at the same time. In watchdog mode, if bit 11 is set to 0 (default), the watchdog timer counter will be loaded internally from the Counter Constant Register, automatically upon a direct write to the Counter Constant Register. However, if bit 11 is set to 1, then the watchdog timer counter will not be loaded from the Counter Constant Register until initiated by applying a minimum 140ns pulse (polarity is programmable via bit 4) to the external counter input (pin 4, Digital Channel 2).

Bit-12, when read high "1", identifies a pending interrupt from one of the following counter functions 1) Watchdog, 2) Event Counter, 3) Input Pulse Width Measurement, 4) Input Period Measurement, 5) Pulse Width Modulation, or 6) One Shot generation. Writing a logic "1" to bit-12 will release a pending interrupt.

An interrupt caused by the Watchdog function must first be cleared by disabling Watchdog mode or by reinitializing the counter. Once an interrupt request (caused by a counter function) is generated on the APC730, it will continue to assert the interrupt request until Interrupt Release bit-12 is set to logic "1" or interrupts are disabled. The counter interrupt can be disabled via bit-8 of the counter control register, and all APC730 interrupts can be disabled via bit-0 of the Interrupt register at base address + 0.

Upon detection of a count value equal to 0, the watchdog timer will initiate an interrupt. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized. An interrupt can also be generated when an event count reaches the value stored in the Counter Constant 1 register. An interrupt may also be generated when a pulse-width or periodic-rate measurement has been completed. Finally, an

interrupt may also be generated at each signal transition for Pulse Width Modulation or One-Shot generation. For these interrupts to be enabled, bit 8 of this Counter Control Register must be set to a logic high and bit-0 of the Interrupt register at base address + 0 must also be set to a logic high.

The Counter Control Register is cleared (set to 0) following a reset, thus disabling the counter/timer. Reading or writing to this register is possible via 32-bit, or 16-bit data transfers.

Counter Readback Register (Read Only) - (Base + 54H)

This read-only register is a dynamic function register that returns the current value held in the counter. The contents of this register is updated with the value stored in the internal counter, each time it is read.

The internal counter is generally initialized with the value in the Counter Constant Register, and its value is incremented or decremented according to the application. For event counters, this register holds the current number of events that have occurred since triggering the event counter. For input pulse-width or period measurement, this register holds the measured pulse-width or periodic rate of the input signal in number of clock cycles. In watchdog counting mode, this register holds the number of clock cycles that remain since triggering the timer and until a watchdog timer time-out will occur. These registers are cleared (set to 0) following a system or software reset. Reading this register is possible via 32-bit long-word accesses, only.

Counter Constant 1 Register (Write Only) - (Base + 58H)

This write-only register is used to store the counter/timer constant 1 value (initial value) for the various counting modes. Accesses to this register are allowed on a 32-bit long-word basis, only. This is necessary to allow the constant value to be loaded into the counter in one clock cycle.

For event counters, this register is used to set the maximum count value. Upon reaching this count value an interrupt can be generated.

For pulse width modulation, this register holds the width of the first half of the pulse. The width is defined by this constant value multiplied by period of the clock signal selected via control register bits 9 & 10. Writing the Counter Constant 1 value loads the counter with the written value. Once triggered the counter will count down until a terminal count (0) is reached. At this time, Counter Constant 2 is loaded into the counter.

For watchdog timers, this register stores the initial count value from which the timer starts counting.

Note that in any counter mode (except when Counter Control Register bit 11 is set), when you write to the Counter Constant Register the internal counter register will be written with the same value at the same time. Setting bit 11 of the Counter Control Register to 1 will instead cause the timer counter to be loaded from the Counter Constant Register, only after an external input pulse occurs (140ns minimum pulse width) for watchdog mode.

Note that since this register is write-only, the counter constant value cannot be read back. However, the value loaded into this register can be read back indirectly from the Counter Readback Register prior to initially counting.

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

Counter Constant 2 Register (Write Only) - (Base + 5CH)

This write-only register is used to store the counter/timer constant 2 value for pulse width modulation counting mode. Access to this register is allowed on a 32-bit long-word basis, only.

For pulse width modulation, this register holds the width of the second part of the pulse. The width is defined by this constant 2 value multiplied by period of your clock signal selected via control register bits 9 & 10.

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

Counter Trigger Control Register (Write Only) - (Base + 60H)

Bit-0 of this register is used to implement software triggering for the counter timer. All other bits of this register are not used. When the software trigger source has been selected for a counter function (via bits 6 & 7 of the Counter Control register), writing a 1 to bit-0 of this register will cause the counter function to be triggered. This bit is not stored and merely acts as a trigger for the start of the corresponding counter function.

Triggering may be used to initiate pulse width modulation, one-shot, watchdog countdown (initiates countdown), or pulse-width or period measurement. It may also be used to initiate event counting, but unlike the other counter/timer functions, event counters will automatically recycle without re-triggering.

Writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Calibration Access Register (Write, 64H)

This register is used to initiate a read of the DAC gain and offset calibration coefficients or ADC reference voltage values.

The analog output calibration data is provided so that software can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each of the 8-analog output channel's unique offset and gain calibration coefficients are stored in this memory at the addresses given in Table 3.14. The coefficients are 16-bit values with the most significant byte at the even addresses and the least significant bytes at the odd addresses. See the "Use of Calibration Data" section for analog output calibration correction details.

Reference voltage values are provided so that software can adjust and improve the accuracy of the analog input voltage over the uncalibrated state. The reference voltages are precisely measured at the factory and then stored to this location at the addresses given in Table 3.13. See the "Use of Calibration Reference Signals" section for analog input calibration correction details.

The Calibration Access Register is a write-only register and is used to configure and initiate a read cycle to the calibration memory. Setting bit-15 of this register high, to a "1'', initiates a read cycle. Setting bit-15 of this register low, to a "0'', initiates a write cycle.

The address of the calibration value to be read must be specified on bits 14 to 8 of the Calibration Access register. The addresses of all calibration data and references are given in Table 3.14.

Calibration Access Register		
Read or Write~	Address	Write Data
15	14, 13, 12, 11, 10, 9, 8	7 down to 0

Table 3.14: Calibration Address Map

DAC Channel		Offset Coefficient Address (Hex)		Gain Coefficient Address (Hex)	
		MSB	LSB	MSB	LSB
±10 Volt Range	0	00	01	02	03
	1	04	05	06	07
	2	08	09	0A	0B
	3	0C	0D	0E	0F
	4	10	11	12	13
	5	14	15	16	17
	6	18	19	1A	1B
	7	1C	1D	1E	1F

ADC Reference Voltages Follow							
Address of 9.88 Volt Reference (Hex)							
20	21	22	23	24	25	26	27
Address of 4.94 Volt Reference (Hex)							
30	31	32	33	34	35	36	37
Address of 2.47 Volt Reference (Hex)							
40	41	42	43	44	45	46	47
Address of 1.23 Volt Reference (Hex)							
50	51	52	53	54	55	56	57

Reference voltages are stored in memory as a null terminated ASCII character string. For example, if the value 9.88335 were stored to memory the corresponding ASCII characters would be 39, 2E, 38, 38, 33, 33, 35, 00 as shown in Table 3.15. Note, the ASCII equivalent of a decimal point is 2E and the null character is 00. For this example, the memory should be read starting at address 20H until the null ASCII character is read. This string can then be converted into a float by using your compiler's ATOF function.

Table 3.15: Example Reference Voltage

Address (Hex)							
20	21	22	23	24	25	26	27
Example Reference Value							
9	.	8	8	3	3	5	Null
ASCII Characters As Stored In Memory							
39	2E	38	38	33	33	35	00

The address corresponding to each of the reference voltage digits is given in hex. The most significant digit is stored at address 20 hex.

For additional details on the use of the reference voltage, refer to the "Use of Calibration Reference Signals" section.

Write accesses to the Reference Voltage Access register are possible via 32-bit or 16-bit data transfers, only. Storing the gain, offset, and reference voltages to memory is normally only performed at the factory.

A software or hardware reset has no affect on this register.

Calibration Read Data/Status Register (Read, 68H)

The Calibration Read Data/Status register is a read-only register used to access calibration data and determine the status of a read cycle initiated by Calibration Access register. In addition, this register is used to determine the status of a write cycle to the memory. When bit-1 of this register is set, it indicates the memory is busy completing a write cycle.

All read accesses to this Data/Status register initiate an approximately 1millisecond access to the memory. **Thus, you must wait 1 millisecond after reading this Data/Status register before a new read or write cycle to the memory can be initiated, (an EEPROM latency limitation).**

A read request, initiated through the Calibration Access register, will provide the addressed calibration value on data bits 15 to 8 of the Calibration Read Data/Status register. Although the read request via the Calibration Access register is accomplished in nano seconds, typically, the reference voltage digit will not be available in the Calibration Read Data/Status register for approximately 2.5 milliseconds.

Bit-0 of the Calibration Read Data/Status register is the read complete status bit. This bit will be set high to indicate that the requested calibration value is available on data bits 15 to 8 of the Calibration Read Data/Status register. This bit is cleared upon initiation of a new read access of the memory or upon issue of a hardware reset.

Reference Voltage Read Data/Status Register			
Read Data	Not Used	Write Busy	Read Complete
15 Down to 8	7 Down to 2	1	0

Writes to Calibration memory require a special enable code and are normally only performed at the factory. The board should be returned to Acromag if the reference voltages must be re-measured and stored to memory.

A write operation to the memory, initiated via the Calibration Access register, will take approximately 5 milliseconds. Bit-1 of the Calibration Read Data/Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation and will remain high until the requested write operation has completed. New read or write accesses to the memory, via the Calibration Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A hardware reset of the board will also clear this bit.

Read accesses to the Calibration Read Data/Status register are possible via 32-bit or 16-bit data transfers, only. A software or hardware reset will clear all bits to zero.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the APC730. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-948 as you review this material.

LOGIC/POWER INTERFACE

The logic interface to the board is made through the P1 of the PCI connector (refer to Table 2.3). This connector also provides +5V and ±12V power to the board. Note that the signals in bold italic are not used.

A Field Programmable Gate-Array (FPGA) installed on the APC730 board provides an interface to the PCI Bus to the CPU board. The interface to the CPU board allows complete control of all APC730 functions.

PCI INTERFACE LOGIC

The APC730 is a target only board, with the PCI bus interface logic imbedded within the FPGA. This logic includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCI target interface performs parity error detection, uses a single 4K base address register, and implements target abort, retry, and disconnect. The APC730 logic also implements interrupt requests via interrupt line INTA#.

ADC CONVERSION CONTROL LOGIC

All logic to control data conversions is imbedded in the PCI board's FPGA. The control logic of the board is responsible for controlling the programmed mode of operation. Once the PCI board has been configured, the control logic performs the following:

- Controls the channel multiplexers based upon start and end channel values, and single ended or differential analog input mode.
- Controls serial transfer of data from the ADC to the FPGA memory buffer.
- Controls conversion rate as user programmed.
- Provides memory buffer switch control.
- Provides external or internal trigger control.
- Controls read and write access to the reference voltage values stored in memory.
- Controls interrupt requests to the carrier/CPU and responds to interrupt select cycles.

Field Analog Input

The field I/O interface to the board is provided through front connector (refer to Table 2.2). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operational errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-947 for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. APC730 control logic automatically programs the multiplexers for selection of the required analog input channel.

The required control is based upon selection of single ended or differential analog input and the Start and End channel register values.

Single ended and differential channels cannot be mixed (i.e. they must all be single ended or differentially wired). Up to 32 single ended inputs can be monitored, where each channel's + input is individually selected along with a single sense lead for all channels. Up to 16 differential inputs can be monitored, where each channel's + and - inputs are individually selected.

The output of the multiplexer stage feeds an instrumentation amplifier (INAMP) stage. The INAMP has a fixed gain of one. The INAMPs high input impedance allows measurement of analog input signals without loading the source. The INAMP takes in the channel's + and - inputs and outputs a single ended voltage proportional to it.

The output of the INAMP feeds the ADC. The ADC is a state of the art 16-bit, successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then, it returns to sample mode to acquire the next analog input signal. Once a conversion has been completed, control logic on the board automatically reads the digitized value corresponding to the previous converted channel. This allows the input to settle for the next channel while the previous channel is converting. This pipelined mode of operation facilitates maximum system throughput.

A miniature DIP switch on the board controls the range selection for the ADC (-3.3 to +3.3, -5 to +5, -10 to +10, 0 to 5, and 0 to 10 Volts) as detailed in section 2. DIP switch selection should be made prior to powering the unit. Thus, all channels will use the same selected ADC range.

The board contains four precision voltage references and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for the desired ADC range and gain combination, when compared to fixed hardware potentiometers for offset and gain calibration of the ADC and INAMP.

Data Transfer ADC to FPGA

A wait of 10μ seconds is implemented, after a software or external start convert signal is generated. This time ensures the channel multiplexers are set as required for conversion of the first selected channel. This wait of 10μ seconds is not implemented in the External Trigger Only mode of operation.

Serially shifting the 16-bits of digitized data to the FPGA and then writing to the Memory buffer is completed 8μ seconds after ADC convert signal goes active.

A 16-bit serial shift register is implemented in the FPGA. This serial shift register interfaces to the ADC. A clock signal provided by the converter is used to serially shift the new data from the converter to the FPGA's 16-bit serial shift register. Use of the converter's clock signal (instead of an external clock) minimizes the danger of digital noise feeding through and corrupting the results of a conversion in process.

The converted data serially shifted from the ADC to the FPGA, represents the analog signal digitized in the previous convert cycle. That is, the ADC transfers digitized analog input data to the FPGA one convert cycle after it has been digitized.

Upon initiation of an ADC convert cycle, the analog input data is digitized and stored into an internal ADC buffer. Also, during this cycle, the last converted data value is moved from the ADC buffer to the FPGA's Memory Buffer

Understanding this sequence of events is important when using the External Trigger Only scan mode. The first digitized value received from the ADC in External Trigger Only mode will not be written to the Memory buffer if the Start Convert bit is set prior to issuance of the first external trigger signal. This first value received from the ADC is digitized data that has remained in the ADC's buffer from a previous data acquisition session. Likewise, to update the Memory buffer with the last desired digitized data value one additional convert cycle is required.

For all other scan modes, the FPGA control logic will automatically discard the first digitized data value received from the ADC. It is not written to the Memory buffer. In addition, the FPGA logic also automatically generates the required "flush" convert signals to obtain the last converted data value from ADC.

Timed Periodic Trigger Circuit

Timed Periodic Triggering is provided by two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by the 8MHz. board clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 10μ seconds to 2.0889 seconds. The output of the second counter is used to trigger the start of new ADC conversions for the Uniform Scan modes of operation. For the Burst Continuous mode, the interval between conversions of each channel is fixed at 15μ seconds. However, the interval between the group (burst) of channels can be controlled by the Interval Timer.

ADC Memory Buffer Switch Control

Two 512 sample memory buffers are provided in the FPGA logic to control simultaneous data acquisition and data reading via the PCI bus. One memory buffer accepts new ADC data input samples along with a channel tag value. The other memory buffer is available for data reading at PCI burst data rates over the PCI bus. The Memory Threshold value is used to control transition between the two 512 sample memory buffers. When the analog input memory buffer contains more samples then the Memory Threshold value the memory banks will switch. See section 3.0 for programming details and use of the ADC Memory Threshold register.

Burst Read of APC730 ADC Memory

Burst read of the APC730 memory buffer will allow a 40Mbyte per second data read rate. With every three PCI clock cycles a new data sample is read from the memory buffer. The APC730 will automatically stop the burst operation upon reaching the end of the ADC Memory buffer.

ADC External Trigger

The external trigger connections are made via pin 2 (Digital Channel 0) of the Field I/O Connector. For all modes of operation, when the external trigger is enabled as an input via bits 1 and 2 of the control register, the falling edge of the external trigger will initiate conversions. Once the external trigger signal has been driven low, it should remain low for a minimum of 250n seconds for proper external trigger operation. The external trigger input signals must be TTL compatible.

As an output, an active-low TTL signal is driven from the PCI board. The trigger pulse generated is low for 500n seconds, typical. The external trigger connections are made via pin 36 (Digital Channel 8) of the Field I/O Connector. For all modes of operation, the external trigger is enabled as an output via bits 1 and 2 of the control register. See section 3.0 for programming details to make use of this signal.

ADC Interrupt Control Logic

The APC730 can be configured to generate an interrupt using a programmable Memory Threshold level. When the memory buffer has more samples than set in the Memory Threshold register the PCI interrupt signal INTA# is driven active to the carrier/CPU to request an interrupt. Bit-1 of the Interrupt register (at Base Address + 0H) can be read to identify a pending interrupt. The interrupt release mechanism employed is release on register access. The APC730 will release the interrupt request when bit-12 of the ADC Control register (at Base Address + 04H) is set to a logic "1".

ADC Reference Voltage Memory Control Logic

The FPGA of the APC730 board contains control logic that implements read and write accesses to reference voltage memory. The reference voltage memory (EEPROM) contains an ASCII null terminated string that represents the exact voltage of the on board reference circuit as measured and stored at the factory.

DAC CONVERSION CONTROL LOGIC

All logic to control data conversions is imbedded in the board's FPGA. The control logic of the APC730 is responsible for controlling the user specified mode of operation. Once the board has been configured, the control logic performs the following:

- Controls serial transfer of data from the FPGA to the corresponding DAC register based on the selected mode of operation.
- Provides external or internal trigger control.
- Controls read and write access to calibration memory.
- Controls issue of interrupt requests.
- Provides status on FIFO Full, FIFO Threshold, and Empty conditions.

Field Analog Output

The field I/O interface to the board is provided through the front connector (refer to Table 2.1). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring ground loops may cause operation errors, and with extreme abuse, possible circuit damage.

The output range for the DACs is fixed at -10 to +10 volts as detailed in chapter 2.

Data Transfer FPGA To DACs

A serial shift register is implemented in the board's FPGA for each of the supported channels. Internal FPGA counters are used to synchronize the transfer of FIFO data to the corresponding serial shift register for output to its converter. Channels 0 to 3 are output to one DAC while channels 4 to 7 are output to the other DAC.

DAC Conversion Timer

The DAC update interval may be controlled by the conversion timer, which is a 24-bit counter implemented in the FPGA. The conversion counter is clocked by an 8MHz clock signal. Periods from 12.375μ seconds to 2.0889 seconds can be programmed. The output of this conversion counter is used to trigger the start of new conversions. Triggers generated by the conversion counter are also referenced as hardware timer generated triggers in chapter 3 of this manual.

The conversion counter is used to synchronize the transfer of DAC FIFO data to the DAC ICs. By the count of 20hex all eight channels of FIFO data have been read from the FIFO and loaded into internal FPGA data holding registers. At this time channels 0 to 3 and 4 to 7 will be moved serially to their corresponding DAC.

The FIFO read circuitry uses the PCI clock which must not be less than 16MHz for DAC loading circuit to function correctly.

It is not required to update all DAC data on every FIFO refresh cycle. Channels not updated will retain their last valid DAC data value. The update of a subset of all the channels, if desired, is controlled by the use of the FIFO Sample Valid Flag bit-19 which goes active (high) on the last valid data for the present FIFO cycle. Those channels not updated will retain their last analog output value. On power-up or software reset the holding registers will be cleared.

DAC External Trigger

The external trigger connections are made via pin 3 (Digital Channel 1) of the Field I/O Connector. For all modes of operation, when the external trigger input is enabled via bits 3 and 2 of the DAC Control register, the falling edge of the external trigger will initiate conversions for all channels. For External Trigger Input mode (bits 3 and 2 set to digital value "01"), each falling edge of the external trigger causes a conversion at the DAC. Once the external trigger signal has been driven low, it should remain low for a minimum of 250n seconds for proper external trigger operation. The external trigger input signals must be TTL compatible.

As an output, an active-low TTL signal is driven from the APC730. The trigger pulse generated is low for 500n seconds, typical. The external trigger connections are made via pin 37 (Digital Channel 9) of the Field I/O Connector. For all modes of operation, the external trigger is enabled as an output via bits 3

and 2 of the control register. See section 3.0 for programming details to make use of this signal.

DAC Interrupt Control Logic

The APC730 can be configured to generate an interrupt on a programmable FIFO Threshold. When the FIFO contains less samples than the set Threshold an interrupt will be issued. The interrupt will remain asserted to the system as long as the FIFO contains less data than the set threshold and interrupts remain enabled.

DAC Calibration Memory Control Logic

The FPGA of the APC730 board contains control logic that implements read and write accesses to calibration memory. The calibration memory (EEPROM) contains offset and gain coefficients for each of the DAC channels. Calibration of the individual DACs is implemented via software to avoid the mechanical drawbacks of hardware potentiometers.

COUNTER TIMER CONTROL LOGIC

Six different counter/timer modes may be selected: Pulse Width Modulation, Watchdog, Event Counting, Pulse Measurement, Period Measurement, and One Shot.

Counter output is an open drain n-channel mosfet. The drain is pulled-up to +5V via an on board 4.7K resistor (default), or can be left for external pull-up (according to the placement of the SW1 – Position 10). The SW1 DIP switch location is shown in Drawing 4501-946. The use of an external supply allows the drain pullups to adjust to different drive levels.

Counter timer input control signals: counter input, external clock, gate-off, and external trigger are available via digital I/O channels 2 to 5. See table 2.2 for the list of these signals and their corresponding digital channel. The digital channels 0 to 7 must all be selected as input if any one of these counter timer input control signals is to be used.

DIGITAL INPUT/OUTPUT LOGIC

The digital field I/O interface to the APC730 board is provided through Field I/O Connector (refer to Table 2.2). Field I/O points are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

Digital input/output signals to the FPGA are buffered using octal-buffered line drivers. Field inputs to these buffers include transient protection devices on each line and 4.7K pullups to +5V. Output operation is considered 'Fail-safe'. That is, the Digital Input/Output signals are always configured as input upon power-up reset or software reset. This is done for safety reasons to ensure reliable control under all conditions.

Digital channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions on all channels (channels 0-15). The interrupt is released via a write to the corresponding bit of the Digital Interrupt Status register.

Digital Input Debounce Control Logic

Each of the 16 digital channels can be individually debounced. Four debounce durations are available 4μ seconds, 64μ seconds, 1m second, and 8m seconds. The digital input signal must have a duration greater than the selected debounce duration in order to be recognized as a valid input signal.

APC Software

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/NT4/2000/XP®) applications accessing Acromag PMC I/O module products, PCI I/O Cards, and CompactPCI I/O Cards. This software (Model PCISW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments including Visual C++™, Visual Basic®, Borland C++ Builder® and others. The DLL functions provide a high-level interface to PMC modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

In addition, Acromag provides a software product (sold separately) consisting of APC730 VxWorks® library or QNX® library. This software (Model PMCSW-API-VXW or Model PCISW-API-QNX) is composed of VxWorks® or QNX® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

The APC730 is shipped pre-calibrated by Acromag and may be returned at the discretion of the customer to measure the accuracy of the calibration at some defined period. Recalibration, if required, can be performed by the customer if the proper equipment is available to them and is otherwise offered through the Service Department at Acromag for a fee.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag’s Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration…… Short PCI 5 Volt Board. (+3.3 V Tolerant)
- Height..... 4.200 inches (106.68 mm).
- Depth…….. 6.600 inches (167.64 mm).
- Board Thickness..... 0.062 inches (1.59 mm).
- Max Component Height….. 0.570 inches (14.48 mm).
- Recommended Card Spacing…….. 0.800 inches (20.32 mm).

Connectors:
- PCI Local Bus interface…... PCI Specification Version 2.2. 5 V card "finger" edge spacing. (+3.3 V Tolerant)
- Field I/O…….. 68-pin, SCSI-3, female receptacle header (AMP 787082-7 or equivalent).

Power Requirements		Board APC730
5V[2] (±5%)	Typical	245 mA
	Max.	290 mA
+12V[3] (±5%)	Typical	100 mA
	Max.	140 mA
-12V[3] (±5%)	Typical	85 mA
	Max.	125 mA

Note:
1. Circuit board is selectively coated with a fungus resistant acrylic conformal coating.
2. Maximum rise time of 100m seconds.
3. Note: This board also uses a DC-DC converter, which uses the 5V supply from the PCI bus connector (P1) and generates +/-15 volt supplies for the board.

ENVIRONMENTAL

Operating Temperature..... 0 to +70°C. -40°C to +85°C (E Version)
Relative Humidity…..... 5-95% Non-Condensing.
Storage Temperature..... -55°C to 100°C.
Non-Isolated..... Logic and field commons have a direct electrical connection.

Radiated Field Immunity[3] (RFI). Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.5% of FSR.

Electromagnetic Interference Immunity[3] (EMI)…..... Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity…… Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity[3](EFT)…….. Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions[3]…..... Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

Note:
4. Reference Test Conditions: Temperature 25°C, 50K conversions/second, using a 2 meter shielded cable length connection to the field analog input and output channels.

ENVIRONMENTAL

FCC: All Models are compliant to standard FCC PART 15, Subpart.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this installation does cause harmful interference to the radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or experienced radio/TV technician for help.*

Reliability Prediction

Mean Time Between Failure….. MTBF = TBD hours (not available at time of printing) @ 25°C, Using MIL-HDBK-217F, Notice 2.

ANALOG INPUTS

Input Channels (Field Access).. 32 Single-ended or 16 Differential

	Via 68-pin front panel connector.
Input Ranges (DIP switch selectable):	Bipolar –3.3 to +3.3 Volts[4] Bipolar -5 to +5 Volts[4] Bipolar -10 to +10 Volts[4] Unipolar 0 to +5 Volts[4] Unipolar 0 to +10 Volts[4]

Note:

4. Input signal ranges may actually fall short of reaching the specified endpoints due to hardware limitations. If an input may reach zero volts or less, a bipolar input range should be selected.

   Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating. It must be referenced to analog common on the PCI board and be within the normal input voltage range.

   Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Drawing 4501-947 for analog input connections for differential-ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

A/D Conversion Time	10uS Maximum
Conversion Rate	100KHz Maximum
Analog Input Memory Buffer	512 Sample Memory
Input Signal Type	Voltage (Non-isolated).
Input Overvoltage Protection	+55 to -40 Volts Power Off

ADC Spec's

ADC	Analog Devices AD977AR or TI/Burr Brown ADS7809U
A/D Resolution	16-bits.
Data Format	Binary 2's Complement and Straight Binary
No Missing Codes	No Missing Codes 15-bits ADC
A/D Integral Linearity Error	±3 LSB Maximum ADC
Unipolar Zero Error[5]	±10mV Maximum, for Unipolar Ranges.
Bipolar Offset Error[5]	±10mV Maximum, for Bipolar Ranges.
Full Scale Error[5]	±0.5% Maximum.
Input Resistance	1GΩ, Typical

Instrumentation Amplifier

INAMP	TI/Burr-Brown INA128
Nonlinearity	±0.001% of FSR Maximum
Offset Voltage[5]	±550μ Volt Maximum
Gain Error[5]	±0.024% Maximum
Settling Time	7μ seconds Typical to 0.01%

Note:

5. Software calibration minimizes these error components.

Calibration Reference Voltages

Calibration Voltage[6]	Maximum Tolerance[7] @25 ^{O}C (Volts)	Maximum Temperature Drift[8] (ppm/^{O}C)
9.88V	±300μV	±25
4.94V	±300μV	±25
2.47V	±300μV	±25
1.23V	±300μV	±25
0.0V	±300μV	0

Note:

6. The calibration voltages are not set precisely to these voltages. The actual calibration voltages must be read from the calibration coefficient memory of the APC730 board (see Table 3.13).
7. A total of 512 input samples were averaged with a throughput Rate of 200khz conversions/second.
8. Worst case temperature drift is the sum of the ±10 ppm/^{O}C drift of the calibration voltage reference, plus the ±10 ppm/^{O}C of series resistor R2, plus the ±5 ppm/^{O}C drift of the resistors in the voltage divider.

Maximum Overall Calibrated Error @ 25°C

The maximum corrected (i.e. calibrated) error is the worst-case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C.

ADC Range (Volts)	Max Err[9,10,11] ±LSB (% Span)	Typ. Err[9,10,11] ±LSB (% Span)
-3.33 to +3.33	±15.39 LSB (0.0235%)	±5 LSB (0.007%)
-5 to +5	±7.3 LSB (0.0111%)	±4.6 LSB (0.007%)
-10 to +10	±7.13 LSB (0.0108%)	±2 LSB (0.0031%)
0 to +5	±13.73 LSB (0.0209%)	±7 LSB (0.01%)
0 to +10	±8.91 LSB (0.0135%)	±5 LSB (0.007%)

Note:

9. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.
10. Reference Test Conditions: Temperature 25°C, Differential inputs, channels 0 to 15, 100K conversions/second, 512 input samples averaged, 512 autozero values averaged, and 512 calibration voltages averaged, with a 2-meter shielded cable length connection to the field analog input signals.
11. For critical applications, multiple input samples should be averaged to improve performance.

Input Noise[12]..... 3 LSB rms, Typical. ±10V input range

Note:

12. Temperature 25°C, Differential inputs, channels 0 to 15, 100K conversions/second. A total of 2048 input samples were taken statistically, assuming a normal distribution, to determine the RMS value.

ADC External Trigger Input/Output

As An Input:..... Must be an active low 5 volt logic TTL compatible, signal referenced to digital common. Conversions are triggered on the active low state of this trigger signal. Minimum pulse width 250nano seconds. Conversions are triggered 250nano to 375nano seconds after the external trigger signal goes active for External Trigger Only scan mode. For all other scan modes the first conversion is triggered 10μ seconds after the external trigger or software trigger goes active.

Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for typically 500nano seconds

As An Output:.....

ANALOG OUTPUTS

Output Channels…… Eight Single Ended Channels
FIFO Buffer…… 1024 samples buffer, shared for all channels
Output Signal Type..... Voltage (Non-isolated).
Output Range[13]…… Bipolar -10 to +10 Volts

Note:

13. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.

    The accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads > 100KΩ) provide the best accuracy. For low impedance loads, the effects of source and cabling resistance should be considered.

Output Current…… -10mA to +10mA (Maximum); this corresponds to a minimum load resistance of 1KΩ with a 10V output.
DAC Data Format…… Straight Binary.
Resolution..... 16-bits.
Monotonicity over Temperature 15-bits
Linearity Error…… ±2LSB
System Accuracy[14]…… ±3LSB

Note:

14. Offset and gain calibration coefficients stored in coefficient memory must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error and is with outputs unloaded at 25°C.

Conversion Time (per channel)[15]. 12.375μSec
Settling Time[15]…… 12uS to within 0.01% of FSR for a 18V step change (load of 2KΩ in parallel with 8pF).

Note:

15. The conversion time includes the time from software start convert or external trigger until a Load DAC signal goes active. To obtain the overall time to the point when the signal settles to 0.01% of FSR, the settle time must be added to the conversion time. However, for continuous conversions the conversion time and settle time will overlap so continuous conversions can be performed every 12.375μSec.

Output at Reset…… Bipolar Zero Volts
Output Noise…… 2mV rms in a 20MHz bandwidth, Typical.
Short Circuit Protection…… Indefinite at 25°C

Output Load Stability……	Maximum recommended capacitive load is 100pF. Capacitive loads up to 0.01μF can be tolerated, but with additional overshoot.
Offset Voltage Error[16]…..……	34.2mV@25°C
Gain Voltage Error[16]……	62mV@25°C
Offset Voltage Drift……	84μV/°C
Gain Voltage Drift…..……	123.75μV/°C

Note:

16. Software calibration minimizes these error components.

External Trigger Input/Output

As An Input:.....…..…	Negative edge triggered. Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered within 12.375μ seconds of the falling edge. Minimum pulse width is 250n seconds.
As An Output…….....	Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for typically 500n seconds.

Digital Input/Output[17]

Channel Configuration……..	16 Bi-directional TTL Transceivers Direction controlled as two groups of 8 channels.
Reset/Power Up Condition…..	Default to Input.
Pull-up Resistors…….....	4.7KΩ resistor networks are installed in sockets. Each network has 8 resistors.
V_{OH}……	3.0V typical
V_{OL}……..	0.3V typical
I_{OH}…….....	-15.0mA
I_{OL}……..	64mA
V_{IH}…….....	2.0V minimum
V_{IL}…….....	0.8V maximum
Input Signal Hysteresis……	200mV typical
Input Debounce……..	Debounce circuitry allows individual debounce of 16 channels.
Debounce Intervals……	4μs, 64μs, 1m, and 8m

Note:

17. The 16 digital I/O lines of this board are assembled in groups of eight. Each group of eight can be configured as input or output. The first group of eight is on pins 2 to 9 while the other is on pins 36 to 43. The digital I/O signals are TTL with 4.7K socketed pull-up resistors. These digital signals as inputs can be used to control the operation of the 32-bit Counter/Timer provided in this board. These signals can also be used for external trigger input or output for the ADC and DAC logic.

32-Bit Counter

Counter Functions…..……	Pulse Width Modulation, Watch Dog, Event Counting, Pulse Measurement, Period Measurement, or One Shot
Counter Clock Frequencies….	8MHz, 4MHz, 1MHz, or External up to 3.4MHz

Counter Output[17]

Mosfet ……..……..	IPS024G International Rectifier
Continuous Drain to Source Voltage……..	35 Volts maximum recommended
Continuous Drain Current……..	1 A maximum
Rise Time…….....	0.9μs typical
Fall Time……..	1.3μs typical

Note:

17. The Counter Output, on pin 1, is programmable as active high or low. This output is the open-drain of an N-channel mosfet with a common source connection. The drain 4.7K pull-up to +5 volts is the default configuration. Placing SW1 Dip Switch – Position 10 to "OFF" position will require the use of an external voltage (35 volts maximum) and external pull-up resistor.

Board Crystal Oscillator

Clock Frequency…….....	16MHz
Frequency Stability……..…	100ppm This is ±6.25ps for each clock cycle. For example, if you were to measure a pulse with a half second duration, using the counter measurement function, your accuracy would be ±50μs.

PCI Local Bus Interface

Compatibility.....….....	Conforms to PCI Local Bus Specification, Revision 2.2
Electrical/Mechanical Interface..	Short 5V Board
PCI Target ……..……	Implemented by Altera FPGA
4K Memory Space Required…	One Base Address Register
PCI commands Supported…..	Configuration Read/Write Memory Read/Write, 32,16, and 8-bit data transfer types supported.
Signaling …….....	5V Compliant, 3.3V Tolerant
INTA#……..……	Interrupt A is used to request an interrupt. Source of interrupt can be from the ADC, DAC, Digital I/O, or Counter Function.

Access Times…… 8 PCI Clock Cycles for all non-burst register accesses. Burst read of the 512 sample ADC memory buffer requires three PCI clock cycles for each sample read.

A write access to the DAC FIFO Buffer will typically be executed in 8 PCI clock cycles. On rare occasions the write will complete as a **retry termination.** The retry termination is necessary to avoid FIFO Buffer contention when a FIFO read is initiated simultaneously with an internal FIFO write. On a retry termination the bus master is forced to initiate another write to the same address at a later time.

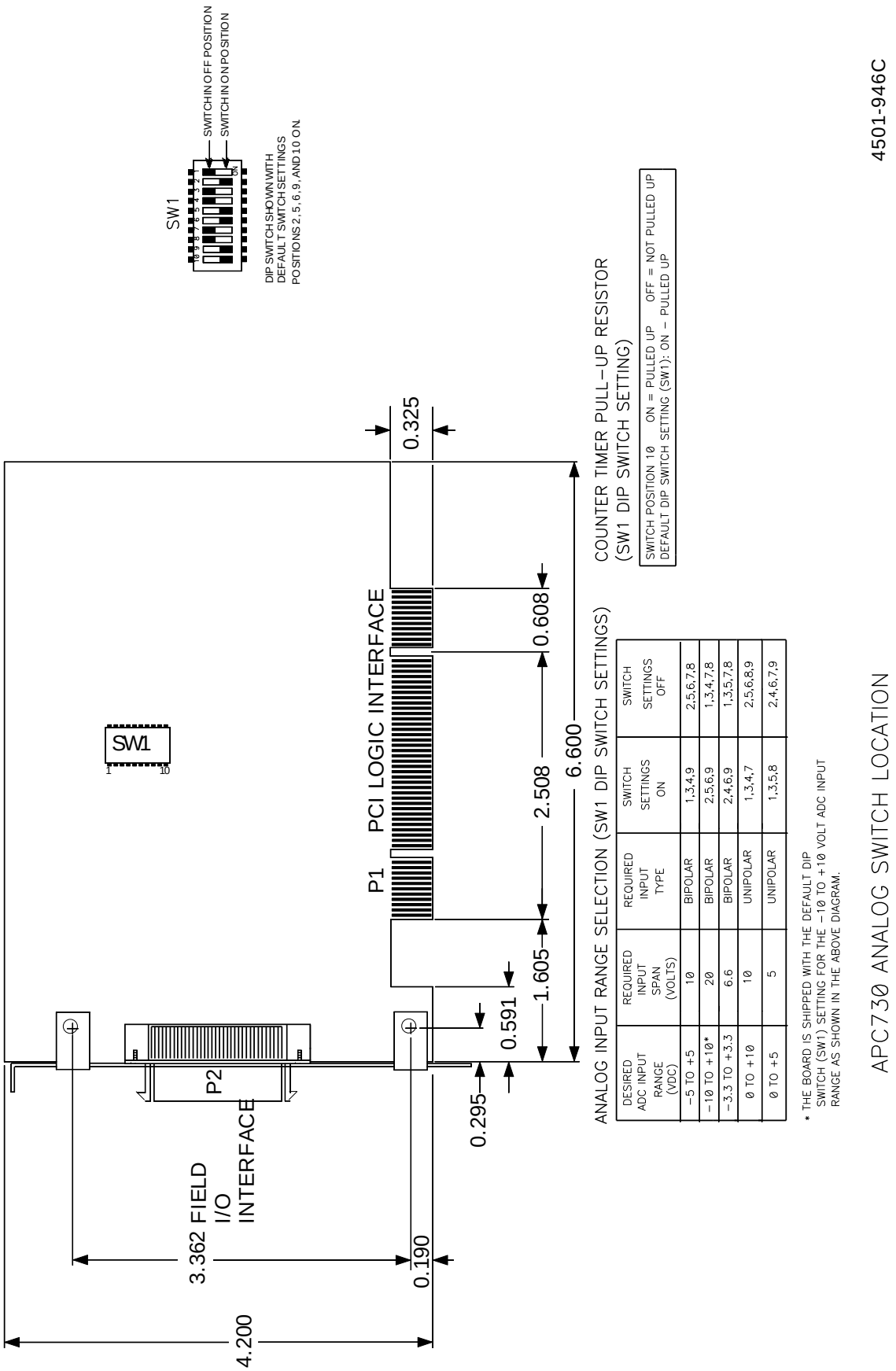
APPENDIX

CABLE: MODEL 5028-432 (SCSI-3 to SCSI-3, Shielded)

Type: Round shielded cable, 34 twisted pairs (SCSI-3 male connector at both ends). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-288 termination panel to the APC730 Board.
Length: Standard length is 2 meters (6.56 feet). Consult factory for other lengths. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 68 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: SCSI-3, 68-pin male connector with backshell.
Keying: The SCSI-3 connector has a “D Shell”.
Schematic and Physical Attributes: See Drawing 4501-919.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-3 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-3 connector spec.’s).
Operating Temperature: -30°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-288

Type: Termination Panel For PCI Board Boards
Application: To connect field I/O signals to the PCI Board.
Termination Panel: Acromag Part 4001-066. The 5025-288 termination panel facilitates the connection of up to 68 field I/O signals and connects to the PCI Board (connectors only) via a round shielded cable (Model 5028-432). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-68) correspond to field I/O (pins 1-68) on the PCI board. Each PCI board has its own unique pin assignments. Refer to the PCI board manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-920.
Field Wiring: 68-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.0 pounds (0.5kg) packaged.



COUNTER TIMER PULL-UP RESISTOR
(SW1 DIP SWITCH SETTING)

SWITCH POSITION 10	ON = PULLED UP	OFF = NOT PULLED UP
DEFAULT DIP SWITCH SETTING (SW1):	ON – PULLED UP	

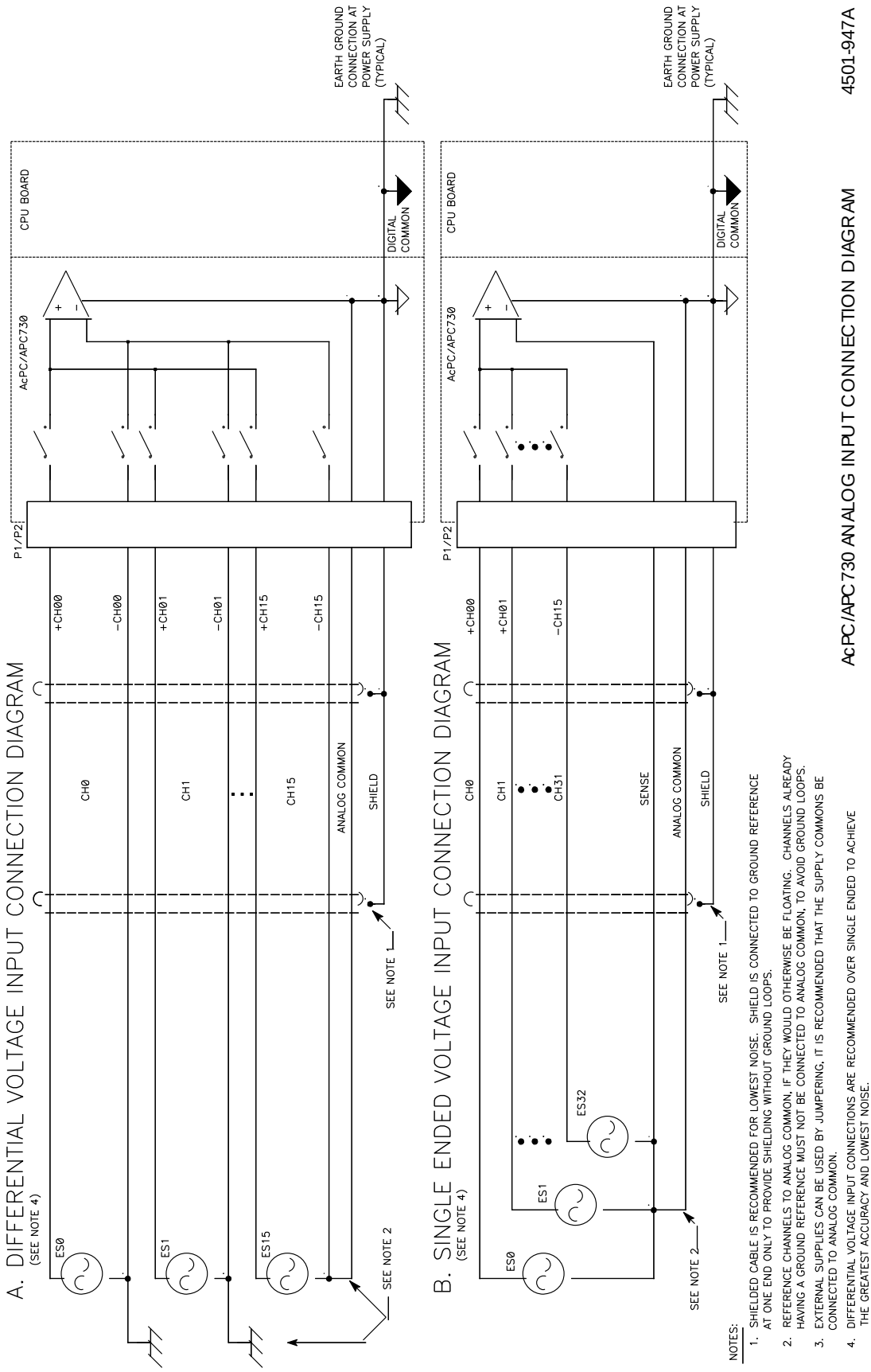
ANALOG INPUT RANGE SELECTION (SW1 DIP SWITCH SETTINGS)

DESIRED ADC INPUT RANGE (VDC)	REQUIRED INPUT SPAN (VOLTS)	REQUIRED INPUT TYPE	SWITCH SETTINGS ON	SWITCH SETTINGS OFF
–5 TO +5	10	BIPOLAR	1,3,4,9	2,5,6,7,8
–10 TO +10*	20	BIPOLAR	2,5,6,9	1,3,4,7,8
–3.3 TO +3.3	6.6	BIPOLAR	2,4,6,9	1,3,5,7,8
0 TO +10	10	UNIPOLAR	1,3,4,7	2,5,6,8,9
0 TO +5	5	UNIPOLAR	1,3,5,8	2,4,6,7,9

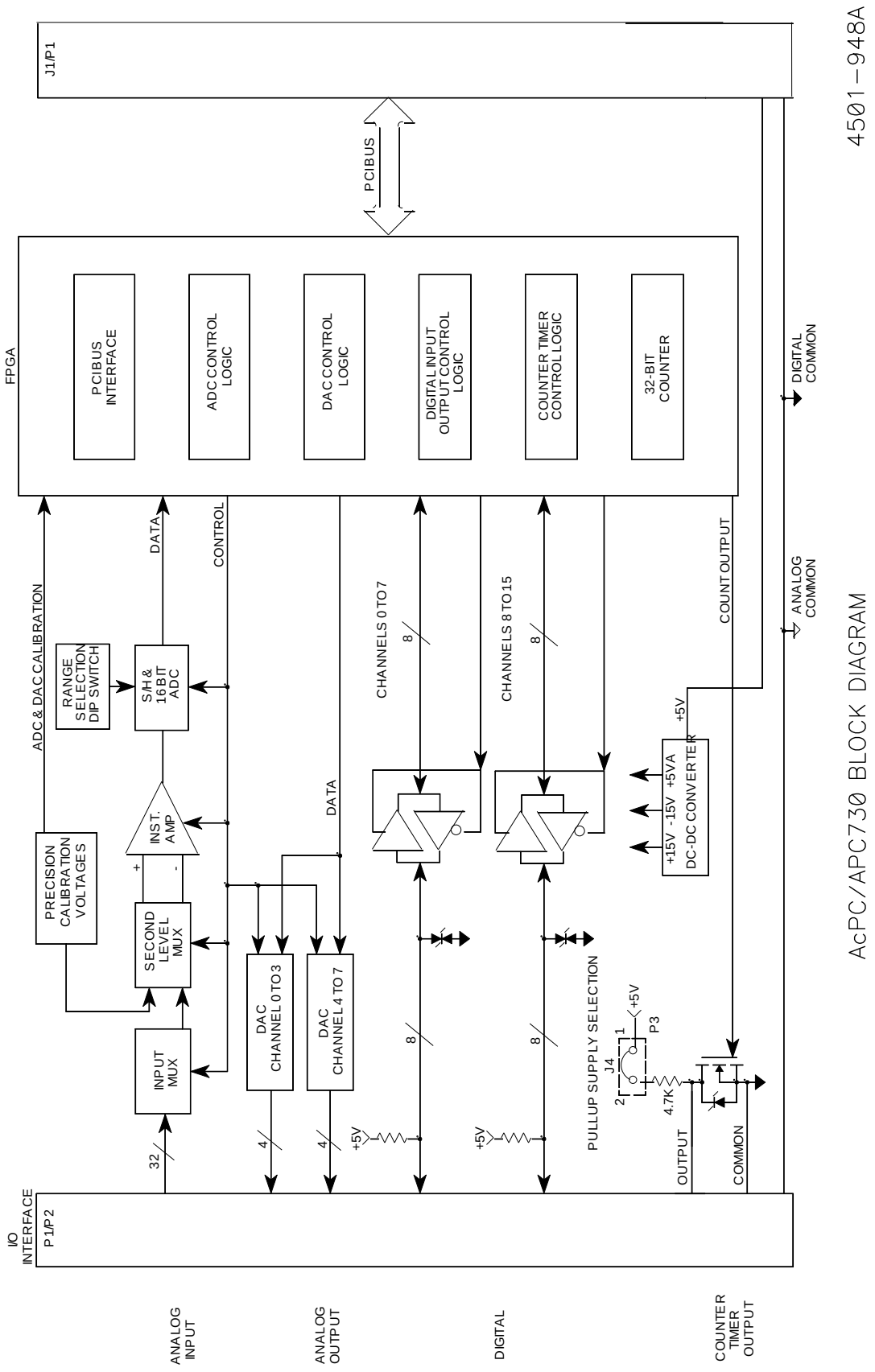
* THE BOARD IS SHIPPED WITH THE DEFAULT DIP SWITCH (SW1) SETTING FOR THE –10 TO +10 VOLT ADC INPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

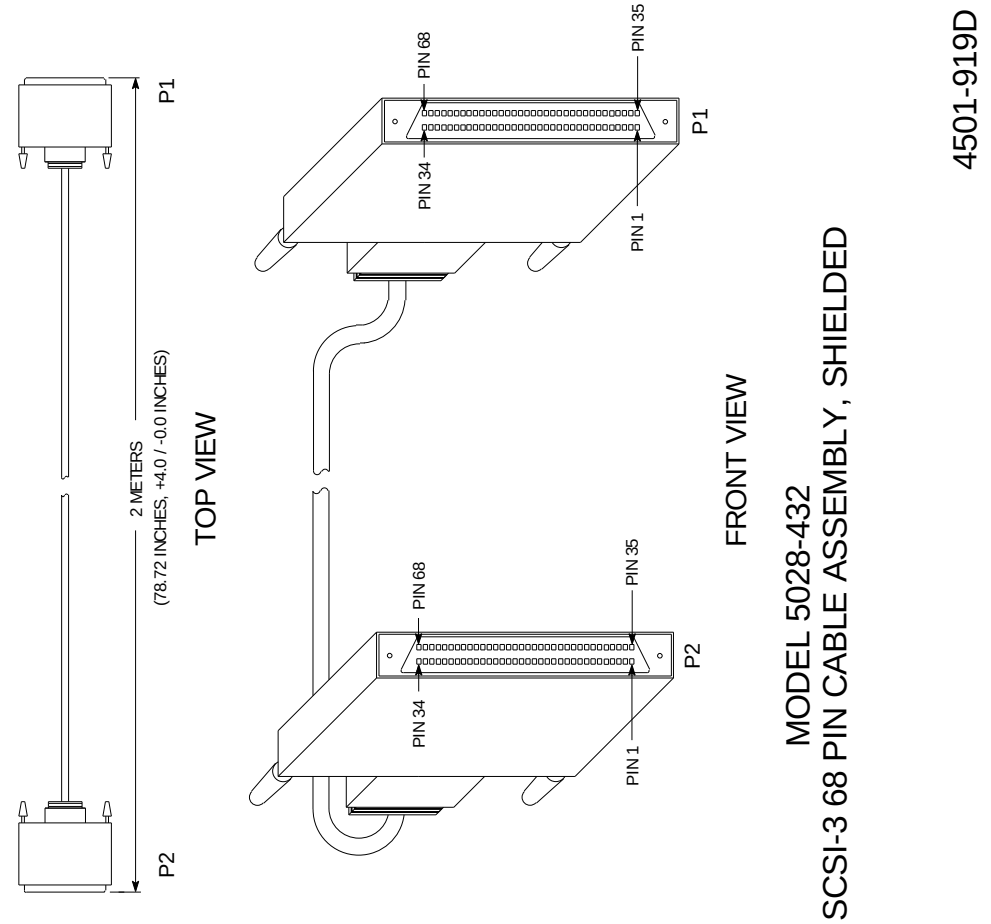
APC730 ANALOG SWITCH LOCATION

4501-946C



AcPC/APC730 ANALOG INPUT CONNECTION DIAGRAM 4501-947A


4501-948A
AcPC/APC730 BLOCK DIAGRAM
J1/P1
PCIBUS
FPGA
PCIBUS INTERFACE
ADC CONTROL LOGIC
DAC CONTROL LOGIC
DIGITAL INPUT OUTPUT CONTROL LOGIC
COUNTER TIMER CONTROL LOGIC
32-BIT COUNTER
DIGITAL COMMON
ANALOG COMMON
ADC & DAC CALIBRATION
RANGE SELECTION DIP SWITCH
S/H & 16BIT ADC
DATA
CONTROL
CHANNELS 0 TO 7
CHANNELS 8 TO 15
COUNT OUTPUT
+5V
+15V -15V +5VA
DC-DC CONVERTER
INST. AMP
PRECISION CALIBRATION VOLTAGES
SECOND LEVEL MUX
INPUT MUX
DAC CHANNEL 0 TO 3
DAC CHANNEL 4 TO 7
PULLUP SUPPLY SELECTION
J4
P3
4.7K
OUTPUT
COMMON
I/O INTERFACE
P1/P2
ANALOG INPUT
ANALOG OUTPUT
DIGITAL
COUNTER TIMER OUTPUT

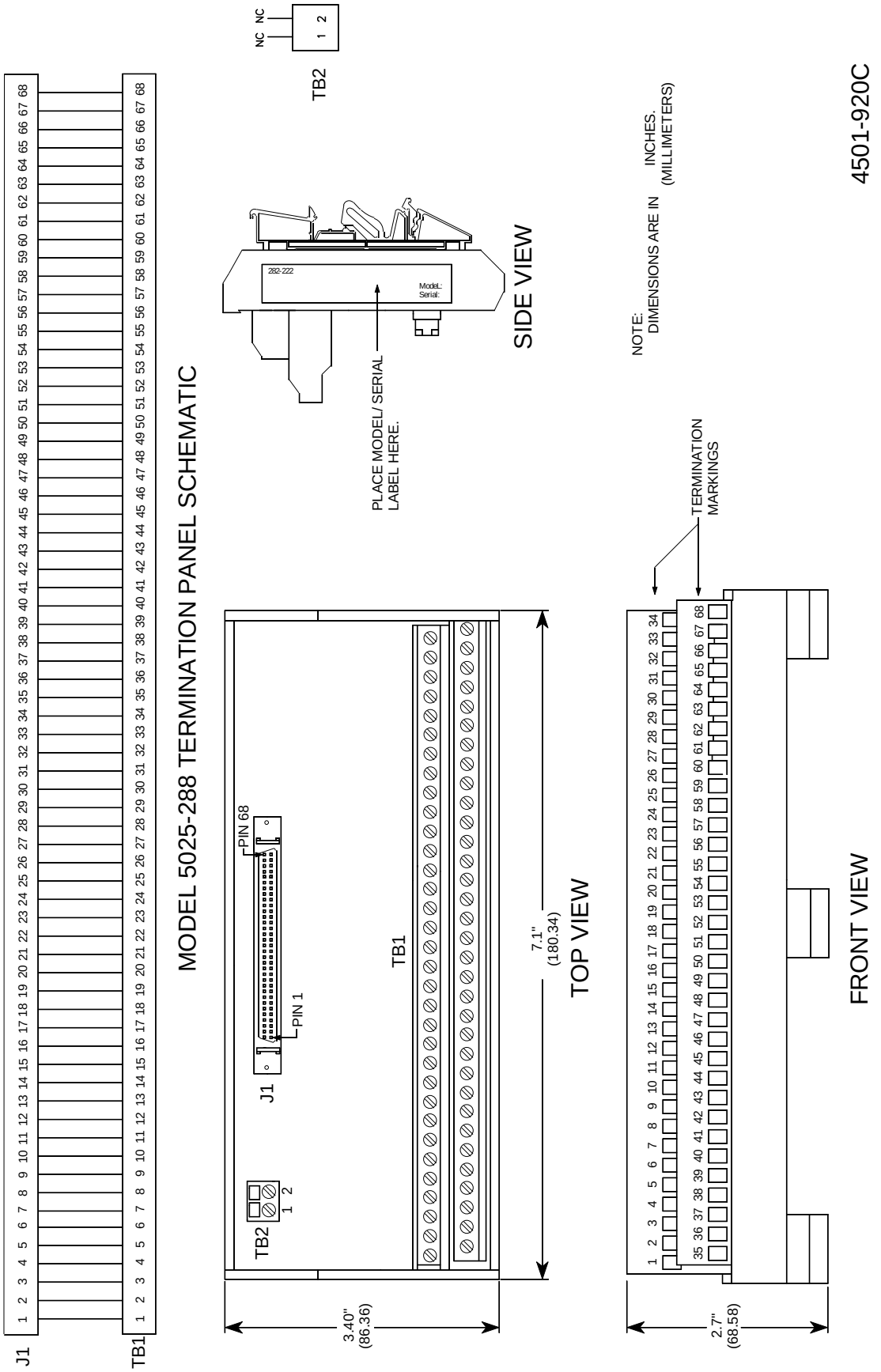


MODEL 5028-432
SCSI-3 68 PIN CABLE ASSEMBLY, SHIELDED

4501-919D



SCHEMATIC


MODEL 5025-288 TERMINATION PANEL SCHEMATIC
J1
TB1
TB2
NC NC
1 2
SIDE VIEW
282-222
Model:
Serial:
PLACE MODEL/ SERIAL LABEL HERE.
NOTE:
DIMENSIONS ARE IN INCHES.
(MILLIMETERS)
4501-920C
TERMINATION MARKINGS
PIN 68
PIN 1
TOP VIEW
7.1"
(180.34)
3.40"
(86.36)
FRONT VIEW
2.7"
(68.58)

NOTES:

REVISION HISTORY

The following table details the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
30-OCT-2002	A	CAP/KLK	Initial Acromag release.
25-NOV-2014	F	CAP/ARP	Updated manual for use of SW1 – Position 10 description and drawing 4501946 APC730 Analog Switch Location. Reference ECO #14L013.
03 AUG 2017	G	CAP/JAA	Remove CE Mark due to non-RoHS compliant part. Refer to ECN# 17G016.

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