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Acromag®

Series AVME9125 VMEbus 6U Card

16-Bit High Density Analog Input

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The AVME9125 VMEbus card performs precision 16-bit analog to digital conversions. The AVME9125 supports 16 channels of differential analog inputs. With the addition of the companion card the EXP9125, up to 32 channels of differential analog inputs can be selected for conversion.

The AVME9125 offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

KEY AVME9125 FEATURES

- **Interface for 32 Differential Channels** - Provides an electrical and mechanical interface for up to 32 Differential Channels. 16 differential channels are individually input via the P2 connector of the AVME9125 and the other 16 differential channels are multiplexed to a single differential pair using a companion Expander Card (EXP9125).
- **A/D 16-Bit Resolution** - 16-bit capacitor-based successive approximation Analog to Digital Converter (ADC) with integral sample and hold and reference.
- **Real Time Correction -** Correction logic is provided along with calibration autozero and autospan precision voltages to permit real time hardware correction of conversion errors. Trimmed calibration voltages include: 0V (local analog ground), and 9.79V.
- **Diagnostic Capability** - Diagnostic capability using ground and reference.
- **11.25µsec Conversion Time** - A maximum conversion rate of ≅ 88KHz is supported.

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- ±**10V A/D Range** - Bipolar ±10V range is supported.
- **Individual Channel Mail Box -** A storage buffer register is available for each of the 32 differential channels.
- **Programmable Control of Channel Scanning** - Scan all channels or a subset of the channels to allow an overall higher sample rate. Digitized channels include all sequential channels beginning with a specified start-channel value and ending with a specified end-channel value.
- **User Programmable Interval Timer** - Controls the delay between each channel converted when Uniform-Continuous or Single Scan modes are selected. If Burst-Continuous is selected, the Interval Timer controls the delay after a group of channels are converted before conversion is initiated on the group again. Supports a minimum interval of 11.25μsec and a maximum interval of 2.09 seconds.
- **Uniform Continuous Scanning Mode** - All channels selected for scanning are continually digitized in a round robin fashion with the interval between conversions controlled by the programmed interval timer. The results of each conversion are stored in the channel's corresponding mail box buffer. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Burst Continuous Scanning Mode** - All selected input scan channels are sequentially digitized at a ≅ 67KHz conversion rate (≅ 15μ second conversion time). At the end of a programmed interval time a new conversion of all channels is re-initiated. The conversion results are stored in each channel's mail box buffer. This mode can be used as a pseudo-simultaneous sampling mode for low to medium speed applications requiring simultaneous channel acquisition. For example, if four channels are selected then they could be pseudo-simultaneously converted every 60μ seconds (each of the channels actually takes ≅ 15μ seconds). This is repeated in bursts determined by the programmed interval time. The scan is initiated by a software or external trigger. Scanning is stopped by software control.
- **Uniform Single Cycle Scan Mode** - All channels selected for scanning are digitized once with the idle time between each channel conversion controlled by the programmed interval timer. The scan is initiated by a software or external trigger.
- **Burst Single Cycle Scan Mode** - All channels selected for scanning are digitized once at ≅ 67KHz conversion rate (≅15μsec/Channel). The scan is initiated by a software or external trigger.
- **Interrupt Upon Conversion Complete Mode** - May be programmed to interrupt upon completion of conversion for each individual channel or upon completion of conversion of the group of all scanned channels.
- **Software Programmable Interrupt Level** - The VMEbus interrupt level is software programmable. Additional registers are associated with each interrupt request for control and status monitoring.
- **New Data Register** - This register can be polled, to indicate when new digitized data is available in the mail box. A set bit indicates a new digitized data value is available in the bit's corresponding mail box register. Register bits are cleared upon read of their corresponding mail box register or start of a new scan cycle.
- **Missed Data Register** - A set bit in the Missed Data register indicates that the last digitized value was not read by the host computer quickly enough and has been overwritten by a new conversion. The Missed Data register has a bit corresponding to each of the 32 differential channels. Each Missed Data register bit is cleared by a read of its corresponding mail box data value or start of a new scan cycle.
- **Fault Protected Input Channels** - Analog input overvoltage protection from -35 V to +55 V is provided in the event of power loss or power off.
- ±**15 Volt Power Supplies -** On board ±15 volt power supplies are provided to accommodate the ±10 volt input signal span.
- **Individually Filtered Power** - Filtered +5V, +15V, and -15V DC power is provided to the card via passive filters present on each supply line. This provides optimum filtering and isolation between the system and the board and allows analog signals to be accurately measured without signal degradation from the system.
- **Base Address Jumpers -** The only hardware jumper settings required on the board set the base address of the card in the VMEbus short I/O space.

VMEbus INTERFACE FEATURES

- **Slave Module**-Board Register Short I/O Access A16, D16/D08(O)
- **Supports Short I/O Address Modifiers** - Supports short I/O (A16) address modifiers 29H, 2DH (H = Hex), only. The board base address is set by hardware jumpers and decoded on 256 byte boundaries.
- **Supports Read-Modify-Write Cycles** - The board supports VMEbus read-modify-write cycles.
- **Interrupt Support** - I(1-7) interrupter D16/D08 (O). The VMEbus interrupt level is software programmable. The board's software programmable registers are utilized as interrupt request control and status monitors. Interrupt release mechanism is Release On Register Access (RORA) type.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

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For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.



This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of this board, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured for different applications. All possible configuration settings will be discussed in the following Sections.

VMEbus INTERFACE CONFIGURATION

The board is shipped from the factory configured as follows:

- With VMEbus Short I/O Base Address of 00XXH. Board will respond to both Address Modifiers 29H (short non-privileged I/O) and 2DH (short supervisory I/O). Registers on the board will be accessible.
- Programmable software registers default to interrupt requests-disabled and VMEbus interrupt level-none.

Address Decode Jumper Configuration

The AVME9125 board interfaces with the VMEbus as a 256 byte block of address locations in the VMEbus short I/O address space (refer to Section 3 for memory map details). J1 decodes the eight most significant address lines A8 through A15 to provide 256 byte segments of address space. The configuration of the jumpers for different base address locations is shown in Table 2.1. "IN" means that the pins are shorted together with a shorting clip. "OUT" indicates that the clip has been removed. The jumper locations are shown in Drawing 4501-679.

Table 2.1: Address Decode Jumper Selections (J1 Pins)

Addr Line	Jumper Pins	Base Addr 00XXh	Base Addr 07XXh	Base Addr 1BXXh	Base Addr FFXXh[1]
A15	15-16	OUT	OUT	OUT	IN
A14	13-14	OUT	OUT	OUT	IN
A13	11-12	OUT	OUT	OUT	IN
A12	09-10	OUT	OUT	IN	IN
A11	07-08	OUT	OUT	IN	IN
A10	05-06	OUT	IN	OUT	IN
A09	03-04	OUT	IN	IN	IN
A08	01-02	OUT	IN	IN	IN

1) When the board is shipped from the factory, it is configured for default hardware jumper configuration of 00XX hex.
2) Consult your host CPU manual for detailed information about addressing the VMEbus short I/O (A16, 16-bit) space. In many cases, CPU's utilizing 24-bit addressing will start the 16-bit address at FF0000 (Hex), and 32-bit CPU's at FFFF0000 (Hex).

VMEbus Address Modifiers

No hardware jumper configuration is needed. The AVME9125 board will respond to both address modifiers 29H and 2DH in the VMEbus short I/O space. This means that both short supervisory and short non-privileged accesses are supported.

Interrupt Configuration

No hardware jumper configuration is required. All interrupt enabling, status, and VMEbus interrupt level selections are configured via programmable registers on the AVME9125 board (see Section 3 for programming details).

VMEbus Connections

The AVME9125 communicates with the Host computer in the short I/O addressing space on the P1 connector. The P2 connector is used to receive 16 differential analog input signals for analog to digital conversion. In addition, the P2 connector is used to communicate with the Expander card (EXP-9125) for interface to an additional 16 differential analog signals.

Table 2.2 indicates the pin assignments for the VMEbus signals at the P1 connector. The P1 connector is the upper rear connector on the AVME9125 board, as viewed from the front. The connector consists of 32 rows of three pins labeled A, B, and C. Pin A1 is located at the upper left hand corner of the connector if the board is viewed from the front.

VMEbus connector P2 is the lower rear connector on the AVME9125 board, as viewed from the front. Table 2.3 indicates the pin assignments for the signals of the P2 connector.

Refer to the VMEbus specification for additional information on the VMEbus signals.

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Pin assignments for the P1 connectors of the AVME9125 are shown in Table 2.2:

TABLE 2.2: VMEbus P1 CONNECTIONS

Pin	Description	Pin	Description	Pin	Description
1A	D00	1B	***BBSY****	1C	D08
2A	D01	2B	***BCLR****	2C	D09
3A	D02	3B	***ACFAIL****	3C	D10
4A	D03	4B	BG0IN*	4C	D11
5A	D04	5B	BG0OUT*	5C	D12
6A	D05	6B	BG1IN*	6C	D13
7A	D06	7B	BG1OUT*	7C	D14
8A	D07	8B	BG2IN*	8C	D15
9A	GND	9B	BG2OUT*	9C	GND
10A	SYSCLK	10B	BG3IN*	10C	***SYSFAIL****
11A	GND	11B	BG3OUT*	11C	***BERR****
12A	DS1*	12B	***BR0****	12C	SYSRESET*
13A	DS0*	13B	***BR1****	13C	LWORD*
14A	WRITE*	14B	***BR2****	14C	AM5
15A	GND	15B	***BR3****	15C	***A23***
16A	DTACK*	16B	AM0	16C	***A22***
17A	GND	17B	AM1	17C	***A21***
18A	AS*	18B	AM2	18C	***A20***
19A	GND	19B	AM3	19C	***A19***
20A	IACK*	20B	GND	20C	***A18***
21A	IACKIN*	21B	***SERCLK***	21C	***A17***
22A	IACKOUT*	22B	***SERDAT****	22C	***A16***
23A	AM4	23B	GND	23C	A15
24A	A07	24B	IRQ7*	24C	A14
25A	A06	25B	IRQ6*	25C	A13
26A	A05	26B	IRQ5*	26C	A12
27A	A04	27B	IRQ4*	27C	A11
28A	A03	28B	IRQ3*	28C	A10
29A	A02	29B	IRQ2*	29C	A09
30A	A01	30B	IRQ1*	30C	A08
31A	-12V	31B	***+5V STDBY***	31C	+12V
32A	+5V	32B	+5V	32C	+5V

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by the board.

The P2 connector provides the analog input interface for the AVME9125 and the companion Expander board (EXP9125). The P2 pin assignments are given in Table 2.3. When reading Table 2.3 note that channel designations are abbreviated to save space. For example channel 0 plus input is abbreviated CH0+.

Channels 0 to 15 are input direct to the AVME9125 while channels 16 to 31 are multiplexed on the EXP9125 board and a single input pair signals Analog+ and Analog- are connected for input to the AVME9125 via the P2.

Pins 1 to 6 of rows A and C are used to interface to the EXP9125. Signals CHSel3 to CHSel0 are used to control an analog multiplexer for selection of one of channels 16 to 31. Signal CHSel0 also serves to indicate the presence of the EXP9125 to the AVME9125. The EXP9125 will pull CHSel0 high when present. Lastly, the AVME9125 provides ± 15 volts to the EXP9125 via the P2 connector.

Pin assignments for the P2 connectors of the AVME9125 are shown in Table 2.3:

Table 2.3: AVME9125 P2 Pin Assignments

Pin	Description	Pin	Description	Pin	Description
1A	ChSel3	1B	Not Used	1C	Ground
2A	ChSel2	2B	Not Used	2C	Analog+
3A	ChSel1	3B	Not Used	3C	Analog-
4A	ChSel0/ EXP9125 Present	4B	Not Used	4C	Ground
5A	Autoz/Ch_	5B	Not Used	5C	Ground
6A	+15V DC	6B	Not Used	6C	-15V DC
7A	Not Used	7B	Not Used	7C	Not Used
8A	Not Used	8B	Not Used	8C	Shield
9A	Analog Com	9B	Not Used	9C	Analog Com
10A	CH14-	10B	Not Used	10C	CH15-
11A	CH14+	11B	Not Used	11C	CH15+
12A	Analog Com	12B	Not Used	12C	Analog Com
13A	CH12-	13B	Not Used	13C	CH13-
14A	CH12+	14B	Not Used	14C	CH13+
15A	Analog Com	15B	Not Used	15C	Analog Com
16A	CH10-	16B	Not Used	16C	CH11-
17A	CH10+	17B	Not Used	17C	CH11+
18A	Analog Com	18B	Not Used	18C	Analog Com
19A	CH8-	19B	Not Used	19C	CH9-
20A	CH8+	20B	Not Used	20C	CH9+
21A	Analog Com	21B	Not Used	21C	Analog Com
22A	CH6-	22B	Not Used	22C	CH7-
23A	CH6+	23B	Not Used	23C	CH7+
24A	Analog Com	24B	Not Used	24C	Analog Com
25A	CH4-	25B	Not Used	25C	CH5-
26A	CH4+	26B	Not Used	26C	CH5+
27A	Analog Com	27B	Not Used	27C	Analog Com
28A	CH2-	28B	Not Used	28C	CH3-
29A	CH2+	29B	Not Used	29C	CH3+
30A	Analog Com	30B	Not Used	30C	Analog Com
31A	CH0-	31B	Not Used	31C	CH1-
32A	CH0+	32B	Not Used	32C	CH1+

POWER-UP TIMING AND LOADING

The AVME9125 board uses Field Programmable Gate-Arrays (FPGA) to handle the bus interface and control logic timing. Upon power-up, the FPGAs automatically clocks in configuration vectors from a local serial PROM to initialize the logic circuitry for normal operation. This time is measured as the first 145mS (typical) after the +5 Volt supply rises to +2.5 Volts at power-up. The VMEbus specification requires that the bus master drive the system reset for the first 200mS after power-up, thus inhibiting any data transfers from taking place.

IP control registers are also reset following a power-up sequence, disabling interrupts, etc. (see Section 3 for details).

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DATA TRANSFER TIMING

VMEbus data transfer time is measured from the falling edge of DSx* to the falling edge of DTACK* during a normal data transfer cycle. Typical transfer times are given in the following table.

Register	Data Transfer Time
All Registers	800 nS, Typical.

FIELD GROUNDING CONSIDERATIONS

The AVME9125 board is designed with passive filters on each supply line. This provides maximum filtering and signal isolation between the AVME9125 board and the VMEbus system. However, the boards are considered non-isolated, since there is electrical continuity to the VMEbus grounds. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed.

A signal being measured cannot be floating—it must be referenced to analog common on the AVME9125. See Drawing 4501-688 for analog input connections for differential inputs.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to operate the AVME9125 non-intelligent VMEbus board.

The board is addressable on 256 byte boundaries in the Short I/O (A16) Address Space. This Acromag VMEbus non-intelligent slave has a Board Status register and Card Identification information. The 256 bytes of memory consumed by the board is composed of Card Identification, Status, Control, and Converted Data registers. The memory map for AVME9125 is shown in Tables 3.1 and 3.2.

MEMORY MAP

Table 3.1: AVME9125 6U Bd Short I/O Memory Map

Base Addr+	EVEN Byte D15 D08	ODD Byte D07 D00	Base Addr+
00 ↓ 3E	Card Identification Space Not Used	Card Identification Space Low Byte	01 ↓ 3F
40	Status Register		41
42	Control Register		43
44	Timer Prescaler	Interrupt Vector Register	45
46	Conversion Timer		47
48	End Channel Value	Start Channel Value	49
4A	New Data Register Channels 0 to 15		4B
4C	New Data Register Channels 16 to 31		4D
4E	Missed Data Register Channels 0 to 15		4F
50	Missed Data Register Channels 16 to 31		51
52	Not Used Bits15 to Bit 01	Start Convert Bit-0	53
54	Offset Coefficient		55
56	MSW of Gain Coefficient		57
58	LSW of Gain Coefficient		59
5A	Not Used[1]		5B
5C	Not Used[1]		5D
5E	Not Used[1]		5F
60	Mail Box Ch 00		61
62	Mail Box Ch 01		63
64	Mail Box Ch 02		65
66	Mail Box Ch 03		67
68	Mail Box Ch 04		69
6A	Mail Box Ch 05		6B
6C	Mail Box Ch 06		6D
6E	Mail Box Ch 07		6F
70	Mail Box Ch 08		71
72	Mail Box Ch 09		73
74	Mail Box Ch 10		75
76	Mail Box Ch 11		77
78	Mail Box Ch 12		79
7A	Mail Box Ch 13		7B
7C	Mail Box Ch 14		7D
7E	Mail Box Ch 15		7F
80	Mail Box Ch 16		81
82	Mail Box Ch 17		83
84	Mail Box Ch 18		85
86	Mail Box Ch 19		87
88	Mail Box Ch 20		89
8A	Mail Box Ch 21		8B
8C	Mail Box Ch 22		8D
8E	Mail Box Ch 23		8F
90	Mail Box Ch 24		91
92	Mail Box Ch 25		93
94	Mail Box Ch 26		95
96	Mail Box Ch 27		97
98	Mail Box Ch 28		99
9A	Mail Box Ch 29		9B
9C	Mail Box Ch 30		9D
9E	Mail Box Ch 31		9F
A0 ↓ FE	Not Used[1]		A1 ↓ FF

Notes (Table 3.1):

1. The board will not respond to addresses that are "Not Used".

This memory map reflects byte accesses using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte.

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Card Identification Space - (Read Only, 32 Odd-Byte Addresses)

The AVME9125 contains 32 identification bytes. This information includes the "VMEID" identifier, “ACR” manufacturer's identification code, and board model number. Identification bytes are addressed using only the odd addresses in a 64-byte block. The Identification contents are shown in Table 3.2.

Table 3.2: AVME9125 Identification Bytes

Hex Offset From Base Address (Hex)	ASCII Character Equivalent	D7-D0 Numeric Value (Hex)	Field Description
01	V	56	‘VMEID’
03	M	4D	
05	E	45	
07	I	49	
09	D	44	
0B	A	41	Manufacturers ID ‘ACR’ for Acromag
0D	C	43	
0F	R	52	
11	9	39	Card Model Number
13	1	31	
15	2	32	
17	5	35	
19		20	
1B		20	
1D		20	
1F	1	31	Number of KILOBYTES of address space[1]
21		20	
23 to 3F	Undefined		Reserved

Notes (Table 3.1):

1. The board uses 256 bytes of address space.

Board Status Register - (Read/Write, Base + 40H)

The Board Status Register reflects and controls functions globally on the board.

MSB D15 to D4	D3	D2	D1	LSB D0
Not Used	Soft Reset	Not Used	Global Int. Pending	EXP9125 Present

Where:

Bits 7, 6, 5, 4 — Not used - equal "0" if read

Bit 3 Software Reset (Write) — Writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. The effect of software reset on the various registers is noted in the description of each register. Reset Condition: Set to "0".

Bit 2 — Not used - equal "0" if read

Bit 1 Global Interrupt Pending (GIP) (Read) — This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the board's pending interrupt status, even if the Global Interrupt Enable bit is set to "0". Reset condition: Set to "0".

Bit 0 EXP9125 Board Present Status (Read) — This bit will be "1" when the EXP9125 Expander board is present in a slot adjacent to the AVME9125. A set bit indicates that 32 analog input ports are available. This bit will be "0" when the EXP9125 is not present adjacent to the AVME9125. A zero bit indicates that 16 analog ports are available.

Control Register, (Read/Write) - (Base + 42H)

This read/write register is used to: select the interrupt request level, acquisition input source, scan mode, enable/disable the timer, and select the interrupt mode.

Table 3.3: Control Register

BIT	FUNCTION
0 to 2	These bits control the VMEbus interrupt request level associated with the interrupt requests as illustrated in the following. 000 = No Interrupt Level 001 = Interrupt Level 1 010 = Interrupt Level 2 011 = Interrupt Level 3 100 = Interrupt Level 4 101 = Interrupt Level 5 110 = Interrupt Level 6 111 = Interrupt Level 7
3	Used Internally; Leave Set to ‘0’
5,4	Acquisition Input Source 00 = All Channels Differential Input 01 = 9.79V Calibration Voltage Input 10 = Auto Zero Calibration Voltage Input 11 = Expander Auto Zero Calibration Voltage
7,6	Used Internally; Leave Set to ‘00’
10,9,8	Scan Mode 000 = Disable 001 = Uniform Continuous 010 = Uniform Single 011 = Burst Continuous 100 = Burst Single 101 = Convert on External Trigger Only 110, 111 = Not Used See the Modes of Operation section for a description of each of these scan modes.
11	Timer Enable 0 = Disable 1 = Enable
13,12	Interrupt Control 00, 11 = Disable Interrupts 01 = Enable Interrupt After Convert of Each Channel 10 = Enable Interrupt After Conversion of all selected channels is completed. A group of channels includes all channels from the Start Channel up to and including the End Channel value.
14,15	Not Used[1]

Notes (Table 3.3):

1. All bits labeled “Not Used” will return on a read access the last value written.

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The function of each of the control register bits are described in Table 3.3. The control register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all control register bits to zero.

Analog Input Range and Corresponding Digital Output Code

The ideal input voltage corresponding to the ±10 volt input range is given in Table 3.4. In Table 3.5 the digital output code corresponding to each of the ideal analog input values is given. The hex codes for the converted digital output values are returned in binary two's complement format.

Table 3.4: Supported Full-Scale Ranges and Ideal Analog Input

DESCRIPTION	ANALOG INPUT
Input Range	±10V
LSB (Least Significant Bit) Weight	305μV
+ Full Scale Minus One LSB	9.999695Volts
Midscale	0V
One LSB Below Midscale	-305μV
- Full Scale	-10V

Table 3.5: Digital Output Codes and Input Voltages

DESCRIPTION	DIGITAL OUTPUT Binary 2's Comp (Hex Code)
+ Full Scale - 1 LSB	7FFF
Midscale	0000
1 LSB Below Midscale	FFFF
- Full Scale	8000

Interrupt Vector Register (Read/Write, 45H)

The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the system bus upon an active interrupt acknowledge cycle. Read or writing to this register is possible via 16-bit or 8-bit data transfers. 16-bit data transfers will implement simultaneous access of the Interrupt Vector and Timer Prescaler registers. The register contents are cleared upon reset.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

Interrupts are released on an interrupt acknowledge cycle. Reading of the interrupt vector during an interrupt acknowledge cycle signals the board to remove its interrupt request.

Timer Prescaler Register (Read/Write, 44H)

The Timer Prescaler register can be written with an 8-bit value to control the time interval between conversions.

Timer Prescaler Register							
MSB							LSB
15	14	13	12	11	10	09	08

This 8-bit number divides an 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 5A hex or 90 decimal. A Timer Prescaler value of less then 90 (decimal) will result in an empty Mail Box Register buffer.

Read or writing to this register is possible via 16-bit or 8-bit data transfers. A 16-bit data transfer will implement simultaneous access to the Interrupt Vector and Timer Prescaler registers. The Timer Prescaler register contents are cleared upon reset.

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which follows immediately.

Conversion Timer Register (Read/Write, 46H)

The Conversion Timer Register can be written to control the interval time between conversions. Read or writing this register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Conversion Timer Register															
MSB															LSB
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

This 16-bit number is the second divisor of an 8MHz clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversions is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by an 8MHz clock signal. The output of this clock is input to the second counter, the Conversion Timer, and this output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{8} = \text{T in } \mu \text{ seconds}$$

Where: **T =** time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 90 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval that can be programmed to occur is 11.25μ seconds which can be implemented as (90 * 1) ÷ 8. Any combination of the Timer Prescaler and Conversion Timer are allowed as long as the Timer Prescaler value used is not programmed to a value below 90 decimal.

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Start Channel Value Register (Read/Write, 49H)

The Start Channel Value register can be written with a 5-bit value to select the first channel that is to be converted once conversions have been triggered. All channels including and between the start and end channel values are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The Start Channel Value register can be read or written with 8-bit data transfers. In addition, the Start Channel Value register can be simultaneously accessed with the End Channel Value via a 16-bit data transfer. The unused bits are zero when read. The register contents are cleared upon reset.

Start Channel Value Register							
Unused			Start Channel Value				
07	06	05	04	03	02	01	00

After a data conversion cycle, the internal hardware pointers are reinitialized to the start channel value. Thus, when conversions are started again, the first channel converted is defined by the Start Channel Value register.

End Channel Value Register (Read/Write, 48H)

The End Channel Value register can be written with a 5-bit value to indicate the last channel in a sequence to be converted. When scanning, all channels between and including the start and end channels are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The End Channel Value register can be read or written with 8-bit data transfers. In addition, the End Channel Value register can be simultaneously accessed with the Start Channel Value with a 16-bit data transfer. The unused data bits are zero when read. The register contents are cleared upon reset.

End Channel Value Register							
Unused			End Channel Value				
15	14	13	12	11	10	09	08

New Data Registers (Read Only, 4AH to 4DH)

The New Data registers can be read to determine which channels of the Mail Box buffer contain new converted data. A set bit in the New Data register indicates that the Mail Box buffer, corresponding to the channel of the set bit, contains new converted data. A set New Data register bit is cleared upon a read of its corresponding Mail Box buffer.

The New Data bits are also cleared at the start of all new data acquisition cycles initiated with the Software Start Convert command. This is done to avoid mistaking data from an old scan cycle with that of a new scan cycle.

The New Data registers can be read via 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

New Data Register (Read Only, 4BH)								
Data Bit	07	06	05	04	03	02	01	00
Channel	07	06	05	04	03	02	01	00
New Data Register (Read Only 4AH)								
Data Bit	15	14	13	12	11	10	09	08
Channel	15	14	13	12	11	10	09	08
New Data Register (Read Only 4DH)								
Data Bit	07	06	05	04	03	02	01	00
Channel	23	22	21	20	19	18	17	16
New Data Register (Read Only 4CH)								
Data Bit	15	14	13	12	11	10	09	08
Channel	31	30	29	28	27	26	25	24

Missed Data Registers (Read Only, 4EH to 51H)

The Missed Data registers can be read to determine if a channel's Mail Box buffer has been overwritten with new converted data before the last converted value was read. A set bit in the Missed Data register indicates a converted value corresponding to the channel of the set bit was overwritten before being read. A set Missed Data register bit is cleared upon a read of its corresponding Mail Box buffer.

The Missed Data bits are also cleared at the start of all new data acquisition cycles initiated with the Software Start Convert command. This is done to avoid mistaking missed data from an old scan cycle with that of a new scan cycle.

The Missed Data registers can be read via 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

Missed Data Register (Read Only, 4FH)								
Data Bit	07	06	05	04	03	02	01	00
Channel	07	06	05	04	03	02	01	00
Missed Data Register (Read Only 4E)								
Data Bit	15	14	13	12	11	10	09	08
Channel	15	14	13	12	11	10	09	08
Missed Data Register (Read Only 51H)								
Data Bit	07	06	05	04	03	02	01	00
Channel	23	22	21	20	19	18	17	16
Missed Data Register (Read Only 50H)								
Data Bit	15	14	13	12	11	10	09	08
Channel	31	30	29	28	27	26	25	24

Start Convert Register (Write Only, 52H)

The Start Convert register is a write-only register and is used to trigger conversions by setting data bit-0 of this register to a logic one. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Control, Timer Prescaler, Conversion Timer, Start Channel Value, End Channel Value, and Interrupt Vector.

This register can be written with either a 16-bit or 8-bit data value. Data bit-0 must be a logic one to initiate data conversions.

Start Convert Register	
Not Used	Start Convert
D15 to D01	D00

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At least 5μ seconds of input acquire time should be provided after programming of the Control register and Start Value register before a Software Start Convert command is issued. These configuration registers control the on board multiplexers which select a channel for input to the converter.

Offset Coefficient Register (Read/Write, 54H)

This Offset Coefficient register is read/writeable and is used to store the offset coefficient to 1/4 bit resolution. The least significant 10 bits of the register comprise the offset coefficient stored as a two's complement value. Bits 15 to 10 of the register are not used. The weight corresponding to bits 9 to 0 are shown in the last row of the table below.

Offset Coefficient Register									
7 Bits and a Sign Bit								2 Bits to 1/4 Bit Resolution	
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}
-128	64	32	16	8	4	2	1	1/2	1/4

In an ideal system, the offset coefficient would be exactly 0. The deviation from 0 provides correction for the actual circuit components. The offset coefficient should be determined by taking several readings (e.g. 64) of the auto zero calibration voltage and then averaging the several auto zero values measured to provide the offset coefficient. Several auto zero values averaged together reduce the measurement uncertainty.

Refer to the "Programming Considerations for Acquiring Analog Inputs" section for details on how to acquire auto zero values for determination of the offset coefficient.

An example illustrating how the offset coefficient value is determined for the offset of -9.25 is presented here. Since the offset value desired (-9.25) is negative, the sign bit D9 must be set. If the offset were a positive value then the sign bit D9 would not be set.

We continue by working in order from bit D8 down to bit D0. The current offset (-128) with bit D9 only set is less than -9.25 thus bit D8 must also be set. The offset with bits D9 and D8 set is now -64 (-128+64). A bit can be set if the offset value resulting is less then or equal to the target offset value. Since -64 is < -9.25, we must also set bits D7, and D6. The offset with bits D9, D8, D7, and D6 set correspond to an offset of -16 (-128+64+32+16). We now continue to bit D5 and determine we can not set this bit since this would give and offset of -8 which is greater then -9.5. Bits D4 and D3 must be set to give an offset of -10. Bit D2 can not be set since an offset of -9 would result and -9 is greater then -9.25. Finally bits D1 and D0 are also set. The value written to the offset coefficient must be 3DB hex as seen in the table below.

3		D				B			
1	1	1	1	0	1	1	0	1	1
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-128	64	32	16	8	4	2	1	1/2	1/4

The Offset Coefficient register can be read or written via 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

Gain Coefficient Registers (Read/Write, 56H & 58H)

The Gain Coefficient registers are read/writeable and are used to store the gain coefficient to 1/4 bit resolution. A gain coefficient is a 19-bit value; thus, two 16-bit registers are used to hold a gain coefficient. The least significant 16 bits are stored in one register while the most significant 3 bits are stored in the other.

Registers at addresses 56H and 58H are used to hold the most significant and least significant parts of the gain coefficient corresponding to channels 0 to 31.

The least significant 16 bits and most significant 3 bits of the gain coefficient are shown in the following table. The weight corresponding to each bit is also given in the table. Refer to the "Programming Considerations for Acquiring Analog Inputs" section for details on how to determine the gain coefficient.

The Gain Coefficient value is determined by working in order from bit D2 of the most significant gain register down to bit D0 of the least significant gain register. A bit can be set if the gain value resulting is less then or equal to the target gain value.

Most Significant Gain Coefficient Register							
Data Bits 15 to 8 of Most Significant Word							
Not Used							
Data Bits 7 to 0 of Most Significant Word							
D07	D06	D05	D04	D03	D02	D01	D00
Not Used					2^0	2^{-1}	2^{-2}

Least Significant Gain Coefficient Register							
Data bits 15 to 8 of Least Significant Word							
D15	D14	D13	D12	D11	D10	D09	D08
2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}
Data bits 7 to 0 of Least Significant Word							
D07	D06	D05	D04	D03	D02	D01	D00
2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

In an ideal system, the gain coefficient would be exactly 1. The deviation from 1 provides correction for the actual circuit components. A gain coefficient of 1 is obtained by writing a value of 4 hex to the Most Significant Gain Coefficient register and a value of 0 to the Least Significant Gain Coefficient register.

The Gain Coefficient register can be read or written via 16-bit or 8-bit data transfers. Upon reset the register contents will be set to a gain coefficient of 0 which will result in a digital values of zero in the mailbox registers.

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Mail Box Buffer (Read Only, 60H - 9EH)

The Mail Box Buffer is read-only, and contains 16-bit digitized input channel values. The Mail Box Buffer has 32 storage locations-one for each of the 32 channels supported. See Table 3.1 which gives the Mail Box Buffer address locations corresponding to each of the 32 channels.

The New Data register can be read to determine which Mail Box Buffers contain updated digitized data. A set bit in the New Data register indicates an updated digitized data value resides in its corresponding Mail Box Buffer. In addition, the Missed Data register can be read to determine if a Mail Box Buffer has been overwritten with a new digitized value before the previous one had been read. A set bit in the Missed Data register indicates that a digitized data value has been overwritten.

A read access to the Mail Box Buffer could take up to an extra 625n seconds if a read is issued while a hardware write to the same Mail Box is currently underway. Holding off the data read of the Mail Box prevents contention which could result in the writing of erroneous data to the Mail Box.

MODES OF OPERATION

The AVME9125 provides four different modes of analog input acquisition to give the user maximum flexibility for each application. These modes of operation include: uniform continuous, uniform single, burst continuous, and burst single. In all modes a single channel or a sequence of channels may be converted. The following sections describe the features of each and how to best use them.

Uniform Continuous-Mode

In uniform continuous mode of operation, conversions are performed continuously (in sequential order) for all channels between and including the Start and End Channel Values. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit.

Stopping the execution of uniform continuous conversions is possible by writing 000 to the Scan Mode bits (8-10) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register address location.

Interrupts can be enabled to activate after conversion of each channel or the group of channels defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 10.5μ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 10.5μ seconds after the interval time of the last selected channel has expired.

If interrupts are selected to go active after conversion of each channel be sure to program a large enough interval between conversions to allow adequate time for execution of an interrupt service routine. It may also be necessary to allow time for your computer to perform other housekeeping operations between servicing interrupts.

Uniform Single-Mode

In uniform single mode of operation, conversions are performed once (in sequential order) for all channels between and including the Start and End Channel Values. After the channels defined by the End Channel Value are converted conversions are halted.

The interval between conversions of each channel is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 10.5μ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 10.5μ seconds after the interval time of the last selected channel has expired.

Burst Continuous-Mode

In burst continuous mode of operation, conversions are continuously performed in sequential order from the channel defined by the Start Channel Value to the channel defined by the End Channel Value. Within a group of channels, the interval between conversions is fixed at ≅ 15μ seconds. However, the interval after conversion of a group of channels can be controlled by the interval timer (Timer Prescaler and Conversion Timer).

Burst modes can be used to provide pseudo-simultaneous sampling for many low to medium speed applications requiring simultaneous channel acquisition. The 15μ seconds between conversion can essentially be considered simultaneous sampling for low to medium frequency applications.

After software selection of the burst continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit.

Stopping the execution of burst continuous conversions is accomplished by writing 000 to the Scan Mode bits (8-10) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register address location.

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Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued every 15μ seconds. If interrupt upon completion of a group of channels is selected, an interrupt will be issued ≅ 25.5μ seconds after conversion of the last channel in the group has started.

At this time 15μ seconds between interrupts is not sufficient time to perform back to back interrupt acknowledge cycles on the VME and PC platforms. Thus, interrupting after each channel is converted cannot be recommended.

Burst Single-Mode

In burst single mode of operation conversions are performed once for all channels (in sequential order) starting with Start Channel and ending with the End Channel. The interval between conversions of each channel is fixed at ≅ 15μ seconds. The interval timer has no functionality in this mode of operation.

After software selection of the burst single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued every 15μ seconds (not recommended). If interrupt upon completion of a group of channels is selected, an interrupt will be issued 25.5μ seconds after conversion of the last channel has started.

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The AVME9125 board register architecture makes the configuration fast and easy. The only set of configuration hardware jumpers is for the base address of the board in the VMEbus short I/O space. Once the board is mapped to the desired base address, communication with the board registers is straightforward.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided to improve the accuracy over the uncalibrated state. The use of calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

The AVME9125 provides DSP (Digital Signal Processing) logic for real-time calibration of digitized values. The on-board hardware implements the required multiplication to adjust the gain and also the summation to correct the offset. The gain and offset coefficients required to implement this calibration must be determined by software and stored in AVME9125 register before conversion are triggered to obtain calibrated digital values (refer to the memory map for these register locations). The reset condition of the offset and gain coefficients are zero which will result in digital values of zero in the mailbox registers.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Instrumentation Amplifier and the Analog to Digital Converter (ADC). The instrumentation amplifier and ADC have significant offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated Performance

Very accurate gain and offset coefficients for the AVME9125 can be calculated by using the calibration voltages present on the board. The voltage reference and the analog ground (auto zero signal) are used to determine two points of a straight line which defines the analog input characteristic. The calibration reference voltage is precisely adjusted at the factory to provide optimum performance, as detailed in chapter 6.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages.

$$\text{CorrectedCount} = \left[\text{CountActual} - \text{OffsetCoef}\right] * \left[\text{GainCoef}\right] \quad (1)$$

$$\text{CorrectedCount} = \left[\text{CountActual} - \text{Count}_{0V}\right] * \left[\frac{32{,}080}{\text{Count}_{9.79V} - \text{Count}_{0V}}\right] \quad (2)$$

By comparison of equations (1) and (2) it can be seen that the offset coefficient = Count_{0V} and the gain coefficient is the term given in equation (3):

$$\text{GainCoef} = \left[\frac{32{,}080}{\text{Count}_{9.79V} - \text{Count}_{0V}}\right] \quad (3)$$

Where:

$\text{Count}_{9.79V}$	=	Actual ADC Data Read With 9.790039V Calibration Voltage Applied
Count_{0V}	=	Actual ADC Data Read With Auto Zero Calibration Voltage Applied
CountActual	=	Actual Uncorrected ADC Data For Input Being Measured

The calibration gain and offset coefficients should not be determined immediately after startup but after the module has reached a stable temperature and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 64) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

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Calibration Programming Example 1

Assume that channels 0 to 3 are connected differentially, and corrected input channel data is desired. The calibration parameters ($Count_{9.79V}$ and $Count_{0V}$) remain to be determined before the gain and offset coefficients can be calculated.

Determination of the $Count_{0V}$ Value

1. Execute Write of 0420H to Control Register at Base Address + 42H.
   - A. Select No Interrupt Level
   - B. Auto Zero Calibration Voltage
   - C. Burst Single Scan Mode
   - D. Timer Disabled
   - E. Interrupts Disabled
2. Execute Write of 1F00H to End/Start Channel Value Register at Base Address + 48H. This will permit 32 conversions of the Auto Zero value to be stored in the 32 Mail Box Buffers.
3. Execute Write 0001H to the Start Convert Bit at Base Address + 52H. This starts the burst single mode of conversions. Thirty two conversions of the Auto Zero are implemented and stored in the 32 Mail Box Buffers.
4. Execute Read of the 32 Mail Box Buffers at Base Address + 60H to 9EH.
5. Take the average of the 32 ADC values and save this number as $Count_{0V}$.
6. **Determination of the $Count_{9.79V}$ Value**
7. Execute Write of 0410H to Control Register at Base Address + 42H.
   - A. Select No Interrupt Level
   - B. Select 9.79V Calibration Voltage
   - C. Burst Single Scan Mode
   - D. Timer Disabled
   - E. Interrupts Disabled
8. Writing the Start Channel Value, End Channel Value, and the Gain Selects is not necessary if they have not been changed from that programmed in steps above.
9. Execute Write 0001H to the Start Convert Bit at Base Address + 48H. This starts the burst single mode of conversions. Thirty two conversions of the 9.79 volt calibration voltage are implemented and stored in the 32 Mail Box Buffers.
10. Execute Read of the 32 Mail Box Buffers at Base Address + 60H to 9EH.
11. Take the average of the 32 ADC values and save this number as $Count_{9.79V}$.
12. **Calculate Gain and Offset Coefficients and Write to Corresponding Registers**
13. Since all parameters are known, the gain and offset coefficients can be determined.
    - A. The offset coefficient is the average of the 32 $Count_{0V}$ values measured. An example, illustrating how the offset coefficient value is determined, is given in the Offset Coefficient Register section.
    - B. The gain coefficient can be calculated using the averaged $Count_{9.79V}$ and $Count_{0V}$ values as shown in equation 3. The procedure for determining the coefficient, down to 1/4 bit resolution, is given in the Gain Coefficient Register section.
14. Execute Write of the least significant word of the Gain Coefficient to board register at Base Address + 58H.
15. Execute Write of the most significant word of the Gain Coefficient to board register at Base Address + 56H.
16. Execute Write of the Offset Coefficient to board register at Base Address + 54H.
17. **Measure Channels 0 to 3**
18. Execute Write of 0400H to Control Register at Base Address + 42H.
    - A. Select No Interrupt Level
    - B. Burst Single Scan Mode
    - C. Timer Disabled
    - D. Interrupts Disabled
19. Execute Write of 0300H to End/Start Channel Value Register at Base Address + 48H. This will permit conversions of channels 0 to 3.
20. Execute Write 0001H to the Start Convert Bit at Base Address + 52H. This starts the burst single mode of conversions. Conversions of channels 0 to 3 are implemented and corresponding results are stored in the first four Mail Box Buffer locations at Base Address + 60H to 66H.
21. Execute Read of the 4 Mail Box Buffers at Base Address + 60H to 66H. The data represents the desired, corrected value.
22. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

GENERATING INTERRUPTS

The AVME9125 board initiates interrupts and uses the Interrupt Level data of the Control register to map the request to the desired VMEbus interrupt level. The board then waits for an interrupt acknowledge from the VMEbus host after asserting the appropriate VMEbus interrupt request.

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When the board recognizes an interrupt acknowledge cycle on the VMEbus, it checks for a match of the interrupt request. If an interrupt is not pending or the interrupt level does not match, it will pass the acknowledgment signal along, without consuming it. If there is a match, the board will initiate an acknowledgment cycle and supply the interrupt vector during the cycle.

Interrupt Configuration Example

1. Write interrupt vector to board address 45H.
2. Write to the Interrupt Level in the control register to program the desired interrupt level per bits 2,1,0. Also enable the interrupt type in control register bits 12 and 13.

Sequence of Events For an Interrupt

1. The AVME9125 asserts an interrupt request by asserting IRQx* as programmed in the interrupt level bits of the control register.
2. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
3. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9125, the board will check if the level requested matches that specified by the host. If so, the board will put the interrupt vector on the data bus (D00-D07 if an D08 (O) interrupter or D00-D15 if a D16 interrupter), and asserts DTACK* to the system master.
4. The host uses the vector as a pointer to an interrupt handler to execute and begins its execution.
5. Example of Generic Interrupt Handler Actions:
   A. Take any specific action required to remove the interrupt request at its source.
6. If the interrupt stimulus has been removed and no other interrupts are pending, the interrupt cycle is completed (i.e. the board negates its interrupt request).
   A. If another interrupt is pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the AVME9125 board. Refer to the Block Diagram shown in the Drawing 4501-678 as you review this material.

AVME9125 BOARD OVERVIEW

The AVME9125 board is a VMEbus slave board providing up to 32 differential analog to digital input channels with expander board EXP9125. The board's VMEbus interface allows an intelligent single board computer (VMEbus Master) to monitor 32 analog channels.

VMEbus Interface

The board's VMEbus interface is used to program and monitor and board's registers for configuration and control of the board's documented modes of operation (see section 3).

The VMEbus interface is implemented in the logic of a Field Programmable Gate-Array (FPGA). The FPGA implements VMEbus specification revision C.1 as an interrupting slave including the following data transfers types.

- A16, D16/D08(O) Short I/O Access

The board's VMEbus data transfer rates are typically:

- 800ns for accesses to the AVME9125 board registers.

The board's FPGA monitors the base address jumper setting which is jumperable on 256 byte boundaries in the VMEbus Short I/O (A16) Address Space. When the selected base address matches the (A16) address provided by the VMEbus master, the FPGA controls and implements the required bus transfer allowing communication with the AVME9125 board's registers.

Board Registers and Control Logic

All logic to control data acquisition is imbedded in two board FPGAs. One FPGA is dedicated to the VMEbus interface while the other FPGA handles control of data acquisition. The data acquisition control logic performs the following:

- Controls the channel multiplexers based upon start and end channel values.
- Controls data conversion at the A/D Converter based on one of four different scan modes of operation.
- Controls data transfer from the A/D Converter to the FPGA's 16-bit serial shift register.
- Controls and updates the Mail Box buffer, New Data register, and Missed Data register.
- Stops data acquisition for Single Cycle Scan modes.
- Controls the interval between data conversions.
- Issues interrupt requests to the system master.

INTERNAL CHANNEL POINTERS

Internal counters in the FPGA are used as pointers to: control the multiplexers for selection of the current channel's analog signal and control update of the Mail Box RAM buffer. The start channel register controls the value at which these counters start and the end value register controls the maximum channel number which is reached.

In the continuous modes of operation these counters continuously cycle, in sequential order, from the defined start value to the defined end value. When the continuous mode of operation is halted by disabling the scan mode via the control register, the internal hardware counter remains at the count value reached when halted. Upon start of a new scan mode, via the software start convert bit, the internal pointers are reinitialized. Thus, the first channel converted, upon restart of data conversions, will correspond to that set in the start value register.

A 16-bit serial shift register is implemented in the board's FPGA. This serial shift register interfaces to the A/D Converter. A clock signal provided by the converter is used to serially shift the new data from the converter to the FPGA's 16-bit serial shift register. Use of the converter's clock signal (instead of an external clock) minimizes the danger of digital noise feeding through and corrupting the results of a conversion in process.

The converted data serially shifted, from the A/D Converter to the FPGA, represents the analog signal digitized in the previous convert cycle. That is, the A/D Converter transfers digitized analog input data to the FPGA one convert cycle after it has been digitized. Serially shifting of the 16-bits of digitized data to the FPGA and then writing to the Mail Box buffer is completed 10.5μ seconds after start of the convert cycle.

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Upon initiation of an A/D convert cycle, the analog input data is digitized and stored into an internal A/D Converter buffer. Also during this cycle, the last converted data value is moved from the A/D Converter buffer to the FPGA for correction and then storage into the Mail Box Buffer. At this time, the New Data Available bit corresponding the previous converted channel is set in the FPGA register.

For all other scan modes the FPGA control logic will automatically discard the first digitized data value received from the A/D Converter. It is not written to the Mail Box buffer. In addition, the FPGA logic also automatically generates the required "flush" convert signals to obtain the last converted data value from the A/D Converter.

TIMED PERIODIC TRIGGER CIRCUIT

Timed Periodic Triggering is provided by two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by an 8MHz clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 11.25μ seconds to 2.0889 seconds. The output of the second counter is used to trigger the start of new A/D conversions for the Uniform Scan modes of operation. For the Burst Continuous mode, the interval between conversions of each channel is fixed at ≅ 15μ seconds. However, the interval between the group (burst) of channels can be controlled by the Interval Timer.

VME INTERRUPT CONTROL LOGIC

The AVME9125 can be configured to generate an interrupt after completion of conversion of a single channel or after conversion of a group of channels is completed. Interrupts are enabled on the board via the Control Register (see section 3 for programming details).

A board interrupt will cause the board to release the interrupt to the VMEbus. The board releases the interrupt to the VMEbus by asserting the interrupt request level as pre-programmed in the Interrupt Level bits of the Control register. The board's interrupt logic then monitors the VMEbus Interrupt Acknowledge Input (IACKIN*) signal.

An active IACKIN* signal, detected by the board, is either passed to Interrupt Acknowledge Output (IACKOUT*) or consumed by the board. IACKIN* is passed to IACKOUT* if the VMEbus interrupt level does not match that programmed into the Interrupt Level bits. If a match is detected, the board responds to the interrupt by consuming IACKIN*.

The board also responds to an interrupt by placing the interrupt vector on the data bus and asserts DTACK* active, and the VMEbus master responds by executing the code at the address of the interrupt vector.

The interrupt release mechanism is Release On Acknowledge (ROAK) type. That is, the board will release the request signal during an interrupt acknowledge cycle.

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The field I/O interface to the board is provided through connector P2 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

Analog inputs and calibration voltages are selected via analog multiplexers. The AVME9125 control logic automatically programs the multiplexers for selection of the required analog input channel. The multiplexer control is based upon selection of differential analog input and the Start and End channel register values.

Up to 32 differential inputs can be monitored. Channel's 0 to 15 + and - inputs are individually selected. Channels 16 to 31 are multiplexed on the companion Expander board (EXP9125) and a single + and - input pair is connected to the AVME9125 via the P2 connector.

The output of a Instrumentation Amplifier feeds the A/D (Analog to Digital) Converter. The A/D Converter is a state of the art, 16-bit, successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the A/D has accurately digitized the input. Then it returns to sample mode to acquire the next channel. Once a conversion has been started, control logic on the AVME9125 automatically updates the multiplexers for the next channel to be converted as required. This allows the input to settle for the next channel while the previous channel is converting. This pipelined mode of operation facilitates a maximum system throughput.

The board contains a precision voltage reference and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for the desired A/D Converter range when compared to fixed hardware potentiometers for offset and gain calibration of the A/D Converter.

The FPGA will automatically correct the converted data by using software calculated offset and gain coefficients. The software calculated coefficients should be updated whenever the operating temperature environment of the board changes. The software calculated calibration coefficients are calculated using the precision voltage reference and auto zero (refer to the calibration section).

Power Supply Filters

Power line filters are dedicated to each supply line for filtering of the +5, +15, and -15 volt supplies. The filters provide improved noise performance as is required on precision analog boards.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

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Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration.....AVME9125 (6U)
Length.....9.187 inches (233.3 mm)
Width.....6.299 inches (160.0 mm)
Board Thickness.....0.062 inches (1.59 mm)
Max Component Height.....0.550 inches (13.97 mm)
Recommended Card Spacing..0.800 inches, (20.32mm)

Connectors:
P1 (VMEbus).....DIN 41612 96-pin Type C, Level II.
P2 (VMEbus).....DIN 41612 96-pin Type C, Level II.

Power:
The AVME9125 board individually filters +5V from the VMEbus. On-board +15V and -15V supplies are also individually filtered.

The power supply filters are typically capable of attenuating undesirable noise and oscillations in the high frequency range.

Current:
+5 Volts (±5%).....AVME9125 450mA, Typical 600mA, Maximum.

VMEbus COMPLIANCE

Specification.....This device meets or exceeds all written VME specifications per revision C.1 dated October 1985, IEC 821-1987 and IEEE 1014-1987.
Data Transfer Bus.....A16:D16/D08 (EO) DTB slave; supports Read-Modify-Write cycles.
VMEbus Access Time.....800nS Typical (all board registers); measured from the falling edge of DSx* to the falling edge of DTACK*.

VMEbus Address Modifier Codes:
Short I/O Space.....Base address is hardware jumper selected. Occupies 256 bytes. Responds to both address modifiers 29H & 2DH in the VMEbus short I/O space for board registers

Interrupts.....Creates I(1-7) programmable request levels
D16/D08(O) interrupter.
Board control & status register interrupt monitoring. Interrupt release mechanism is Release On Acknowledge (ROAK) type.
Interrupt Events.....Vectored Interrupt on end of channel conversion or end of group of channel conversions

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Input Channels (P2 Access).....32 Differential Channels
Input Signal Type.....Voltage (Non-isolated).
Input Range Bipolar.....-10 to +10 Volts
Input Overvoltage Protection.....VSS - 20 V to VDD + 40 V with Power ON.
-35 V to +55 Volts Power OFF
Input Resistance.....100 MΩ, Typical.
Input Bias Current.....1nA., Typical.
Common Mode
Rejection Ratio (60Hz).....90 dB., Typical.
Channel to Channel
Rejection Ratio (60Hz).....90 dB., Typical.

(ADC) ADS7809UB @25°C:

ADC.....Burr-Brown ADS7809UB
A/D Resolution.....16-bits.
No Missing Codes.....No Missing Codes 15bits ADC
A/D Integral Linearity Error.....±1 LSB Typical, ±2 LSB Maximum ADC
Bipolar Offset Error[1].....±10mV Max, for ±10V Range
Full Scale Error[1].....±0.5% Maximum.

Note 1. Software calibration eliminates these error components.

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Programmable Calibration Voltages

Calibration Signal	Ideal Value (Volts)	Maximum Temperature Drift[2] (ppm/^{O}C)
Auto Zero	0.0000	N/A
CAL	9.790039	±6

Note 2. Worst case temperature drift of the calibration voltage reference.

Maximum Overall Calibrated Error @ 25°C

The maximum corrected (i.e. calibrated) error is the worst case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, Instrumentation Amp and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25^{O}C.

Input Range (Volts)	Max. Err ±LSB (% Span)	Typ. Er[3] ±LSB (% Span)
-10 to +10	±8.8 LSB (±0.0113%)	±3 LSB (±.0.0045%)

Note 3. A total of 256 input samples, were averaged with the throughput Rate of 31KHz conversions/second. A 3 foot shielded analog input ribbon was used.

Settling Time (20V step).....3.5uS to 0.01%, Typical
A/D Conversion Time.....11.25uS Maximum
Conversion Rate.....88.8KHz Maximum
A/D Triggers.....Software and External
Input Noise.....1.4 LSB rms, Typical[4].
Temperature Coefficient.....See spec of calibration voltages.

Note 4. A total of 2048 input samples were averaged with the throughput Rate of 31KHz conversions/second, using the uniform single sample mode. A 3 foot shielded analog input ribbon was used.

ENVIRONMENTAL

Operating Temperature.....0 to +70°C
Relative Humidity.....5-95% non-condensing. The printed circuit board is coated with a fungus resistant acrylic conformal coating in the area in the area of the sensitive analog circuitry.

Storage Temperature.....-25 to +85°C

Non-Isolated.....VMEbus and AVME9125 commons have a direct electrical connection. As such, the field I/O connections of the P2 are not isolated from the VMEbus.

Radiated Field Immunity (RFI).....Designed to comply with IEC1000-4-3 Level 3 (10V/m at frequencies 27MHz to 500MHz) and European Norm EN50082-1.

Electromagnetic Interference Immunity (EMI).....Error less than ±0.25% of FSR (RMS) under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge Immunity (ESD).....Complies with IEC1000-4-2 Level 1 (2KV direct contact discharge) at input/output terminals and European Norm EN50082-1.

Surge Immunity.....Not required per European Norm EN50082-1.

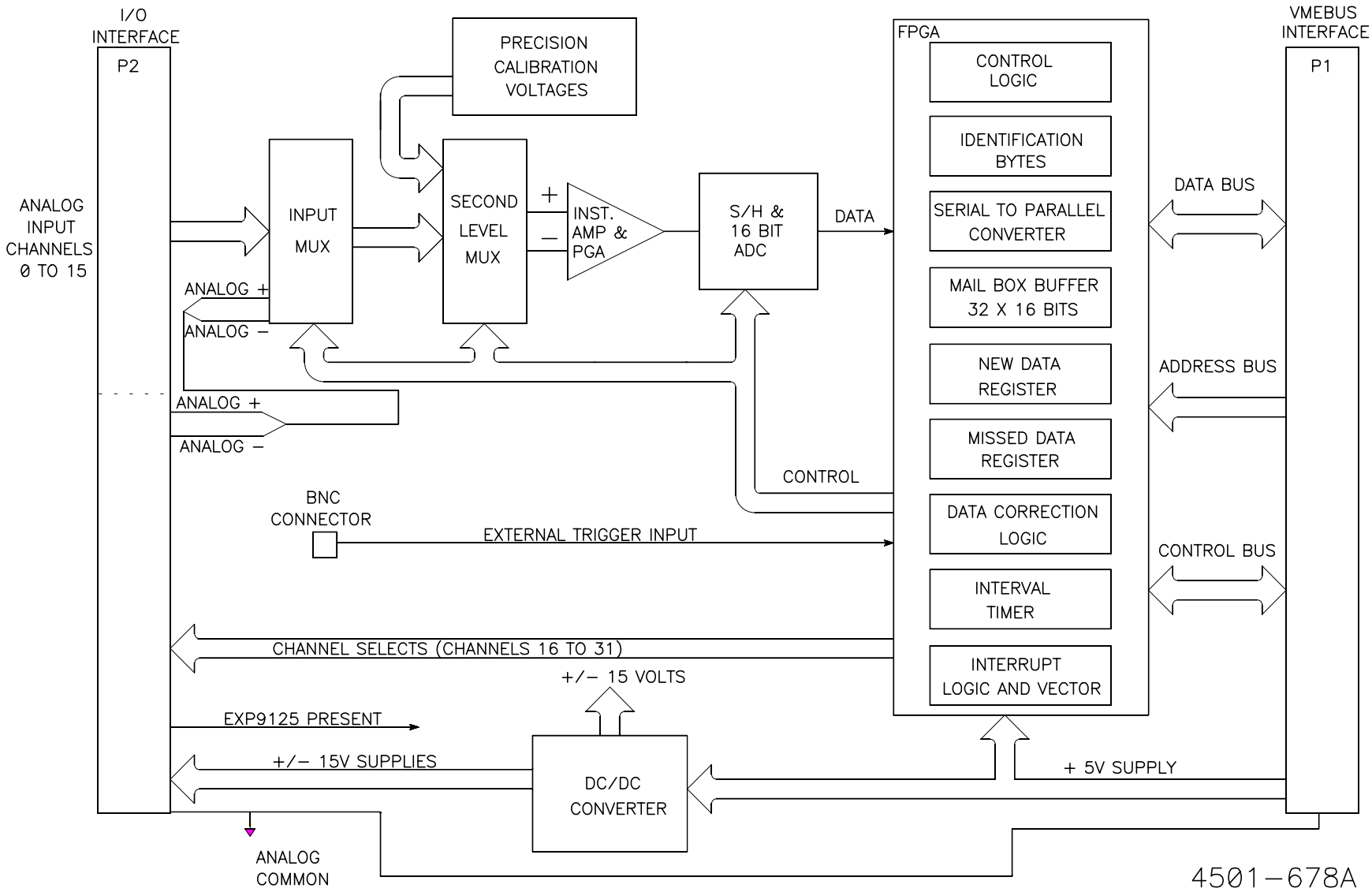
Electric Fast Transient Immunity (EFT).....Complies with IEC1000-4-4, Level 2 (0.5KV at input and output terminals) and European Norm EN50082-1

Radiated Emissions.....Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

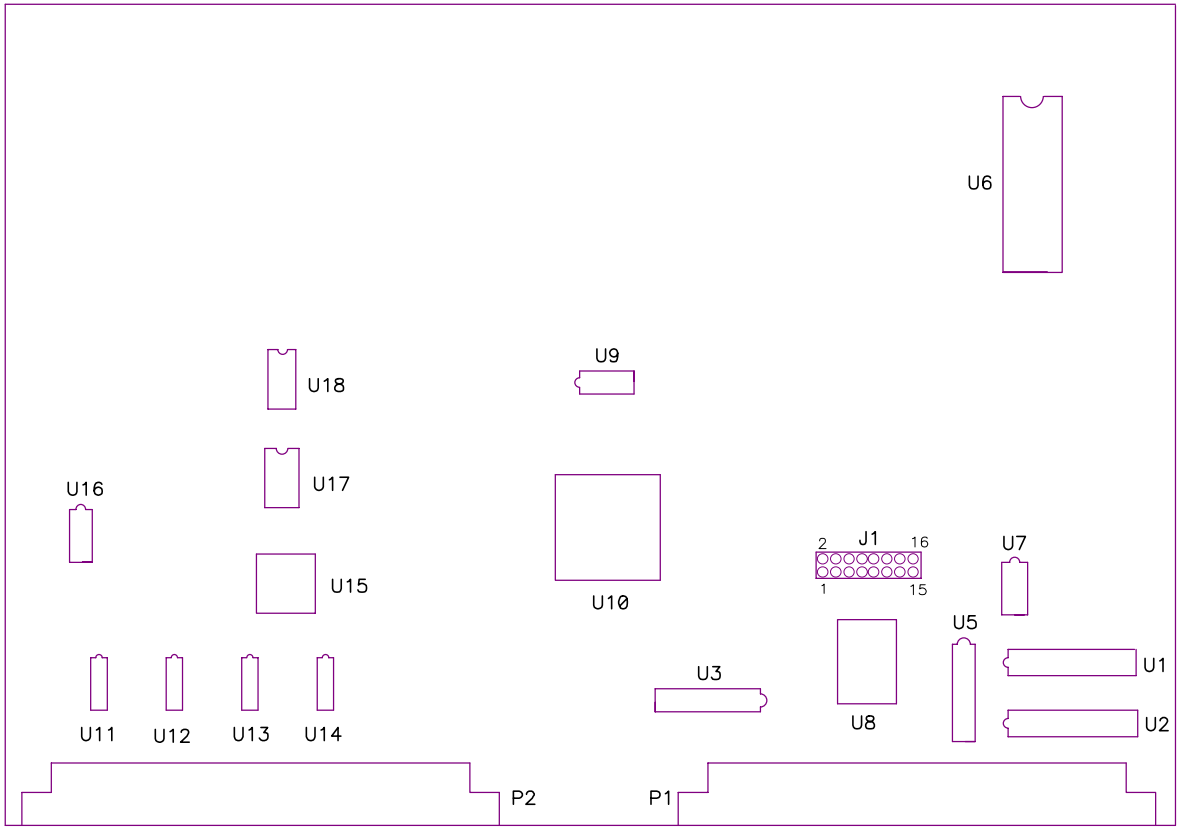
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AVME9125 BLOCK DIAGRAM



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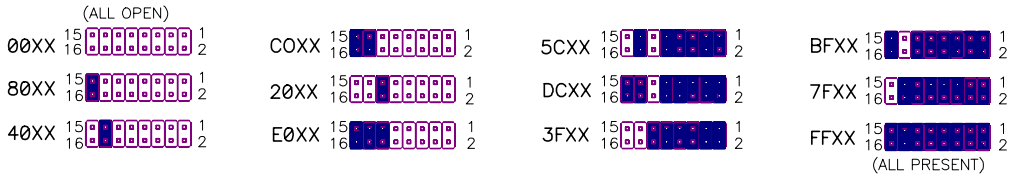
AVME9125 JUMPER LOCATION DRAWING



4501-679A

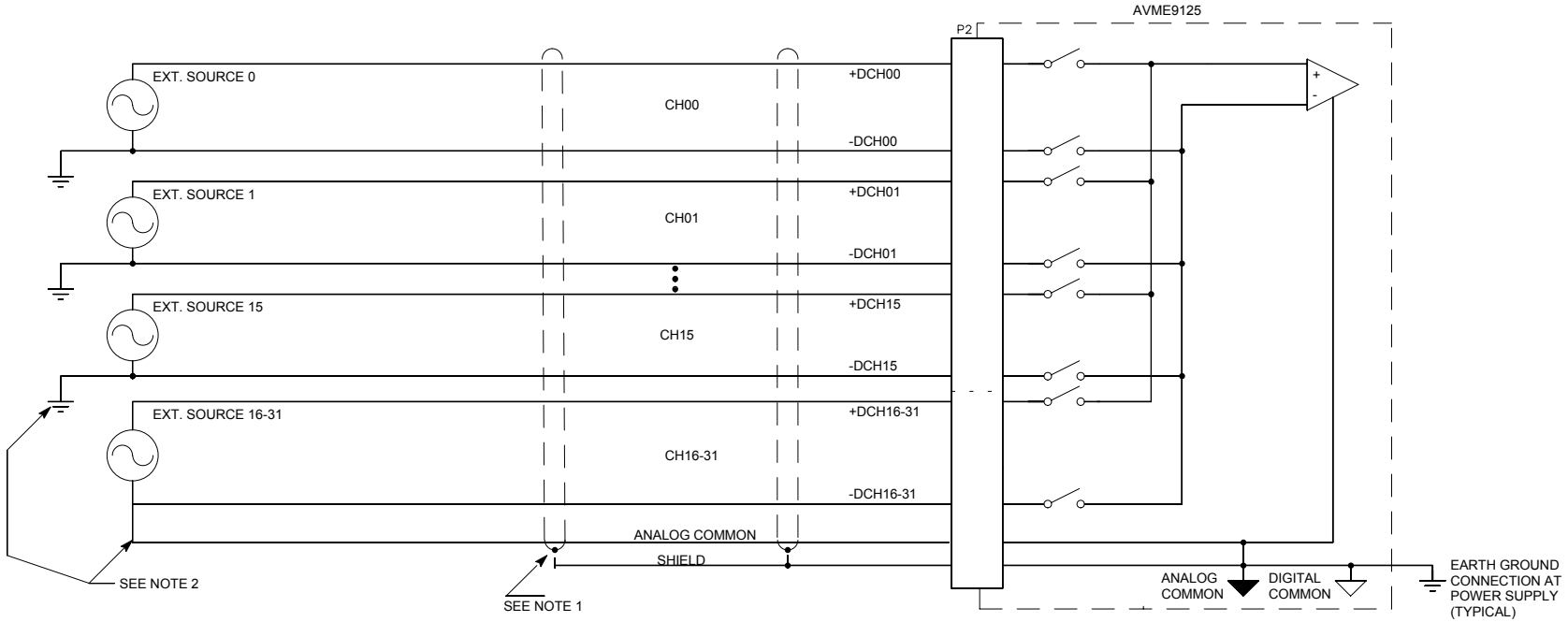
BASE ADDRESS PROGRAMMING:

ADJACENT PINS OF JUMPER JI REPRESENT THE UPPER 8 BITS OF THE BASE ADDRESS (A15 TO A8).
A JUMPER PRESENT REPRESENTS A BIT VALUE OF 1.
A JUMPER REMOVED REPRESENTS A BIT VALUE OF 0.



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ANALOG INPUT CONNECTION DIAGRAM



NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.

4501-688A

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