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Series 947x
Industrial Digital I/O Board

USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 INTRODUCTION

The AVME 947X Industrial Digital I/O Board provides a means for interfacing various discrete devices to a VME based computer system. The board is divided into independent I/O sections. The heart of each section is the Z8036 Counter I/O chip (CIO). This chip provides the section with 20 individually programmable I/O points and a flexible array of software controllable features such as three counter/timers, comprehensive interrupt capabilities, and handshaking support.

A Logic Cell Array (LCA) controls the input & output circuitry between the Z8036 and your application. Each section's LCA is configured with a jumper selectable program. These LCA programs are optimized to take advantage of specific features of the CIO and can also provide enhancements such as input debouncing.

Table 1.1

MODEL	POINTS	FRONT ACCESS	REAR ACCESS	P2 SAFE	SECTIONS AVAILABLE
AVME 9470	80 I/O	P3 - P6			0, 1, 2, 3
AVME 9471	80 I/O		P2 (A,B,C)	NO	0, 1, 2, 3
AVME 9472	40 I/O	P3 & P4			0, 1
AVME 9473	40 I/O		P2 (A & B)	NO	0, 1
AVME 9475	40 I/O		P2 (A & C)	YES	2, 3

1.2 FEATURES OF THE AVME 947X

The VME Digital I/O Board features:

- Pass/Fail Status indicators on the front panel.
- TTL and CMOS compatible.
- Compatible with industry standard solid state relays, PB16 and PB24 termination panels.
- Optional universal termination panel available for use with contact closures, relays, incandescent lamps.
- I/O accessible through the front panel or out the rear of the card cage.
- Can read state of points configured as outputs.

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- 64 programmable general purpose I/O points, which can sink up to 100 mA from an external 5V source. (Ports A and B of each Section).

- 16 programmable special purpose I/O points which can sink up to 60 mA from an external source. (Port C of each Section).

- Four interrupt modes available:

  Change of state (COS).
  Eight bit pattern match.
  Edge sensitive - positive or negative.
  Level sensitive - positive or negative.

- Up to twelve 16 bit counter/timers.

- Four handshaking modes available, with interrupts on single or double byte data transfers:

  Interlocked.
  Strobed.
  3-wire.
  Pulsed.

Some features of the AVME 947X are mutually exclusive. In other words, the use of one feature may preclude the use of another. Precise information on this relationship can be found in Chapter 2 "Preparation For Use." Table 1.2 shows some typical combinations.

Table 1.2

TYPICAL COMBINATIONS PER SECTION (9470/71 HAVE 4 SECTIONS, 9472/73/75 HAVE 2 SECTIONS)								
INDEPENDENT I/O POINTS	20	16	12	8	8	4	0	0
8-BIT HANDSHAKE PORTS	0	0	0	1	0	1	2	1
COUNTER/TIMERS	0	1	2	0	3	1	0	2

1.3 VMEbus INTERFACE

- Slave Module A24/A16, D16/D08 (EO)

- D08(O) ROAK Interrupter

- Single or Multiple Interrupt Vectors

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- Responds to standard address modifier codes 39H, 3DH and to short address modifier codes 29H, 2DH (a capital H suffix indicates a hexadecimal number).

- Board occupies 1K bytes of memory space (jumper selectable).

- Board Identification PROM.

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2.0 PREPARATION FOR USE

This chapter provides information about preparing the Industrial Digital I/O Board for system operation.

2.1 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.



The board is physically protected with foam and electrically protected with an antistatic bag during shipment. It is advisable to visually inspect the board for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static safe work station.

2.2 CARD CAGE CONSIDERATIONS

Refer to the specifications for bus loading and power requirements. Be sure that the system power supplies are able to accommodate the additional requirements within the voltage tolerances specified.

IMPORTANT

The VMEbus cage should be powered up before the field I/O signals. Otherwise, the AVME947x board may not power up correctly.

Adequate circulation of air must be provided to prevent a temperature rise above the maximum operating temperature. Large and continuing fluctuations in ambient air temperature should be avoided. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air filtering.

2.3 INDUSTRIAL DIGITAL I/O BOARD CONFIGURATION

The Digital I/O Board may be configured in a variety of ways for many different applications. Each possible jumper setting will be discussed in the following sections. The jumper locations are shown in Figure 2.1.

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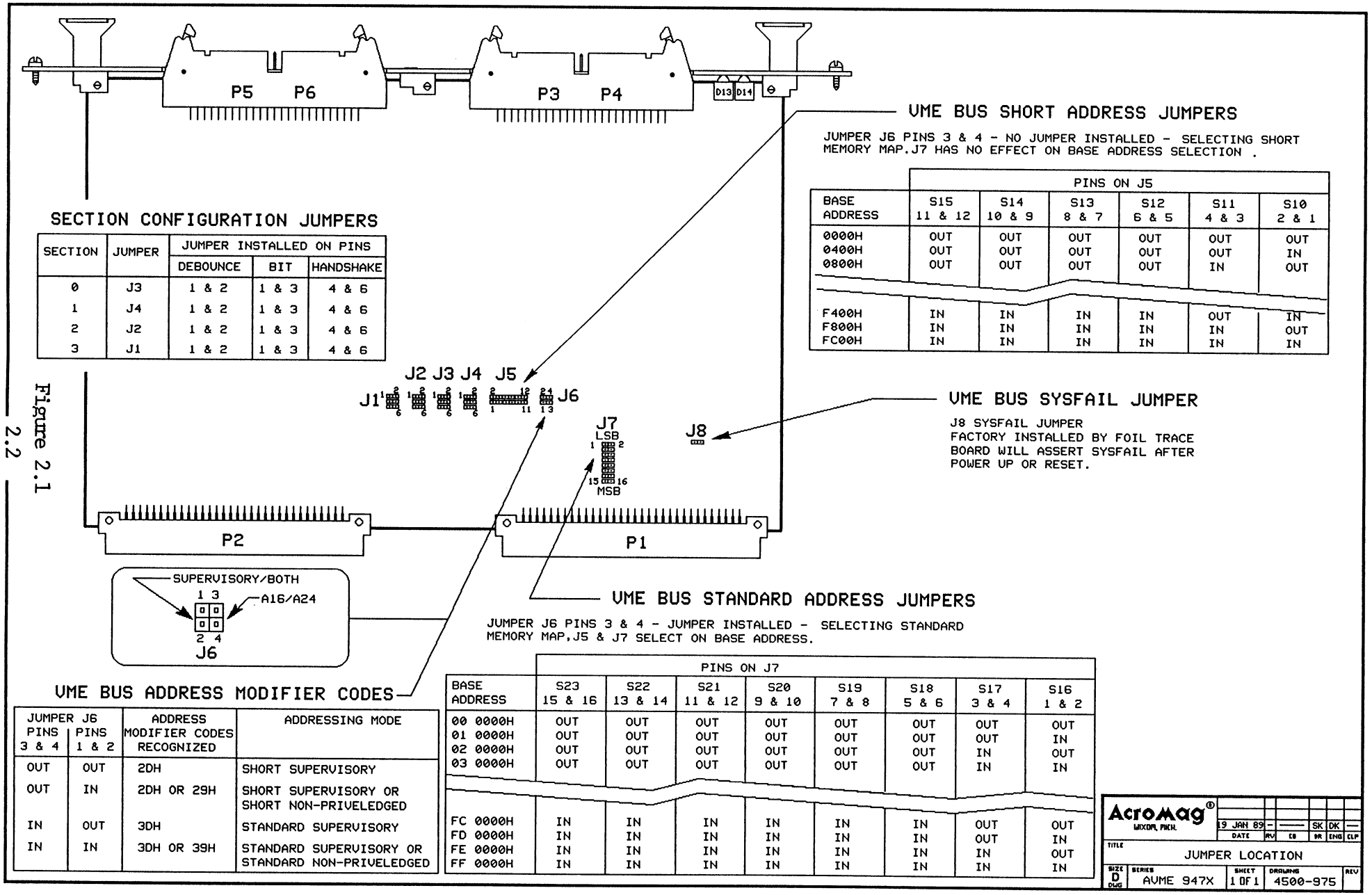


Figure 2.1

2.2

SECTION CONFIGURATION JUMPERS

SECTION	JUMPER	JUMPER INSTALLED ON PINS		
		DEBOUNCE	BIT	HANDSHAKE
0	J3	1 & 2	1 & 3	4 & 6
1	J4	1 & 2	1 & 3	4 & 6
2	J2	1 & 2	1 & 3	4 & 6
3	J1	1 & 2	1 & 3	4 & 6

VME BUS SHORT ADDRESS JUMPERS

JUMPER J6 PINS 3 & 4 - NO JUMPER INSTALLED - SELECTING SHORT MEMORY MAP.J7 HAS NO EFFECT ON BASE ADDRESS SELECTION .

BASE ADDRESS	PINS ON J5					
	S15 11 & 12	S14 10 & 9	S13 8 & 7	S12 6 & 5	S11 4 & 3	S10 2 & 1
0000H	OUT	OUT	OUT	OUT	OUT	OUT
0400H	OUT	OUT	OUT	OUT	OUT	IN
0800H	OUT	OUT	OUT	OUT	IN	OUT
F400H	IN	IN	IN	IN	OUT	IN
F800H	IN	IN	IN	IN	IN	OUT
FC00H	IN	IN	IN	IN	IN	IN

VME BUS SYSFAIL JUMPER

J8 SYSFAIL JUMPER
FACTORY INSTALLED BY FOIL TRACE
BOARD WILL ASSERT SYSFAIL AFTER
POWER UP OR RESET.

VME BUS STANDARD ADDRESS JUMPERS

JUMPER J6 PINS 3 & 4 - JUMPER INSTALLED - SELECTING STANDARD MEMORY MAP,J5 & J7 SELECT ON BASE ADDRESS.

BASE ADDRESS	PINS ON J7							
	S23 15 & 16	S22 13 & 14	S21 11 & 12	S20 9 & 10	S19 7 & 8	S18 5 & 6	S17 3 & 4	S16 1 & 2
00 0000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01 0000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
02 0000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT
03 0000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
FC 0000H	IN	IN	IN	IN	IN	IN	OUT	OUT
FD 0000H	IN	IN	IN	IN	IN	IN	OUT	IN
FE 0000H	IN	IN	IN	IN	IN	IN	IN	OUT
FF 0000H	IN	IN	IN	IN	IN	IN	IN	IN

VME BUS ADDRESS MODIFIER CODES

JUMPER J6 PINS 3 & 4	JUMPER J6 PINS 1 & 2	ADDRESS MODIFIER CODES RECOGNIZED	ADDRESSING MODE
OUT	OUT	2DH	SHORT SUPERVISORY
OUT	IN	2DH OR 29H	SHORT SUPERVISORY OR SHORT NON-PRIVELEDGED
IN	OUT	3DH	STANDARD SUPERVISORY
IN	IN	3DH OR 39H	STANDARD SUPERVISORY OR STANDARD NON-PRIVELEDGED

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2.3.1 Default Jumper Configuration

VMEBUS INTERFACE CONFIGURATION

When a board is shipped from the factory, it is configured as follows:

- VMEbus Short I/O Address of 0000H.
- Set to respond to both Address Modifiers 2DH and 29H.
- All sections set up for Bit Mode.

2.4 ADDRESS ASSIGNMENT

Jumpers J5, J6, and J7 are used to establish the base address for the 1k byte block of memory the AVME 947X will occupy in the Memory Map. J5 and J7 selects the base address. An open, or no jumper installed, corresponds to a logic 0 state. Refer to Table 2.2 Address Decoding. J6 selects the address modifier codes and the Standard or Short Memory Map. An open on J6 pins 1 and 2 selects only the Supervisory Access (3DH or 2DH) code. A short on J6 pins 1 and 2 will allow the card to recognize both the Supervisory and the Non-Priviledged Access codes. An open, or no jumper installed, on J6 pins 3 and 4 selects Short Memory Map. A short, or jumper installed, selects Standard Memory Map. Refer to Table 2.1.

Table 2.1 VMEbus Address Modifier Codes

Jumper J6 Pins 3 & 4	Jumper J6 Pins 1 & 2	Address Modifier Codes Recognized	Addressing Mode
OUT	OUT	2DH	Short Supervisory
OUT	IN	2DH OR 29H	Short Supervisory or Short Non-Privileged
IN	OUT	3DH	Standard Supervisory
IN	IN	3DH OR 39H	Standard Supervisory or Standard Non-Privileged

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Table 2.2 VMEbus Address Decoding

Jumper J6 Pins 3 & 4 - No Jumper Installed - Selecting The Short Memory Map. J7 Has No Effect On The Base Address Selection.

	Pins on J5					
Base Address	S15 11 & 12	S14 10 & 9	S13 8 & 7	S12 6 & 5	S11 4 & 3	S10 2 & 1
0000H	OUT	OUT	OUT	OUT	OUT	OUT
0400H	OUT	OUT	OUT	OUT	OUT	IN
0800H	OUT	OUT	OUT	OUT	IN	OUT
F400H	IN	IN	IN	IN	OUT	IN
F800H	IN	IN	IN	IN	IN	OUT
FC00H	IN	IN	IN	IN	IN	IN

Jumper J6 Pins 3 & 4 - Jumper Installed - Selecting The Standard Memory Map, J5 & J7 Select The Base Address.

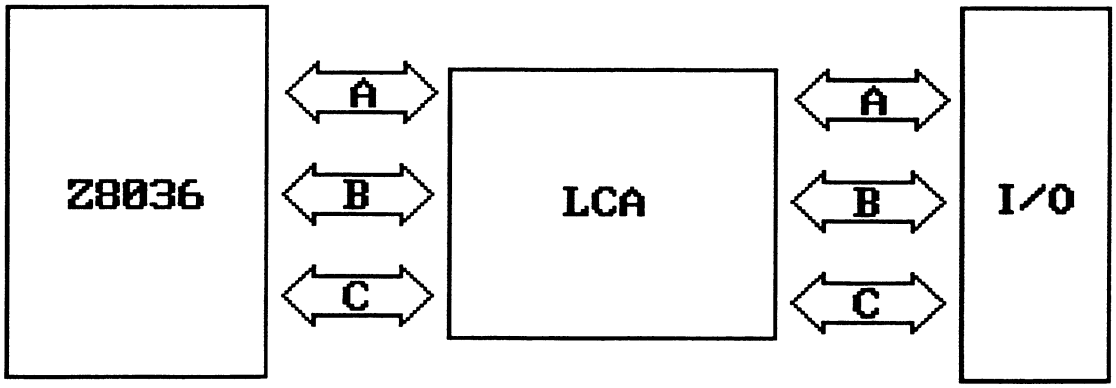
	Pins on J7							
Base Address	S23 15 & 16	S22 13 & 14	S21 11 & 12	S20 9 & 10	S19 7 & 8	S18 5 & 6	S17 3 & 4	S16 1 & 2
00 0000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01 0000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
02 0000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT
03 0000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
FC 0000H	IN	IN	IN	IN	IN	IN	OUT	OUT
FD 0000H	IN	IN	IN	IN	IN	IN	OUT	IN
FE 0000H	IN	IN	IN	IN	IN	IN	IN	OUT
FF 0000H	IN	IN	IN	IN	IN	IN	IN	IN

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2.5 CONFIGURATION JUMPERS

The AVME 947X Industrial Digital I/O Boards offer either two or four independent I/O "sections" depending on the model. Each section contains a Zilog Z8036 Counter/Timer and Parallel I/O Unit (CIO). The Z8036 provides each section with 20 I/O points each. These I/O points are divided into two 8-bit ports (ports A and B) and one 4-bit port (port C). Some points are configurable as counter/timer or handshake control signals.

A Field Programmable Logic Cell Array (LCA) controls the input & output circuitry between the Z8036 and your application. Each section's LCA is configured with a jumper selectable program that is automatically loaded upon power up. These LCA programs are optimized to take advantage of specific features of the CIO and can also provide enhancements such as input debouncing.



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There are three jumper selectable LCA configuration programs for each section. The three programs are DEBOUNCE, BIT and HANDSHAKE. Not all of the 947X's resources are available with each program. Use the following paragraphs and Tables 2.3, 2.4, and 2.5 to select the proper configuration for your application. Table 2.6 identifies the jumper number with the section and shows which pins to select for the different LCA configuration programs.

NOTE: The configuration must be selected before power is applied to the board. Changing the configuration jumper after power has been applied will not alter the operation of the section until after power has been cycled off and on again.

2.5.1 DEBOUNCE Configuration

The DEBOUNCE configuration offers the ability to filter the mechanical switch noise on ports A and B of any section. This is accomplished by inserting a shift register in the input line and summing the outputs of the shift register to give a clean transition from one level to another. The clock for this shift register is provided by the 16 bit counter/timer of port C. The counter/timer of port C must always provide a clock. This allows only 3 pins of port C to be used as I/O points, with the forth pin being used as the debounce clock. This configuration also allows port B to be used in the bit mode or have full use of the two 16 bit counter/timers. If the operator attempts to program the CIO for a handshake mode, the section will automatically be reset configuring the I/O points as inputs. See table 2.3 for the different operating modes available in this configuration.

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Table 2.3

Section Resources Available With "DEBOUNCE" Jumper Installed

CIO OPERATING MODE	Port A	Port B								Port C			
		C/T #1				C/T #2				C/T #3			
	A7 - A0	B7	B6	B5	B4	B3	B2	B1	B0	C3	C2	C1	C0
BIT I/O	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	NA
PR/Interrupt	OK	OK	OK	OK	OK	OK	OK	OK	OK	NA	NA	NA	NA
HANDSHAKE PORT I/O	NA RESET*	NA	NA	NA	NA RESET*	NA	NA	NA	NA RESET*	NA	NA	NA	NA
COUNTER/TIMER	NA	GI	TI	CI	CO	GI	TI	CI	CO	DEBOUNCE CLK			

NOTES:

CIO OPERATING MODE is determined by the bits programmed in the Port Mode, Port Handshake, & Counter/Timer Specification Registers of the CIO.

PR/Interrupt refers to the bit's ability to be used for Pattern Recognition and Interrupt Generation on transitions, levels, changes of state, or word matches as determined by the bits programmed in the Pattern Definition Registers of the CIO.

DEBOUNCE CLK indicates that C/T #3 is used as a source for the debounce clock.

RESET*: If the CIO is configured for this mode the section will automatically reset itself.

KEY:
OK-Bit is available for this type of use.
NA-Bit is not available for this type of use.
CO-Counter Output, CI-Counter Input, TI-Trigger Input, GI-Gate Input.

2.5.2 BIT Configuration

The BIT configuration is nearly identical to the DEBOUNCE configuration. The difference is the elimination of the debounce circuitry. This configuration allows all of the ports to be used in the bit mode or allows full use of the three 16 bit counter/timers. If the operator attempts to program the section for a handshake mode, the section will automatically be reset, configuring the I/O points as inputs. See Table 2.4 for the different operating modes available in this configuration.

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Table 2.4
Section Resources Available With "BIT" Jumper Installed

CIO OPERATING MODE	Port A	Port B		Port C
		C/T #1	C/T #2	C/T #3
	A7 - A0	B7 B6 B5 B4	B3 B2 B1 B0	C3 C2 C1 C0
BIT I/O	OK	OK OK OK OK	OK OK OK OK	OK OK OK OK
PR/Interrupt	OK	OK OK OK OK	OK OK OK OK	NA NA NA NA
HANDSHAKE PORT I/O	NA RESET*	NA NA NA NA RESET*	NA NA NA NA RESET*	NA NA NA NA
COUNTER/TIMER	NA	GI TI CI CO	GI TI CI CO	GI TI CI CO

NOTES:

CIO OPERATING MODE is determined by the bits programmed in the Port Mode, Port Handshake, & Counter/Timer Specification Registers of the CIO.

PR/Interrupt refers to the bit's ability to be used for Pattern Recognition and Interrupt Generation on transitions, levels, changes of state, or word matches as determined by the bits programmed in the Pattern Definition Registers of the CIO.

RESET*: If the CIO is configured for this mode the section will automatically reset itself.

KEY:
OK-Bit is available for this type of use.
NA-Bit is not available for this type of use.
CO-Counter Output, CI-Counter Input, TI-Trigger Input, GI-Gate Input.

2.5.3 HANDSHAKE Configuration

The HANDSHAKE configuration allows the section to operate in any of the four handshake modes. Port A can be operated only in a handshake mode, while port B can be operated in bit, handshake or the counter/timer modes. Ports A and B can also be linked together to form a 16 bit handshake port. Port C supplies the additional control signals needed to operate ports A and B in a handshake mode. The HANDSHAKE configuration offers two additional interrupt options. Interrupt after one or two bytes of data transfers. If the operator attempts to program port A for a bit mode, the section will automatically be reset, configuring the I/O points as inputs. See Table 2.5 for the different operating modes available in this configuration.

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Table 2.5
Section Resources Available With "HANDSHAKE" Jumper Installed

CIO OPERATING MODE	Port A	Port B								Port C			
		C/T #1				C/T #2				C/T #3			
	A7 - A0	B7	B6	B5	B4	B3	B2	B1	B0	C3	C2	C1	C0
BIT I/O	RESET*	OK	OK	OK	OK	OK	OK	OK	OK	NA	NA	OK	OK
PR/Interrupt	NA	OK	OK	OK	OK	OK	OK	OK	OK	NA	NA	NA	NA
HANDSHAKE PORT I/O													
Interlocked	OK	OK	OK	OK	OK	OK	OK	OK	OK	RD	AK	RD	AK
w Request/Wait*	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	RW	BT
Bidirectional	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	BT	IO
Strobed	OK	OK	OK	OK	OK	OK	OK	OK	OK	RD	AK	RD	AK
w Request/Wait*	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	RW	BT
Bidirectional	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	BT	IO
Pulsed	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	BT	BT
w Request/Wait*	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	AK	RW	BT
3-Wire													
Input	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	RD	RW	DC
Output	OK	NA	NA	NA	NA	NA	NA	NA	NA	RD	DC	RW	RD
COUNTER/TIMER	NA	GI	TI	CI	CO	GI	TI	CI	CO	NA	NA	NA	NA

NOTES:

CIO OPERATING MODE is determined by the bits programmed in the Port Mode, Port Handshake, & Counter/Timer Specification Registers of the CIO.

PR/Interrupt refers to the bit's ability to be used for Pattern Recognition and Interrupt Generation on transitions, levels, changes of state, or word matches as determined by the bits programmed in the Pattern Definition Registers of the CIO.

RESET*: If the CIO is configured for this mode the section will automatically reset itself.

KEY:
OK-Bit is available for this type of use.
NA-Bit is not available for this type of use.
CO-Counter Output, CI-Counter Input, TI-Trigger Input, GI-Gate Input.
RD-RFD or DAV*, AK-ACKIN*, RW-Request/Wait*, BT-Bit I/O,
IO-Bidirectional In/Out*, DC-DAC.

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Table 2.6 Configuration Jumpers

SECTION	JUMPER	CONFIGURATION		
		jumper installed on pins		
		DEBOUNCE	BIT	HANDSHAKE
0	J3	1 & 2	1 & 3	4 & 6
1	J4	1 & 2	1 & 3	4 & 6
2	J2	1 & 2	1 & 3	4 & 6
3	J1	1 & 2	1 & 3	4 & 6

2.6 I/O CONNECTIONS

On Model AVME9470, four 50-pin ribbon cable connectors (labeled P3, P4, P5 and P6) on the front panel are used to access the 80 I/O points to termination panels. Sections 0 through 3 are available.

On Models AVME9471 and AVME9473, the I/O points are accessible through a 96 pin DIN 41612 connector labeled P2. These models use I/O adapter card Model 9921-16 (this adapter is not P2 safe), which is mounted to the back of a VME cage to provide the mating socket for P2. On Model AVME9471, four 50-pin ribbon cable connectors on the I/O adapter card are used to access the 80 points to termination panels. Sections 0 through 3 are available. On Model AVME 9473, two 50-pin ribbon cable connectors on the I/O adapter card are used to access the 40 I/O points to termination panels. Sections 0 and 1 are available.

CAUTION: DO NOT PLUG P2 INTO ANY BACKPLANES IN A CARD CAGE

On Model AVME9472, two 50-pin ribbon cable connectors (labeled P3 and P4) on the front panel are used to access the 40 I/O points to termination panels. Sections 0 and 1 are available.

On Model AVME9475, the 40 I/O points are accessible through a 96 pin DIN 41612 connector labeled P2. This model uses I/O adaptor card Model 9922-16 (this adapter is P2 safe), which is either mounted to the back of a P2 backplane or to the P2 connector of this board. Two 50-pin ribbon cable connectors on the I/O adapter card are used to access the 40 I/O points to termination panels. Sections 2 and 3 are available.

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Refer to table 2.7 for I/O connector pin assignments and the following pages for the appropriate termination panel connection diagrams.

Table 2.7 I/O Connectors P2, P3, P4, P5 & P6

Functions	P2 Pin #	P3 Pin #	P4 Pin #
SECTION 0			
Port A I/O Bit 7	B25	33	
6	B26	35	
5	B27	37	
4	B28	39	
3	B29	41	
2	B30	43	
1	B31	45	
0	B32	47	
Port B I/O Bit 7	B17	17	
6	B18	19	
5	B19	21	
4	B20	23	
3	B21	25	
2	B22	27	
1	B23	29	
0	B24	31	
Port C I/O Bit 3	B10	3	
2	B11	5	
1	B12	7	
0	B13	9	
+5V	B9	1,49	
GND	B14	2 thru 50	
GND	B15,B16	Even	
SECTION 1			
Port A I/O Bit 7	A25		33
6	A26		35
5	A27		37
4	A28		39
3	A29		41
2	A30		43
1	A31		45
0	A32		47
Port B I/O Bit 7	A17		17
6	A18		19
5	A19		21
4	A20		23
3	A21		25
2	A22		27
1	A23		29
0	A24		31

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Table 2.7 Continued

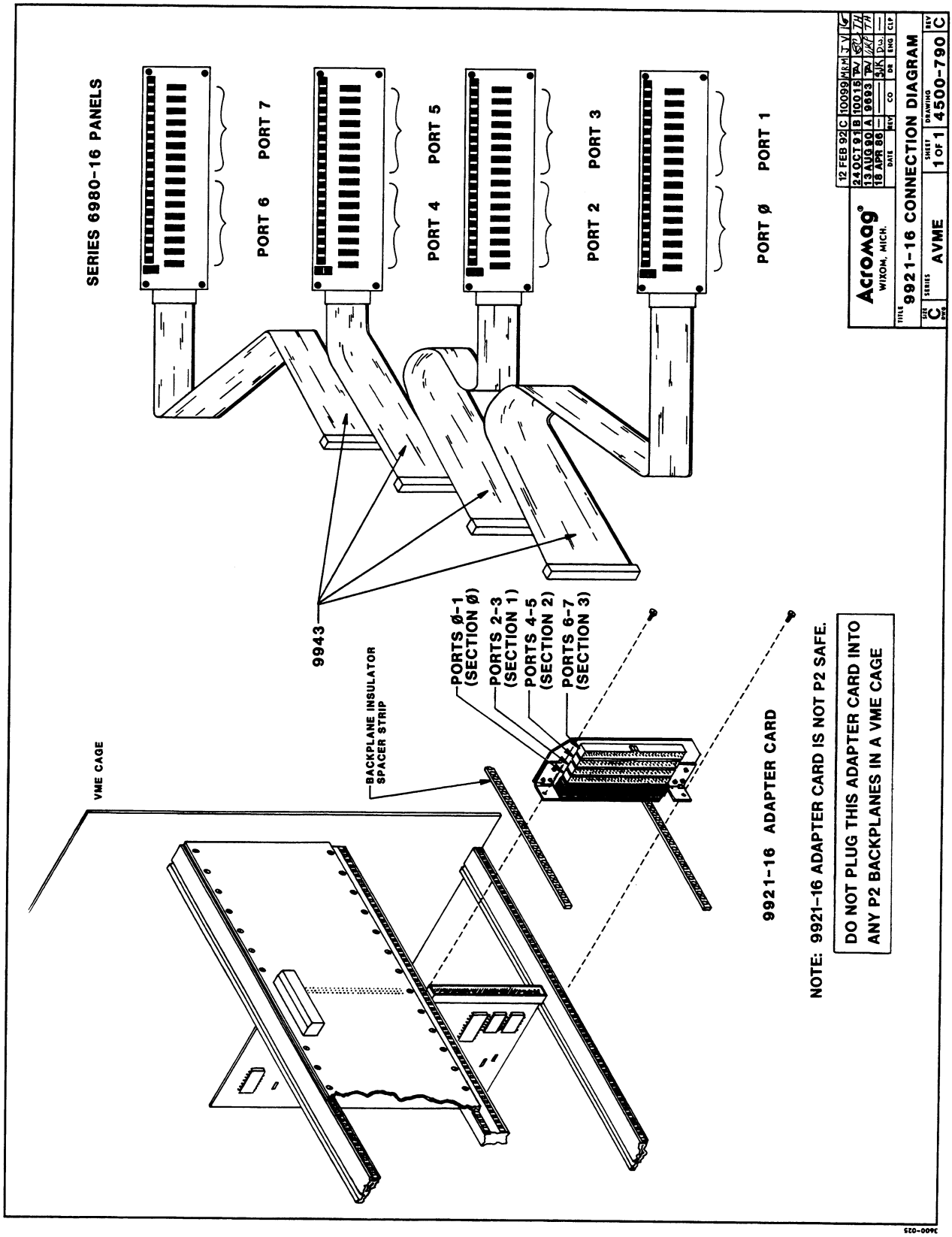
Functions	P2 Pin #	P5 Pin #	P4 Pin #
Port C I/O Bit 3	B2		3
2	B3		5
1	B4		7
0	B5		9
+5V	B1		1,49
GND	B6		2 thru 50
GND	B7,B8		Even
			P6 Pin#
SECTION 2			
Port A I/O Bit 7	C25	33	
6	C26	35	
5	C27	37	
4	C28	39	
3	C29	41	
2	C30	43	
1	C31	45	
0	C32	47	
Port B I/O Bit 7	C17	17	
6	C18	19	
5	C19	21	
4	C20	23	
3	C21	25	
2	C22	27	
1	C23	29	
0	C24	31	
Port C I/O Bit 3	C10	3	
2	C11	5	
1	C12	7	
0	C13	9	
+5V	C9	1,49	
GND	C15,C16	2 thru 50	
GND	C14	Even	
SECTION 3			
Port A I/O Bit 7	A8		33
6	A7		35
5	A6		37
4	A5		39
3	A4		41
2	A3		43
1	A2		45
0	A1		47

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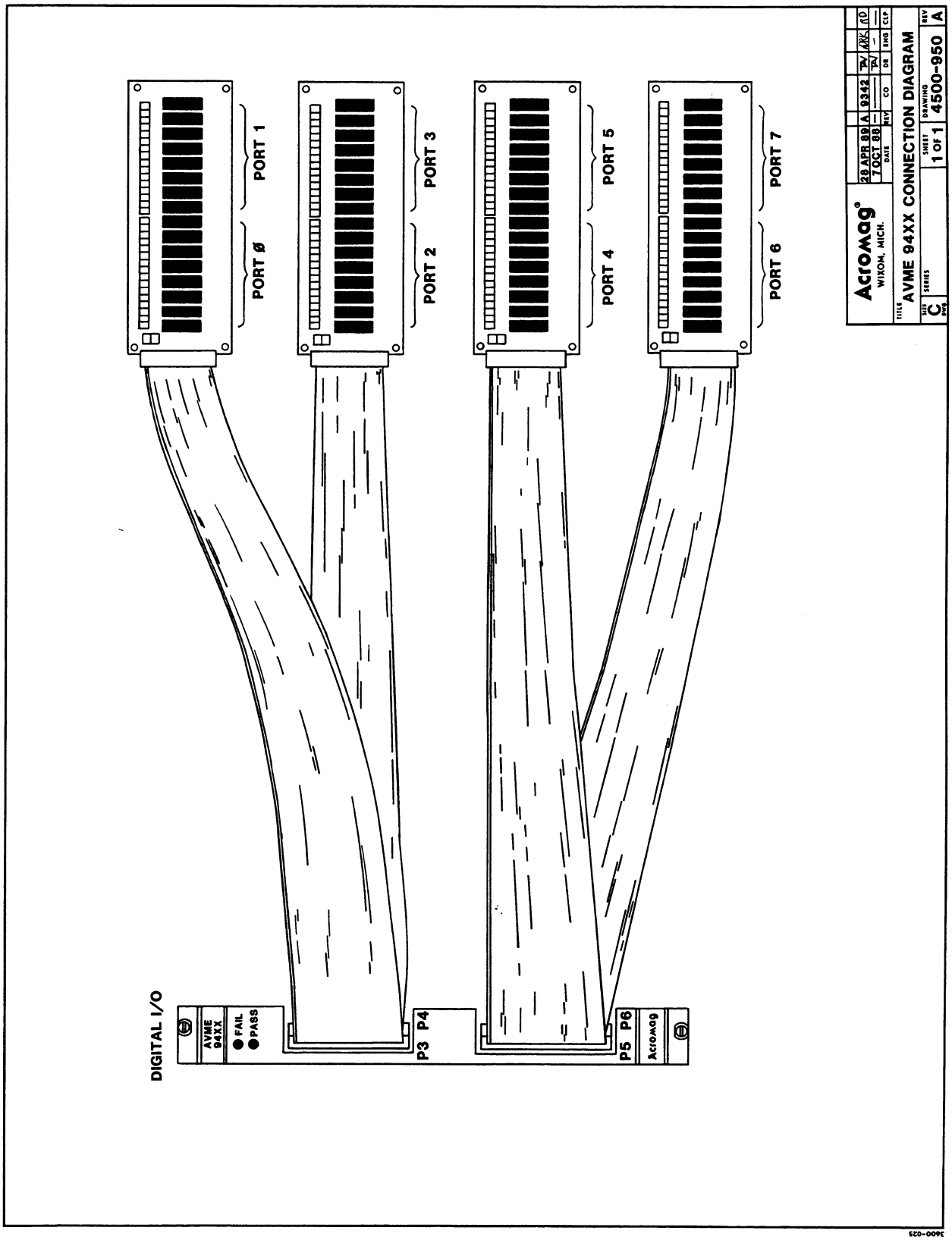
Table 2.7 Continued

Functions	P2 Pin #	P5 Pin #	P6 Pin #
Port B I/O Bit 7	A16		17
6	A15		19
5	A14		21
4	A13		23
3	A12		25
2	A11		27
1	A10		29
0	A9		31
Port C I/O Bit 3	C2		3
2	C3		5
1	C4		7
0	C5		9
+5V	C1		1,49
GND	C6		2 thru 50
GND	C7,C8		Even

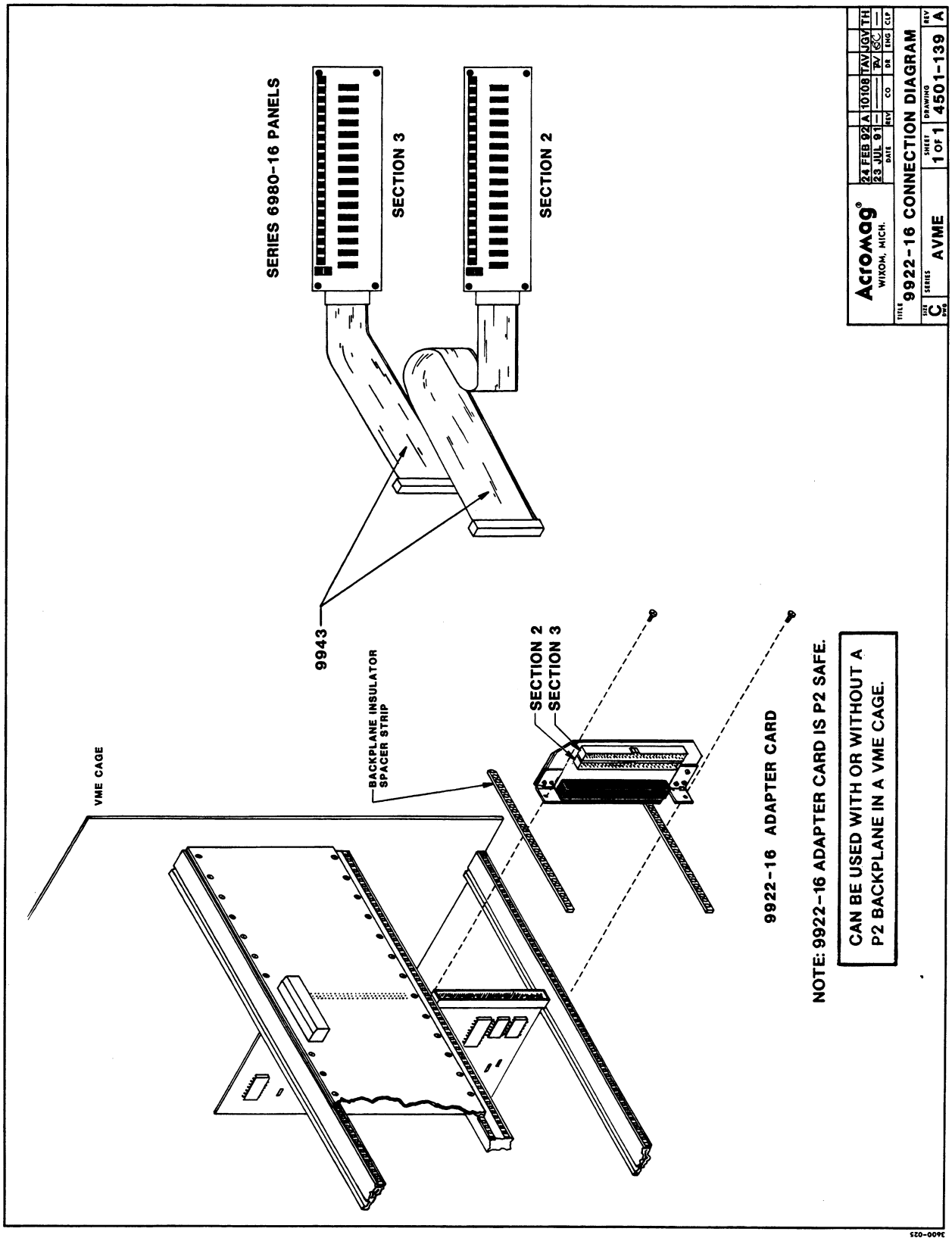
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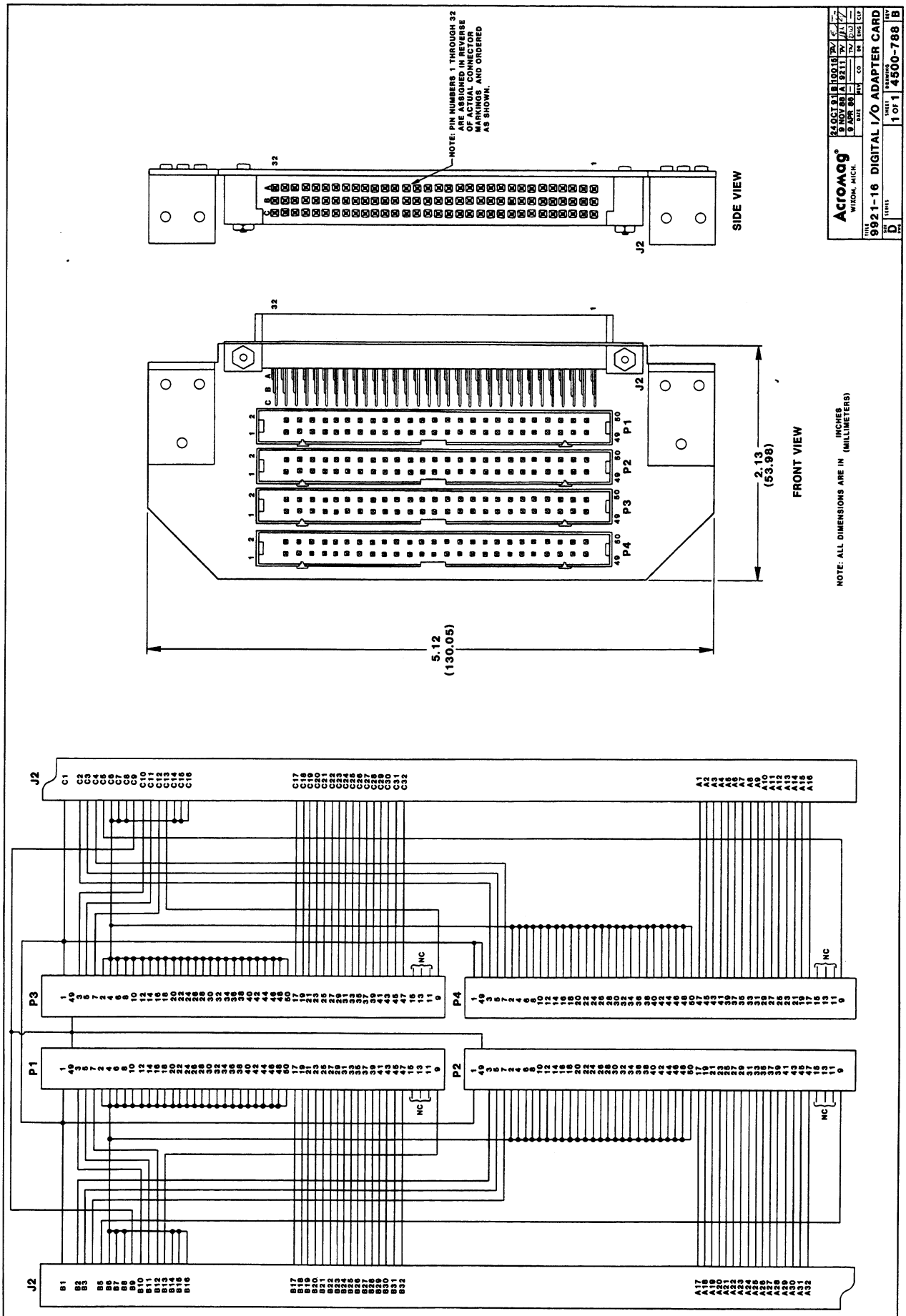
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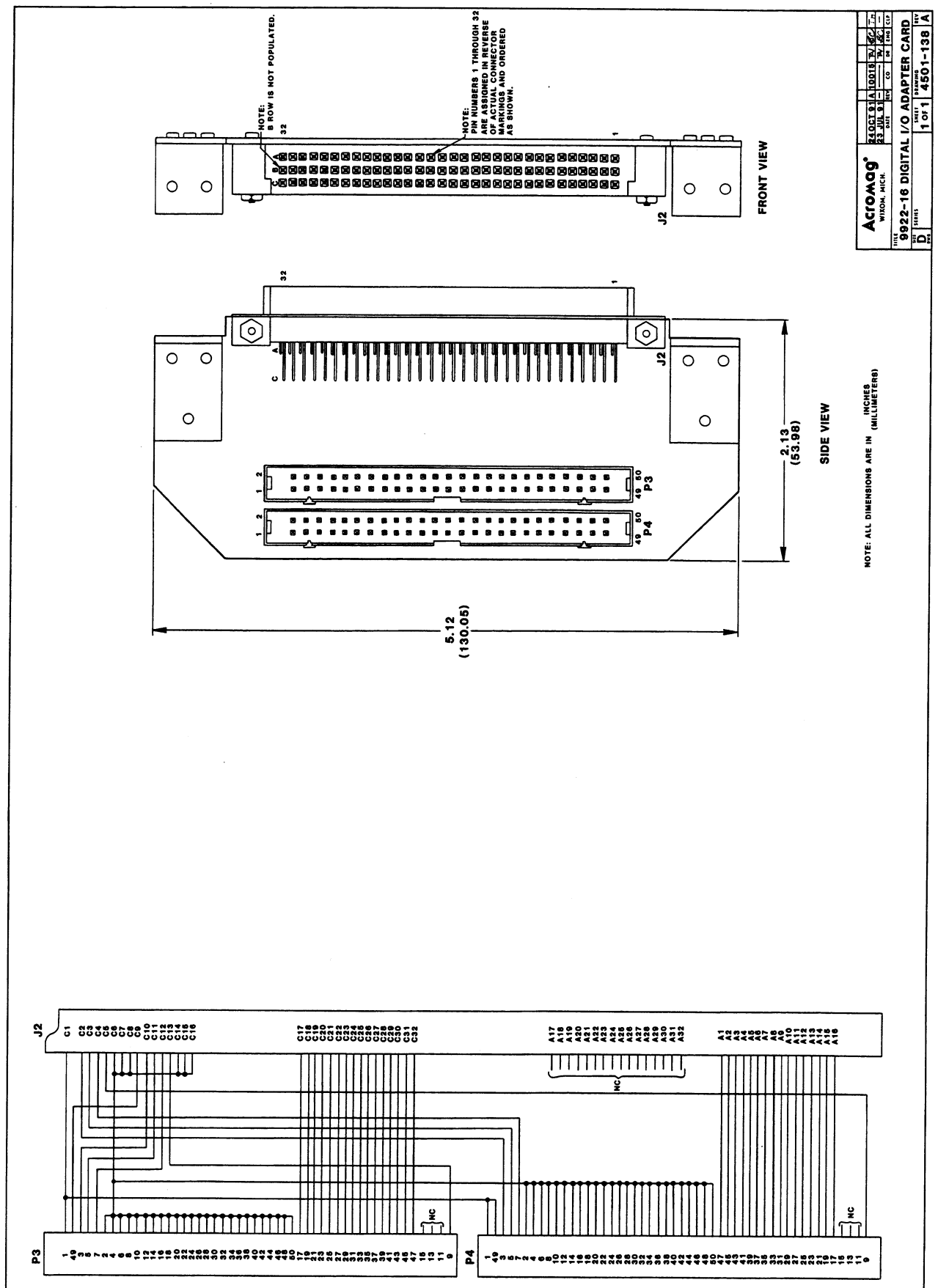
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2.7 BACKPLANE REQUIREMENTS

The AVME947X is electrically and mechanically compatible with the VMEbus Specification Manual, Revision C.1. The backplane connection is made through the 96 pin DIN 41612 connector labeled P1. The signals used are listed in Table 2.8.

Table 2.8 Backplane Connector P1.

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00		D08
2	D01		D09
3	D02		D10
4	D03		D11
5	D04		D12
6	D05		D13
7	D06		D14
8	D07		D15
9	GND		GND
10	SYSCLK		SYSFAIL*
11	GND		BERR*
12	DS1*		SYSRESET*
13	DS0*		LWORD*
14	WRITE*		AM5
15	GND		A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31			
32	+5V	+5V	+5V

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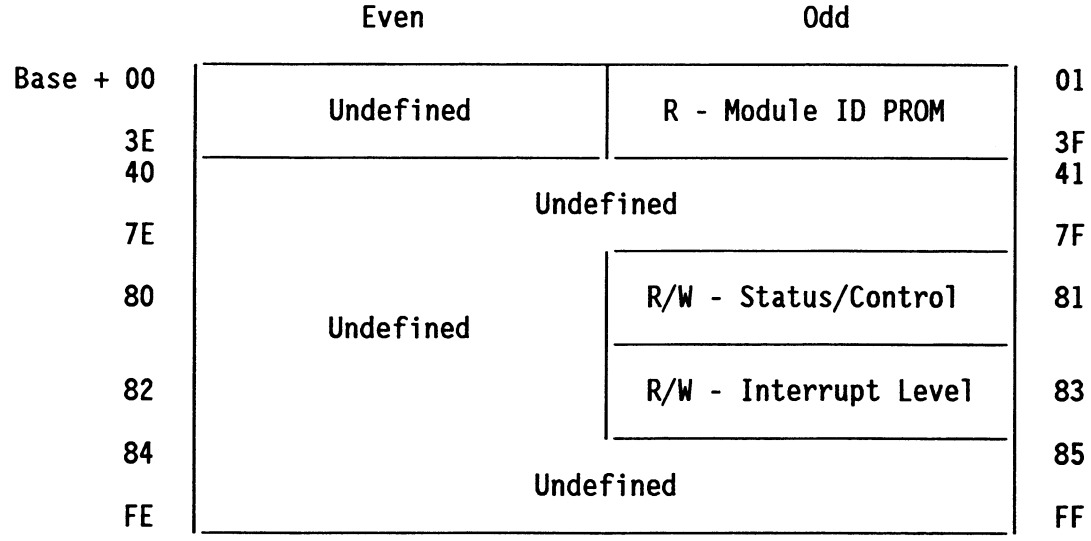
3.0 PROGRAMMING INFORMATION

This chapter provides the specific information necessary to program the Digital I/O Board.

3.1 MEMORY MAP

The memory map for the Industrial Digital I/O board, a Non Intelligent I/O architecture is shown figure 3.1. The Industrial Digital I/O board is addressable on 1K byte boundaries in either the Short or Standard address space. All Acromag VMEbus non-intelligent slaves have a standard interface configuration which consists of a 32 byte board ID prom and a Board Status register. The rest of the 1K byte address space contains registers or memory specific to the function of the board. All addresses are in hexadecimal. The letters R and W indicate whether a register may be read and/or written. The areas marked "undefined" in the memory map will read as all bits equal to one if read. These areas are reserved for future use. For future compatibility, application programs should not use these areas for any reason.

FIG. 3.1 AVME 947X Industrial Digital I/O Board Memory Map



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FIG. 3.1 AVME 947X Industrial Digital I/O Board Memory Map Cont.

	I/O SECTION 0 (9470-73) I/O SECTION 2 (9475)	I/O SECTION 1 (9470-73) I/O SECTION 3 (9475)	
100	Master Interrupt Ctrl	Master Interrupt Ctrl	101
102	Master Config Control	Master Config Control	103
104	A Interrupt Vector	A Interrupt Vector	105
106	B Interrupt Vector	B Interrupt Vector	107
108	C/T Interrupt Vector	C/T Interrupt Vector	109
10A	C Data Path Polarity	C Data Path Polarity	10B
10C	C Data Direction	C Data Direction	10D
10E	C Special I/O Control	C Special I/O Control	10F
110	A Command & Status	A Command & Status	111
112	B Command & Status	B Command & Status	113
114	CT1 Command & Status	CT1 Command & Status	115
116	CT2 Command & Status	CT2 Command & Status	117
118	CT3 Command & Status	CT3 Command & Status	119
11A	A Data	A Data	11B
11C	B Data	B Data	11D
11E	C Data	C Data	11F
120	CT1 Current Count-MSB	CT1 Current Count-MSB	121
122	CT1 Current Count-LSB	CT1 Current Count-LSB	123
124	CT2 Current Count-MSB	CT2 Current Count-MSB	125
126	CT2 Current Count-LSB	CT2 Current Count-LSB	127
128	CT3 Current Count-MSB	CT3 Current Count-MSB	129
12A	CT3 Current Count-LSB	CT3 Current Count-LSB	12B
12C	CT1 Time Constant-MSB	CT1 Time Constant-MSB	12D
12E	CT1 Time Constant-LSB	CT1 Time Constant-LSB	12F
130	CT2 Time Constant-MSB	CT2 Time Constant-MSB	131
132	CT2 Time Constant-LSB	CT2 Time Constant-LSB	133
134	CT3 Time Constant-MSB	CT3 Time Constant-MSB	135
136	CT3 Time Constant-LSB	CT3 Time Constant-LSB	137
138	CT1 Mode Specification	CT1 Mode Specification	139
13A	CT2 Mode Specification	CT2 Mode Specification	13B
13C	CT3 Mode Specification	CT3 Mode Specification	13D
13E	Current Vector	Current Vector	13F
140	A Mode Specification	A Mode Specification	141
142	A Handshake Specification	A Handshake Specification	143
144	A Data Path Polarity	A Data Path Polarity	145
146	A Data Direction	A Data Direction	147
148	A Special I/O Control	A Special I/O Control	149
14A	A Pattern Polarity	A Pattern Polarity	14B
14C	A Pattern Transition	A Pattern Transition	14D
14E	A Pattern Mask	A Pattern Mask	14F
150	B Mode Specification	B Mode Specification	151
152	B Handshake Specification	B Handshake Specification	153
154	B Data Path Polarity	B Data Path Polarity	155
156	B Data Direction	B Data Direction	157
158	B Special I/O Control	B Special I/O Control	159
15A	B Pattern Polarity	B Pattern Polarity	15B
15C	B Pattern Transition	B Pattern Transition	15D
15E	B Pattern Mask	B Pattern Mask	15F

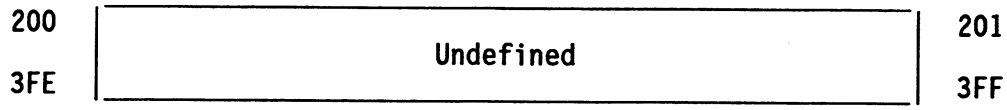
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FIG. 3.1 AVME 947X Industrial Digital I/O Board Memory Map Cont.

	I/O SECTION 2 (9470-73) I/O SECTION 2 (9475)	I/O SECTION 3 (9470-73) I/O SECTION 3 (9475)	
180	Master Interrupt Ctrl	Master Interrupt Ctrl	181
182	Master Config Control	Master Config Control	183
184	A Interrupt Vector	A Interrupt Vector	185
186	B Interrupt Vector	B Interrupt Vector	187
188	C/T Interrupt Vector	C/T Interrupt Vector	189
18A	C Data Path Polarity	C Data Path Polarity	18B
18C	C Data Direction	C Data Direction	18D
18E	C Special I/O Control	C Special I/O Control	18F
190	A Command & Status	A Command & Status	191
192	B Command & Status	B Command & Status	193
194	CT1 Command & Status	CT1 Command & Status	195
196	CT2 Command & Status	CT2 Command & Status	197
198	CT3 Command & Status	CT3 Command & Status	199
19A	A Data	A Data	19B
19C	B Data	B Data	19D
19E	C Data	C Data	19F
1A0	CT1 Current Count-MSB	CT1 Current Count-MSB	1A1
1A2	CT1 Current Count-LSB	CT1 Current Count-LSB	1A3
1A4	CT2 Current Count-MSB	CT2 Current Count-MSB	1A5
1A6	CT2 Current Count-LSB	CT2 Current Count-LSB	1A7
1A8	CT3 Current Count-MSB	CT3 Current Count-MSB	1A9
1AA	CT3 Current Count-LSB	CT3 Current Count-LSB	1AB
1AC	CT1 Time Constant-MSB	CT1 Time Constant-MSB	1AD
1AE	CT1 Time Constant-LSB	CT1 Time Constant-LSB	1AF
1B0	CT2 Time Constant-MSB	CT2 Time Constant-MSB	1B1
1B2	CT2 Time Constant-LSB	CT2 Time Constant-LSB	1B3
1B4	CT3 Time Constant-MSB	CT3 Time Constant-MSB	1B5
1B6	CT3 Time Constant-LSB	CT3 Time Constant-LSB	1B7
1B8	CT1 Mode Specification	CT1 Mode Specification	1B9
1BA	CT2 Mode Specification	CT2 Mode Specification	1BB
1BC	CT3 Mode Specification	CT3 Mode Specification	1BD
1BE	Current Vector	Current Vector	1BF
1C0	A Mode Specification	A Mode Specification	1C1
1C2	A Handshake Specification	A Handshake Specification	1C3
1C4	A Data Path Polarity	A Data Path Polarity	1C5
1C6	A Data Direction	A Data Direction	1C7
1C8	A Special I/O Control	A Special I/O Control	1C9
1CA	A Pattern Polarity	A Pattern Polarity	1CB
1CC	A Pattern Transition	A Pattern Transition	1CD
1CE	A Pattern Mask	A Pattern Mask	1CF
1D0	B Mode Specification	B Mode Specification	1D1
1D2	B Handshake Specification	B Handshake Specification	1D3
1D4	B Data Path Polarity	B Data Path Polarity	1D5
1D6	B Data Direction	B Data Direction	1D7
1D8	B Special I/O Control	B Special I/O Control	1D9
1DA	B Pattern Polarity	B Pattern Polarity	1DB
1DC	B Pattern Transition	B Pattern Transition	1DD
1DE	B Pattern Mask	B Pattern Mask	1DF

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FIG. 3.1 AVME 947X Industrial Digital I/O Board Memory Map Cont.



Note: Sections 2 and 3 present only on Models AVME 9470, 9471, 9475.

3.1.1 Board Identification PROM (I.D. PROM) - (Read Only) (01-3F)

The Board Identification PROM occupies the 32 odd bytes beginning at location 01. These bytes contain ASCII character strings that identify various characteristics of the board. See figure 3.1.

Table 3.1: Board Identification PROM

Offset From Board Base Address	Value ASCII Character	Value Numeric	Descriptions
01H	V	56H	Always VMEID for all boards.
03H	M	4DH	
05H	E	45H	
07H	I	49H	
09H	D	44H	
0BH	A	41H	Manufacturers I.D., ACR for ACROMAG.
0DH	C	43H	
0FH	R	52H	
11H	9	39H	Board Model Number (7 characters, blank filled).
13H	4	34H	
15H	7	37H	
17H	0	30H	
19H		20H	
1BH		20H	
1DH		20H	
1FH	1	31H	Number of Kilobytes of address space used.
21H		20H	
23H THRU 3FH	UNDEFINED		Reserved

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3.1.2 Status/Control Register - (R/W) (81)

The Status/Control Register reflects and controls functions globally on the card.

7	6	5	4	3	2	1	0
<-------Reserved------->			Software Reset	Global Int. Enable	Global Int. Pending	Green LED	Red LED

Where:

Bits 7,6,5: Reserved for future use - will read as 0.

Bit 4: Software Reset (W) - writing a 1 to this bit causes a software reset. Writing "0" or reading the bit has no affect. A software reset switches all of the ports to input ports. The effect of a software reset on the various registers is determined in the discussion of each of the registers. (Note: Following a software reset, the host should wait at least 100mS. before accessing the card, otherwise, a bus error could result.)

Bit 3: Global Interrupt Enable (R/W) - writing a 1 to this bit enables interrupts to occur from the AVME947X board. A "0" prevents interrupts.

Reset Condition: All interrupts disabled.

Bit 2: Global Interrupt Pending (R) - this bit will be a 1 when there is an interrupt pending from any of the sections. This bit will be "0" when there are no interrupts pending.

Reset condition: No effect.

Bit 1: Green LED (R/W) - this bit when written will control the state of the green LED on the front panel. A "1" will turn it on, a "0" will turn it off. Reading it will reflect its current state.

Reset Condition: Reset to "0", LED off.

Bit 0: Red LED (R/W) - this bit when written will control the state of the red LED on the front panel and the state of the VMEbus SYSFAIL* signal. A "1" will turn it off and set SYSFAIL* high, a "0" will turn it on and set SYSFAIL* low. Reading it will reflect its current state.

Reset Condition: Reset to "0", LED on and SYSFAIL* is set low.

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The status register bits 1 and 0 along with the green and red LEDs provide the user with a means of keeping track of a board's functionality in the system. Since there is no intelligence on the board, the host computer controls these bits. The following is one possible use of the bits in the status register and the LEDs on the front panel.

On power-up the bits in the status register will read low, with the green LED off, the red LED lit, and SYSFAIL* low. This indicates that the board has failed or that it hasn't been tested yet.

The Status Register Bit 1 reads low and Bit 0 reads high. The LEDs will both be off and SYSFAIL* is high. This indicates an inactive board.

The Status Register Bit 1 reads high and Bit 0 reads low. The LEDs will both be lit and SYSFAIL* is low. This indicates the board is undergoing a diagnostic checkout.

The Status Register Bits 1 and 0 read high. The green LED will be lit with the red LED off and SYSFAIL* is high. This indicates the board is fully functional.

3.1.3 Interrupt Level Register - (R/W) (83)

The Interrupt Level Register maintains the VMEbus Interrupt Request level (IRQ7-IRQ1).

```
     7      6      5      4      3      2      1      0
-------------------------------------------------------------------
 <-------------Reserved--------------->   MSB<---Level--->LSB
```

Where:

Bits 7,6,5,4,3: Reserved for future use - will read as "0".

Bit 2,1,0: Must be programmed with a number from one to seven which is the VMEbus Interrupt Request Level that will be asserted when the board is requesting an interrupt.

Reset Condition: Hardware Reset zeros the Register. No interrupts can be generated from this board. Software reset has no effect on this Register.

3.1.4 Programming the Sections

The technical manual for the Z8036 CIO is reprinted in appendix Z. Refer to the technical manual in appendix Z for a complete discussion of the registers and operation of the CIO. Table 3.2 lists all of the CIO's registers and the offsets of the registers. To obtain the address of each register in a section, add the base address of the section and the register address offset. All register address numbers are hexadecimal.

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Table 3.2 CIO's Registers

Main Control Registers

Register Address	Register Name
00	Master Interrupt Control
02	Master Configuration Control
08	Counter/Timer Interrupt Vector
3E	Current Vector

Port A Registers

Register Address	Register Name
10	Command and Status
1A	Data
40	Mode Specification
42	Handshake Specification
44	Data Path Polarity
46	Data Direction
48	Special I/O Control
4A	Pattern Polarity
4C	Pattern Transition
4E	Pattern Mask
04	Interrupt Vector

Port B Registers

Register Address	Register Name
12	Command and Status
1C	Data
50	Mode Specification
52	Handshake Specification
54	Data Path Polarity
56	Data Direction
58	Special I/O Control
5A	Pattern Polarity
5C	Pattern Transition
5E	Pattern Mask
06	Interrupt Vector

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Table 3.2 CIO's Registers Continued

Port C Registers

Register Address	Register Name
1E	Data
0A	Data Path Polarity
0C	Data Direction
0E	Special I/O Control

Counter/Timer 1 Registers

Register Address	Register Name
14	Command and Status
20	Current Count-MSBs
22	Current Count-LSBs
38	Mode Specification
2C	Time Constant-MSBs
2E	Time Constant-LSBs

Counter/Timer 2 Registers

Register Address	Register Name
16	Command and Status
24	Current Count-MSBs
26	Current Count-LSBs
3A	Mode Specification
30	Time Constant-MSBs
32	Time Constant-LSBs

Counter/Timer 3 Registers

Register Address	Register Name
18	Command and Status
28	Current Count-MSBs
2A	Current Count-LSBs
3C	Mode Specification
34	Time Constant-MSBs
36	Time Constant-LSBs

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3.1.4.1 Master Interrupt Control Register ($00)

7	6	5	4	3	2	1	0
MIE	DLC	NV	PA VIS	PB VIS	CT VIS	RJA	RESET

Bits 7,6,4,3,2,0: See Appendix Z.

Bit 5: No Vector (NV). DO NOT SET THIS BIT TO A "1". When this bit is set to a "1" it inhibits the CIO from outputting a vector during the interrupt acknowledge cycle. There is no external circuitry on the Industrial Digital I/O Board to supply a vector, so with this bit set to a 1 the CPU will respond unpredictably trying to service an interrupt.

Bit 1: Right Justified Address (RJA). DO NOT SET THIS BIT TO A "1". If this bit is programmed to a 1 then you will not be able to access the section registers. To regain control of the section you must reset the section by writing $01 to this register and then write $00 to clear the reset.

See Appendix Z pages 2-3 for a detailed discussion of the Master Interrupt Control Register.

3.1.4.2 Special I/O Control Registers

The special I/O Control Register allows the user to configure the output of the port to be either a totem-pole or open drain output. There are no external pull up resistors on the CIO's outputs. Therefore, don't program the output for the open drain configuration. See Appendix Z pages 2-10 for a detailed discussion of the special I/O control registers.

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3.2 COUNTER/TIMER OPERATION

There are three Counter/Timers to each CIO. Counter/Timers 1 and 2 are accessible through Port B and Counter/Timer 3 is accessible through Port C. The clock to the Counter/Timers may be either the internal clock or supplied by the user. The internal clock is 2 MHz which is half of the PCLK input. The external clock must be less than or equal to 3.33 MHz with a minimum pulse width of 170ns. The output formulas are listed below. Refer to Appendix Z Chapter 4 for a detailed discussion of the Counter/Timers.

Continuous Square Wave Output Frequency (FO)

$$FO = \frac{CLOCK}{2 \times COUNT} \qquad \begin{array}{l} CLOCK = 2\ MHz\ or\ External \\ 1 < COUNT < 65{,}536 \end{array}$$

Oneshot Output Time (OS)

$$OS = \frac{COUNT}{CLOCK} \qquad \begin{array}{l} CLOCK = 2\ MHz\ or\ External \\ 1 < COUNT < 65{,}536 \end{array}$$

3.2.1 Debounce Counter/Timer Operation

If a section is in the debounce configuration then Counter/Timer 3 must supply a debounce clock for any of the inputs to work. The Counter/Timer must be set up in the continuous square wave mode with the external output enabled. This brings the clock out on bit 0 of Port C.

The debounce delay time (i.e. delay before the transition propagates to the output) is given by the following formula. Refer to paragraph 3.2.4 for the counter/Timer initialization example.

Debounce Time (DBNC)

$$\frac{2}{FO} \leq DBNC \leq \frac{3}{FO}$$

Where: CLOCK = 2 MHz. or External; 1 < COUNT < 65,536; and the uncertainty of 1 clock period is due to the asynchronous nature of the input.

Note that input pulses of duration less than 1 clock cycle will not appear at the output; input pulses of 1-2 clock cycles may appear at the output; input pulses more than 2 cycles will appear at the output.

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3.3 PROGRAMMING EXAMPLES

The following examples detail the hardware setup and programming steps required to operate the Industrial Digital I/O Board in one of the modes listed in Tables 2.3, 2.4 and 2.5.

3.3.1 Reset

There are several different ways to reset the board, some are global and the others reset by section only. Assume that the base address of the board is $FF0000.

Global Resets:

----------ACTION----------	----------RESULT----------
1. Depress Reset Switch on CPU Board.	-Turns off Global Interrupt Enable (bit 3="0") in the Status/Control register. -Turns off Green LED (bit 1="0") in the Status/Control register. -Turns on Red LED (bit 0="0") in the Status/Control Register and asserts SYSFAIL*. -Interrupt Level register equals "0". -All ports of all the sections are programmed to be inputs.
2. Write $00 to Master Interrupt Control register of all the sections.	-Turns off reset bit. All CIO registers operate normally.
1. Write $10 to the Status/Control register $FF0081.	-Turns off Global Interrupt Enable (bit 3="0") in the Status/Control register. -Turns off Green LED (bit 1="0") in the Status/Control register. -Turns on Red LED (bit 0="0") in the Status/Control Register and asserts SYSFAIL*. -All ports of all the sections are programmed to be inputs.
2. Write $00 to Master Interrupt Control register of all the sections.	-Turns off reset bit. All registers operate normally.

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Section Reset:

----------ACTION----------	----------RESULT----------
1. Write $01 to Master Interrupt Control register.	-Turns on reset bit -All ports of the section are programmed to be inputs. -All registers now in reset mode.
2. Write $00 to Master Interrupt Control register.	-Turn off reset bit. All registers operate normally.

Programming a port for a restricted mode within the section configuration will also cause a section to reset. See Tables 2.3, 2.4 and 2.5.

1. Section Configured as a DEBOUNCE section. Write $40 to Port A Mode register.	-Turn on reset bit -All ports of the section are programmed to be inputs. -All registers in reset mode.
2. Write $00 to Master Interrupt Control register.	-Turn off reset bit. All registers operate normally.
1. Section Configured as a BIT section. Write $80 to Port B Mode register.	-Turn on reset bit -All ports of the section are programmed to be inputs. -All registers in reset mode.
2. Write $00 to Master Interrupt Control register.	-Turn off reset bit. All registers operate normally.
1. Section Configured as a HANDSHAKE section. Write $00 to Port A Mode register.	-Turn on reset bit -All ports of the section are programmed to be inputs. -All registers in reset mode and read "0".
2. Write $00 to Master Interrupt Control register.	-Turn off reset bit. All registers operate normally.

3.3.2 Board Initialization

Assume that the base address of the board is $FF0000.

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Board Initialization:

ACTION	RESULT
1. Write a $10 to the Status/ Control register $FF0081.	-This will reset the board.
2. Write a $03 to the Status/ Control register $FF0081.	-This turns off the red LED, negates SYSFAIL*, and turns on the green LED.
3. Write a $01 to the Interrupt Level Register $FF0083.	-This will cause the interrupt request level to be 1 (IRQ1*).

3.3.3 Bit Mode

The Bit Mode is the simplest of the CIO's operating modes. In this example Port A has 5 output bits and 3 input bits. Port B is programmed as a output port and Port C is programmed to be an input port. For this example we will be using section 3 in the BIT configuration. Assume that the base address of the board is $FF0000. The base address of Section 3 is $FF0181.

Hardware setup: Place a jumper on J1 pins 1 and 3. Apply power.

Software Port Initialization:

ACTION	RESULT
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to section 3 Master Interrupt Control register $FF0181.	-This negates the reset bit for the section.
3. Write a $E0 to Port A Data Direction Register $FF01C7.	-Bits 7,6,5 will be inputs with bits 4,3,2,1,0 as outputs.
4. Write a $00 to Port B Data Direction Register $FF01D7.	-All of the bits in port B are outputs.
5. Write a $0F to Port C Data Direction Register $FF018D.	-All of the bits in port C are inputs.
6. Write a $0A to Port A Data register $FF019B.	-Port A bits 4,3,2,1,0 will output a XXX0 1010.
7. Write a $5A to Port B Data Register $FF019D.	-Port B will output 0101 1010.
8. Write a $94 to the Master Configuration Control Register $FF0183.	-This enables ports A,B and C.

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Using the Ports:

----------ACTION----------	----------RESULT----------
1. Write a $15 to Port A Data Register $FF019B.	-Port A bits 4,3,2,1,0 will output a XXX1 0101.
2. Read Port A Data Register $FF019B.	-Port A bits 7,6,5 will read the state of the I/O points, bits 4,3,2,1,0 will read XXX1 0101.
3. Write a $A0 to Port B Data Register $FF019D.	-Port B will output 1010 0000.
4. Read Port B Data Register $FF019D.	-Port B will read $A0.
5. Write a $0F to Port C Data Register $FF019F.	-Port C will not output anything it is in an input mode.
6. Read Port C Data Register $FF019F.	-Port C will read the state of the I/O points.

3.3.4 Debounced Change of State Mode

The debounced Change of State mode is a modification to the basic bit mode. In this example Port A will be a debounced input port with its mode setup as Change of State (COS). The debounce clock will be set up with a period of 10 mSec giving a debounce time of 30 mSec. Interrupts will be enabled for port A. Port B is programmed as an output port. Port C is also programmed as an output port. Counter/Timer 3 will output a square wave on bit 0 of port C for the debounce clock. For this example we will be using section 0 in the DEBOUNCE configuration. Assume that the base address of the board is $FF0000. The base address of section 0 is $FF0100.

Hardware setup: Place a jumper on J3 pins 1 and 2. Apply power.

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Software Port Initialization:

----------ACTION----------	----------RESULT----------
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to section 0 Master Interrupt Control register $FF0100.	-This negates the reset bit for the section.
3. Write a $FF to Port A Data Direction Register $FF0146.	-All of the bits in port A in the input mode.
4. Write a $00 to Port B Data Direction Register $FF0156.	-All of the bits in port B are outputs.
5. Write a $00 to Port C Data Direction Register $FF010C.	-All of the bits in port C are outputs.
6. Write a $5A to Port B Data Register $FF011C.	-Port B will output 0101 1010.
7. Write a $3F to Port C Data register $FF011E.	-Port C will output a 1100.
8. Write a $94 to the Master Configuration Control Register $FF0102.	-This enables ports A,B and C.

Software Counter/Timer 3 Initialization:

9. Write a $C2 to Counter/Timer 3 Mode Specification Register $FF013C.	-This sets up the counter/timer for a continuous square wave with the external output enabled.
10. Write a $27 to Counter/Timer 3 Time Constant Register MSB $FF0134.	-These two writes sets up the counter /timer to have a period of 10 mSec.
11. Write a $10 to Counter/Timer 3 Time Constant Register LSB $FF0136.	
12. Write a $06 to Counter/Timer 3 Command Status Register $FF0118.	-This gates the counter on, and triggers the counter to start the square wave.

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Software Interrupt Initialization:

----------ACTION----------	----------RESULT----------
13. Write a $F0 to the Port A Pattern Transition Register $FF014C.	-These two writes sets up bits 7,6,5,4 to interrupt on any Transition and bits 3,2,1,0 no interrupts.
14. Write a $00 to the Port A Pattern Mask Register $FF014E.	
15. Write a $40 to Port A Interrupt Vector Register $FF0104.	-The vector returned during an interrupt acknowledge cycle will be $40.
16. Write a $04 to Port A Mode Register $FF0140.	-This programs Port A for a bit mode with an "OR" pattern match mode.
17. Write $20 to Port A Command/ Status register $FF0110.	-This clears any interrupts that occurred during initialization.
18. Write a $C0 to Port A Command and Status Register $FF0110.	-This sets the interrupt enable bit.
19. Write a $80 to the Master Interrupt Control Register $FF0100.	-This set the master interrupt enable bit for the section.
20. Write a $0B to the Control/ Status Register $FF0081.	-This enables interrupts on a board level.

Interrupts may now occur from Section 0 Port A.

Using the Ports:

----------ACTION----------	----------RESULT----------
1. Read Port A Data Register $FF011A.	-Port A bits will read the state of the I/O points.
2. Write a $A0 to Port B Data Register $FF011C.	-Port B will output 1010 0000.
3. Read Port B Data Register $FF011C.	-Port B will read $A0.
4. Write a $0F to Port C Data Register $FF011E.	-Port C will output 111X.
5. Read Port C Data Register $FF011E.	-Port C will read 1111 111X.

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Interrupt Service Routine:

----------ACTION----------	----------RESULT----------
1. Write a $20 to Port A Command and Status Register $FF0110.	-This clears the Interrupt Pending and Interrupt Under Service flags.
2. Write a $C0 to Port A Command and Status Register $FF0110.	-This reenables interrupts.

3.3.5 Interlocked and Pulsed Handshake Mode

The Handshake Modes requires the use of all of the bits in Port C for control signals. Port A will be programmed as an Interlocked Output Port. Port B will be programmed for a pulsed handshake input port. For this example we will be using Section 2 in the HANDSHAKE configuration. Assume that the base address of the board is $FF0000. The base address of Section 2 is $FF0180.

Hardware setup: Place a jumper on J2 pins 4 and 6. Apply power.

Port C Handshake Control Signals

Bit 3	$\overline{\text{DAV}}$	Output	Data available
Bit 2	$\overline{\text{ACKIN}}$	Input	Acknowledge input
Bit 1	RFD	Output	Ready for data
Bit 0	$\overline{\text{ACKIN}}$	Input	Acknowledge input

Software Port Initialization:

----------ACTION----------	----------RESULT----------
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to Section 2 Master Interrupt Control register $FF0180.	-This negates the reset bit for the section.
3. Write a $90 to Port A Mode Specification Register $FF01C0.	-This sets up port A for a handshake output port.
4. Write a $00 to Port A Handshake Specification Register $FF01C2.	-This specifies the Interlocked Handshake Mode.
5. Write a $50 to Port B Mode Specification Register $FF01D0.	-This sets up Port B for handshake input port.

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----------ACTION----------	----------RESULT----------
6. Write $80 to Port B Handshake Specification Register $FF01D2.	-This specifies the pulsed handshake mode.
7. Write a $0F to Port C Data Direction Register $FF018C.	-All of the bits in port C are inputs.
8. Write a $94 to the Master Configuration Control Register $FF0182.	-This enables ports A, B and C.

Software Counter/Timer #3 Initialization:

Counter/Timer #3 operation is necessary for the pulsed handshake mode.

----------ACTION----------	----------RESULT----------
1. Write a $ 02 to Counter/Timer #3 Mode Specification Register $FF01BC.	-This sets up the Counter/Timer for a single cycle square wave mode.
2. Write $10 to Counter/Timer #3 Time Constant LSB Register $FF01B6.	-These two writes give a square wave frequency of 62.5 kHZ.
3. Write $00 to Counter/Timer #3 Time Constant MSB Register $FF01B4.	
4. Write $04 to Counter/Timer #3 Command/Status Register $FF0198.	-This enables the counter.

Using the Ports:

----------ACTION----------	----------RESULT----------
1. Read Port A Command/Status Register $FF0190.	-If bit 3 is high then new data may be written to the data register.
2. Write $AA to Port A Data Register $FF019A.	-This will cause Port A to transfer a $AA to the receiver.
3. Read Port B command/Status Register $FF0192.	-If Bit 2 is high then new data is available in the data register.
4. Read Port B Data Register $FF019C.	-Port B will read the value transmitted.

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3.3.6 3-Wire Handshake

The 3-Wire Handshake Mode requires the use of 3 of the bits in Port C for control signals. Port A will be our handshake port programmed in a 3-wire output mode. Port B is programmed as an output port in a bit mode and Port C will be programmed to be an input port. For this example we will be using Section 0 in the HANDSHAKE configuration. Assume that the card is addressed $FF0000 in the short address space. The base address of Section 0 is $FF0100.

Hardware setup: Place a jumper on J3 pins 4 and 6. Apply power.

Port C Handshake Control Signals

Bit 3	$\overline{\text{DAV}}$	Output	Data available
Bit 2	DAC	Input	Data accepted
Bit 1	Bit I/O	Either	
Bit 1	RFD	Input	Ready for data

Software Initialization:

----------ACTION----------	----------RESULT----------
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to Section 0 Master Interrupt Control Register $FF0100.	-This negates the reset bit for the section.
3. Write a $90 to Port A Mode specification Register $FF0140.	-This sets up Port A for a handshake output port.
4. Write a C0 to Port A Handshake Specification Register $FF0142.	-This specifies the 3-Wire Handshake Mode.
5. Write a $00 to Port B Data Direction $FF0156.	-All of the bits in Port B are outputs.
6. Write a $0F to port C Data Direction Register $FF010C.	-All of the bits in Port C are inputs.
7. Write a $5A to Port B Data Register $FF011C.	-Port B will output 0101 1010.
8. Write a $94 to the Master Configuration Control Register $FF0102.	-This enables Ports A, B, and C.

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Using the Ports:

----------ACTION----------	----------RESULT----------
1. Read Port A Command Status Register $FF0110.	-If bit 3 is high then new data may be written to the data register.
2. Write $55 to Port A Data Register $FF011A.	-This will cause Port A to transfer a $55.
3. Write a $A0 to Port B Data Register $FF011C.	-Port B will output 1010 0000.
4. Read Port B Data Register $FF011C.	-Port B will read $A0.
5. Write a $0F to Port C Data Register $FF011E.	-Port C will not output anything it is in an input mode.
6. Read Port C Data Register $FF011E.	-Port C bits 3, 2, and 0 are used in Port A handshaking operation, bit 1 will read the state of the I/O points.

3.3.7 Bidirectional Handshake Mode

The Bidirectional Handshake Mode requires the use of three of the bits in Port C for control signals. Port A will be our handshake port programmed in a Interlock Master mode. For this example we will be using Section 0 in the HANDSHAKE configuration. Assume that the card is addressed $FF0000 in the short address space. The base address of Section 0 is $FF0100.

Hardware setup: Place a jumper on J3 pins 4 and 6. Apply power.

Port C Handshake Control Signals

Bit 3	RFD or $\overline{DAV}$	Output	Ready for data or data available
Bit 2	$\overline{ACKIN}$	Input	Acknowledge input
Bit 1	Bit I/O	Either	
Bit 0	In/$\overline{Out}$	Output*	Data direction

* Bit 0 is an output because this port is the master.

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Software Initialization:

ACTION	RESULT
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to Section 0 Master Interrupt Control Register $FF0100.	-This negates the reset bit for the section.
3. Write a $D0 to Port A Mode Specification Register $FF0140.	-This sets up Port A for a handshake bidirectional port.
4. Write a $00 to Port A Handshake Specification Register $FF0142.	-This specifies the Interlocked Handshake Mode.
5. Write a $0E to Port C Data Direction Register $FF010C.	-Bit 0 is an output, bits, 3,2,1 are inputs.
6. Write a $02 to Port C Data Register $FF011E.	-This makes the port an output port.
7. Write a $14 to the Master Configuration Control Register $FF0102.	-This enables Ports A and C.

Using the Ports:

ACTION	RESULT
1. Write a $A5 to Port A Data Register $FF011A.	-This will transfer a $A5.
2. Write a $20 to Port A Command/ Status Register $FF0110.	-This will initiate the data transfer.
3. Write a $01 to Port C Data Register $FF011E.	-This will change the direction of the data flow.
4. Write $20 to Port A Command/ Status Register $FF0110.	-This clears the interrupt pending bit.
5. Read Port A Command/Status Register $FF0110.	-If Bit 2 is high then new data is in the Data Register.
6. Read Port A Data Register $FF011A.	-This is the data transferred.
7. Write $20 to Port A Command/ Status $FF0110 Register.	

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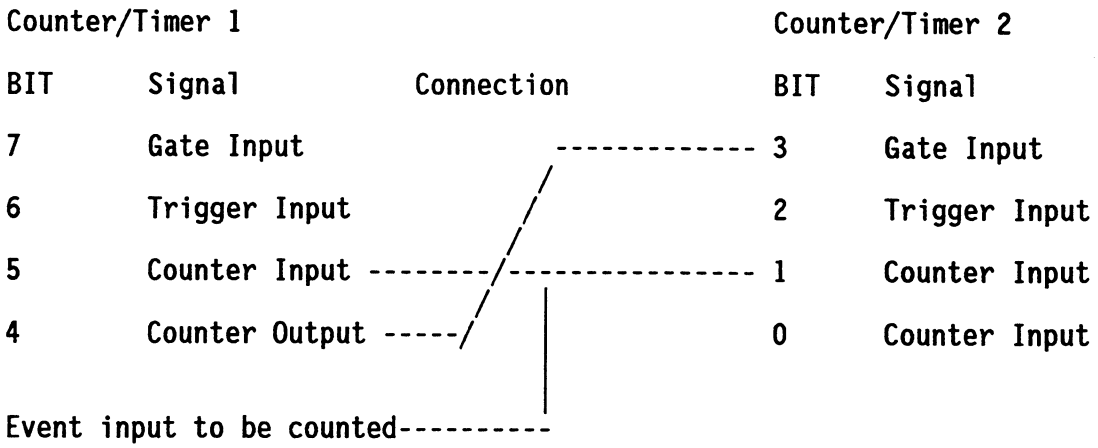
----------ACTION----------	----------RESULT----------
8. Write $00 to Port C Data Register $FF011E.	-This will change direction of the data transfer.
9. Write $20 to Port A Command/ Status Register $FF0110.	-This clears the interrupt pending bit.

3.3.8 Counter/Timer Modes

Counter/Timers 1 and 2 are contained in Port B with Counter/Timer 3 in Port C. For this example Counter/Timers 1 and 2 will be combined to form a 32 bit Event Counter. This is accomplished by externally tying Counter/Timer 1's Output to Counter/Timer 2's Gate Input. Counter/Timer 3 will be set up as a Watch Dog Timer to interrupt after 32.8 mSEC if it is not retriggered. For this example we will be using Section 1 in the BIT configuration. Assume that the base address of the board is $FF0000. The base address of Section 1 is $FF0101.

Hardware setup: Place a jumper on J4 pins 1 and 3. Apply power.

Port B Counter/Timer Signals



Software Initialization:

----------ACTION----------	----------RESULT----------
1. Execute the Board Initialization routine. See Paragraph 3.3.2.	
2. Write a $00 to Section 1 Master Interrupt Control Register $FF0101.	-This negates the reset bit for the section.
3. Write a $EF to Port B Data Direction Register $FF0157.	-Bit 4 will be an output with the rest of the bits of Port B, inputs.

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----------ACTION----------	----------RESULT----------
4. Write a $A8 to Counter/Timer 1 Mode Specification Register $FF0139.	-This puts the counter 1 in the continuous pulse output mode with the counter output enabled and the external count and gate inputs enabled.
5. Write a $A8 to Counter/Timer 2 Mode Specification Register $FF013B.	-This puts the counter in the continuous mode with external gate and count input enabled.
6. Write $FF to the Time Constant Registers $FF012D, $FF012F, $FF0131, $FF0133.	-This initializes the count to $FFFFFFFF.
7. Write $E0 to the Master Configuration Control Register $FF0103.	-This enables counters 1 and 2.
8. Write a $05 to Counter/Timer 3 Mode Specification Register $FF013D.	-This sets up the counter for single cycle retriggerable oneshot.
9. Write $FF to Counter/Timer 3 Time Constant Registers $FF0135 and $FF0137.	-The oneshot time will be 32.8 mSec.
10. Write $F0 to the Master Configuration Control Register $FF0103.	-This enables counter 3.
11. Write a $40 to Counter/Timer Interrupt Vector Register $FF0109.	-The vector returned during an interrupt acknowledge cycle will be $40.
12. Write a $80 to the Master Interrupt Control Register $FF0101.	-This sets the master interrupt enable bit for the section.
13. Write a $0B to the Control/Status Register $FF0081.	-This enables interrupts on a board level.
14. Write a $06 to the counter/timer 1 Command/Status Register $FF0115.	-This triggers and gates the Counter/Timer on.
15. Write a $06 to the Counter/Timer 2 Command/Status Register $FF0117.	-This triggers and gates the Counter/Timer on.
16. Write a $C6 to Counter/Timer Command and Status Register $FF0119.	-This sets the interrupt enable bit and starts the counter.

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Using the Counter/Timers:

----------ACTION----------	----------RESULT----------
1. Read Counter/Timer 1 Command Status Register $FF0115.	
2. "OR" Counter/Timer 1 Command Status Register with $08.	
3. Write the "ORed" value back to Counter/Timer 1 Command Status Register $FF0115.	-This freezes the count.
4. Read counter value in the following order.	
A. Counter/Timer 2 Current Count Register MSB $FF0125	
B. Counter/Timer 2 Current Count Register LSB $FF0127	
C. Counter/Timer 1 Current Count Register MSB $FF0121	
D. Counter/Timer 1 Current Count Register LSB $FF0123	
5. Write a $06 to Counter/Timer 3 Command Status Register $FF0115. This write must be a least once every 32.8 mSec to keep the watch dog timer from interrupting.	-Retriggers the oneshot.

3.3.8.1 Changing Counter/Timer Output Frequency

Each Counter/Timer (C/T) can output a continuous square-wave. The frequency of this output is controlled by the Time Constant placed in the Time Constant Register. The specifics of setting up the 947X to use this C/T mode is left to the user. However, there is one area which needs some additional consideration. Specifically, how can the square-wave frequency be changed smoothly (no glitches) while the signal is still being generated?

The Down-Counter (an internally accessed register), the Time Constant Register, and the C/T Command and Status Register are involved in the method discussed below. See Appendix Z for a complete description of these registers.

When operating in the continuous mode, the Down-Counter is automatically loaded with the value of the Time Constant Register every half cycle. This value determines the duration of each half cycle. To change the output frequency simply requires changing the value in the Time Constant Register. The new value would automatically be loaded into the Down-Counter at the end

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of the current half-cycle changing the frequency of the output. The trick is to avoid changing the Time Constant Register while its contents are being loaded into the Down-Counter.

The suggested method involves the use of interrupts. There are other methods which may be used in specific situations, however, this method is more universal. Note that the C/T can generate an interrupt when the Down-Counter is ready to be reloaded with a Time Constant (the Down-Counter has reached Terminal Count). However, without the Interrupt Enable (IE) bit set in the C/T Command and Status Register, the C/T will not generate this interrupt. Also note that the Count-In-Progress (CIP) bit of the C/T Command and Status Register is asserted while the square-wave is being generated except when the Down-Counter is reloading.

The method consists of:

* Set up C/T to interrupt on Terminal Count, but be sure the IE bit is NOT set.

* Program the other parameters of C/T (continuous mode, time constant value, external output enable, gate command bit, etc.).

* Trigger the C/T starting the square-wave output.

* When a change of frequency is desired, enable the C/T to interrupt. This involves clearing IUS and IP in the Command and Status register (be sure that GCB stays set!) then setting IE.

* An interrupt will occur when the Down-Counter is reloading. The Interrupt Service Routine (ISR) should check CIP to make sure the Down-Counter is done reloading (CIP is set), program the Time Constant, clear IUS/IP, and disable IE (again make sure GCB stays set).

The interrupt signals that it will soon be safe to change the Time Constant Register. The timing of this operation is critical. If the ISR was itself interrupted, it may change the Time Constant at the incorrect time. To avoid this the ISR could change the interrupt mask to level 7. This would prevent preemption by another interrupt. Of course this must be done with EXTREME care. Lengthy interrupt service routines should be avoided if this technique is used.

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3.4 CHANGE OF STATE PROCESSING

There are several methods of processing Change of State (COS) interrupts on the AVME947X. To cause change of state interrupts, the CIO's Pattern Match logic must be set up and interrupts enabled both within the CIO and in the board's Status/Control Register. Each bit within a port can cause a pattern match. There are three pattern matching modes, which may cause interrupts, available for each port. Of the three pattern match modes two pertain to COS processing, they are the "OR" mode and the "OR Priority Encoded Vector" mode. The word match or "AND" mode will not be discussed. With either the "OR" or "OR Priority Encoded Vector" pattern match modes the port's pattern match logic may be set up to be either edge or level sensitive on one or all of the bits of the port. Refer to appendix Z, paragraphs 2.5.1, 2.7, 3.3.2 for a more detailed discussion of the pattern match operation.

3.4.1 "OR" Method of COS Processing

With the pattern match logic in the "OR" mode, the user may set up the logic to be edge sensitive. There are three edge sensitive setups, rising edge, falling edge, or either edge. This would appear to be the proper method to use the port, however there are two problems. The first problem is identification of the bit that caused the interrupt if more than two bits are enabled. This may be solved by using the one's catcher. The second problem is the occurrence of multiple pattern matches, caused when more than one bit changes, within the port. The first pattern match will cause the interrupt but if a second pattern match occurs before the first one is cleared, a second interrupt will not be generated. The time between the two matches can not be specified because it is dependant upon a number of things such as the system CPU, CPU clock speed, the operating system, etc. If the user can tolerate these problems then this is the most efficient method for COS processing.

3.4.2 "OR Priority Encoded Vector" Method of COS Processing

To use the "OR Priority Encoded Vector" mode for COS processing the user must set up the CIO to sense a logic level "1" with the one's catcher enabled. This method allows the user three ways to determine which bit caused the interrupt. Using the first way, the interrupt vector is modified, automatically by the CIO, with the bit position of the interrupting bit. This provides an individual vectored interrupt for each bit in the port. The second way uses a common vector for all the bits in the port. When the port's "Vector Register" is read by the interrupt handler, the interrupt handler will read a vector modified with the bit position of the interrupting bit. Using the last way, the port's "Data Register" is read. Since the one's catcher has be enabled, the highest bit which is read as a "1" will be the interrupting bit.

The "OR Priority Encoded Vector" mode will cause an interrupt for each pattern match (bit change) that occurs no matter when the match occurs. This mode will continue to cause interrupts as long as the pattern match conditions are met. For this reason the interrupt handler must clear the pattern match before it clears the Interrupt Pending (IP) bit in the port's Command/Status register. With this method there are no interrupts missed as in the "OR" method.

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3.4.2.1 "OR Priority Encoded Vector" COS Example

The following example uses the pattern match logic in the "OR Priority Encoded Vector" mode with the one's catcher enabled. It uses one interrupt vector for all eight bits of the port. This method has been tested and has detected both edges of a 50 nsec pulse that was simultaneously applied to all eight bits of the port. The result was 16 interrupts.

Initialization Procedure

* Initialize the board for interrupts.
* Initialize the port for Bit I/O operation.
* Write the interrupt vector into the port's Interrupt Vector Register.
* Set up the interrupter mode for the "OR Priority Encoded Vector" mode in the port Mode Register.
* Set up the pattern match registers to match on a level "1". In this example all 8 bits of the port will be unmasked and have the ability to cause interrupts. This is accomplished by writing:

  $FF to the Pattern Polarity Register.
  $00 to the Pattern Transition Register.
  $FF to the Pattern Mask Register.

* Write $FF to the Special I/O Control Register to enable the one's catcher for each bit.
* Enable the port by writing to the Master Configuration Register.
* Read the Port's Data Register and write this value to the Data Path Polarity register. This zeros the inputs to the one's catcher.
* Write $00 to the port's Data Register to zero the one's catcher.
* Clear any pending interrupts by writing to the port's Command/Status Register.
* Enable interrupts by writing to the port's Command/Status Register.
* Enable the CIO's interrupts by writing to the Master Interrupt Control Register.

  Interrupts will now occur when any of the input signals change state.

Interrupt Handler Routine

* Read the port's Interrupt Vector Register. Bits 3,2, and 1 of the data returned will tell which bit caused the interrupt.
* Read the Data Path Polarity Register and flip the bit that caused the interrupt. Write this new value back out to the Data Path Polarity Register. This zeros the input to the one's catcher and sets up the bit to interrupt on the opposite level.
* Write a "0", to the bit position that caused the interrupt, to the port's Data Register. This will clear the one's catcher.
* Clear the interrupt pending bit in the port's Command/Status Register.

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4.0 PRINCIPLES OF OPERATION

This chapter describes the circuitry of the Industrial Digital I/O Board. A block diagram of this board is shown in Figure 4.1. Schematics of the board are in chapter 7.

4.1 LCA PROGRAMMING

There are five Logic Cell Arrays (LCA) on the Industrial Digital I/O Board. The LCAs are RAM based programmable logic devices that must be programmed every time power is applied to the board. The programming for the LCAs is done automatically and begins when the SYSRESET* signal is negated after power is applied. The LCA programming takes approximately 20 mSec to complete. The EPROM (U49) contains 4 LCA programs. Bit 0 of the EPROM contains the VME Interface program which gets loaded into U38. Bits 1,2 and 3 contain the different configuration programs for the sections. The configuration program for the sections are selected by installing jumpers on J1,J2,J3 and J4 (See Chapter 2 section 5). The programming is controlled by U38 which supplies the clock and terminates the programming sequence upon completion. U33, U34, U47 and U48 form a 16 bit counter to supply the EPROM with the proper address. There are no means on the board to program the LCA's on the fly. If a new configuration is required for a section then the card must be turned off and then back on to program the LCA with the proper configuration.

4.2 VMEbus INTERFACE

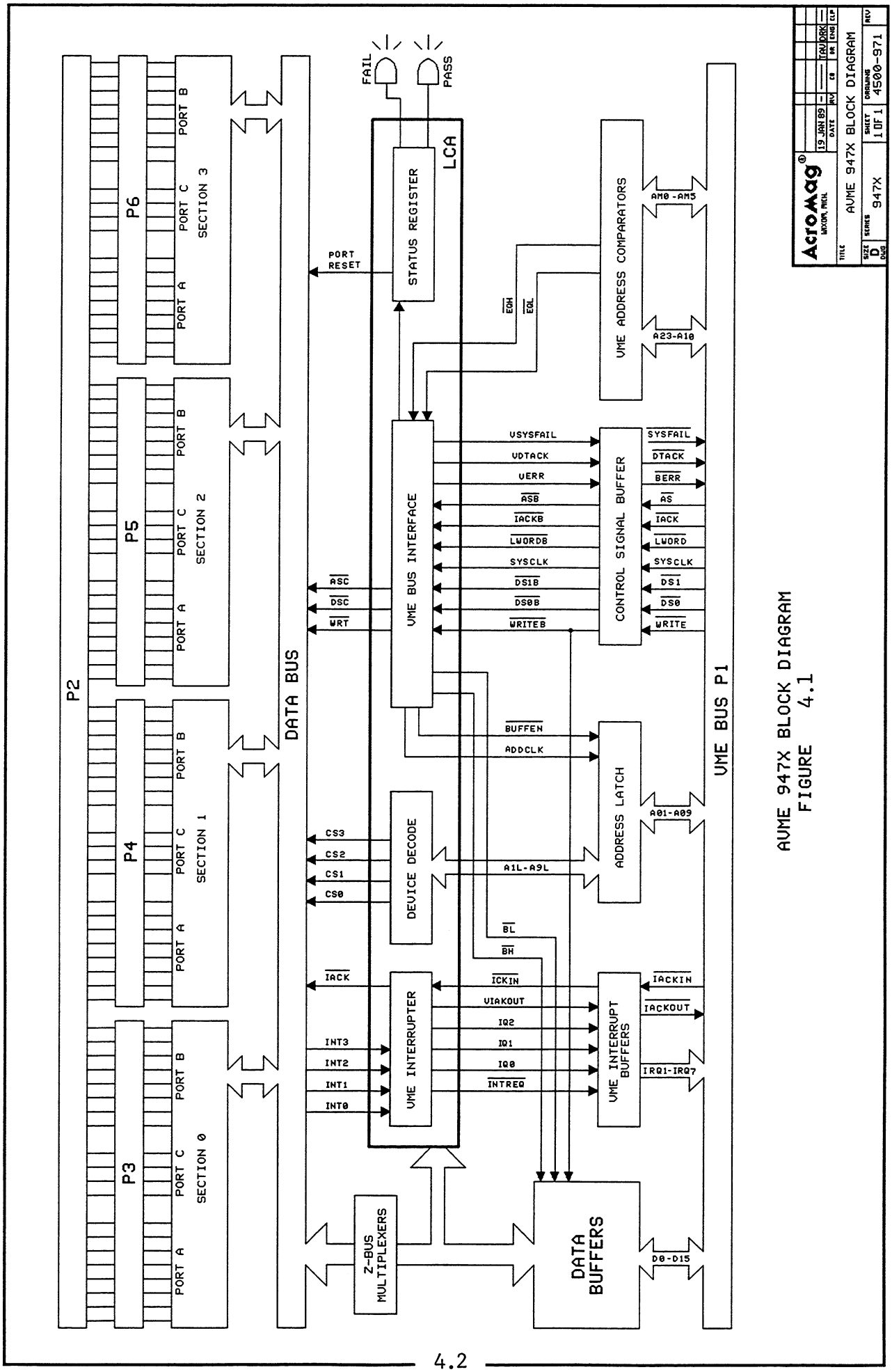
The VMEbus interface consists of three functional circuit areas:

- VMEbus Address, Data, Control and Interrupt Request Buffers.
- Board Controller
- Z-Bus Multiplexers

4.2.1 VMEbus Buffers

- Data Buffers are U57 and U58 (D15-D0).
- Address Comparators are U52 and U53 (A23-A10,AM5 and AM3).
- Address Latch is U50 (A1-A8).
- Address buffer is U54 (A9,AM0-AM2,AM4,LWORD*).
- Control buffer is U55 (SYSRESET*, SYSCLK, AS*, IACK*, WRITE*, DS1*, DS0* IACKIN*).
- Output buffer is U56 (DTACK*, BERR*, SYSFAIL*, IACKOUT*).
- Interrupt request buffer U51 (IRQ7*-IRQ1*).

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AVME 947X BLOCK DIAGRAM
FIGURE 4.1

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4.2.2 Board Controller

The Board Controller (U38) controls the VMEbus interface and creates a Z-Bus interface for the four Zilog Z8036 Counter/Timer and Parallel I/O Units (CIO) on the board. The following is a list of the functional logic blocks contained within U38 and a list of the inputs and outputs for each block.

Board Decode:

Inputs EQHI*, EQLO*, SP-BT, A16-A24, AM4B, AM2B-AM0B.

Device Decode:

Inputs A9, A8L-A1L, LWRD*, ICK*, DS1B*, DS0B*.
Outputs PROM*, CS3CB*, CS3C, CS2CB*, CS2C, CS1CB*, CS1C, CS0CB*, CS0C.

VMEbus Controller:

Inputs SYSRESET*, CLK16, DS1B*, DS0B*, WRT*, LWRDB*.
Outputs BEN*, ADDCLK*, BH*, BL*, VDTACK, VBERR.

Status/Control Register:

Inputs D7B-D0B
Outputs D7B-D0B, GRN*, RED*, VSYSFL.

Interrupt Control Register:

Inputs D7B-D0B
Outputs D7B-D0B, IQ2-IQ0.

CIO Z-Bus Interface:

Outputs ASC*, DSC*, ADD/DT*, CRDEN*, MUXEN*, CLK4.

Interrupter :

Inputs ASB*, ICKIN*, INT3*-INT0*.
Outputs VIACKOUT, INTREQ*, IACKSEL, INTACK*.

4.2.3 Z-Bus Multiplexers

The Z-bus uses a multiplexed address and data bus. U16, U26, U39, U40, U41, U42, U43 splits and combines the three busses. D15B-D0B, A6L-A1L, AD15-AD0.

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4.3 I/O SECTIONS

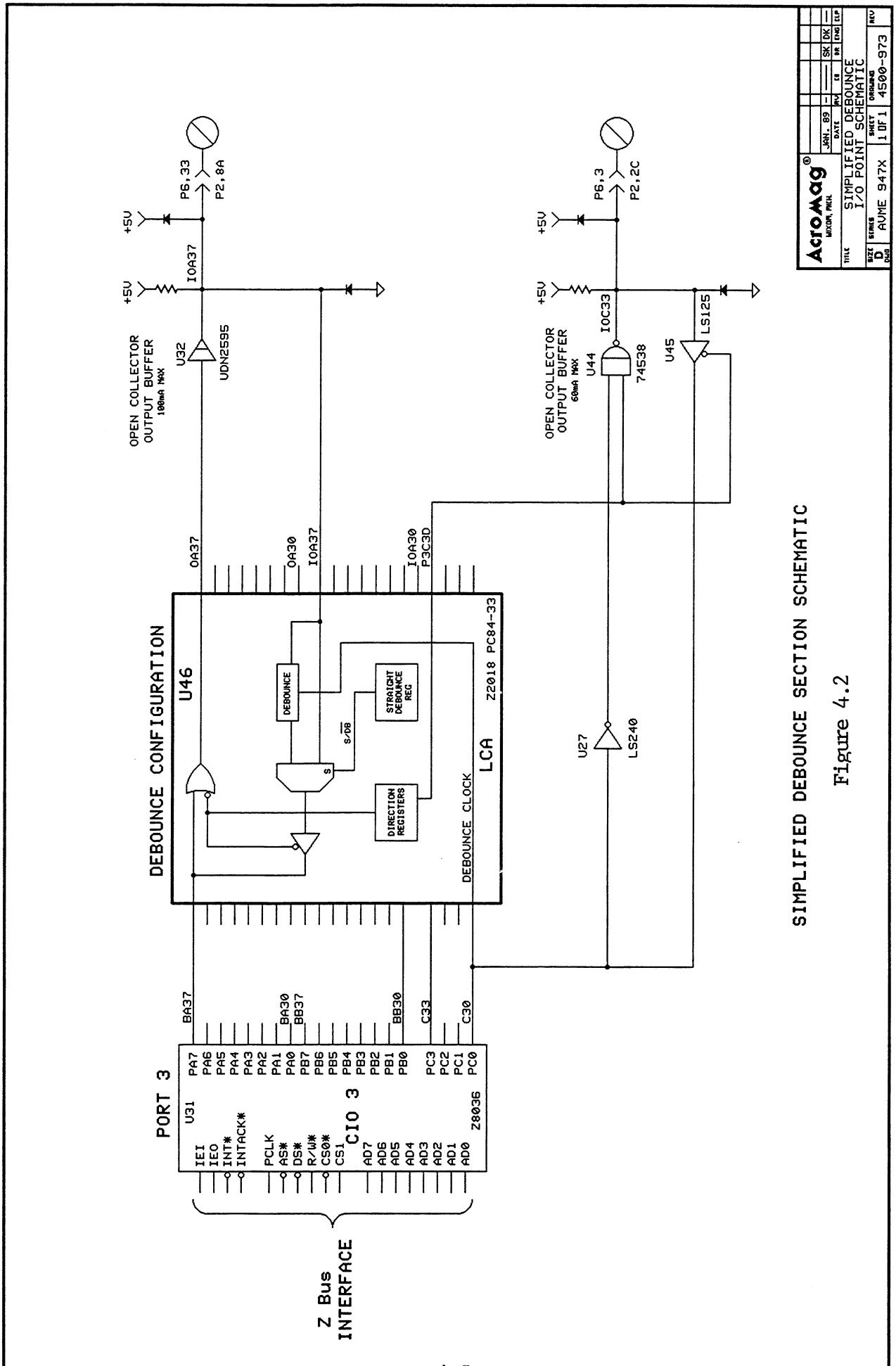
There are four sections on the Industrial Digital I/O Board consisting of a CIO, a LCA and the I/O buffers. Essentially all the board does is provide a VMEbus interface for the CIOs and then buffer the ports for protection and drive capabilities. Refer to the Simplified Section Schematics Figures 4.2 and 4.3. Appendix Z gives a detailed discussion of the operation of the CIOs. The operation of the LCAs is transparent to the user, in that when writing to the CIO you also write to the LCA.

4.4 INTERRUPTS

Only the CIOs within the sections can cause interrupts. Ports A and B and the three Counter/Timers may originate an interrupt request. The four CIOs are connected in an interrupt daisy chain to prevent more than one CIO from suppling a vector during an interrupt acknowledge cycle. The interrupt priority daisy chain establishes Section 3 with the highest priority, and with Section 0 the lowest priority, on Models AVME9470 and AVME9471. Whenever a higher priority section requests an interrupt it automatically shuts off the lower priority interrupt requests. During an interrupt acknowledge cycle all interrupt requests are frozen until the end of the cycle.

NOTE: Models AVME9472 and AVME9473 have two sections available. Section 1 has highest priority and section 0 has lowest priority. Model AVME9475, has two sections available. Section 3 has highest priority and section 2 has lowest priority.

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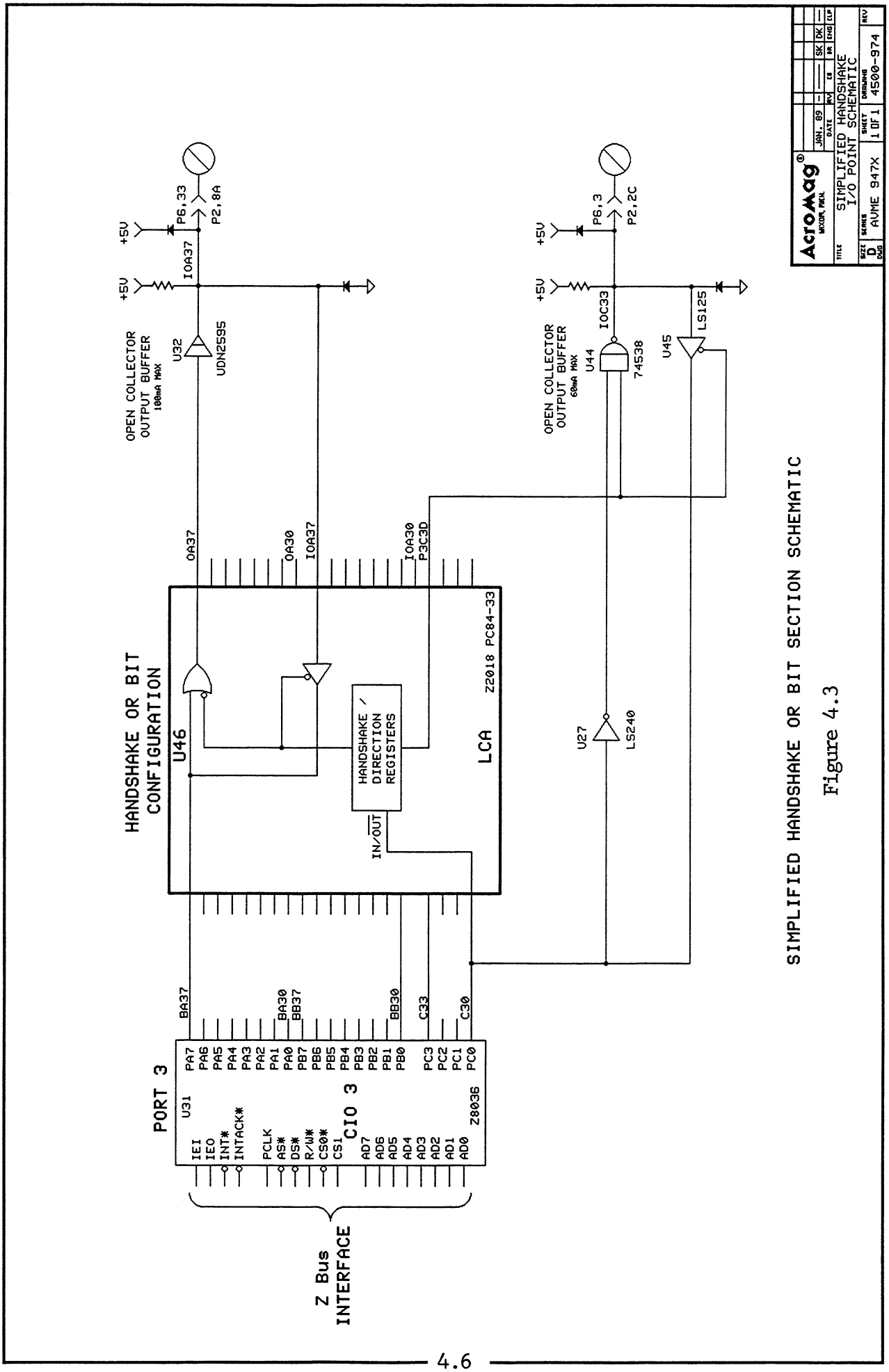


Figure 4.3

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5.0 SERVICE AND REPAIR INFORMATION

This section provides calibration procedures, service diagrams and instructions on how to obtain service and repair assistance.

5.1 SERVICE AND REPAIR ASSISTANCE

It is highly recommended that a non-functioning board be returned to Acromag for repair. Acromag uses tested and burned-in parts, and in some cases, parts that have been selected for characteriestics beyond that specified by the manufacturer. Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any reqair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

5.2 PRELIMINARY SERVICE PROCEDURE

Before beginning calibration or repair, be sure that all of the procedures in Chapter 2, Preparation For Use, have been followed. The procedures are necessary since the board has jumpers that must be properly configured.

NOTE: It has been observed that on occasion a "boot" program for a disk operating system will "hang" waiting for the VMEbus SYSFAIL* signal to be released by an intelligent disk controller board. Acromag's non-intelligent slave boards assert the SYSFAIL* signal as described by the VMEbus Specification Rev. C.1 and therefore, the disk operating system will remain "hung". The best solution to this problem is to correct the boot program so that it is no longer dependent upon the SYSFAIL* signal. When this solution is not practical, it is possible to disconnect the SYSFAIL* from the circuitry on the Acromag board by cutting a PC board foil between the two pads for J8. Caution should be exercised so as not to cut any other foils nor to damage the board in any other way. Call Acromag's Applications Engineering Department for assistance.

5.3 CALIBRATION PROCEDURE

Due to the digital nature of the AVME947X, no maintenance or calibration is required during normal operation of the board.

5.4 REPLACEABLE PARTS

The Replaceable Parts List (Table 5.1) is provided as an aid to the user in troubleshooting the Board. Replacement parts and repair services are available from Acromag. If repair is deemed necessary in this circuitry, it is highly recommended that the Board be returned to Acromag for repair and recalibration.

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Changes are sometimes made to improve the product, to facilitate delivery, or to control cost. It is therefore important to include the Reference Number, the Acromag Part Number, the Board Model Number, and the Board Serial Number when providing information to order parts.

Table 5.1 Replaceable Parts

REFERENCE NO.	ACROMAG PART NO.	DESCRIPTION
U2,4,7,9,12,14 U29,32	1033-735	UDN2595A
U5,10,15,31	1033-736	Z0803606
U16,39,40,41,42,43	1033-278	SN74LS257AND
U17,20,23,44	1033-739	SN74S38N
U18,21,24,45	1033-734	74LS125A
U19,22,25,38,46	1033-715	XC20118PLC84-33
U26,54,55	1033-273	SN74LS244ND
U33,34,47,48	1033-285	74LS161
U27,35	1033-272	SN74LS240ND
U36	1033-622	74F00
U37	5016-698 - 5016-702	32X8 3S
U49	5016-696/5016-697	AT27C256-15-DC
U50	1033-283	SN74LS373ND
U51	1033-048	SN7445N
U52,53	1033-626	AM25LS2521PCB
U56	1033-623	N74F38N
U57,58	1033-627	SN74LS645-1ND
R1,2,5,6,7,8,9,10	1100-490	RES NETWORK 9 1000 OHM
R14	1100-266	RES NETWORK 5 4700 OHM
R3,4,11,12	1100-263	RES NETWORK 5 2200 OHM
R13,15	1100-490	RES NETWORK 9 1K
R16	1000-825	RES 330 OHM
C1-29	1002-530	CAP MONO 0.1UF
C30	1002-320	CAP TAN 1 UF
D1,3,5,7,9,11,15 D17,20,22	1001-168	DIODE NETWORK DAP801
D2,4,6,8,10,12,16 D18,19,21	1001-190	DIODE NETWORK DAN801
F1	1030-496	FUSE 2 AMP.
P1,2	1004-505	CONN. EDGE 96 MALE RT
P3,5	1004-592	CONN. TWO 50 POS

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6.0 DIGITAL I/O BOARD SPECIFICATIONS

The following specifications are given for 25°C ambient temperature and nominal power supply values unless otherwise noted.

GENERAL INFORMATION

Operating Temperature	0° to 70° C
Storage Temperature	-25° to +85° C
Humidity	90% max. non-condensing
Physical Characteristics	
Configuration	NEXP (non-expanded bus, double VME board)
Length	233.35 mm (9.187 in)
Width	160 mm (6.299 in)
Board Thickness	1.5875 mm (0.0625 in)
Warpage, Component Height and Lead Length	See Rule 7-14 and 7-15 in VME spec.
Board Spacing	20.32 mm (0.8 in)
Mating Connectors	
VMEbus	96 contacts, 603-2-IEC-C096-F
Front Panel	200 contacts, (4) 50 contact connectors
P2	96 contacts, 603-2-IEC-C096-F
Power Requirements	
+5 Volts +0.25/-0.125	1.3 Amps typical
+12 Volts	no load
-12 Volts	no load
Digital Input/Output	
Points per Board	80 or 40
Input Voltage Range	0 to 5V DC
Input Threshold (L to H)	2.0V DC minimum
(H to L)	0.8V DC maximum
Input Current	5uA
Output type	Open collector with pull up resistor.
Output Voltage Range	0 to 5V DC
Output Current Sink	100mA max., Ports A and B (See Note 1).
Output Saturation	0.5V max., 0.4 typ. Voltage @ 100mA
Output Current Sink	60mA max., Ports C (See Note 2).
Output Saturation	0.5V max. Voltage @ 60mA
Logic Compatibility	TTL, LSTTL, CMOS
VMEbus INTERFACE	
Data Transfer Mode	A24/A16 D16/D08(EO), D08(O) ROAK Interrupter
Bus Loading	Refer to VMEbus Spec, Section 7.5
Bus Drive	Refer to VMEbus Spec, Appendix E and Section 7.4
VMEbus Access Time (approx.) (measured from falling edge of DSx* to the falling edge of DTACK*)	
Board & Section status register	1500nS
I/O Ports (all sections)	1500nS

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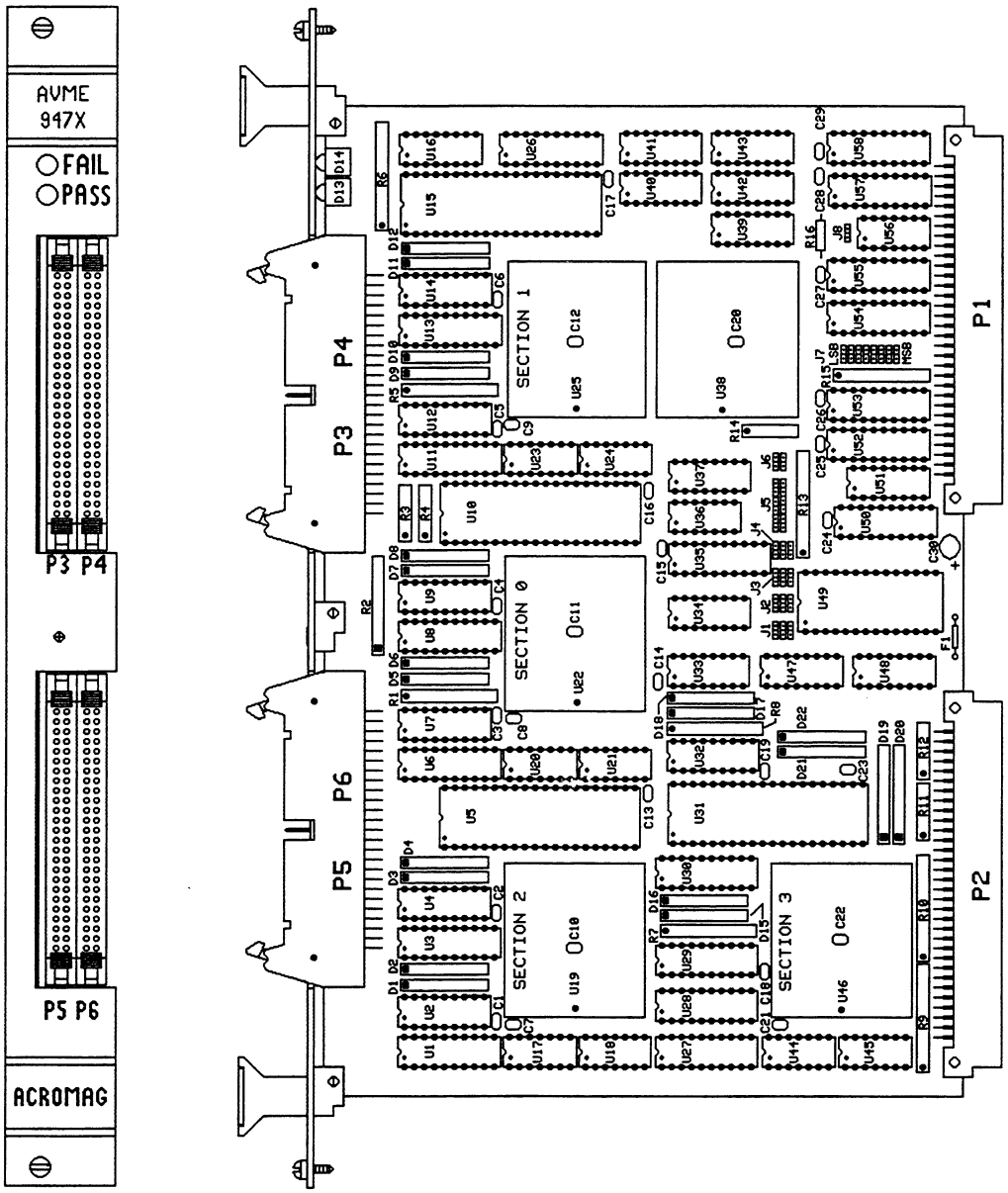
Counter/Timer	
Frequency Output	100 KHz maximum (See Notes 1 and 2) with internal pullup resistors. 15.26 Hz minimum, 333 KHz maximum (See Notes 1 and 2) with external pullup resistors.
One Shot Output	32mS maximum. 500nS minimum (See Notes 1 and 2).
Frequency Input	3.3 MHz maximum 170nS min. Pulse width
Debounce Delay	0.2 S maximum. 3uS minimum.

NOTES:

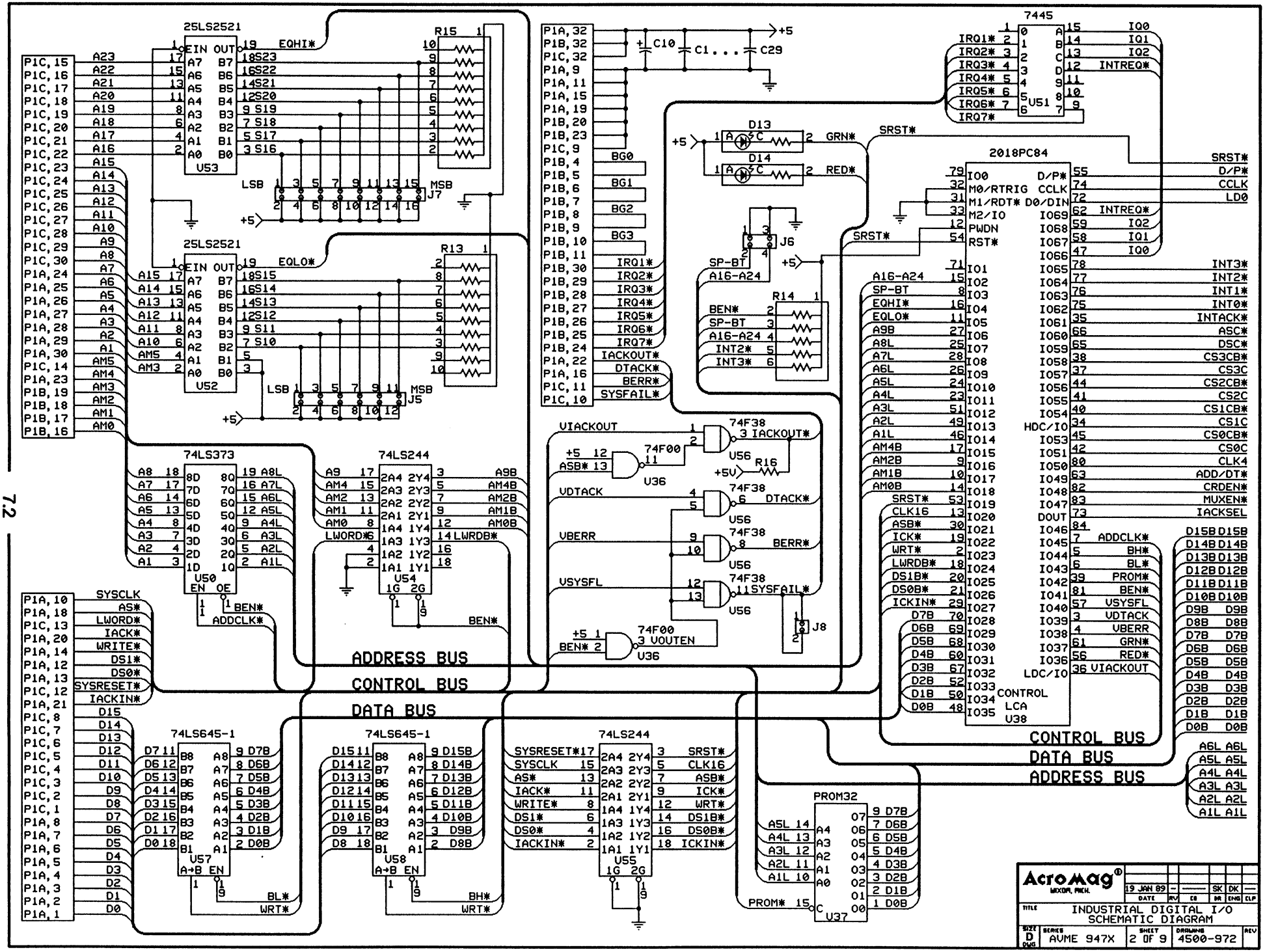
1. The output response time on Ports A and B is limited by the high current output drivers. The response time is 5uS., typical (output low to high) and 0.5uS., typical (output high to low).

2. The output response time on Port C is much faster than Ports A and B. The response time is 500nS., typical (output low to high) and 100nS., typical (output high to low).

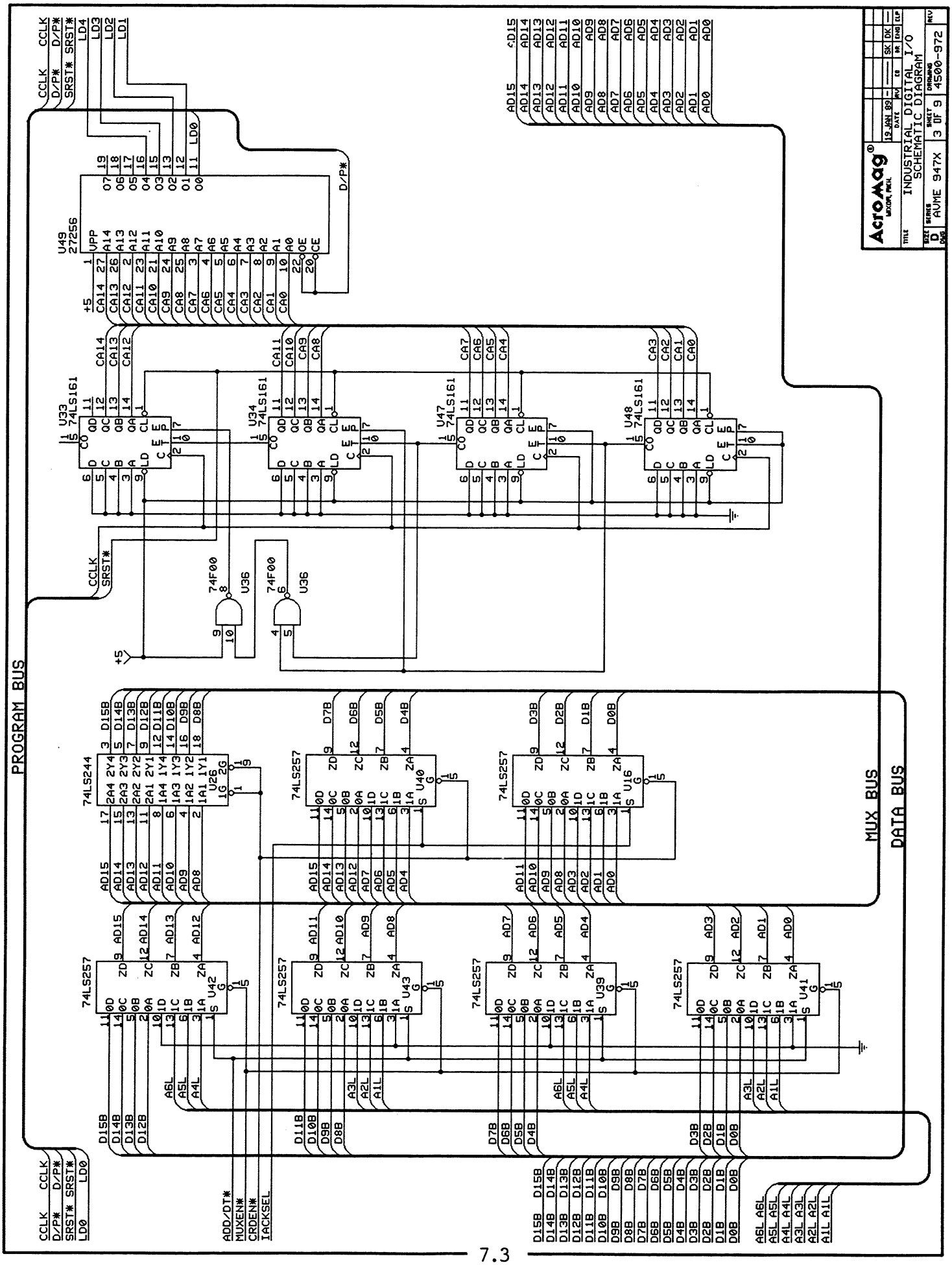
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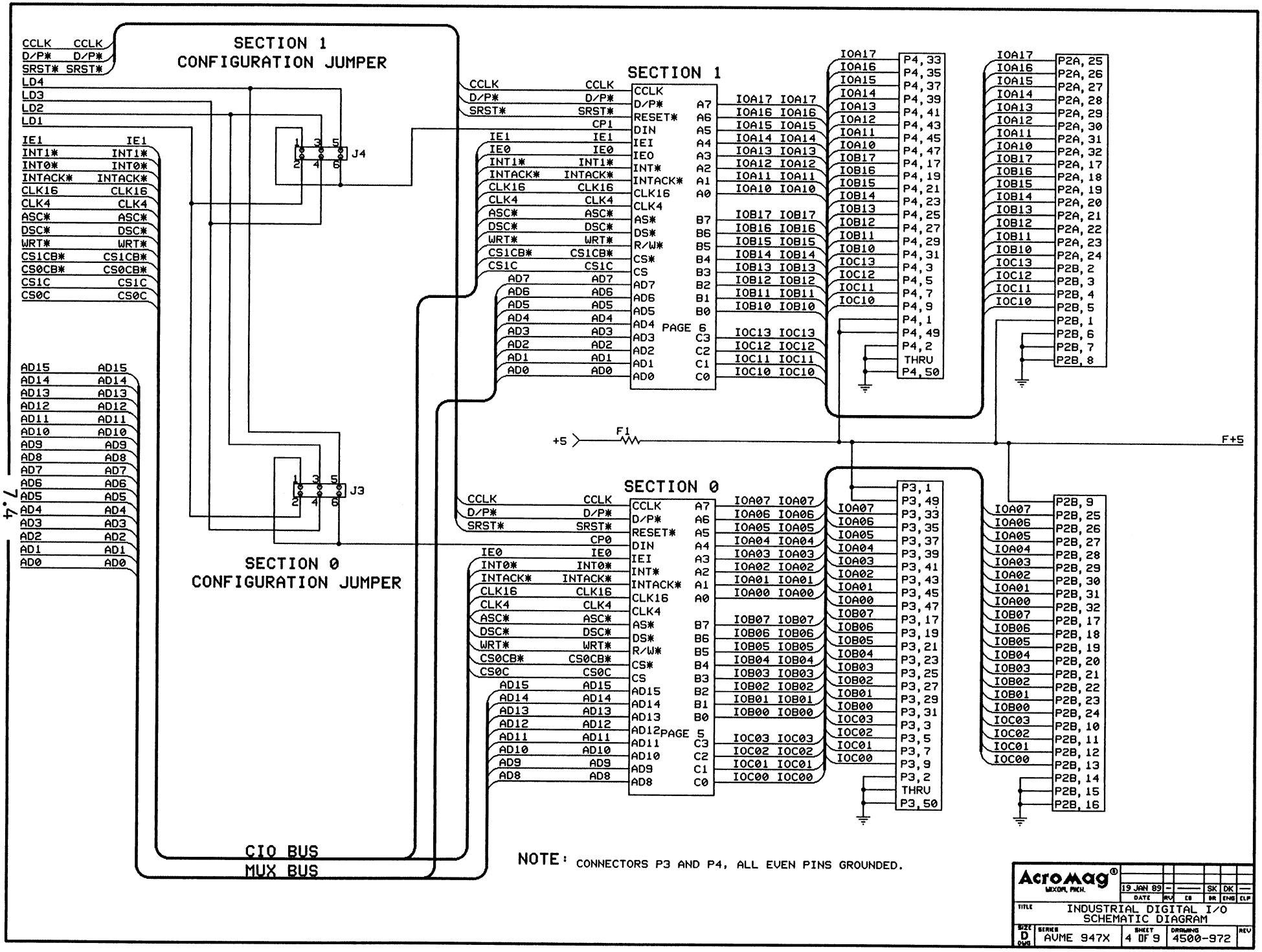
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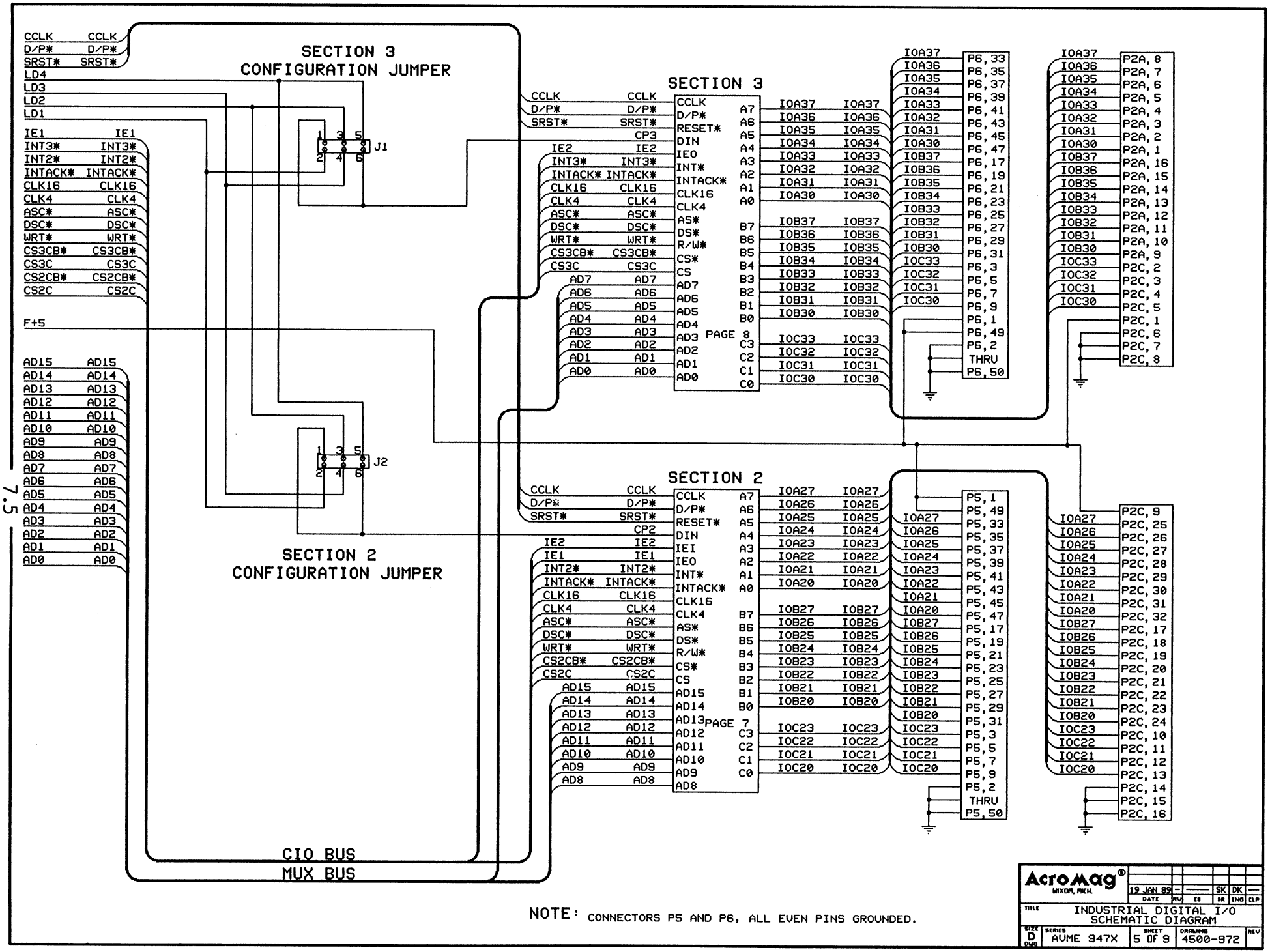
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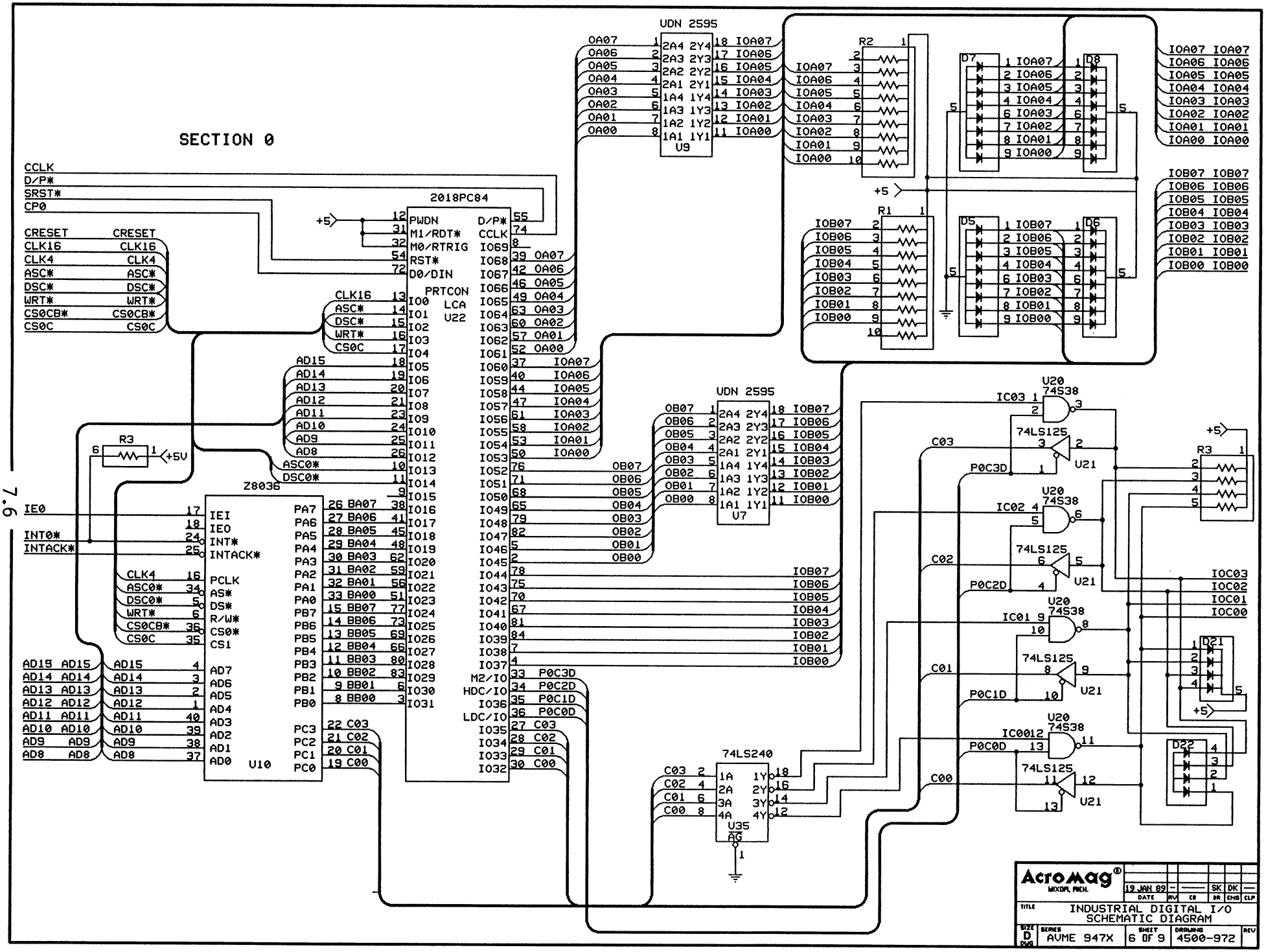


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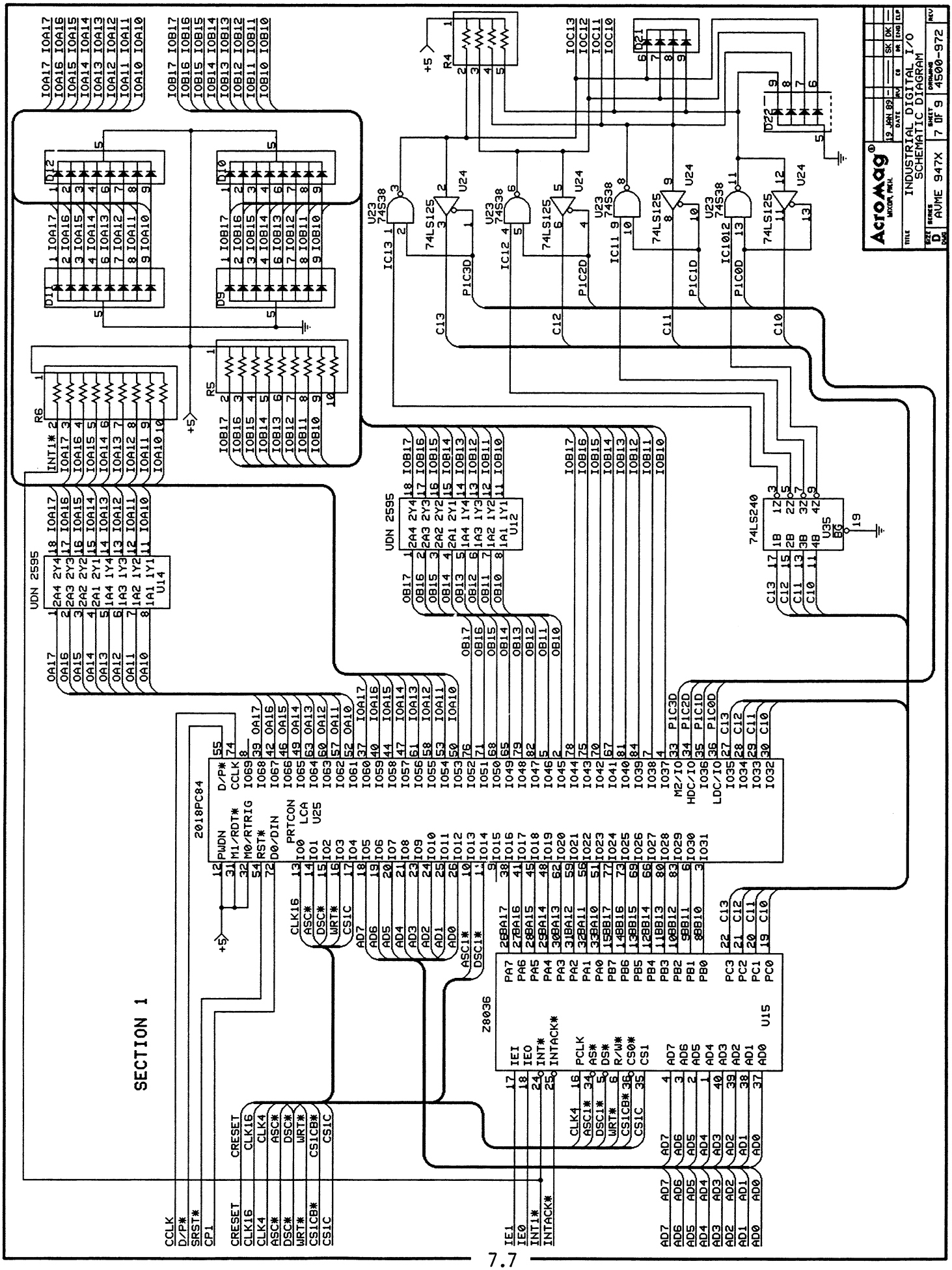


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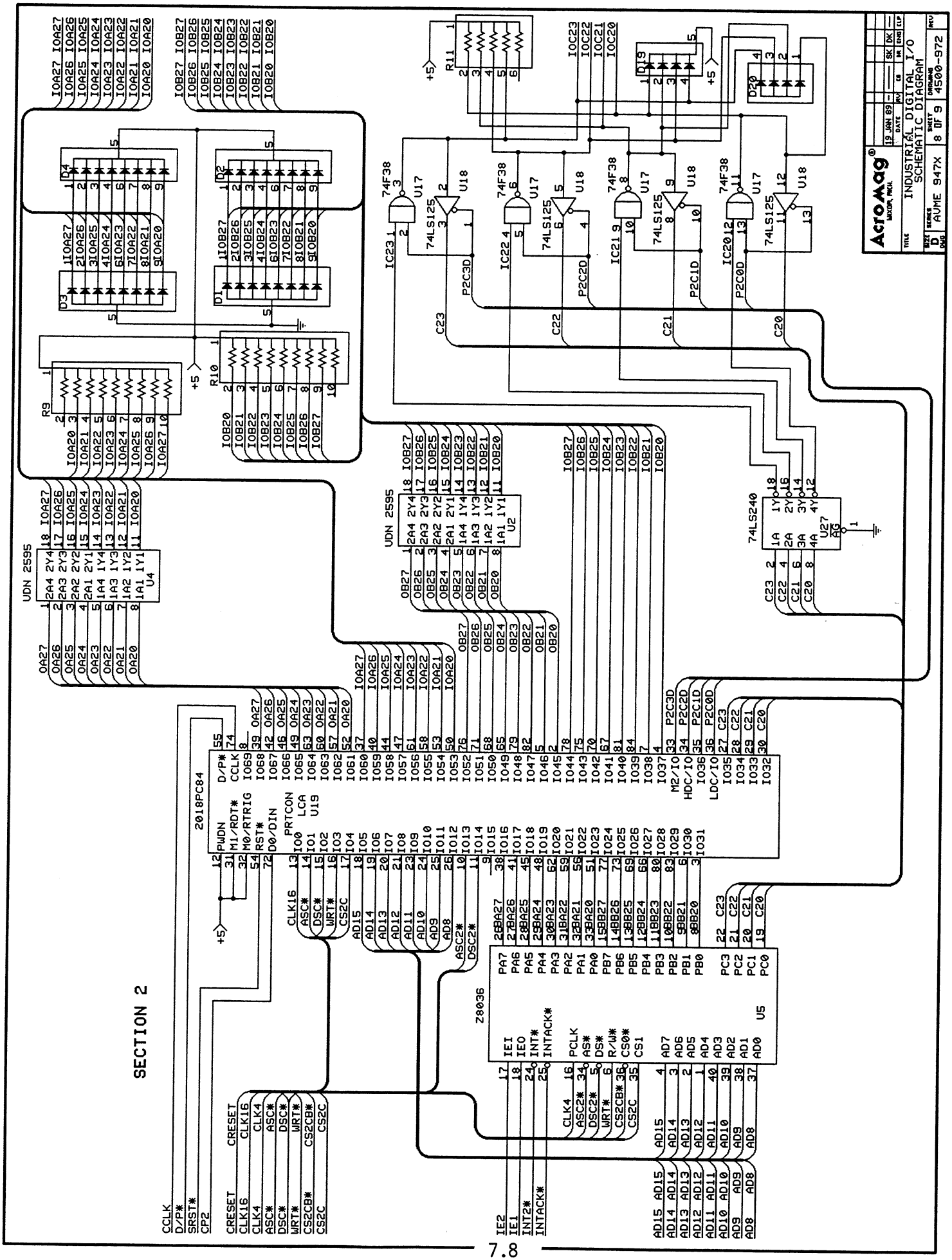
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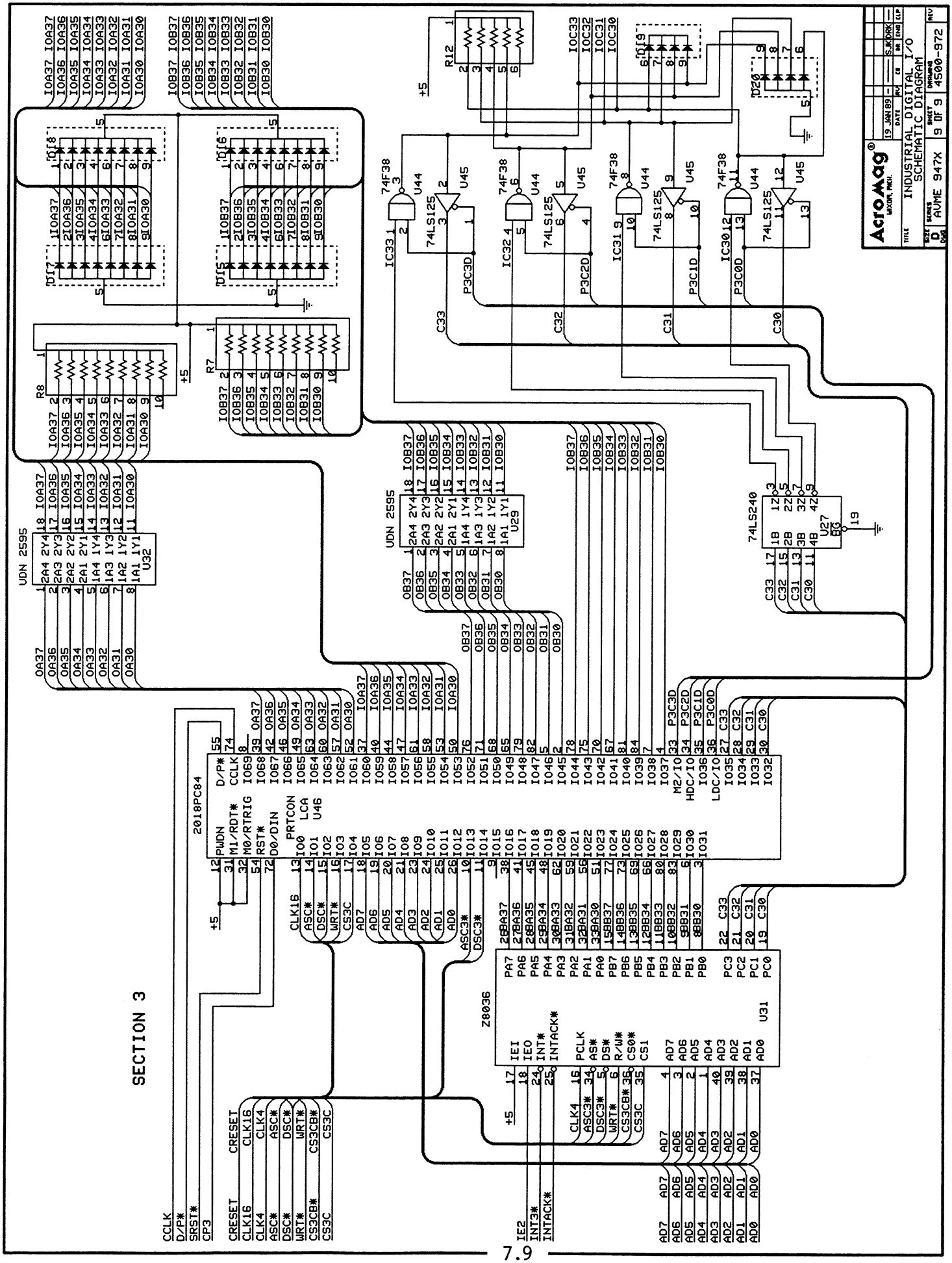
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A.1 USE WITH SOLID STATE RELAYS

The AVME 947X Digital I/O Board may interface with industry standard solid state relays and termination panels PB16A, PB24 and their equivalents.

Table A.1 lists the PB16A Module Number Bit Positioning for the I/O port registers. Table A.2 lists the PB24 Module Number Bit Position for the I/O port registers.

TABLE A.1 PB16A Module Number Bit Positioning

I/O Port Number	Module Number 7	6	5	4	3	2	1	0	PB16A connected to
SECTION 0									
A	7	6	5	4	3	2	1	0	P3
B	15	14	13	12	11	10	9	8	P3
SECTION 1									
A	7	6	5	4	3	2	1	0	P4
B	15	14	13	12	11	10	9	8	P4
SECTION 2									
A	7	6	5	4	3	2	1	0	P5
B	15	14	13	12	11	10	9	8	P5
SECTION 3									
A	7	6	5	4	3	2	1	0	P6
B	15	14	13	12	11	10	9	8	P6

For bit positions corresponding to output modules, a 0 state will turn the I/O point on and the output will sink current. A 1 state will turn the module off. For bit positions corresponding to input modules, a 0 state indicates the presence of a low voltage for the "on" state of the module. A 1 state indicates a high voltage present.

A.1.1 Configuring The PB16A

If the PB16A is to get power from the AVME947X, install a jumper at pin 1 or pin 49 on the PB16A termination panel. Install appropriate solid state relay modules. Connect the 50 Pin ribbon cable between PB16A and the AVME947X observing the pin 1 index mark.

A.1.2 Configuring The PB24

Install appropriate solid state relay modules. Connect the 50 pin ribbon cable between PB24 and the AVME947X observing the pin 1 index mark.

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A.2 USE WITH OTHER DEVICES

The AVME947X Digital Boards can interface with a variety of discrete devices such as relays, switches, contact closures, and indicators. Optional termination panel 6980-16U can be used to connect field wiring to the digital I/O card. The following guidelines should be followed to insure proper interfacing.

A.2.1 Relays And Other Inductive Loads

When driving relays coils or other inductive loads. Each load will need its own external diode. See figure A.1 Relay Driver and Input Configurations, for relay driver configurations.

A.2.2 Contact Closures And Switches

When sensing contact closures that already are connected to a voltage source the input voltage should be within the range listed in Specifications, Section 6. For isolated or grounded contacts the pull-ups and the +5 volt supply can be used to establish an input voltage. See figure A.2 Relay Driver and Input Configurations, for various input configurations.

TABLE A.2 PB24 Module Number Bit Positioning

I/O Port Number	Module Number 7 6 5 4 3 2 1 0	PB24 connected to
SECTION 0		
A	7 6 5 4 3 2 1 0	P3
B	15 14 13 12 11 10 9 8	P3
C	22 21 20 19	P3
SECTION 1		
A	7 6 5 4 3 2 1 0	P4
B	15 14 13 12 11 10 9 8	P4
C	22 21 20 19	P4
SECTION 2		
A	7 6 5 4 3 2 1 0	P5
B	15 14 13 12 11 10 9 8	P5
C	22 21 20 19	P5
SECTION 3		
A	7 6 5 4 3 2 1 0	P6
B	15 14 13 12 11 10 9 8	P6
C	22 21 20 19	P6

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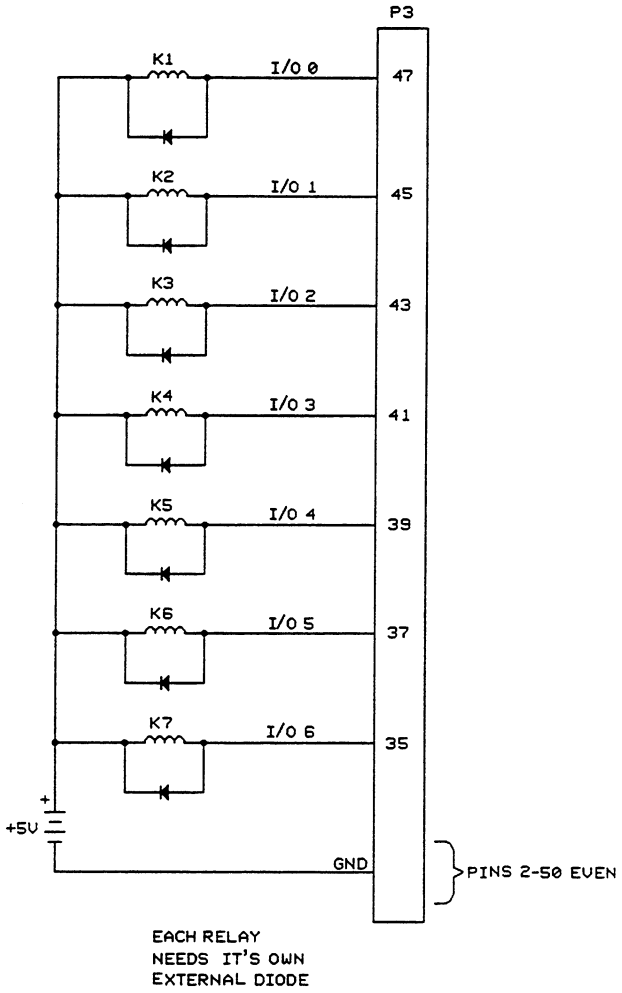


FIGURE A.1: RELAY DRIVER CONFIGURATIONS

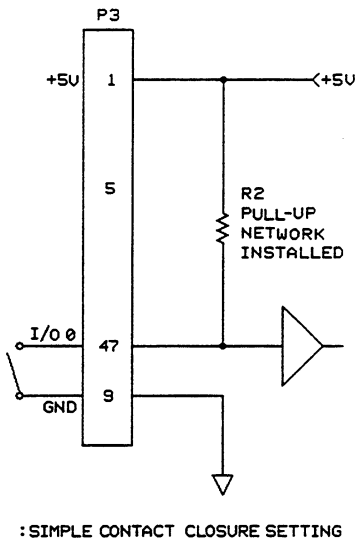


FIGURE A.2 : INPUT CONFIGURATIONS

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B.1 IEEE-488 (GPIB) Interface

The AVME947X can be used as a GPIB bus controller. One individual GPIB bus may be connected to each of the sections, allowing up to fifteen instruments to be controlled from that section. One or all four sections may be used as GPIB bus controllers to control up to a maximum of 60 instruments from one board. The GPIB bus controller is compatible with the ANSI/IEEE 488.1-1987 Standard. The GPIB bus controller has the following attributes:

- SH1 Complete Source Handshake capability.
- AH1 Complete Acceptor Handshake capability.
- T1 Basic Talker with Serial Poll and Talk only modes.
- TE1 Basic Extended Talker with Serial Poll and Talk only modes.
- L2 Basic Listener.
- LE2 Basic Extended Listener.
- SR0 No Service Request capabilities.
- RL0 Remote operation only, no Local capabilities.
- PP0 No Parallel Poll message capabilities.
- DC0 No Device Clear capabilities.
- DT0 No Device Trigger capabilities.
- C26 System Controller, no other controllers allowed. Has the ability to send Interface Clear (IFC), Remote Enable (REN), Interface (I.F.) messages, respond to a Service Request (SRQ), and conduct a Parallel Poll.
- E1 Open collector drivers.

B.1.1 IEEE-488 (GPIB) Setup

The following list is the setup procedure to configure a section to operate in the GPIB bus controller mode:

1. Address the board according to section 2.4 of this manual.

2. Select the section to be used as the GPIB controller. See Table B.1 below.

3. Configure the section for the Bit Configuration by shorting pins 1 & 3 of the jumper for the section selected. See Table B.1 below.

4. Install the resistor networks, shipped with the GPIB bus interface cable, in the IC positions listed in Table B.1. The resistor networds are to be installed in the sockets without any regard to orientation. There is not a wrong way to install the resistor packs.

5. Install the board in the card cage and connect the GPIB cable to the proper connector listed in Table B.1.

6. Power up the card cage and install the driver software per the instructions listed in the INFOGPIB.TXT file found in the GPIB947X directory or level. It is recommended that the user experiment with the GPIB bus and the instruments connected to it using the GPIB Demo program. There is a variable in the GPIB9470.H

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file called GPIB_TIME_OUT that is used to limit how long the software will wait for a response from the instruments on the bus. This may be adjusted by the user to accommodate the speed of the instruments connected to the GPIB bus. Also in the GPIB9470.H file is a variable called CONTROLLER_ADDR which is the GPIB bus address of the AVME947X controller. This may also be changed by the user.

Table B.1 Section Reference Table

Section	Front Panel Connector	9921-16 Connector	Jumper	Resistor Pack Locations
0	P3	P1	J3 pins 1 & 3	socket side of U6, U8
1	P4	P2	J4 pins 1 & 3	socket side of U11, U13
2	P5	P3	J2 pins 1 & 3	socket side of U1, U3
3	P6	P4	J1 pins 1 & 3	socket side of U28, U30

B.1.2 IEEE-488 (GPIB) Cable

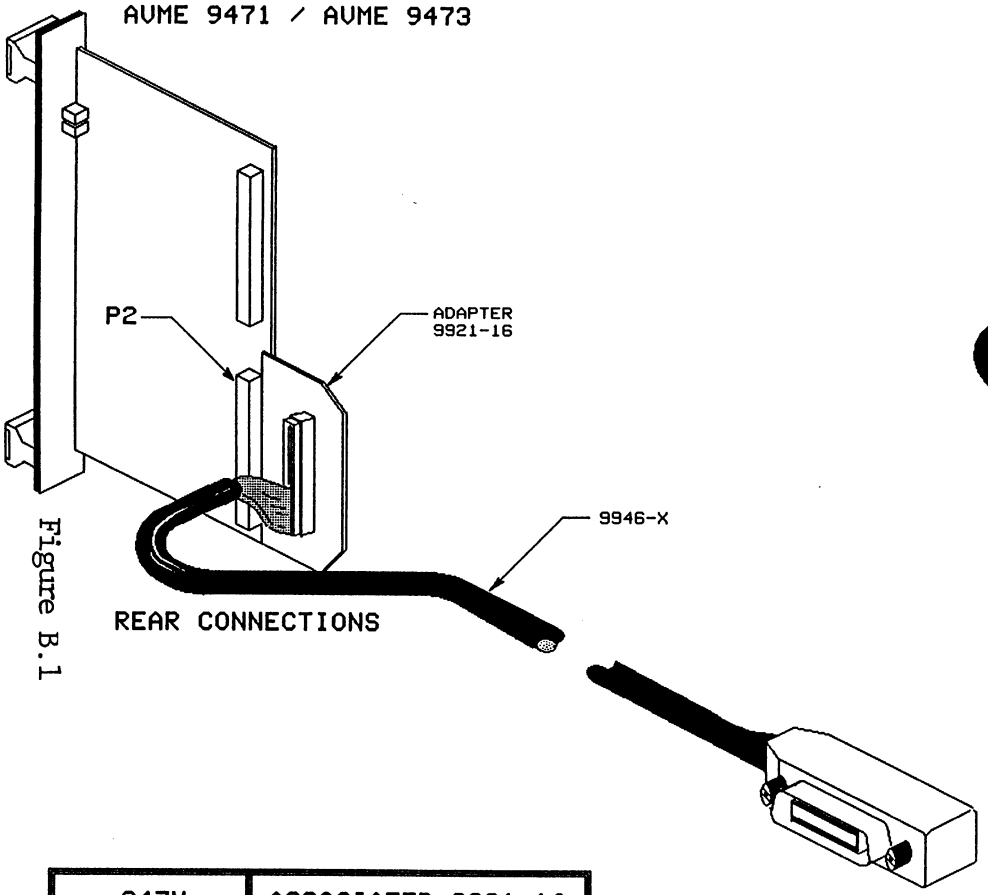
On models AVME9470 and AVME9472 the IEEE-488 (GPIB) interface is accessible through the two or four 50 pin ribbon cable connectors located on the front panel. Connect the GPIB cable (9946-X) to P3,P4,P5 or P6. Refer to the AVME947X GPIB Interface Connections drawing Figure B.1.

On models AVME9471/9473/9475 the IEEE-488 (GPIB) interface is accessible through the P2 96 pin connector. The 9921-16 adapter board is used to separate the individual sections to the four 50 pin ribbon cable connectors. Connect the GPIB cable (9946-X) to P3,P4,P5 or P6. Refer to the AVME947X GPIB Interface Connections drawing Figure B.1.

The schematic for the GPIB interface cable is shown in Figure B.2.

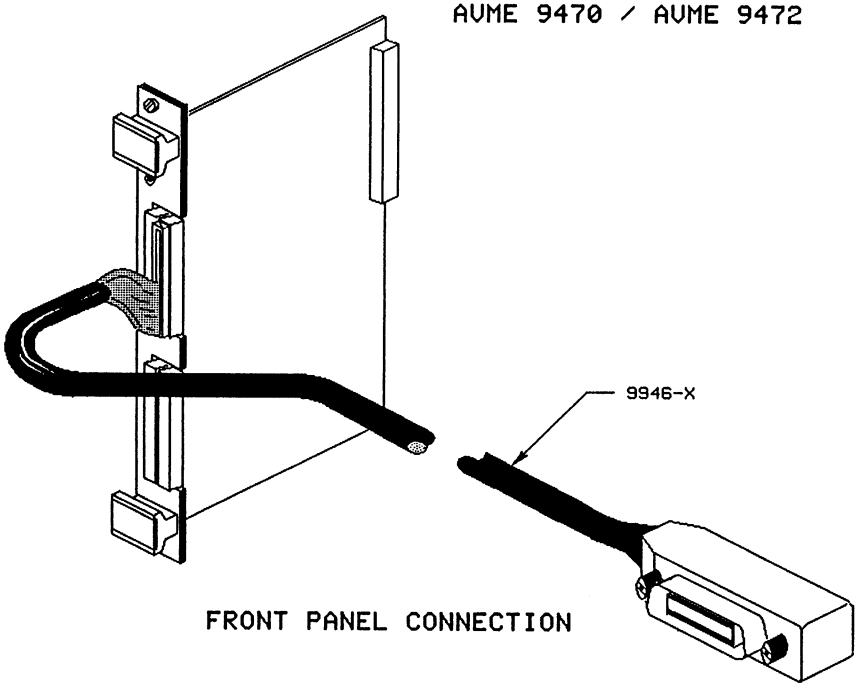
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AVME 9471 / AVME 9473



REAR CONNECTIONS

AVME 9470 / AVME 9472



FRONT PANEL CONNECTION

Figure B.1

947X SECTION	ASSOCIATED 9921-16 ADAPTER CONNECTION
0	P1
1	P2
2	P3
3	P4

947X SECTION	ASSOCIATED FRONT PANEL CONNECTOR
0	P3
1	P4
2	P5
3	P6

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DATE	REV	CO	DR	ENG	ELP
20 DEC. 89	–	——	SJK	DRK	—

TITLE: AVME 947X GPIB INTERFACE CONNECTIONS

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	9946-X	1 OF 1	4500-996	

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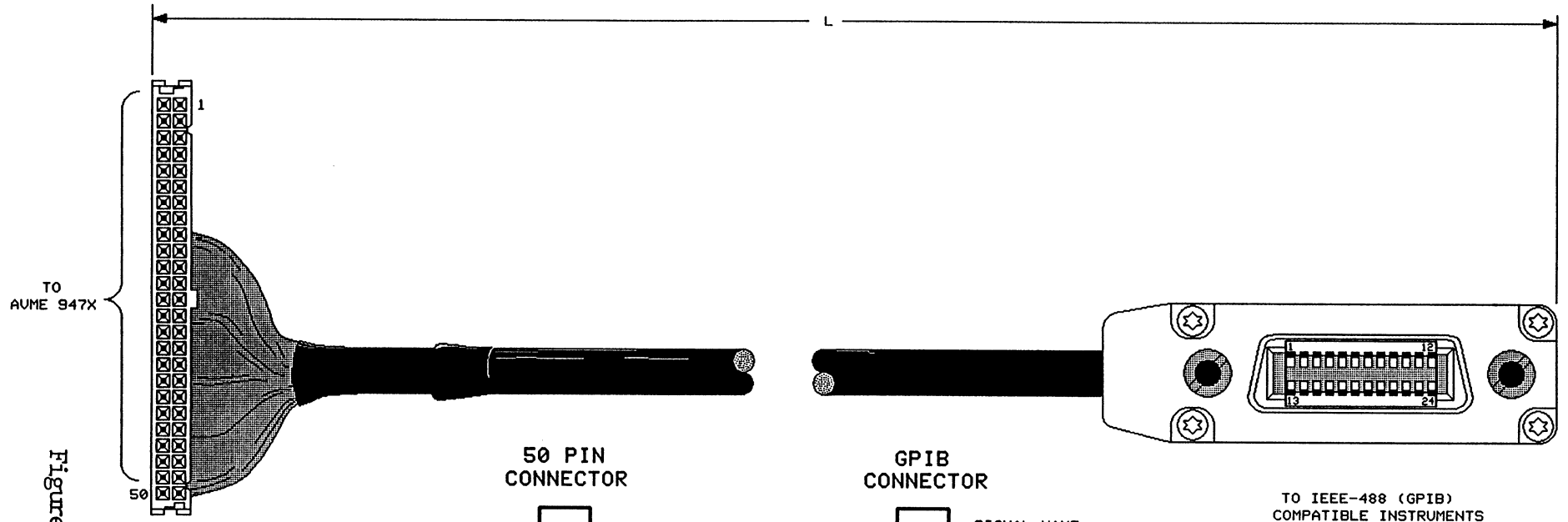


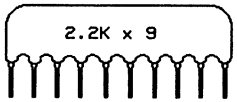
Figure B.2

TO IEEE-488 (GPIB)
COMPATIBLE INSTRUMENTS

50 PIN CONNECTOR			GPIB CONNECTOR	SIGNAL NAME
DATA BUS	A/7	33	16	DIO8
	A/6	35	15	DIO7
	A/5	37	14	DIO6
	A/4	39	13	DIO5
	A/3	41	4	DIO4
	A/2	43	3	DIO3
	A/1	45	2	DIO2
	A/0	47	1	DIO1
HANDSHAKE BUS	B/7	17	6	DAV
		18	18	DAV GND
	B/6	19	7	NRFD
		20	19	NRFD GND
	B/5	21	8	NDAC
		22	20	NDAC GND
INTERFACE MANAGEMENT BUS	B/4	23	9	IFC
		24	21	IFC GND
	B/3	25	10	SRQ
		26	22	SRQ GND
	B/2	27	11	ATN
		28	23	ATN GND
	B/1	29	5	EOI
	B/0	31	17	REN
		50	24	LOGIC GND
			12	SHIELD

ALL EVEN PINS
(2 THROUGH 50)
ARE GROUND.

CABLE SHIPPED
WITH TWO
RESISTOR NETWORKS
ACROMAG PART NUMBER
1100-265



MODEL	L
9946-3	3 FT.
9946-10	10 FT.

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TITLE: AVME 947X GPIB CABLE

SIZE D DWG | SERIES 9946-X | SHEET 1 OF 1 | DRAWING 4500-995 | REV

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C.1 Centronics Compatible Parallel Printer Interface

The AVME947X can be interfaced to a parallel printer. One printer may be driven by each of the four sections on the board. The parallel printer interface and connecting cable are Centronics compatible.

C.1.1 Parallel Printer Interface Setup

The following list is the setup procedure to configure a section to operate a parallel printer:

1. Address the board according to section 2.4 of this manual.

2. Select the section to be used as the Printer Interface. See Table C.1 below.

3. Configure the section for the Handshake Configuration by shorting pins 4 & 6 of the jumper for the section selected. See Table C.1 below.

4. Install the board in the card cage and connect the Printer Interface cable to the proper connector listed in Table C.1.

5. Power up the card cage and install the driver software per the instructions listed in the INFOPRNT.TXT file found in the PRNT947X directory or level.

Table C.1 Section Reference Table

Section	Front Panel Connector	9921-16 Connector	Jumper
0	P3	P1	J3 pins 4 & 6
1	P4	P2	J4 pins 4 & 6
2	P5	P3	J2 pins 4 & 6
3	P6	P4	J1 pins 4 & 6

C.1.2 Centronics Compatible Parallel Printer Interface Cable

On models AVME9470 and AVME9472 the printer interface is accessible through the two or four 50 pin ribbon cable connectors located on the front panel. Connect the Printer cable (9947-X) to P3,P4,P5 or P6. Refer to the AVME947X Printer Interface Connections drawing Figure C.1.

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On models AVME9471/9473/9475 the printer interface is accessible through the P2, 96 pin connector. The 9921-16 adapter board is used to separate the individual sections to the four 50 pin ribbon cable connectors. Connect the printer cable (9947-X) to P3,P4,P5 or P6. Refer to the AVME947X Printer Interface Connections drawing Figure C.1.

The schematic for the printer interface cable is shown in Figure C.2.

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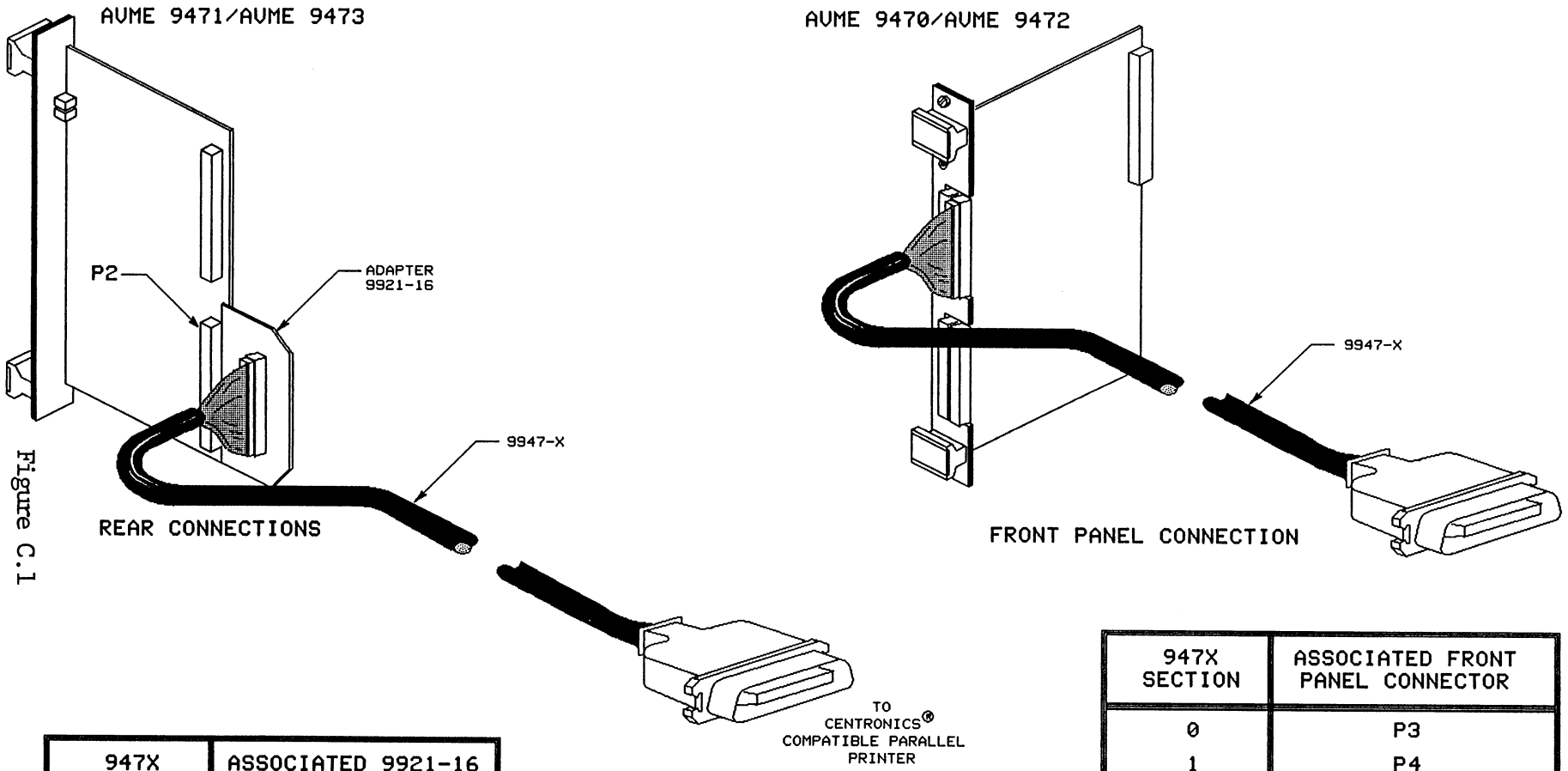


Figure C.1

947X SECTION	ASSOCIATED 9921-16 ADAPTER CONNECTION
0	P1
1	P2
2	P3
3	P4

947X SECTION	ASSOCIATED FRONT PANEL CONNECTOR
0	P3
1	P4
2	P5
3	P6

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DATE	AV	EO	DR	ENG	ELP
20DEC.89	-	———	SJK	DRK	—

TITLE: AVME 947X PRINTER INTERFACE CONNECTIONS

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	9947-X	1 OF 1	4500-997	

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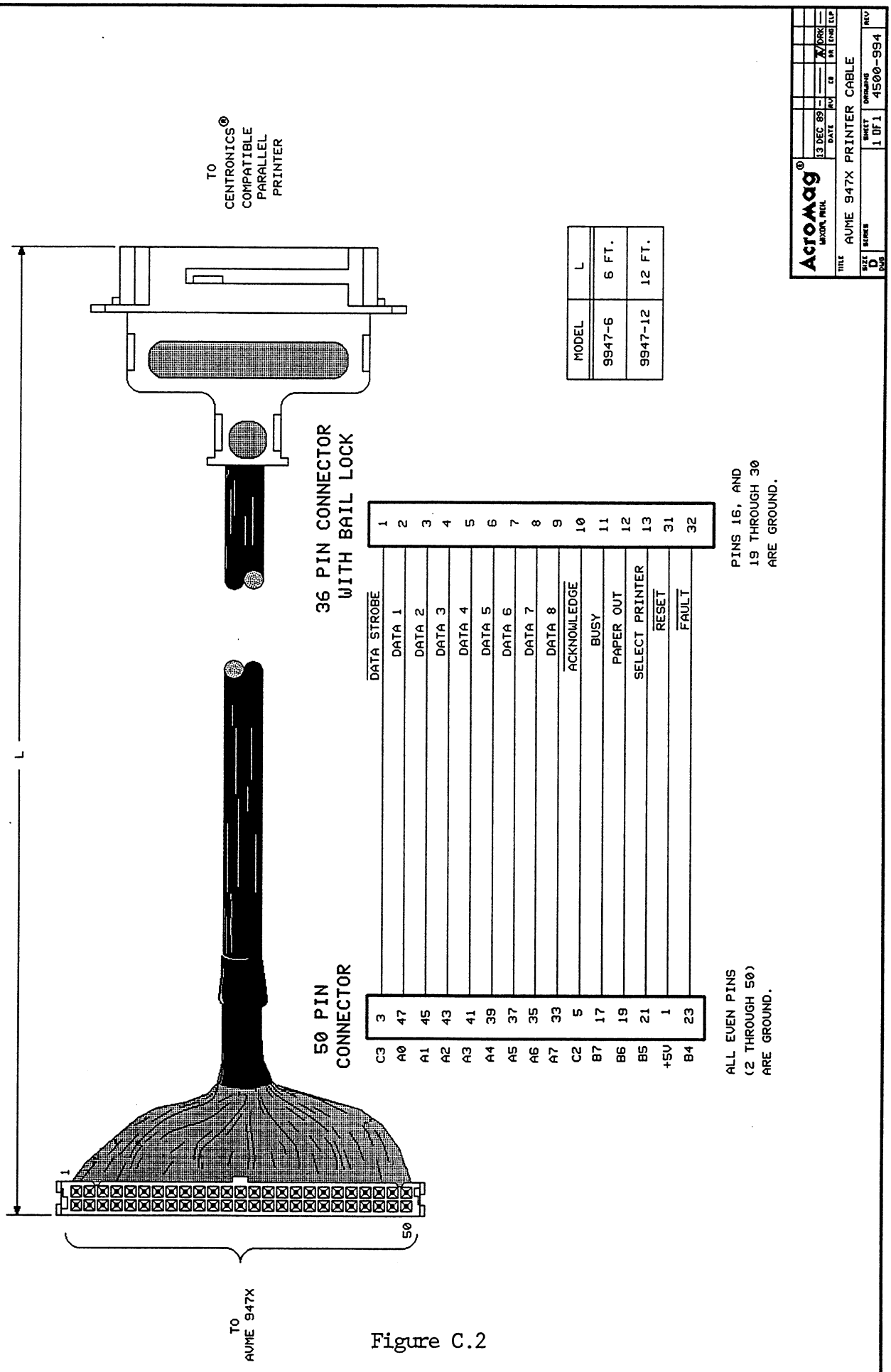


Figure C.2

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