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# Series AVME9660A Industrial I/O Pack

# VMEbus 6U Non-Intelligent Carrier Boards

# USER'S MANUAL

**ACROMAG INCORPORATED**
**30765 South Wixom Road**
**Wixom, MI 48393-2417 U.S.A.**
**Tel: (248) 295-0310**
**Fax: (248) 624-9234**

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# 1.0 GENERAL INFORMATION

## 1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the Industrial Pack module. It is not intended for a general, non-technical audience that is unfamiliar with I/O devices and their application.

## 1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

### 1.2.1 Trademark, Trade Name and Copyright Information

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All rights reserved. Acromag and Xembedded are registered trademarks of Acromag Incorporated. All other trademarks, registered trademarks, trade names, and service marks are the property of their respective owners.

### 1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

### 1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

## 1.3 Carrier Information

The AVME9660A VMEbus card is a carrier for the Industrial I/O Pack (IP) mezzanine board field I/O modules. The carrier board facilitate a modular approach to system assembly, since each carrier can be populated with any

combination of analog input/output and digital input/output IP modules. Thus, the user can create a board which is customized to the application which saves money and space - a single carrier board populated with IP modules may replace several dedicated function VMEbus boards. The AVME9660A non-intelligent carrier boards provide impressive functionality at low cost

### 1.3.1 Ordering Information

Model is available in standard VMEbus 6U size, with support for up to four IP modules. The carrier ordering options are given in the following table.

| *Model Number* | *Operating Temperature Range* | *Supported IP Slots* |
|---|---|---|
| *AVME9660A* | 0 to +70 °C | 4 (A,B,C,D) |
| *AVME9660AE* | -40 to +85°C | 4 (A,B,C,D) |

### 1.3.2 Key Features

- **Interface for Four IP Modules** - Provides an electrical and mechanical interface for up to four industry standard IP modules. IP Modules are available from Acromag and other vendors in a wide variety of Input/Output configurations to meet the needs of varied applications.
- **Provides Full IP Data Access** - Supports accesses to IP input/output, memory, and ID PROM data spaces.
- **Full IP Register Access** - Makes maximum use of logically organized programmable registers on the carrier boards to provide for easy configuration and control of IP modules. The only hardware jumper settings required on the carrier boards set the base address of the card in the VMEbus short I/O space.
- **LED Displays Simplify Debugging** - Front panel LED's are dedicated to each IP module to give a visual indication of successful IP accesses.
- **Front Panel Connectors Access I/O** - Front panel access to field I/O signals is provided via industry standard 50-pin headers. A separate header is provided for each IP module. All headers can be connected to flat ribbon cable from the front panel without interference from boards in adjacent slots. Ejector latches on the headers provide for excellent connection integrity and easy cable removal.
- **Optional Screw Termination Panel** - Model supports field connection via screw terminals using the optional DIN rail mount termination panels.
- **Memory Space Access Support** - IP memory space accesses are supported and software configurable from 1Mbyte to 8Mbytes in

the VMEbus standard address space.

- **Supports Two Interrupt Channels per IP** - Up to two interrupt requests are supported for each IP. The VMEbus interrupt level is software programmable. Additional registers are associated with each interrupt request for control and status monitoring.
- **Supervisory Circuit for Reset Generation** - A power supervisor circuit provides power-on, power-off, and low power detection reset signal to the IP modules per the IP specification.
- **Individually Filtered Power** - Filtered +5V, +12V, and -12V DC power is provided to the IP modules via passive filters present on each supply line serving each IP. This provides optimum filtering and isolation between the IP modules and the carrier board and allows analog signals to be accurately measured or reproduced on IP modules without signal degradation from the carrier board logic signals.

### 1.3.3 Key Features VMEbus Interface

- **Slave Module**-

| | |
|---|---|
| Carrier Register Short I/O Access | A16, D16/D08(O) |
| IP Module ID Space | A16, D16/D08(O) |
| IP Module I/O Space | A16, D16/D08(EO) |
| IP Module Memory Space | A24, D16/D08(EO) |

- **Supports Short I/O Address Modifiers** - Supports short I/O (A16) address modifiers 29H, 2DH (H = Hex). Short I/O space is used for all carrier registers and IP module I/O and ID spaces. The carrier board base address is set by hardware jumpers and decoded on 1K byte boundaries.
- **Supports Standard I/O Address Modifiers** - Supports standard (A24) address modifiers 39H, 3DH (H = Hex). Standard address space is used when an IP supports memory space. The carrier board is configured using programmable registers to set the IP starting address and size (1Mbyte to 8Mbytes).
- **Supports Read-Modify-Write Cycles** - Carrier board supports VMEbus read-modify-write cycles.
- **Interrupt Support** - I(1-7) interrupter D16/D08 (O). Up to two interrupt requests are supported for each IP module. The VMEbus interrupt level is software programmable. Carrier board software programmable registers are utilized as interrupt request control and status monitors. Interrupt release mechanism is Release On Register Access (RORA) type.

## 1.4 Signal Interface Products

(See Appendix for more information on compatible products)

This IP carrier board will mate directly to all industry standard IP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual IP modules):

**Cables:**

Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9660A, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

**Termination Panel:**

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

**Transition Module:**

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9660A boards within the card cage, via flat 50-pin ribbon cable within the card cage (cable Model 5025-550-X or 5025-551-X).

## 1.5 Software Support

The Industry Pack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks

### Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with Industry Pack modules. This software (model IPSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

### VxWorks®

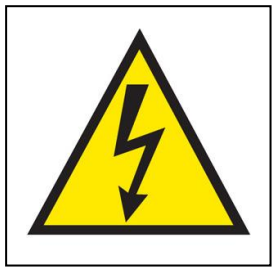
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Industry Pack modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag Industry Pack modules.

### Linux®

Acromag provides a software product consisting of Linux® software. This software (Model IPSW-API-LNX) is composed of Linux® libraries for all Industry Pack modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag Industry Pack modules.

## 2.0 PREPARATION FOR USE

**IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS**



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



***WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.*** This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

### 2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

## 2.2 Installation Considerations

***IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.***

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

## 2.3 Board Configuration

The carrier board may be configured for different applications. All possible configuration settings will be discussed in the following Sections. The jumper locations and IP module positions are shown in Figure 2 (Drawing 5044-452). Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Figure 3 (Drawing 4501-434) and your IP module documentation for specific configuration and assembly instructions.

## 2.4 VMEbus Interface Configuration

The carrier board is shipped from the factory configured as follows:

- Carrier board with VMEbus Short I/O Base Address of 0000H. Board will respond to both Address Modifiers 29H and 2DH. Registers on the carrier board plus the I/O and ID spaces on any installed IP modules will be accessible.
- Programmable software registers default to IP memory space (VMEbus standard address space) accesses disabled.
- Programmable software registers default to IP interrupt requests-disabled and VMEbus interrupt level-none.

## 2.5 Address Decode Jumper Configuration

The carrier board interfaces with the VMEbus as a 1K byte block of address locations in the VMEbus short I/O address space (refer to Section 3 for memory map details). J1 decodes the six most significant address lines A10 through A15 to provide segments of 1K address space. The configuration of

the jumpers for different base address locations is shown in Table 2.1. "IN" means that the pins are shorted together with a shorting clip. "OUT" indicates that the clip has been removed.

### Table 2.1: Address Decode Jumper Selections (J1 Pins)

| BaseAddr* (Hex) | A15 (11&12) | A14 (9&10) | A13 (7&8) | A12 (5&6) | A11 (3&4) | A10 (1&2) |
|---|---|---|---|---|---|---|
| 0000 | OUT | OUT | OUT | OUT | OUT | OUT |
| 0400 | OUT | OUT | OUT | OUT | OUT | IN |
| 0800 | OUT | OUT | OUT | OUT | IN | OUT |
| 0C00 | OUT | OUT | OUT | OUT | IN | IN |
| 1000 | OUT | OUT | OUT | IN | OUT | OUT |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| EC00 | IN | IN | IN | OUT | IN | IN |
| F000 | IN | IN | IN | IN | OUT | OUT |
| F400 | IN | IN | IN | IN | OUT | IN |
| F800 | IN | IN | IN | IN | IN | OUT |
| FC00 | IN | IN | IN | IN | IN | IN |

* Consult your host CPU manual for detailed information about addressing the VMEbus short I/O (A16, 16-bit) space. In many cases, CPU's utilizing 24-bit addressing will start the 16-bit address at FF0000 (Hex), and 32-bit CPU's at FFFF0000 (Hex).

## 2.6 VMEbus Address Modifiers

No hardware jumper configuration is needed. The carrier board will respond to both address modifiers 29H and 2DH in the VMEbus short I/O space. This means that both short supervisory and short non-privileged accesses are supported.

The carrier board will respond to both address modifiers 39H and 3DH in the VMEbus standard address space, when standard address space accesses to IP memory are enabled via programmable registers on the carrier board (refer to Section 3 for programming details).

## 2.7 Interrupt Configuration

No hardware jumper configuration is required. All interrupt enabling, status, and VMEbus interrupt level selections are configured via programmable registers on the carrier board (see Section 3 for programming details). The carrier board passes interrupt requests from the IP modules to the VMEbus--It does not originate interrupt requests. Refer to the IP modules for their specific configuration requirements.

## 2.8 Carrier Field I/O Connectors (IP modules A through D)

Field I/O connections are made via front panel connectors A, B, C, and D for IP modules in positions A through D, respectively. IP module assignment is marked on the front panel for easy identification (see Figure 2 jumper & IP location drawing 5044-452 for physical locations of the IP modules). Flat cable assemblies and Acromag termination panels (or user defined terminations) can be quickly mated to the front panel connectors. Pin assignments are defined by the IP module employed since the pins from the IP module field side correspond identically to the pin numbers of the front panel connectors.

Connectors A through D are 50-pin header (male) connectors (3M 3433-D303). Connectors are high-density, stacked ("Condo") type with A & B and C & D residing on the same part. These connectors include long ejector latches and 30 microns of gold in the mating area for excellent connection integrity (per MIL-G-45204, Type II, Grade C).

## 2.9 IP Field I/O Connectors (IP modules A through D)

The field side connectors of IP modules A through D mate to connectors P7-P10, respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

P7-P10 are 50-pin plug header (male) connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Figure 3 drawing 4501-434 for assembly details).

Pin assignments for these connectors are made by the specific IP model used and correspond identically to the pin numbers of the front panel connectors.

## 2.10 IP Logic Interface Connectors (IP modules A through D)

The logic interface sides of IP modules A through D mate to connectors P11-P14, respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

P11-P14 are 50-pin male plug header connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Figure 3 drawing 4501-434 for assembly details).

Pin assignments for these connectors are defined by the IP module specification and are shown in Table 2.2.

### Table 2.2 Standard IP Logic Interface Connections (P11-P14)

| Pin Description | Number | Pin Description | Number |
|---|---|---|---|
| GND | 1 | GND | 26 |
| CLK | 2 | +5V | 27 |
| Reset* | 3 | R/W* | 28 |
| D00 | 4 | IDSEL* | 29 |
| D01 | 5 | ***DMAReq0**** | 30 |
| D02 | 6 | MEMSEL* | 31 |
| D03 | 7 | ***DMAReq1**** | 32 |
| D04 | 8 | IntSel* | 33 |
| D05 | 9 | ***DMAck0**** | 34 |
| D06 | 10 | IOSEL* | 35 |
| D07 | 11 | ***RESERVED*** | 36 |
| D08 | 12 | A1 | 37 |
| D09 | 13 | ***DMAEnd**** | 38 |
| D10 | 14 | A2 | 39 |
| D11 | 15 | ERROR* | 40 |
| D12 | 16 | A3 | 41 |
| D13 | 17 | INTReq0* | 42 |
| D14 | 18 | A4 | 43 |
| D15 | 19 | INTReq1* | 44 |
| BS0* | 20 | A5 | 45 |
| BS1* | 21 | ***STROBE**** | 46 |
| -12V | 22 | A6 | 47 |

| | | | |
|---|---|---|---|
| +12V | 23 | ACK* | 48 |
| +5V | 24 | ***RESERVED*** | 49 |
| GND | 25 | GND | 50 |

Asterisk (*) is used to indicate an active-low signal. ***BOLD ITALIC*** Logic Lines are NOT USED by the carrier board.

## 2.11 VMEbus Connections

Table 2.3 indicates the pin assignments for the VMEbus signals at the P1 connector. The P1 connector is the upper rear connector on the AVME9660 board, as viewed from the front. The connector consists of 32 rows of three pins labeled A, B, and C. Pin A1 is located at the upper left hand corner of the connector if the board is viewed from the front. VMEbus connector P2 is not used.

Refer to the VMEbus specification for additional information on the VMEbus signals.

### Table 2.3 VMEbus P1 CONNECTIONS

| Pin | Description | Pin | Description | Pin | Description |
|---|---|---|---|---|---|
| 1A | D00 | 1B | ***BBSY**** | 1C | D08 |
| 2A | D01 | 2B | ***BCLR**** | 2C | D09 |
| 3A | D02 | 3B | ***ACFAIL**** | 3C | D10 |
| 4A | D03 | 4B | BG0IN* | 4C | D11 |
| 5A | D04 | 5B | BG0OUT* | 5C | D12 |
| 6A | D05 | 6B | BG1IN* | 6C | D13 |
| 7A | D06 | 7B | BG1OUT* | 7C | D14 |
| 8A | D07 | 8B | BG2IN* | 8C | D15 |
| 9A | GND | 9B | BG2OUT* | 9C | GND |
| 10A | SYSCLK | 10B | BG3IN* | 10C | ***SYSFAIL**** |
| 11A | GND | 11B | BG3OUT* | 11C | ***BERR**** |
| 12A | DS1* | 12B | ***BR0**** | 12C | SYSRESET* |
| 13A | DS0* | 13B | ***BR1**** | 13C | LWORD* |
| 14A | WRITE* | 14B | ***BR2**** | 14C | AM5 |
| 15A | GND | 15B | ***BR3**** | 15C | A23 |
| 16A | DTACK* | 16B | AM0 | 16C | A22 |
| 17A | GND | 17B | AM1 | 17C | A21 |
| 18A | AS* | 18B | AM2 | 18C | A20 |
| 19A | GND | 19B | AM3 | 19C | A19 |

| | | | | | |
|---|---|---|---|---|---|
| 20A | IACK* | 20B | GND | 20C | A18 |
| 21A | IACKIN* | 21B | ***SERCLK*** | 21C | A17 |
| 22A | IACKOUT* | 22B | ***SERDAT**** | 22C | A16 |
| 23A | AM4 | 23B | GND | 23C | A15 |
| 24A | A07 | 24B | IRQ7* | 24C | A14 |
| 25A | A06 | 25B | IRQ6* | 25C | A13 |
| 26A | A05 | 26B | IRQ5* | 26C | A12 |
| 27A | A04 | 27B | IRQ4* | 27C | A11 |
| 28A | A03 | 28B | IRQ3* | 28C | A10 |
| 29A | A02 | 29B | IRQ2* | 29C | A09 |
| 30A | A01 | 30B | IRQ1* | 30C | A08 |
| 31A | -12V | 31B | ***+5V STDBY*** | 31C | +12V |
| 32A | +5V | 32B | +5V | 32C | +5V |

Asterisk (*) is used to indicate an active-low signal. ***BOLD ITALIC*** Logic Lines are NOT USED by the carrier board.

## 2.12 POWER UP TIMING AND LOADING

The AVM9660A boards use a Field Programmable Gate-Array (FPGA) to handle the bus interface and control logic timing. Upon power-up, the FPGA automatically clocks in configuration vectors from a local configuration flash device to initialize the logic circuitry for normal operation. This time is measured as the first 64mS (typical) after the +5 Volt supply rises to +2.5 Volts at power-up. The VMEbus specification requires that the bus master drive the system reset for the first 200mS after power-up, thus inhibiting any data transfers from taking place.

IP control registers are also reset following a power-up sequence, disabling interrupts, etc. (see Section 3 for details).

## 2.13 DATA TRANSFER TIMING

VMEbus data transfer time is measured from the falling edge of AS* to the falling edge of DTACK* during a normal data transfer cycle. Typical transfer times are given in the following table.

| **Register** | **Data Transfer Time** |
|---|---|
| All Carrier Registers | 500 nS, Typical. |
| IP Registers | 500 nS, Typical, One Wait States* |

* See IP module specifications for information on wait states. IP module

register access time will increase by the number of wait states multiplied by 125nS (the period of the 8 MHz clock).

## 2.14 FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each IP module. This provides maximum filtering and signal isolation between the IP modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the VMEbus and the IP grounds. Therefore, unless isolation is provided on the IP module itself, the field I/O connections are not isolated from the VMEbus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP input/output modules.

## 3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to operate the AVME9660A non-intelligent carrier boards.

The board is addressable on 1K byte boundaries in the Short I/O (A16) Address Space. This Acromag VMEbus non-intelligent slave (carrier board) has a Board Status register, but no ID PROM. ID PROM's are provided per the Industrial I/O Pack logic interface specification on the mezzanine (IP) boards which are installed on the carrier. The 1K byte of memory consumed by the board is composed of blocks of memory for the I/O and ID spaces of up to four IP modules. The rest of the 1K byte address space is unused, or contains registers or memory specific to the function of the carrier board. The memory map for AVME9660A is shown in Tables 3.1.

### Table 3.1 AVME9660 Carrier Board Short I/O Memory Map

| **Base Address + (Hex)** | **EVEN Byte D15 D08** | **ODD Byte D07 D00** | **Base Address + (Hex)** |
|---|---|---|---|
| **0000** ↓ **007E** | IP A I/O Space High Byte | IP A I/O Space Low Byte | **0001** ↓ **007F** |
| **0080** ↓ **00BE** | Not Used | IP A ID Space Low Byte | **0081** ↓ **00BF** |
| **00C0** ↓ **00FE** | Not Used | Carrier Board Registers (See Table 3.2) | **00C1** ↓ **00FF** |
| **0100** ↓ **017E** | IP B I/O Space High Byte | IP B I/O Space Low Byte | **0101** ↓ **017F** |
| **0180** ↓ **01BE** | Not Used | IP B ID Space Low Byte | **0181** ↓ **01BF** |
| **01C0** ↓ **01FE** | Not Used | Not Used | **01C1** ↓ **01FF** |

| | | | |
|---|---|---|---|
| **0200**<br>↓<br>**027E** | IP C<br>I/O Space<br>High Byte | IP C<br>I/O Space<br>Low Byte | **0201**<br>↓<br>**027F** |
| **0280**<br>↓<br>**02BE** | Not Used | IP C<br>ID Space<br>Low Byte | **0281**<br>↓<br>**02BF** |
| **02C0**<br>↓<br>**02FE** | Not Used | Not Used | **02C1**<br>↓<br>**02FF** |
| **0300**<br>↓<br>**037E** | IP D<br>I/O Space<br>High Byte | IP D<br>I/O Space<br>Low Byte | **0301**<br>↓<br>**037F** |
| **0380**<br>↓<br>**03BE** | Not Used | IP D<br>ID Space<br>Low Byte | **0381**<br>↓<br>**03BF** |
| **03C0**<br>↓<br>**03FE** | Not Used | Not Used | **03C1**<br>↓<br>**03FF** |

The Input/Output (IO) and Identification (ID) spaces of each IP are accessible via the VMEbus Short I/O space as shown in Table 3.1. The carrier board may optionally occupy memory in the VMEbus standard (A24) address space, if needed for IP modules containing Memory space. IP memory will only be mapped into the standard memory space if it is enabled for a particular IP per the user programmable IP Memory Enable Register (see Table 3.2 and subsequent description). The starting memory address for each enabled IP and the memory size for each enabled IP module is user-programmable via its associated IP Memory Base Address & Size Register (see Table 3.2 and subsequent description).

### Table 3.2 AVME9660 Carrier Board Registers

| **Base Address + (Hex)** | **EVEN Byte D15 D08** | **ODD Byte D07 D00** | **Base Address + (Hex)** |
|---|---|---|---|

| | | | |
|---|---|---|---|
| **00C0** | Not Used | Carrier Board Status Register | **00C1** |
| **00C2** | Not Used | Interrupt Level Register | **00C3** |
| **00C4** | Not Used | IP Error Register | **00C5** |
| **00C6** | Not Used | IP Memory Enable Register | **00C7** |
| **00C8** ↓ **00CE** | Not Used | Not Used | **00C9** ↓ **00CF** |
| **00D0** | Not Used | IP A Memory Base Address & Size Register | **00D1** |
| **00D2** | Not Used | IP B Memory Base Address & Size Register | **00D3** |
| **00D4** | Not Used | IP C Memory Base Address & Size Register | **00D5** |
| **00D6** | Not Used | IP D Memory Base Address & Size Register | **00D7** |
| **00D8** ↓ **00DE** | Not Used | Not Used | **00D9** ↓ **00DF** |
| **00E0** | Not Used | IP Interrupt Enable Register | **00E1** |
| **00E2** | Not Used | IP Interrupt Pending Register | **00E3** |

| | | | |
|---|---|---|---|
| **00E4** | Not Used | IP Interrupt Clear Register | **00E5** |
| **00E6** ↓ **00EE** | Not Used | Not Used | **00E7** ↓ **00EF** |
| **00F0** | Firmware Revision | | **00F1** |
| **00F2** | | Flash Data Reserved | **00F3** |
| **00F4** | | Flash Chip Select Reserved | **00F5** |
| **00F6** | | Not Used | **00F7** |
| **00F8** | XADC Status/Control Register | | **00F9** |
| **00FA** | XADC Address Register | | **00FB** |
| **00FB** ↓ **00FE** | Not Used | Not Used | **00FC** ↓ **00FF** |

## 3.1 Identification PROM (Read Only, 32 Odd Byte Addresses)

Each IP contains an identification (ID) PROM that resides in the ID space per the IP specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information may include unique information required for the module. The identification Section for each IP module is located in the carrier board memory map per Table 3.1. ID PROM bytes are addressed using only the odd addresses in a 64-byte

block. The ID PROM contents are shown in Table 3.3 for a generic IP. Refer to the documentation of your IP module for specific information.

### Table 3.3 Generic IP Module ID Space Identification (ID) PROM

| Hex Offset From ID PROM Base Address | ASCII Character Equivalent | Numeric Value (Hex) | Field Description |
|---|---|---|---|
| 01 | I | 49 | All IP modules have 'IPAC' |
| 03 | P | 50 | |
| 05 | A | 41 | |
| 07 | C | 43 | |
| 09 | | A3 | Acromag ID Code |
| 0B | | mm | IP Model Code[1] |
| 0D | | 00 | Not Used (Revision) |
| 0F | | 00 | Reserved |
| 11 | | 00 | Not Used (Driver ID Low Byte) |
| 13 | | 00 | Not Used (Driver ID High Byte) |
| 15 | | nn | Total Number of ID PROM Bytes |
| 17 | | cc | CRC |
| 19 to (2*nn - 1) | | xx | IP Specific Space |
| (2*nn + 1) to 3F | | yy | Not Used |

**Notes (Table 3.3):**

1. The IP model number is represented by a two-digit code within the ID PROM (e.g. the IP405 model is represented by 01 Hex).

## 3.2 Carrier Board Status Register (Read/Write, Base + C1H)

The Carrier Board Status Register reflects and controls functions globally on the carrier board.

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| ACE[1] | Not Used | Not Used | Soft Reset | GIE[2] | GIP[3] | Not Used | Not Used |

**Notes:**

1. ACE – this bit is Auto Clear Interrupt Enable.
2. GIE – this bit is a Global Interrupt Enable.
3. GIP – this bit is Global Interrupt Pending.

Bits 7

Writing a “1” to this bit will enable automatic clear of pending interrupts on the carrier. When this bit is set pending interrupts will not be latched or registered on the carrier. An interrupt will only remain set as pending on the carrier if its corresponding IP module has an active interrupt request.

Bits 6, 5

Not used - equal "0" if read

Bit 4

Software Reset (Write)

Writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. When set the software reset bit will have a duration of 1us.

Reset Condition: Set to "0".

Bit 3

Global Interrupt Enable (GIE) (Read/Write)

Writing a "1" to this bit enables interrupts to be serviced, provided that interrupts are supported and configured. A "0" disables servicing interrupts.

Reset Condition: Set to "0", interrupts disabled.

Bit 2

Global Interrupt Pending (GIP) (Read)

This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the board's pending interrupt status, even if the Global Interrupt Enable bit is set to "0". Reset condition: Set to "0".

Bits 1, 0

Not used - equal "0" if read

## 3.3 Interrupt Level Register (Read/Write, Base + C3H)

The carrier board passes interrupt requests from the IP modules to the VMEbus. It does not originate interrupt requests. The Interrupt Level Register allows the user to control the mapping of IP interrupt requests to the desired VMEbus interrupt level. Note that the "Global Interrupt Enable" bit in the Carrier Board Status Register must be set for interrupts to be enabled from the carrier board. Also, the specific IP interrupt request must be enabled via its corresponding bit in the Interrupt Enable Register, described subsequently.

| **MSB** **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **LSB** **D0** |
|---|---|---|---|---|---|---|---|
| Not Used | Not Used | Not Used | Not Used | Not Used | IL2 | IL1 | IL0 |

Bits 7,6,5,4,3 — Not used - equal "0" if read

Bits 2,1,0

IL2-IL0 (Read/Write) — These bits control the VMEbus interrupt request level associated with IP interrupt requests as illustrated in the next table.

Reset Condition: Set to "0", no interrupt request.

| VMEbus Interrupt Level | IL2 | IL1 | IL0 |
|---|---|---|---|
| None | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

## 3.4 IP Error Register (Read, Base + C5H)

The IP Error Register allows the user to monitor the Error signals of IP modules A through D. The Industrial I/O Pack specification states that the error signals indicate a non-recoverable error from the IP (such as a

component failure or hard-wired configuration error). Refer to your IP specific documentation to see if the error signal is supported and what it indicates.

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| Not Used | Not Used | Not Used | Not Used | IP-D Error | IP-C Error | IP-B Error | IP-A Error |

Bits 7, 6, 5, 4 — Not used - equal "0" if read

Bit 3
IP-D Error (Read) — This bit will be a "1" when IP D asserts its Error signal. This bit will be "0" when there is no error.
Reset Condition: Bit will be "0" (no error) unless driven by IP.

Bit 2
IP-C Error (Read) — This bit will be a "1" when IP C asserts its Error signal. This bit will be "0" when there is no error.
Reset Condition: Bit will be "0" (no error) unless driven by IP.

Bit 1
IP-B Error (Read) — This bit will be a "1" when IP B asserts its Error signal. This bit will be "0" when there is no error.
Reset Condition: Bit will be "0" (no error) unless driven by IP.

Bit 0
IP-A Error (Read) — This bit will be a "1" when IP A asserts its Error signal. This bit will be "0" when there is no error.
Reset Condition: Bit will be "0" (no error) unless driven by IP.

## 3.5 IP Memory Enable Register (Read/Write, Base + C7H)

The IP Memory Enable Register allows the user to program which IP modules will be accessible in the standard (A24) memory space. An enable bit is associated with each IP A through D. This register must be used in conjunction with the IP Memory Base Address & Size Registers to fully define the addressable memory space of the IP modules. Enabling IP memory has no effect on the I/O and ID spaces of the module.

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| Not Used | Not Used | Not Used | Not Used | IP-D Mem Ena | IP-C Mem Ena | IP-B Mem Ena | IP-A Mem Ena |

| | |
|---|---|
| Bits 7, 6, 5, 4 | Not used - equal "0" if read. |
| Bit 3<br>IP-D Memory Enable<br>(Read/Write) | Writing a "1" to this bit enables the memory space for IP D. A zero disables memory space accesses.<br>Reset Condition: Set to "0", memory space accesses disabled for IP D. |
| Bit 2<br>IP-C Memory Enable<br>(Read/Write) | Writing a "1" to this bit enables the memory space for IP C. A zero disables memory space accesses.<br>Reset Condition: Set to "0", memory space accesses disabled for IP C. |
| Bit 1<br>IP-B Memory Enable<br>(Read/Write) | Writing a "1" to this bit enables the memory space for IP B. A zero disables memory space accesses.<br>Reset Condition: Set to "0", memory space accesses disabled for IP B. |
| Bit 0<br>IP-A Memory Enable<br>(Read/Write) | Writing a "1" to this bit enables the memory space for IP A. A zero disables memory space accesses.<br>Reset Condition: Set to "0", memory space accesses disabled for IP A. |

## 3.6 IP Memory Base Address & Size Register (Read/Write)

### IP_A (Base + D1H), IP_B (Base + D3H), IP_C (Base + D5H), IP_D (Base + D7H),

The IP Memory Base Address & Size Registers are user programmable to define the starting address of standard (A24) memory space and the size of that memory space corresponding to IP modules A through D. The memory size for each enabled IP module is user-programmable from 1MByte to 8MByte in multiples of two. Note that memory on IP modules can only be accessed if enabled within the IP Memory Enable Register, and that the memory bases for enabled IP modules must not be programmed to overlap with each other. The size selected by these registers should be matched to that required by the associated IP.

| **MSB**<br>**D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **LSB**<br>**D0** | |
|---|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | A20 | Not Used | Not Used | 0 | 0 | **1M** |
| A23 | A22 | A21 | Not Used | Not Used | Not Used | 0 | 1 | **2M** |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| A23 | A22 | Not Used | Not Used | Not Used | Not Used | 1 | 0 | **4M** |
| A23 | Not Used | Not Used | Not Used | Not Used | Not Used | 1 | 1 | **8M** |

Bit 7, 6, 5, 4

IP Memory Base

Address (Read/Write)

These bits define the memory base address. Read and write operations are implemented on all bits even if labeled unused. Thus, a read operation will return the last value written.

Reset Condition: Set to "0", memory base address 0.

Bit 3, 2

Not used - equal "0" if read.

Bit 1, 0

IP Memory Size

(Read/Write)

These bits define the memory size selected 1MB, 2MB, 4MB, or 8MB as shown in the previous table.

Reset Condition: Set to "0", 1MB memory size.

## 3.7 IP Interrupt Enable Register (Read, Base + E1H)

The IP Interrupt Enable Register is used to individually enable/disable IP interrupts. Each IP A through D may have up to two requests. Note that the "Global Interrupt Enable" bit in the Carrier Board Status Register must be set for interrupts to be enabled from the carrier board. The user must also configure the VMEbus interrupt level using the Interrupt Level Register. If multiple IP interrupt sources are enabled, they will be serviced in order from highest to lowest priority with bit 0 (IP A Int0) having the highest priority and bit 7 (IP D Int1) having the lowest priority.

| **MSB D7 Lowest Priority** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **LSB D0 Highest Priority** |
|---|---|---|---|---|---|---|---|
| IP D Int1 Enable | IP D Int0 Enable | IP C Int1 Enable | IP C Int0 Enable | IP B Int1 Enable | IP B Int0 Enable | IP A Int1 Enable | IP A Int0 Enable |

All Bits

IP Interrupt Enable

Writing a "1" to a bit enables interrupts for the corresponding IP module and interrupt level. A zero disables the corresponding interrupt.

Reset Condition: Set to "0", IP interrupts disabled.

(Read/Write)

## 3.8 IP Interrupt Pending Register (Read, Base + E3H)

The IP Interrupt Pending Register is used to individually identify pending IP interrupts. If multiple IP interrupts are pending, they will be serviced in order from highest to lowest priority with bit 0 (IP A Int0) having the highest priority and bit 7 (IP D Int1) having the lowest priority.

| **MSB D7 Lowest Priority** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **LSB D0 Highest Priority** |
|---|---|---|---|---|---|---|---|
| IP D Int1 Pend | IP D Int0 Pend | IP C Int1 Pend | IP C Int0 Pend | IP B Int1 Pend | IP B Int0 Pend | IP A Int1 Pend | IP A Int0 Pend |

All Bits

IP Interrupt Pending

(Read)

A bit will be a “1” when the corresponding IP interrupt is pending. A bit will be a “0” when its corresponding interrupt is not pending. Polling this bit will reflect the IP modules pending interrupt status, even if the IP interrupt enable bit is set to “0”.
Reset Condition: Set to "0".

## 3.9 IP Interrupt Clear Register (Write, Base + E5H)

The IP Interrupt Clear Register is used to individually clear the IP interrupt Pending bits set in the IP Interrupt Pending register.

| **MSB D7 Lowest Priority** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **LSB D0 Highest Priority** |
|---|---|---|---|---|---|---|---|
| IP D Int1 Clear | IP D Int0 Clear | IP C Int1 Clear | IP C Int0 Clear | IP B Int1 Clear | IP B Int0 Clear | IP A Int1 Clear | IP A Int0 Clear |

| | |
|---|---|
| All Bits<br>IP Interrupt Clear<br>(Write) | Writing a “1” to a bit causes the corresponding IP interrupt Pending bit to clear. Writing “0” or reading has no effect.<br>Reset Condition: Set to "0". |

## Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200) , Base + F1H

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

## XADC Status/Control Register (Read/Write) - Base + F9H

This read/write register will access the XADC register at the address set in the XADC Address Register.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at Base plus 0xFBH. Next, this register at Base plus 0xF9H is read. Data bits 15 to 6 of this register hold the “ADCcode” temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 16-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(^{\circ}C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

## XADC Address Register (Read/Write) - Base + FBH

This read/write register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 16-bit data transfers.

The address value written to this register can also be read from this register.

### System Monitor Register Map

| Address | Status Register |
|---|---|
| 0x00 | Temperature |

| | |
|---|---|
| 0x01 | Vccint |
| 0x02 | Vccaux |
| 0x20 | Maximum Temperature |
| 0x21 | Maximum Vccint |
| 0x22 | Maximum Vccaux |
| 0x24 | Minimum Temperature |
| 0x25 | Minimum Vccint |
| 0x26 | Minimum Vccaux |

## 3.10 GENERAL PROGRAMMING CONSIDERATIONS

The carrier board register architecture makes the configuration fast and easy. The only set of configuration hardware jumpers is for the base address of the carrier board in the VMEbus short I/O space. Once the carrier board is mapped to the desired base address, communication with its registers and the I/O and ID spaces of the IP modules is straightforward. The carrier board is easily configured to communicate with IP memory space, if present, through two configuration registers. Interrupt configuration/control, if supported by IP modules, is also easily done through registers.

## 3.11 Board Diagnostics

The board is a non-intelligent slave and does not perform self diagnostics. It does, however, provide front panel LED's to indicate successful communication with each of the four IP modules, A through D. These LED's are driven by the corresponding IP acknowledge signal which is lengthened by circuitry on the carrier board to make the access visible to the user. This means that frequent accesses to an IP will result in constant LED illumination. The LED's indicate I/O, memory, interrupt acknowledge, and ID PROM accesses. Note that the LED's will not illuminate during accesses of carrier board registers, or accesses to IP modules which are not physically present, or to unsupported memory space. The LEDs may temporarily illuminate upon initial power-up. Additional information about the error status of the IP modules can be obtained by reading the IP Error Register.

## 3.12 GENERATING INTERRUPTS

Interrupt requests do not originate from the carrier board, but rather, from the IP modules. Each IP may support 0, 1, or 2 interrupt requests. The carrier board processes the request from the IP and uses the Interrupt Level Register data to map the request to the desired VMEbus interrupt level (if locally enabled within the Interrupt Enable Register and globally enabled within the Carrier Board Status Register). The carrier board then waits for an interrupt acknowledge from the VMEbus host after asserting the

appropriate VMEbus interrupt request.

When the carrier board recognizes an interrupt acknowledge cycle on the VMEbus, it checks for a match of the IP interrupt requests. If none is pending or the interrupt level does not match, it will pass the acknowledgment signal along, without consuming it. If there is a match, the carrier board will initiate an acknowledgment cycle with the requesting IP, which must supply the interrupt vector during the cycle. The VMEbus interrupt acknowledge signal is consumed by the carrier board during a valid cycle. Note that if multiple IP interrupt requests are pending, then the carrier board will prioritize the requests and handle them in order.

## 3.13 Interrupt Configuration Example

1. Clear the global interrupt enable bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Write interrupt vector to the location specified on the IP and perform any other IP specific configuration required - do for each supported IP interrupt request.
3. Write to the Interrupt Level Register to program the desired interrupt level per bits 2,1,0.
4. Write “1” to the IP Interrupt Clear Register corresponding to the desired IP interrupt request(s) being configured.
5. Write “1” to the IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (global interrupt enable bit) in the Carrier Board Status Register.

## 3.14 Sequence of Events For an Interrupt

1. The IP asserts an interrupt request to the carrier board (asserts IntReq0* or IntReq1*).
2. The AVME9660A carrier board acts as an interrupter in making the VMEbus interrupt request (asserts IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9660A, the carrier board will check if the level requested matches that specified by the host. If so, the carrier board will assert the

IntSel* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0*; A1 high corresponds to IntReq1*).

5. The IP puts the appropriate interrupt vector on the local data bus (D00-D07 if an D08 (O) interrupter or D00-D15 if a D16 interrupter), and asserts Ack* to the carrier board. The carrier board passes this along to the VMEbus (D08 [O] or D16) and asserts DTACK*.
6. The host uses the vector to point at which interrupt handler to execute and begins its execution.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting IP by writing a "0" to the appropriate bit in the IP Interrupt Enable Register.
   B. Take any IP specific action required to remove the interrupt request at its source.
   C. Clear the interrupting IP by writing a "1" to the appropriate bit in the IP Interrupt Clear Register.
   D. Enable the interrupting IP by writing a "1" to the appropriate bit in the IP Interrupt Enable Register.
8. If the IP interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board negates its interrupt request).
   A. If the IP interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, then the IP should be disabled or reconfigured.
   B. If other IP modules have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

# 4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the carrier board. Refer to the Block Diagram shown in Figure 1 drawing 5044-453 as you review this material.

## 4.1 CARRIER BOARD OVERVIEW

The carrier board is a VMEbus slave board providing up to four industry standard IP module interfaces for the AVME9660A. The carrier board's VMEbus interface allows an intelligent single board computer (VMEbus Master) to control and communicate with electronic devices that are external to the VMEbus card cage. The external electronic hardware is linked to the carrier board via ribbon cable which mates with the IP field connections of the carrier board. The electronic link from the field I/O connections to the carrier board is made via the IP module selected for your specific application.

To facilitate easy connection of external devices to the IP field I/O pins of the carrier board, optional Termination Panels are available. A ribbon cable connects a 50 pin IP field I/O connector on the carrier board to the Termination Panel. At the Termination Panel field I/O signals are connected to a 50 position terminal block via screw clamps. The AVME9660A contains four IP modules and thus 200 I/O connections are provided on the A, B, C, and D connectors.

The VMEbus and IP module logic commons have a direct electrical connection (i.e., they are not electrically isolated). However, the field I/O connections can be isolated from the VMEbus if an IP module that provides this isolation (between the logic and field side) is utilized. A wide variety of IP modules are currently available (from Acromag and other vendors) that allow interface to many external devices for both digital and analog I/O applications.

## 4.2 VMEbus Interface

The carrier board's VMEbus interface is used to program and monitor and carrier board's registers for configuration and control of the board's documented modes of operation (see section 3). In addition, the VMEbus interface is also used to communicate with and control external devices that are connected to an IP module's field I/O signals (assuming an IP module is present on the carrier board).

The VMEbus interface is implemented in the logic of the carrier board's Field Programmable Gate-Array (FPGA). The FPGA implements VMEbus specification revision C.1 as an interrupting slave including the following data transfers types.

| | |
|---|---|
| A16, D16/D08(O) | Carrier Register Short I/O Access |
| A16, D16/D08(O) | IP Module ID Space |
| A16, D16/D08(EO) | IP Module I/O Space |
| A24, D16/D08(EO) | IP Module Memory Space |

The carrier board's VMEbus data transfer rates are typically:

500ns for accesses to the carrier board registers.

500ns for data transfers to the IP modules (assuming 1 wait states on IP).

The carrier board's FPGA monitors the base address jumper setting which is jumperable on 1K byte boundaries in the VMEbus Short I/O (A16) Address Space. When the selected base address matches the (A16) address provided by the VMEbus master, the FPGA controls and implements the required bus transfer allowing communication with the carrier board's registers or IP modules.

## 4.3 Carrier Board Registers

The carrier board registers (presented in section 3) are implemented in the logic of the carrier board's FPGA. An outline of the functions provided by the carrier board registers include:

- Software reset can be issued to reset the FPGA Logic and all IP modules present on the carrier board via the **Status Register**.
- Monitoring the error signal received from each IP module is possible via the **IP Error Register**.
- Configuration of VMEbus A24 standard address space for optional Memory Space on each IP module is possible. Memory Space access to the IP modules can be individually enabled via the **IP Memory Enable Register**. The base address and address range (size) is programmed via carrier registers **IP_A, IP_B, IP_C, and IP_D Memory Base Address & Size Registers**. The address size can be selected from 1M, 2M, 4M, or 8M bytes.
- Enabling of VMEbus interrupt requests from each IP module via the **IP Interrupt Enable Register** is possible. The desired VMEbus interrupt level desired can be set (via the **Interrupt Level Register**), and pending interrupts can be monitored and cleared via carrier registers **IP Interrupt Pending and IP Interrupt Clear Registers**.
- Lastly, pending interrupts can be globally monitored and released to the VMEbus via the **Status Register**.

## 4.4 IP Logic Interface

The IP logic interface is also implemented in the logic of the carrier board's

FPGA. The carrier board implements revision 0.7.1 Industrial I/O Pack logic interface specification and includes four IP logic interfaces on an AVME9660A. The VMEbus address and data lines are linked to the address and data of the IP logic interface. This link is implemented and controlled by the carrier board's FPGA.

The VMEbus to IP logic interface link allows a VMEbus master to :

- Access up to 32 ID Space bytes for IP module identification via D08(O) data transfers using VMEbus A16 short address space.
- Access up to 128 I/O Space bytes of IP data via D16/D08(EO) data transfers using VMEbus A16 short address space.
- Access up to 8Mbytes of IP data mapped to Memory Space via D16 or D08(EO) transfers using VMEbus A24 standard address space.
- Respond to two IP module interrupt requests per IP with software programmable VMEbus interrupt levels.

## 4.5 Carrier Board Clock Circuitry

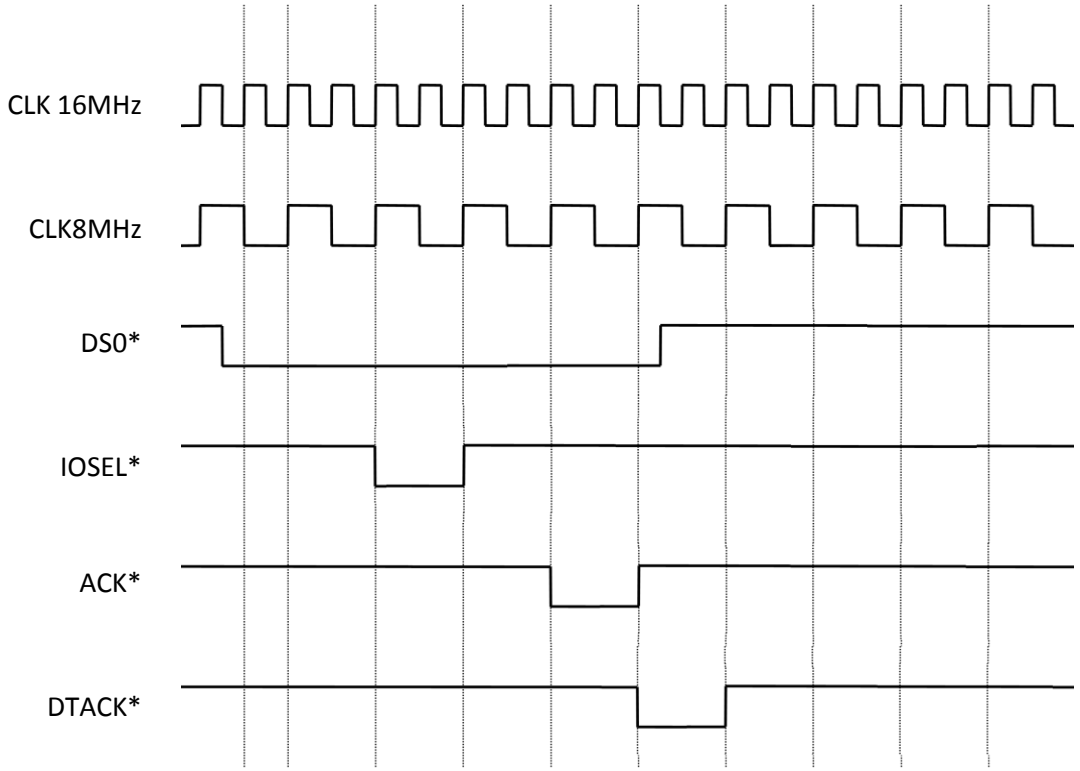
The VMEbus 16MHz system clock is divided down by the FPGA to obtain the IP module 8MHz clock signals. Separate IP clocks are driven to each IP module. All clock lines include series damping resistors to reduce clock overshoot and undershoot, and similar length PC board trace lengths are employed to minimize clock skew between the IP modules.

## 4.6 IP Read and Write Cycle Timing

An IP read or write cycle is carried out via a VMEbus A24 or A16 data transfer. The data transfer starts when the VMEbus Data Strobe 0 (DS0*) goes active and ends when the carrier board drives Data Transfer Acknowledge (DTACK*) active back to the VMEbus master. The carrier board typically has a 500ns IP module data transfer cycle time with one wait state.

A typical IP module data transfer cycle is described here, starting with DS0* going active. DS0* is sampled on the rising edge of the system 16MHz clock edge after it goes active. All operations are then synchronized to the IP 8MHz clock as required by the IP module specification. Thus, typically one 8MHz clock cycles later, an IP select line goes active (IOSEL*, IDSEL*, MEMSEL*, or INTSEL*). With one IP wait states, an active IP Acknowledge (ACK*) signal is driven active by the IP after two rising edges of the 8MHz clock. The carrier board samples ACK* one clock cycle later and then asserts DTACK* active ending the VMEbus data transfer. The carrier board releases the select line (IOSEL*, IDSEL*, MEMSEL*, or INTSEL*) on the first rising edge of the 8MHz clock cycle after driven active.

**Timing Diagram**




The IP module should not expect data to be held after ACK* is detected by the carrier board in a data write cycle.

If a select line (IOSEL*, IDSEL*, INTSEL*, or MEMSEL*) is driven active to an IP module and the IP module does not return ACK* active, then DTACK* will also not be generated by the carrier board. This will cause a bus transfer time-out error and the VMEbus system may need to be reset. In addition, the carrier board will remain in a state waiting for ACK* from the IP. To take it out of this state, a software reset can be issued.

When an IP module places data on the bus, for all data read cycles, any undriven data lines are read by the VMEbus as high because of pull-up resisters on the carrier board's data bus.

## 4.7 VME Interrupter

Interrupts are initiated from an interrupting IP module. However, the carrier board will only pass an interrupt generated by an IP module to the VMEbus if the carrier board has been first enabled for interrupts. Each IP module can initiate two interrupts which can be individually enabled on the carrier board. After interrupts are enabled on the carrier board via the Interrupt Enable Register (see section 3 for programming details), an IP generated interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register.

A carrier board pending interrupt will cause the board to release the interrupt to the VMEbus provided the Global Interrupt Enable bit of the carrier's Status Register has been enabled (see section 3 for programming details).

The carrier board releases the interrupt to the VMEbus by asserting the interrupt request level as pre-programmed in the carrier's Interrupt Level Register. The carrier board's interrupt logic then monitors the VMEbus Interrupt Acknowledge Input (IACKIN*) signal.

An active IACKIN* signal, detected by the carrier board, is either passed to Interrupt Acknowledge Output (IACKOUT*) or consumed by the carrier board. IACKIN* is passed to IACKOUT* if the VMEbus interrupt level does not match that programmed into the carrier's Interrupt Level Register. If a match is detected, the carrier board responds to the interrupt by consuming IACKIN*.

The carrier board also responds to an interrupt by driving IP Interrupt Select (INTSEL*) active to the IP that generated the interrupt provided only one interrupt has been issued. If two or more interrupts occur at the same time, then INTSEL* is driven active to the IP with the highest priority (IP A int0 has the highest priority, IP D Int1 has the lowest priority, see section 3 for more detail). The IP module responds by placing the interrupt vector on the data bus and asserts ACK* active. The carrier then asserts DTACK* active, and the VMEbus master responds by executing the code at the address of the interrupt vector.

The user written interrupt routine should include code to clear the carrier board's pending interrupt via the carrier's Interrupt Clear Register (see section 3) since the interrupt release mechanism is type Release on Register Access (RORA). In addition, the IP module may need similar attention (see your IP module documentation).

## 4.8 Power Failure Monitor

The carrier board contains a 5 volts undervoltage monitoring circuit which provides a reset to the IP modules when the 5 volt power drops below 4.52 volts typical / 4.48 volts minimum. This circuitry is implemented per the Industrial I/O Pack specification.

## 4.9 Access LEDs and Pulse Stretcher Circuitry

An LED display and pulse stretcher circuit is dedicated to each IP module for indication of a data transfer to/from the corresponding IP module. An IP acknowledged data transfer activates the pulse stretcher circuit. The pulse stretcher's circuit is programmed to illuminate the LED for a duration of 0.13 seconds minimum.

## 4.10 Power Supply Filters

Power line filters are dedicated to each IP module for filtering of the +5, +12, and -12 volt supplies. The power line filters are a T type filter circuit comprising ferrite bead inductors and a feed-thru capacitor. The filters provide improved noise performance as is required on precision analog IP modules. Specifically, the filters are typically capable of over 40dB of insertion loss for undesirable noise and oscillations in the 100MHz frequency range and over 20dB of insertion loss for noise and oscillations in the 10MHz frequency range.

# 5.0 SERVICE AND REPAIR

## 5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

## 5.2 Preliminary Service Procedure

**CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS**

Before beginning repair, be sure that all the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty board.

## 5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag web site at acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab or your specific model ordering page.

Acromag’s application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

# 6.0 SPECIFICATIONS

## 6.1 Physical

**AVME9660A**

| | |
|---|---|
| Length: | 233.3 mm (9.187 in) |
| Width: | 160.0 mm (6.299 in) |
| Board Thickness | 1.60 mm (0.063 in) |
| Max Component Height | 13.97 mm (0.55 in) |
| Recommended Card Spacing | 20.32 mm (0.8 in) |

Unit Weight (does not include shipping material):

- AVME9660A 9.6 oz. (272.15 g)
- IPack L x W: 99.05 mm x 45.72 mm (3.9 in x 1.8 in)

**Connectors:**

P1 (VMEbus).....DIN 41612 96-pin Type C, Level II
P2 (VMEbus).....Not Used.

A-D (Carrier Field I/O).....50-pin Male Header x2 stacked “condo type” 3M 3433-D303 with ejector latches

P7-P10 (IP Field I/O).....50-pin male plug header (AMP 173280-3 or equivalent).

P11-P14 (IP Logic Interface)...50-pin male plug header (AMP 173280-3 or equivalent).

## 6.2 Power Requirements

Board power requirements are a function of the installed IP modules. This specification lists currents for the carrier boards only. The carrier boards individually filter and provide +5V, +12V and -12V power to each IP from the VMEbus.

The power supply filters are typically capable of over 40dB of insertion loss for undesirable noise and oscillations in the 100MHz frequency range and over 20dB of insertion loss for noise and oscillations in the 10MHz frequency range.

The power failure monitor circuit provides a reset to IP modules when the 5 volt power drops below 4.52 volts typically / 4.48 volts minimum.

Summarized below are the expected current draws for each of the specified power supply voltages.

| Power Supply Voltage | Current Draw |
|---|---|
| • 5.0 VDC +/- 5% | 0.233 A Typical, 0.275 A maximum |
| • +12 VDC +/- 5% | Not Used |
| • -12 VDC +/- 5% | Not Used |

**Non-Isolated** VMEbus and IP module logic commons have a direct electrical connection. As such, unless the IP module provides isolation between the logic and field side, the field I/O connections are isolated from the VMEbus

**LED illuminate duration** 0.13 second, minimum

## 6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AVME9660A carrier.

### 6.3.1 Operating Temperature

| *Model Number* | *Description* | *Temp Range* |
|---|---|---|
| *AVME9660A-LF* | | *0*°C *to 70*°C |
| *AVME9660AE-LF* | E Version | *-40*°C *to 85*°C |

### 6.3.2. Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

### 6.3.3 Storage Temperature

-55 to +100°C

## EMC Directives

Complies with EMC Directive 2014/30/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  **Note:** This is a Class A product
- **RoHS Directive 2011/65/EU – All Models**

In compliance per EN 50581

## FCC US/Canada

Complies with:

- **FCC Part 15, Class A Digtal Device:**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

## 6.4 Reliability Prediction

### Table 6.4.1 AVME9660AE-LF

**MTBF (Mean Time Between Failure):** MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

| Temperature | MTBF (Hours) | MTBF (Years) | Failure Rate (FIT[1]) |
|---|---|---|---|
| **25°C** | TBD | TBD | TBD |
| **40°C** | TBD | TBD | TBD |

[1] FIT is Failures in $10^9$ hours.

## 6.5 INDUSTRIAL I/O PACK COMPLIANCE

| | |
|---|---|
| **Specification** | This device meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1 |
| **Electrical/Mechanical Interface** | AVME9660A (E) supports four single-size IP modules (A-D), or two double-size. 32-bit IP modules are Not Supported. |
| **I/O Space** | A16/D16 or D08(EO); supports 128 byte values per IP. |
| **ID Space** | A16/D08(O); supports 32 bytes per IP (consecutive odd-byte addresses). D16 is also supported with pull-ups on the carrier board holding the upper 8-bits high. |

| | |
|---|---|
| **Memory Space** | A24/D16 or D08(EO); supports 1M to 8M bytes per IP module. |
| **Interrupts.** | Supports two interrupt requests per IP and interrupt acknowledge cycles, D16/D08(O). |

## 6.6 VMEbus COMPLIANCE

| | |
|---|---|
| **Specification** | This device meets or exceeds all written VME specifications per revision C.1 dated October 1985, IEC 821-1987 and IEEE 1014-1987 |
| **Data Transfer Bus** | A24/A16:D16/D08 (EO) DTB slave; supports Read-Modify-Write cycles. |
| **VMEbus Access Time** | 500nS Typical (all carrier board registers); measured from the falling edge of DSx* to the falling edge of DTACK*. 500nS Typical (IP registers with one wait states). See IP specifications for information on wait states. IP register access time will increase by the number of wait states multiplied by 125nS (the period of the 8 Mhz clock). |
| **VMEbus Address Modifier Codes:**<br>**Short I/O Space** | Base address is hardware jumper selectable. Occupies 1K byte. Responds to both address modifiers 29H & 2DH in the VMEbus short I/O space for carrier board registers and IP I/O and ID PROM spaces. |
| **Standard AddressSpace** | Responds to both address modifiers 39H & 3DH in the VMEbus standard address space when such accesses to IP memory are enabled via programmable registers on the carrier board. Base addresses and sizes of IP memory are programmable from 1M to 8M bytes. |
| **Interrupts** | Creates I(1-7) programmable request levels (up to two requests sourced from each IP). D16/D08(O) interrupter (interrupt vectors come from IP modules). Carrier registers for control & status monitoring. Interrupt release mechanism is Release On Register Access (RORA). |

# APPENDIX

## CABLE Model 5025-550-x (Non Shielded) or Model 5025-551-x (Shielded)

| | |
|---|---|
| **Type** | Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. |
| **Application** | Used to connect Model 5025-552 termination panel to the AVME9660A non-intelligent carrier board A-D connectors. |
| **Length** | Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss. |
| **Cable** | 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent). |
| **Headers** | 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent). |
| **Keying** | Headers at both ends have polarizing key to prevent improper installation. |
| **Shipping Weight** | 1.0 pound (0.5Kg), packed. |

## Termination Panel Model 5025-552

| | |
|---|---|
| **Type** | Termination Panel For AVME9660A Boards |
| **Application** | To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9660A 6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel. |
| **Field Wiring** | 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG. |
| **Connections to AVME9660** | P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as |

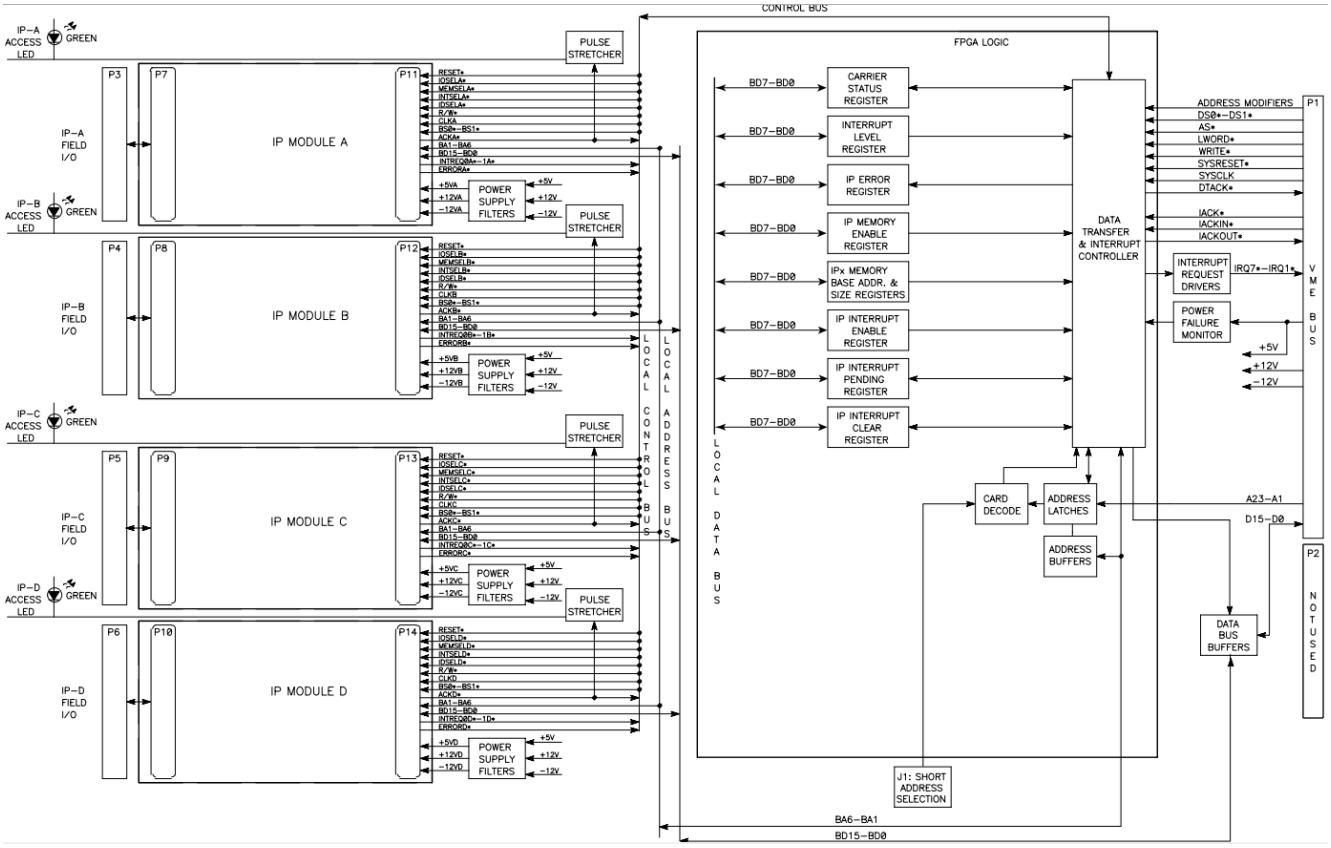
| | |
|---|---|
| | possible to reduce noise and power loss. |
| **Mounting** | Termination panel is snapped on the DIN mounting rail. |
| **Printed Circuit Board** | Military grade FR-4 epoxy glass circuit board, 0.063 inches thick. |
| **Operating Temperature** | -40°C to +100°C. |
| **Storage Temperature** | -40°C to +100°C. |
| **Shipping Weight** | 1.25 pounds (0.6kg) packed. |

## Transition Module: Model TRANS-GP

| | |
|---|---|
| **Type** | Transition module for AVM9660A boards. |
| **Application** | To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9660A boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). |
| **Schematic and Physical Attributes** | See Figure 4 (TRANS-GP drawing 4501-465). |
| **Field Wiring** | 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X) |
| **Connections to AVME9660** | 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9660A boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). |
| **Mounting** | Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage. |
| **Printed Circuit Board** | Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick |
| **Operating Temperature** | -40°C to +85°C. |
| **Storage Temperature** | -55°C to +105°C. |
| **Shipping Weight** | 1.25 pounds (0.6kg) packed. |

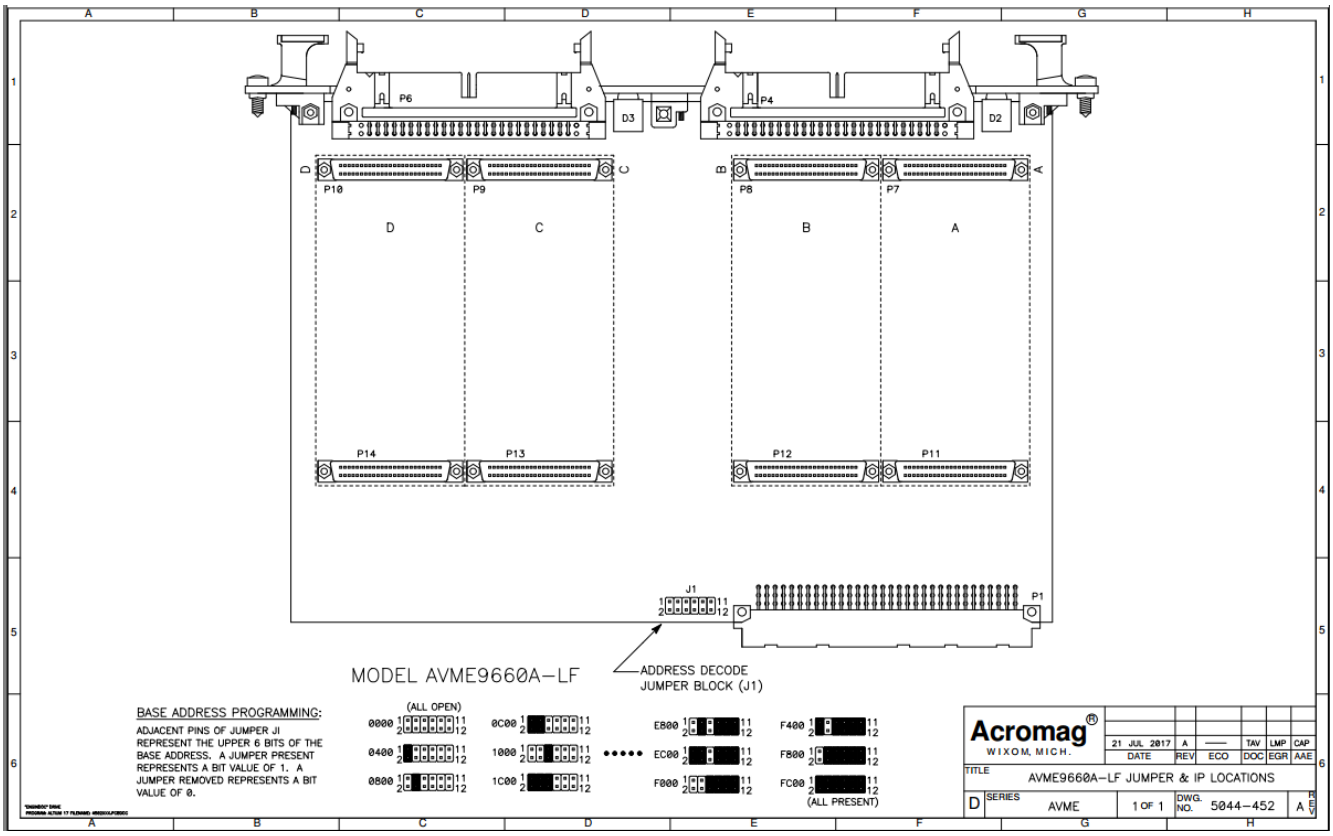
## Figure 1

### AVME9660A Block Diagram



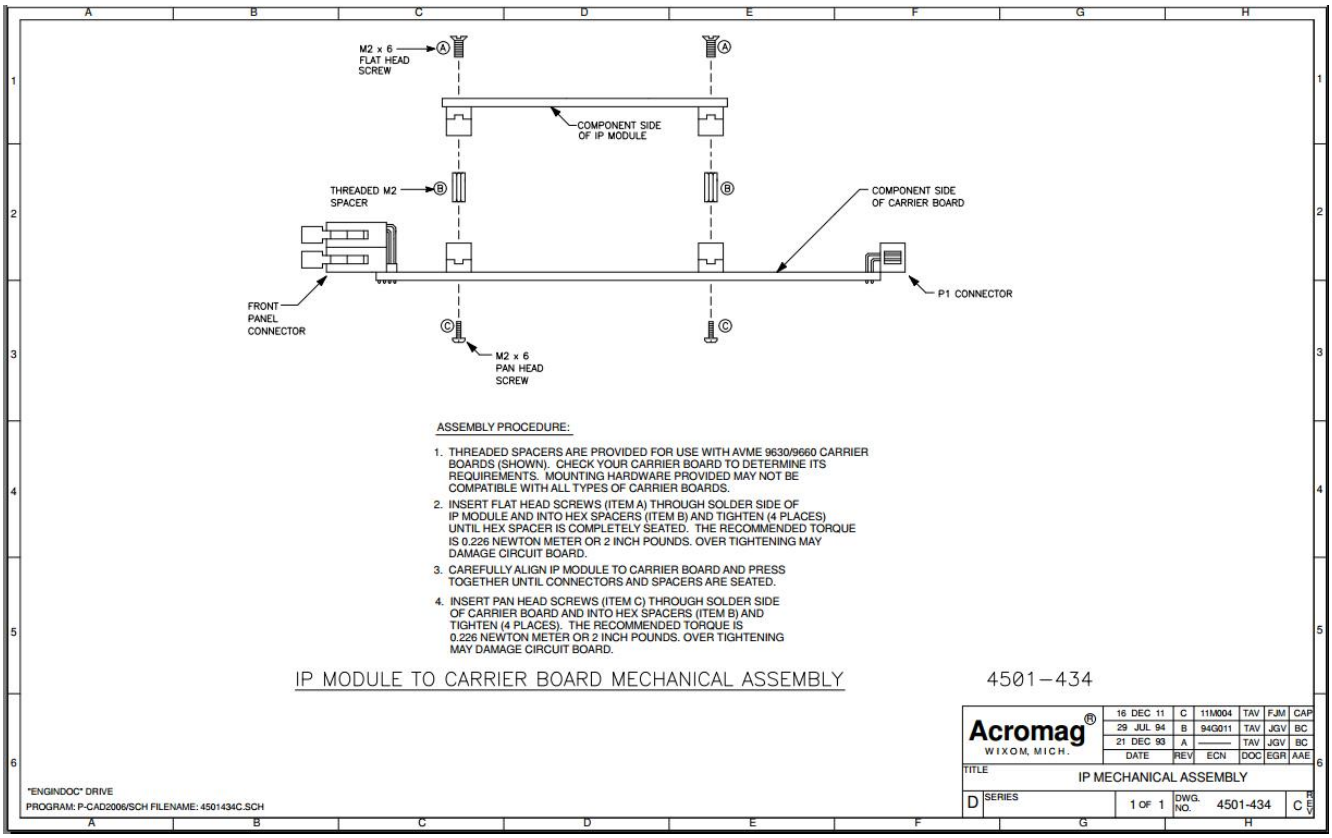
## Figure 2

### Jumper and IP Location Diagram



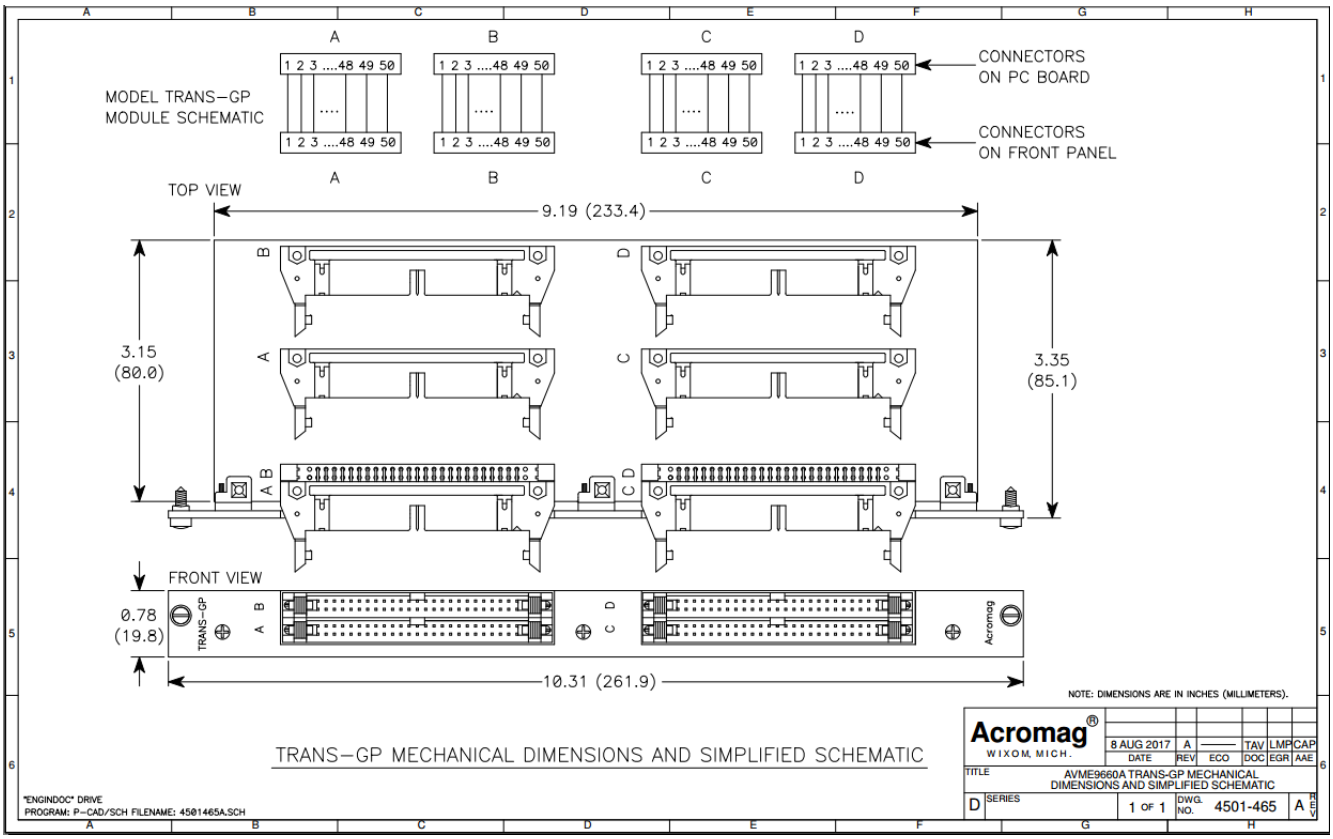
## Figure 3

### IP Mechanical Assembly Diagram



## Figure 4

### TRANS-GP Diagram



## Certificate of Volatility

| | | | | |
|---|---|---|---|---|
| Acromag Model<br>AVME9660A(E)-LF | Manufacturer:<br>Acromag, Inc.<br>30765 Wixom Rd<br>Wixom, MI 48393 | | | |
| Volatile Memory | | | | |
| Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)?<br>■ Yes □ No | | | | |
| Type (SRAM, SDRAM, etc.)<br>Configurable Logic Blocks and Block RAM Blocks | Size:<br>75,520 Logic Cells and 3780 Kb Block RAM | User Modifiable<br>■ Yes<br>□ No | Function:<br>FPGA logic blocks and RAM blocks | Process to Sanitize:<br>Power Down |
| Type (SRAM, SDRAM, etc.) | Size: | User Modifiable<br>□ Yes<br>□ No | Function: | Process to Sanitize: |
| Non-Volatile Memory | | | | |
| Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)?<br>■ Yes □ No | | | | |
| Type (EEPROM, Flash, etc.)<br>Flash | Size:<br>128 Meg x 1bit | User Modifiable<br>■ Yes<br>□ No | Function:<br>Data storage for FPGA | Process to Sanitize:<br>Erase using JTAG |
| Type (EEPROM, Flash, etc.)<br>One Time Programmable area in flash device | Size:<br>1024-byte | User Modifiable<br>■ Yes<br>□ No | Function:<br>The OTP Address Space. | Process to Sanitize:<br>Protect from Programming |

| Acromag Representative | | | | |
|---|---|---|---|---|
| Name:<br>Russ Nieves | Title:<br>Sales and Marketing | Email:<br>solutions@acromag.com | Office Phone:<br>248-295-0310 | Office Fax:<br>248-624-9234 |

## Revision History

The revision history for this document is summarized in the table below.

| Release Date | Version | EGR/DOC | Description of Revision |
|---|---|---|---|
| 21 NOV 2017 | A | LMP/MJO | Initial Release. |
| 09 APR 2018 | B | LMP/ARP | Added CE and FCC specifications. |
| | | | |
| | | | |
| | | | |
| | | | |

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