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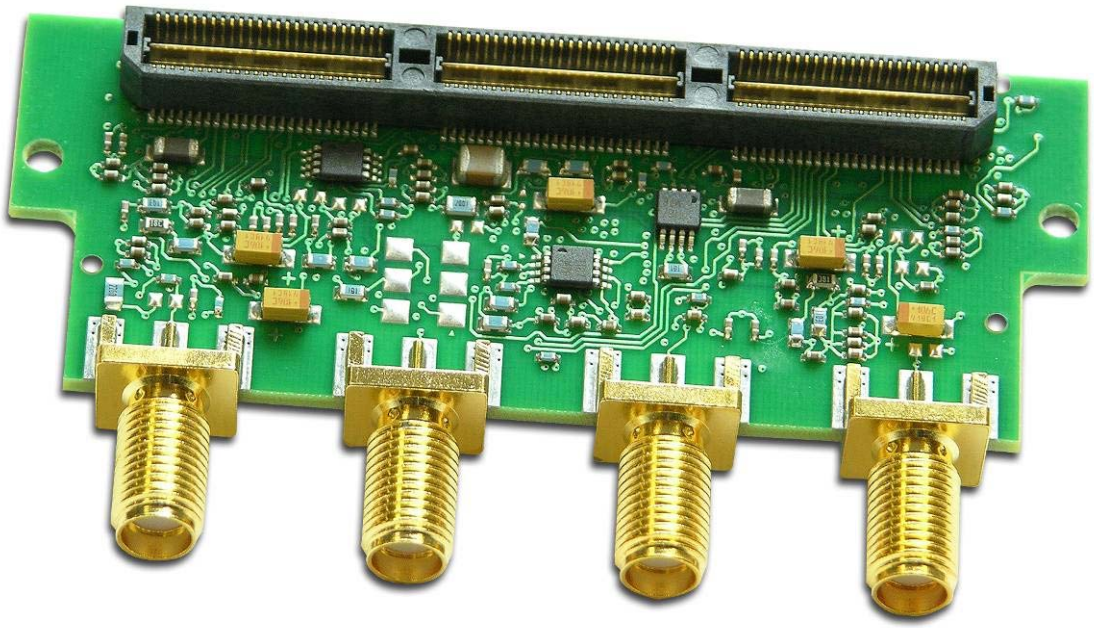
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AXM-A30
2 Analog Input Mezzanine Module

USER'S MANUAL



ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

Tel: (248) 295-0310
Fax: (248) 624-9234

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IMPORTANT SAFETY CONSIDERATIONS

You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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1.0 GENERAL INFORMATION

The AXM-A30 is a high speed analog input mezzanine board for Acromag's line of re-configurable PMC modules. The AXM-A30 has 2 analog inputs, an external clock, and trigger provided via SMA connectors.

In addition to the analog input board, Acromag offers several other options for front panel I/O as detailed in table 1.1.

Table 1.1: *AXM Series Models*

MODEL	Front I/O Type	Front I/O Connector	OPERATING TEMPERATURE RANGE
AXM-A30	2 Analog 3.4Vp-p	SMA	0°C to +70°C
AXM-D02	30 Differential	68 SCSI	-40°C to +85°C
AXM-D03	22 Differential & 16 CMOS	68 SCSI	-40°C to +85°C
AXM-D04	30 LVDS	68 SCSI	-40°C to +85°C
AXM-EDK	JTAG & LVTTL	Xilinx Std JTAG & 34-Pin 0.1" Header	-40°C to +85°C

KEY FEATURES

- **High Speed Analog Input** – Two independent ADC channels provide simultaneous sampling at maximum data rates of 100MHz. The digitized output of each ADC is simultaneously input to the FPGA for data collection and processing.
- **3.4V Peak to Peak Analog Input Range –** A bipolar ±1.7V input range is supported at each of the four ADC inputs.
- **Analog Input Scan Mode –** Burst Continuous, can be enabled via a programmable control register. Data collection continues while enabled and ceases when disabled.
- **External Clock Input or Output–** An external clock signal can be used for A/D collection purposes or used as an output to synchronize operations with other modules.
- **General Purpose Input or Output –** An general purpose I/O signal is available through an SMA connector. This signal can be used to synchronize operation with other modules when used as an output. As an input the signal could be used to enable data collection.
- **Example Design –** The example VHDL design, provided in the base board EDK, includes control of all A/D, external clock, and external trigger.

ENGINEERING DESIGN KIT

Acromag does not provide an engineering design kit specifically for the AXM-A30 module. However, an example design is included in the Engineering Design Kit of the PMC base board. Refer to the PMC base board's manual for further information on the available Engineering Design Kit.

BOARD CONTROL SOFTWARE

Acromag does not provide board control software specifically for the AXM-A30 series board. However, the AXM-A30 module can be accessed via the control software for the base PMC module. These products (sold separately) facilitate the product interface in the following operating systems: Windows® DLL, VxWorks®, and QNX®. Refer to the PMC base board's manual for further information.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

CARD CAGE CONSIDERATIONS

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Remove power from the system before installing board, cables, termination panels, and field wiring.

Default Hardware Configuration

The AXM-A30 board cannot stand-alone and must be mated with a compatible Acromag PMC module. The default configuration of the control register bits at power-up is described in section 3.

Front Panel Field I/O Connector

The front panel connector provides the field I/O interface connections. Four female SMA connectors per MIL-C-39012 are used. Bodies are brass per QQ-B-626, gold plated per MIL-G-45204 0.00001" minimum. Contacts are beryllium copper per QQ-C-530 and gold plated per MIL-G-45204 0.00003" minimum.

The SMA connector at the most right location is SMA connector 1 and corresponds to Analog Input channel 1. All SMA connectors and their corresponding function are listed in Table 2.1. The SMA and corresponding functions are also illustrated on the SMC connector face plate as shown below.

Connector Description	SMA Connector
Analog Input Ch1	1
External Clock	2
External Trigger	3
Analog Input Ch2	4

Table 2.1: *Board Field I/O Pin Connections*

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the boards. These models are daughter cards intended only for use on specific Acromag PMC modules. As such only a small portion of I/O memory space is currently reserved for operation of the daughter card. The remaining memory space is defined in the base boards User's Manual.

AXM-A30 MEMORY MAP

The AXM-A30 specific memory space address map for the board is shown in Table 3.1. Note that the base address from the base PMC module in memory space must be added to the addresses shown to properly access the board registers. Register accesses as 32, 16, and 8-bits in memory space are permitted unless indicated.

Table 3.1: *Memory Map*

Base Addr+	D31 D16	D15 D00	Base Addr+
0003 ↓ 7FFF	Reserved for base PMC Module[1]		0000 ↓ 7FFC
8003	Board Status Register and Software Reset[2]		8000
8007 ↓ 80FF	Reserved for base PMC Module[1]		8004 ↓ 80FC
8103	GPIO Register	AXM-A30 Board Control Register	8100
8107	ADC2 Control/Status Register	ADC1 Control/Status Register	8104
810B	ADC2 Conversion Threshold Register	ADC1 Conversion Threshold Register	8108
810F	ADC2 FIFO Read Port	ADC1 FIFO Read Port	810C
8113	Not Used	Clock Conditioner Control/Status Register	8110
8117	Clock Conditioner R0 FPGA CLK Control Register[3]		8114
811B	Clock Conditioner R1 External CLK Control Register[3]		8118
811F	Clock Conditioner R3 AD Ch 1. CLK Control Register[3]		811C
8123	Clock Conditioner R4 AD Ch 2. CLK Control Register[3]		8120
8127	Clock Conditioner R11 PLL Control Register[3]		8124
812B	Clock Conditioner R13 PLL Control Register[3]		8128
812F	Clock Conditioner R14 PLL Control Register[3]		812C
8133	Clock Conditioner R15 PLL Control Register[3]		8130
8137	Not Used	ADC DP-SRAM Override Register	8134
8137 ↓ 1FFFFF	Reserved for base PMC Module[1]		8134 ↓ 1FFFFC

1. This address space is not defined for this module. This space may be used on the base PMC Module. Refer to the base PMC module User's Manual for further information

2. These registers have bits that are reserved for the base PMC module. See the register definition later in this manual for further details.

3. These registers require 32-bit data transfers and are not affected by a board level reset.

This memory map reflects byte accesses using the "Little Endian" byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses "Little Endian" byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Board Status and Software Reset Register (Read/Write) – (Base Addr + 8000H)

BOARD STATUS AND RESET REGISTER

This read/write register is used the issue a software reset, view and clear pending interrupts, and to identify the attached AXM module. It may also provide other functions that are defined by the base board. Writing a "1" to bit 31 of this register will cause a software reset affecting both the PMC base board and the majority of AXM-A30 registers. Note that the Clock Conditioner Registers on the AXM-A30 are not affected by this software reset. Bits 15 to 13 are used for AXM identification code.

Read of this register reflects the interrupt pending status. Read of a "1" indicates that an interrupt is pending for the corresponding interrupt.

ADC threshold exceeded interrupt will be issued to the system if more samples are present in the ADC FIFO than the set the ADC Conversion Threshold register value. The interrupt request will remain active until disabled via bit-11 of the ADC Control/Status register or when enough FIFO samples have been read and the FIFO has less samples then the set ADC Conversion Threshold register value.

Table 3.2 *Board Status and Reset Register*

BIT	FUNCTION	
8-0	Not Used. Will read logic '0'.	
9	ADC1 Threshold Exceeded Interrupt Pending	
10	ADC2 Threshold Exceeded Interrupt Pending	
12-11	Reserved for PMC base board[3]	
15-13	AXM Identification bits[1,2] (Read Only)	
	AXM-D0x	"001"
	AXM-EDK	"001"
	AXM-A30	"010"
30-16	Reserved for PMC base board[3]	
31	Software Reset (Write Only)	

1. The AXM Identification bits are used to indicate the vhdl version. It is the responsibility of the user to determine if an AXM is physically connected to the base board.
2. All other 3 bit values are reserved for future use.
3. Bit function is defined by the base PMC Module.

This register can be written with 8-bit, 16-bit, or 32-bit data transfers.

ADC OPERATION

Analog Input Ranges and Corresponding Digital Output Codes

The analog input range is 3.4 volts peak to peak with a 50Ω input impedance. In Table 3.4 the digital output code corresponding to the ideal analog input value is given in both binary two's complement and offset binary formats. The AXM-A30 was designed for frequency detection and analysis. The ADC design has an approximate 0.2V DC offset, and a nominal gain of 0.98V/V which make its use difficult for voltage detection. Furthermore due to differences in the precision network that control the gain, the actual full scale range may vary. Use of this module for DC (or near DC) operation, will require extensive calibration as outlined later in this manual.

Table 3.3 *ADC Input Range and Gain*

DESCRIPTION	ANALOG INPUT
Input Range (Min)	±1.7V
Input Range (Max)	±1.825V
Gain (Typ)	0.98V/V

The digital output format is controlled by bit-1 of the ADC Control register. The two formats supported are Binary Two's Complement and Offset Binary. The hex codes corresponding to these two data formats are depicted in Table 3.4.

Table 3.4 *Digital Output Codes and Input Voltages.*

DESCRIPTION	DIGITAL OUTPUT	
	16bit Binary 2's Comp	16 bit Offset Binary
+ Full Scale	7FFF	FFFF
Midscale	0000	8000
1 LSB Below Midscale	FFFF	7FFF
- Full Scale	8000	0000

ADC MODE OF CONVERSION

The ADC will continuously convert data when enabled, via a programmable control register. Data collection continues while enabled and ceases when disabled.

ADC conversions are enabled via bits 5 to 6 in the AXM-A30 Board Control Register at base address plus 8100H. ADC conversions will continue but can not be stored once the FIFO becomes full.

AXM-A30 Board Control Register (Read/Write) – (Base Addr + 8100H)

This read/write register is used to set AXM-A30 global settings including the general purpose I/O functionality, selecting the input clock source, and ADC enables. Bits 0 and 1 determine the functionality of the GPIO as either a digital I/O or a clock output. Bits 3 and 4 control the clock source for the ADC. ADC Conversions can be enabled and disabled for write to FIFO or SRAM via bits 5 and 6. These bits can be used to simultaneously enable and disable ADC channels 1 and 2. If enabled, by setting the bit to logic '1', conversions are implemented and stored to FIFO or SRAM at the ADC clock data rate. Conversions are disabled by setting its corresponding bit to logic '0'. Each channel can also be set to a power down state via bits 9 and 10 to reduce energy consumption when not in use. Bit 10 enables an independent clock from the AXM-A30 to the PMC base Module. The default power-up state of this register is logic low. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

BIT	FUNCTION	
1-0	General Purpose I/O Control: These bits set the functionality of the General Purpose I/O.	
	Logic "00"	Digital Input (Default)
	Logic "01"	Digital Output
	Logic "10"	PLL Clock 2 Output
	Logic "11"	Not Used
2	Not Used	
4-3	Clock Source Control: These bits control the clock source supplied to the "jitter cleaner".	
	Logic "00"	Crystal (Default)
	Logic "01"	Not Used
	Logic "10"	External Clock
	Logic "11"	Not Used
5	ADC Channel 1 Enable/Disable	
	Logic "0"	Disable Channel 1 FIFO/SRAM Storage(Default)
	Logic "1"	Enable Channel 1 FIFO/SRAM Storage
6	ADC Channel 2 Enable/Disable	
	Logic "0"	Disable Channel 2 FIFO/SRAM Storage(Default)
	Logic "1"	Enable Channel 2 FIFO/SRAM Storage
7	Not Used	
8	ADC Channel 1 Op-Amp Power down[1,2]	
	Logic "0"	Disable Channel 1 (Default)
	Logic "1"	Enable Channel 1
9	ADC Channel 2 Op-Amp Power down[1,2]	
	Logic "0"	Disable Channel 2 (Default)
	Logic "1"	Enable Channel 2
10	FPGA Input Clock Enable	
	Logic "0"	Disable FPGA CLK (Default)
	Logic "1"	Enable FPGA CLK
15-11	Not Used	

Table 3.5 *AXM-A30 Board Control Register*

1. Allow at least 10us for power-up after setting this bit.

2. This bit controls the power state of the differential operational ampliflier buffer and not the A/D itself. The best method for disabling the A/D is to disable the clock via the Clock Conditioner Registers.

ADC REGISTERS

General Purpose I/O Status Register (Read/Write) – (Base Addr + 8102H)

This register controls the status of the General Purpose I/O. The input signal levels are determined by reading bit 0 of this register. Likewise, the output signal levels are set by writing to bit 0 of this register. The functionality of the GPIO bit is set via bits 0 and 1 of the AXM-A30 Board Control Register at Base Addr + 8100H.

The default state causes the GPIO to be defined as an input. As such the reset value of this register is determined by the voltage applied to the general Purpose I/O SMA connector. If the GPIO connector is left floating it will read logic high due to an internal pull-up. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Table 3.6 *General Purpose I/O Status Register*

BIT	FUNCTION
0	General Purpose I/O Status: **Read** of this bit reflects the current state of the GPIO if set as a digital input. **Write** of this bit will set the digital value of the GPIO if it is a digital output.
15-1	Not Used

ADC Control/Status Register (Read/Write) – (Base Addr + 8104, 8106H)

The function of each of the control register bits are described in Table 3.7. The ADC Control/Status register at Base address + 8104H corresponds to the first of two on board ADCs, while the ADC Control/Status register at Base address + 8106H corresponds to the second on board ADCs. Both ADC FIFO's must be enabled via the AXM-A30 Board Control Register at base address + 8100H. These registers can be read or written via 32-bit, 16-bit or 8-bit data transfers. A power-up or software reset sets all bits to 0, unless otherwise noted in Table 3.7.

BIT	ADC Control/Status Register	
Bit-0	Not Used	
Bit-1	See Tables 3.3 and 3.4 for a description of these two data formats.	
	Logic "0"	Offset Binary (Default)
	Logic "1"	Binary Two's Complement
Bit-2	An input clock duty cycle stabilizer provides an ADC clock with a nominal 50% duty cycle. This duty clock stabilizer should only be active for ADC Clock input frequencies above 30MHz.	
	Logic "0"	Disable Duty Cycle Stabilizer(Default)
	Logic "1"	Enable Duty Cycle Stabilizer
Bits-3 and 4	Not Used	
Bit-5	ADC FIFO Reset.[1, 2]	
	Logic "0"	No Change
	Logic "1"	ADC FIFO Pointers are Cleared
Bits 6 and 7	Not Used	
Bits 8	ADC Input Voltage Overload Indicator (Read Only)	
	Logic "0"	No Voltage Overload
	Logic "1"	Input Voltage Overload
Bit 9	Not Used	
Bit-10	Stop ADC conversions when FIFO has more samples than set threshold (as set by threshold register).	
	Logic "0"	ADC Conversion not stopped.
	Logic "1"	Stop ADC Conversion On Threshold
Bit-11	If enabled via this bit an interrupt request from the module will be issued to the system if there are more samples in the FIFO than the threshold number selected via the ADC Conversion Threshold register. The interrupt request will remain active until disabled via this bit or when enough FIFO samples have been read and the FIFO has less samples then the set threshold value.	
	Logic "0"	Disable Interrupt
	Logic "1"	Enable Interrupt
Bit-12	Interrupt Pending. **Read** of this bit reflects the interrupt pending status of the ADC logic.	
	Logic "0"	Interrupt Not Pending
	Logic "1"	Interrupt Pending
Bit-13	FIFO Empty Status[3, 4]	
	Logic "0"	FIFO Not Empty
	Logic "1"	FIFO Empty
Bit-14	FIFO Threshold Status: This bit is set when there are more samples in the FIFO than the set threshold value.	
	Logic "0"	FIFO Quantity ≤ Threshold Value
	Logic "1"	FIFO Quantity > Threshold Value
Bit-15	FIFO Full Status[3, 4]	
	Logic "0"	FIFO Not Full
	Logic "1"	FIFO Full

Table 3.7 *ADC Control/Status Register*

All unused bits will return logic "0" when read.

1. For the FIFO reset to function correctly an ADC clock (from the AXM-A30) must be present.

2. Due to the dual clocking nature of the FIFO, allow at least 10us for the reset command to complete after setting this bit.

3. If both the FIFO Empty and FIFO Full Flags are set, the FIFO is in reset mode. An ADC clock must be provided for each channel before the FIFO will operate properly.

4. The status flags are only affected by an ADC FIFO Reset (Bit 5).

ADC Conversion Threshold Register (Read/Write) – (Base Addr + 8108, 810AH)

WARNING: *Be aware that the due to the dual clocking nature of the FIFO, there is a five clock cycle delay for an accurate count of samples in the FIFO. Therefore, when using the stop conversion at threshold function there may be more samples in the FIFO then set by the threshold register. The actual number of additional samples will vary depending of the frequency of the ADC and local bus clock.*

The ADC Conversion Threshold register is a 13-bit read/write register. This threshold register holds a minimum count of conversion to execute before setting bit-14 of the ADC control register and/or issuing of an interrupt. The ADC FIFO is 8191 samples deep and this threshold register can be set to any value between 0 and 8190. Note that when using this register in conjunction with the stop conversion at threshold bit, there may be more samples in the FIFO then indicated by the threshold register. The actual number of additional samples will vary depending of the ADC clock frequency. Interrupts, if desired, must be enabled via bit-11 of the ADC Control/Status register.

The ADC Conversion Threshold register at Base Address + 8108H corresponds to the first on board ADCs, while the ADC Conversion Threshold register at Base Address + 810AH corresponds to the second on board ADCs. The default power-up state of these registers is logic low. Reading or writing to these registers is possible via 32-bit, 16-bit or 8-bit data transfers.

ADC FIFO Read Port (Read Only) – (Base Addr + 810C, or 810EH)

WARNING: *Due to pipeline delay within the ADC, the first 16 samples in the FIFO may be invalid.*

WARNING: *Be aware that the due to the dual clocking nature of the FIFO, the FIFO status bits may be up to five clock cycles behind actual read/write operations.*

Each ADC channel has a dedicated 8191 sample deep FIFO buffer. The ADC samples are 16-bit data values. The ADC FIFO register at Base Address + 810CH corresponds to the first on board ADCs, while the ADC FIFO register at Base Address + 810EH corresponds to the second on board ADCs. FIFO status can be read from the ADC Control/Status Registers. Reading the FIFO is possible via 16 or 32-bit data transfers only. The FIFO will be cleared with either software or hardware reset.

Care should be taken when reading data from the FIFO buffer to insure the FIFO is not empty when a new read is performed. The FIFO Empty/Full status can be read via bits 13 to 15 of the ADC Control/Status register. Reading an empty FIFO will indefinitely return the last good value.

A FIFO Reset via bit 5 of an ADC Control/Status Register may take up to 10us to complete. During this time reading and writing the FIFO will have unpredictable results.

ADC REGISTERS

ADC DP-SRAM OVERRIDE REGISTER (Read/Write) – (Base Addr + 8134H)

This register can be used in conjunction with the Dual-Port SRAM Control Register at Base Address plus 8040H to stream data from an ADC Channel to the SRAM. To stream data to the SRAM, first write the starting address at which data begins filling the SRAM to the SRAM Internal Address register (Base Addr. + 8044H). Write the end address to the DMA Channel 1 Threshold Register (Base Addr. + 804CH). Then select the ADC channel to route to the SRAM via bits 8 and 9 of this register. Enable the override by setting bit 0 of this register. Set the enable for the proper ADC channel via bits 5 & 6 of the Board Control Register (Base Addr. + 8100H). Then start the transfer by setting bit-0 of the Dual-Port SRAM Control Register (Base Addr. + 8040H). Bit-0 of the Dual-Port SRAM Control Register (Base Addr. + 8040H) will automatically be disable once the SRAM is filled to the address specified in the DMA Channel 1 Threshold Value. Reset on DMA Thresholds (bits 3 and 4 of the Dual-Port SRAM Control Register) must be disabled for proper operation of the ADC SRAM Override. These registers can be read or written via 32-bit, 16-bit or 8-bit data transfers. A power-up or software reset sets all bits to 0.

WARNING: Due to the different clock domains between the ADC and the SRAM, the ADC to SRAM feature will only function with ADC clocks less then 66MHz in the example design.

WARNING: Due to pipeline delays & synchronization issues the data located at the first 16 addresses and end addresses in the SRAM may not be valid.

BIT	FUNCTION	
0	ADC SRAM Override. Setting this bit to 1 will allow the data from one ADC channel to be routed to SRAM (as opposed to data from the Rear I/O). Refer to the procedure described in the paragraph above.	
7-1	Not Used	
8	Logic "0"	Disable Channel 1 Storage to SRAM (Default)
	Logic "1"	Enable Channel 1 Storage to SRAM
9	Logic "0"	Disable Channel 2 Storage to SRAM (Default)
	Logic "1"	Enable Channel 2 Storage to SRAM
15-10	Not Used	

Table 3.8 *ADC SRAM Override Register*

Refer to the Base PMC module User's Manual for further information on SRAM operation

ADC CALIBRATION

Uncalibrated ADC Performance

The uncalibrated ADC performance is affected by two primary error sources. These are the differential ADC driver and the Analog to Digital Converter (ADC). The untrimmed differential ADC driver and ADC have offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated ADC Performance

Accurate calibration of the ADC digitized values can be accomplished by using external precision reference voltages. The external reference voltages are used to determine two points of a straight line which defines the analog input characteristic.

The calibration voltages (1.55 and –1.55) are used to find two points that determine the straight line characteristic of the analog channel.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages. The ideal voltage span is typically 3.4 volts (±1.7 volts) into a 50Ω load.

Equation (1):

$$\text{Correct_Count} = \left(\frac{65{,}536}{V_{Full}} \times \text{m} \right) \times \left[\text{Count}_{out} + \frac{-1.55 + (V_{Full}/2)}{\text{m}} - \text{Count}_{out@\text{-}1.55v} \right] \quad (1)$$

where, "**m**" represents the actual slope of the transfer characteristic as defined in equation 2:

Equation (2):

$$\text{Slope} = \text{m} = \left(\frac{1.55_{vhigh} - \left(-1.55_{vlow}\right)}{\text{Count}_{out\,@\,1.55v} - \text{Count}_{out\,@-1.55v}} \right) \quad (2)$$

Vhigh	=	High Calibration Voltage = 1.55 volts
Vlow	=	Low Calibration Voltage = -1.55 volts
$\text{Count}_{out@1.55v}$	=	Actual ADC Data Read With High Calibration Voltage Applied
$\text{Count}_{out@-1.55v}$	=	Actual ADC Data Read With Low Calibration Voltage Applied
Count_{out}	=	Actual Uncorrected ADC Data For Input Being Measured
V_{FULL}	=	This is the full scale voltage. (Typically 3.4V)

The calibration parameters (**$\text{Count}_{out@1.55v}$** and **$\text{Count}_{out@-1.55v}$**) should not be determined immediately after startup but after the module has reached a stable temperature to obtain the best accuracy. Note that several readings (e.g. 512) of the calibration count parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

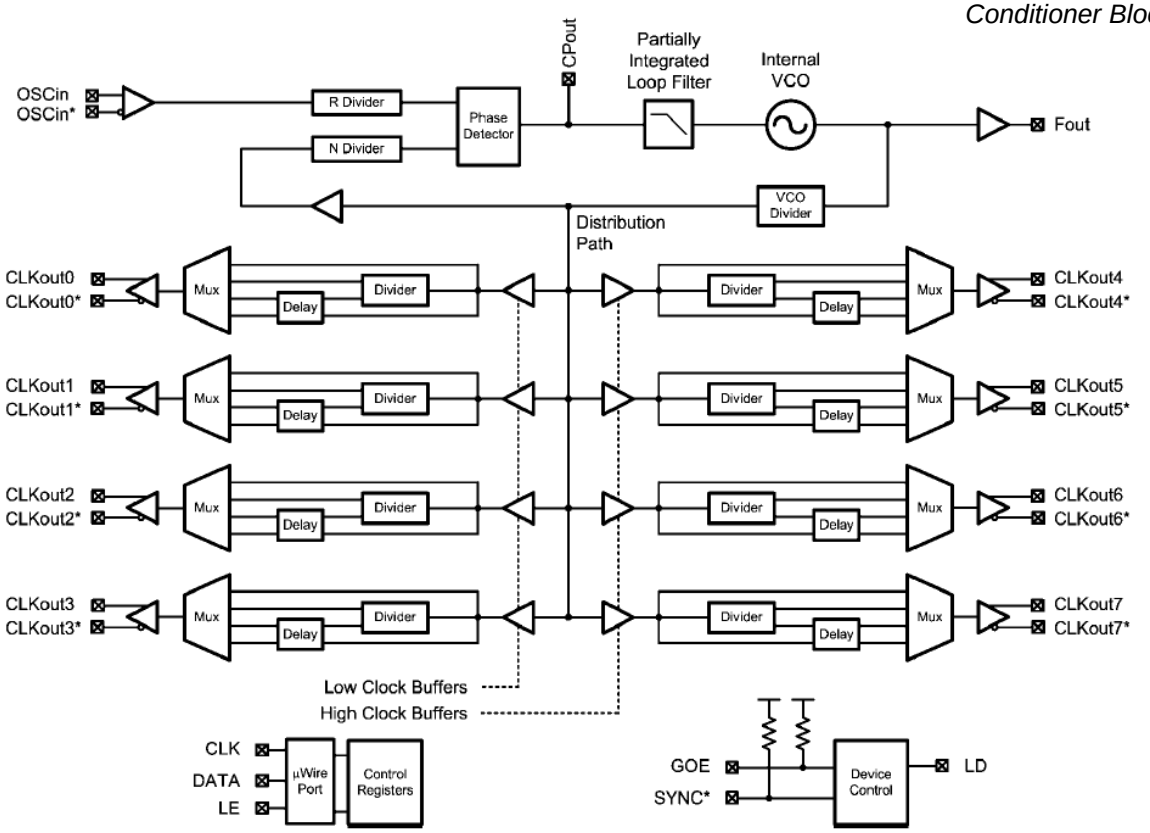
CLOCK CONDITIONER

The AXM-A30 module uses a National Semiconductor clock conditioner IC to reduce the jitter of the analog clocks. There are three possible sources for the clock conditioner input clock, an external user input, an on-board 100MHz crystal, or from the FPGA. To minimize board level noise only one clock should be active at any given time. Furthermore to achieve the best results from the AD conversion, the conditioner input clock must have low jitter (<2ps) and excellent stability (±50ppm) over temperature. A clock with more jitter or inferior stability can be used, but it will compromise the AD accuracy and noise specifications. Given that the clock from the FPGA has a typical jitter of 200ps it should only be used for proof of concept examples.

The clock conditioner contains a PLL with multiple output buffers and supplementary division circuitry as shown Figure 3.1. The PLL and external circuitry has been optimized for the on board oscillator. However in most cases an external clock via a frequency between 1MHz and 105MHz can be used with little change in AD specifications.

For further information on the LMK03000C precision clock conditioner please refer the device data sheet, the AXM-A30 Clock Calculator program included with the EDK or the reference book "PLL Performance, Simulation, and Design. Fourth Edition" by Dean Banerjee.

Figure 3.1: *LMK03000C Clock Conditioner Block Diagram*



Programming the LMK03000C

The LMK03000C device contains a set of write only registers that must be programmed correctly for proper operation. To facilitate programming the applicable registers have been duplicated in the AXM-A30 example design memory map. The duplicated registers contain an RX reference, where X is a number between 0 and 15. Each of these registers must be written using 32-bit data transfers. After each register is written, it is sent over a serial connection to the LMK03000C. Due to this connection, programming one register on the LMK03000 requires up to 10us. During programming the user must not write to any other Clock Conditioner Registers. Writing to a Clock Control Register while programming is in progress will cause errors. To prevent problems, poll Bit 0 of the Clock Condition Control/Status Register at Base Addr. + 8110H. If the status bit is high, then serial programming is in progress and no writes should occur. If the bit is low then it is safe to perform another write.

WARNING: *Failure to follow the proper clock programming procedure will result in improper ADC operation.*

The LMK03000C device requires that the registers be programmed sequentially to avoid configuration errors. Follow the example procedure below to program the clock conditioner.

Clock Conditioner Programming Procedure

1. Set the Clock Control Source bits (3-4) of the AXM-A30 Board Control Register (Base Addr. + 8100H).
2. Disable the Clock Generator outputs by writing 0 to bit 4 of the Clock Conditioner Control/Status Register (Base Addr. + 8110H).
3. If using an external clock verify that a valid clock signal is available to the LMK03000C device. Failure to have an active clock during programming will result in unstable outputs.
4. Program R0 with the Reset bit (31) active. This will ensure that all clock conditioner registers are in their default state.

Use the ***Clock Calculation Program*** *provided in the EDK to provide the proper values for the Clock Conditioner Registers.*

5. Write the following registers in sequence: R0, R1, R3, R4, R11, R13, R14, R15. After writing each register poll the Clock Conditioner Control/Status Register (Base address + 8110H) Bit 0. Do not perform another write until this bit reads logic '0'.
6. Poll the Lock Detect Bit of the Clock Conditioner Control/Status Register (Base Addr. + 8110H). Once this bit is high, write logic high to the bit 5 (Synch enable) in same register to synchronize all outputs to the input clock. If the Lock Detect Bit Fails to read high, then there may be a problem with your input clock. The clock may not meet the specifications as noted in section 6.0 of this manual or the values you entered for the R registers are invalid.
7. Wait at least 10us, then enable the clock generator outputs by writing 1 to bit 4 of the Clock Conditioner Control/Status Register (Base Addr. + 8110H).

Programming the LMK03000C

Clock Conditioner Register Recommended Values.

Acromag recommends the following values for the clock conditioner registers when you are using the 100MHz internal oscillator (See Table 3.8a), or an 10MHz external clock (see table 3.8b). In all cases both ADC channels enabled, and the remaining two clocks are disabled. Note that these values are not the same as the reset values. For users who which to customize the clock, refer to the AXM-A30 clock calculation program provided in the EDK to determine the appropriate register values.

Register	Address (Base Addr+)	Acromag Recommended Values for 100MHz Internal Oscillator (In Hex)			
		5MHz	31MHz	77.5MHz	105MHz
R0	8114H	00023E00	00020A00	00020400	00020300
R1	8118H	00023E01	00020A01	00020401	00020301
R3	811CH	00033E03	00030A03	00030403	00030303
R4	8120H	00033E04	00030A04	00030404	00030304
R11	8124H	0082000B	0082000B	0082000B	0082000B
R13	8128H	0299005D	0299005D	0299005D	0299005D
R14	812CH	083FFF0E	083FFF0E	083FFF0E	083FFA0E
R15	8130H	08632D0F	08632D0F	08632D0F	0864A70F

Table 3.8a: *LMK03000C Register Values for various frequencies using the internal 100MHz oscillator.*

Register	Address (Base Addr+)	Acromag Recommended Values for 10MHz External Clock (In Hex)			
		5MHz	31MHz	77.5MHz	105MHz
R0	8114H	00023E00	00020A00	00020400	00020300
R1	8118H	00023E01	00020A01	00020401	00020301
R3	811CH	00033E03	00030A03	00030403	00030303
R4	8120H	00033E04	00030A04	00030404	00030304
R11	8124H	0082000B	0082000B	0082000B	0082000B
R13	8128H	0282805D	0282805D	0282805D	0282805D
R14	812CH	083FFF0E	083FFF0E	083FFF0E	083FFF0E
R15	8130H	0BDFC20F	0BDFC20F	0BDFC20F	0BEFC10F

Table 3.8b: *LMK03000C Register Values for various frequencies using a 10 MHz external clock.*

CLOCK CONDITIONER REGISTERS

Clock Conditioner Control/Status Register (Read/Write) – (Base Addr + 8110H)

This read/write register is used to set the LMK03000C global settings including a global output enable and global clock synchronization. Bit 0 is the clock conditioner serial programming status bit. If this bit is high then serial programming of the clock conditioner is in progress. Do not write to any of the Clock Conditioner Registers while this bit is high. Bit 1 is the clock conditioner lock indicator. The functionality of this pin is determined via the PLL_MUX bits in the Clock Conditioner R14 PLL Control Register at Base Addr. + 812CH. These bits must be set to "0011" to achieve the active high clock lock indicator. Bit 4 is the LMK03000C Global Clock Enable. All clock outputs should remain disabled until the device is locked. The LMK03000C clock output synchronization function can be activated by writing logic high to bit 5 of this register. This action will cause an active low pulse of at minimum 2us on the LMK03000C Synch pin. Refer to the LMK0300C User Manual for further information. The remaining bits in this register are not used and will return "0" when read. Register functionality is described in more detail in Table 3.9.

Note that this register in not effected by a standard board reset. These registers are only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of these registers is logic low. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Table 3.9 *Clock Conditioner Control/Status Register*

BIT	FUNCTION	
0	Clock Conditioner Serial Programming Status	
	Logic "0"	No action.
	Logic "1"	Clock Conditioner programming in process. Do NOT write to any Clock Conditioner Registers if this bit is logic high.
1	Clock Conditioner Lock Detect[1,2]	
	Logic "0"	Clock Conditioner Output not Locked
	Logic "1"	Clock Conditioner Outputs Locked
3-2	Not Used	
4	Clock Conditioner Global Output Enable	
	Logic "0"	Disable all Clock Outputs (Default)
	Logic "1"	Enable Clock Outputs
5	Writing a Logic "1" to this bit will cause the Clock Conditioner Sync pin to transition low for 8 clock cycles. All Clock outputs enabled will be synchronized 20us after writing this bit. The user should disable all clocks via the Global Output enable bit prior to using this function. The clocks can then be re-enable after approximately 20us.	
31-6	Not Used	

1. Bits 23 to 20 of the R14 PLL Control Register at Base Address + 812CH must be set to "0011" to achieve the described functionality of the lock detect status bit.

2. Lock Detection will fail if the input clock is unstable, has a large amount of jitter, or if one of the Clock Control Registers is improperly set.

Clock Conditioner R0/R1/R3/R4 CLK Control Registers (Read/Write) – (Base Addr + 8114, 8118, 811C, 8120H)

CLOCK CONDITIONER REGISTERS

These registers are accessible via 32-bit data transfers only!

The Clock Conditioner R0/R1/R3/R4 CLK Control Registers correspond directly to the R0, R1, R3 and R4 Registers as outlined in the LMK03000C Datasheet. Register R0 at base address + 8114H controls the clock output routed to the FPGA on the PMC base board. Register R1 at base address + 8118H controls the clock output routed to the General Purpose Output. Register R3 at base address + 811CH controls the clock output routed to ADC Channel 1. Register R4 at base address + 8120H controls the clock output routed to ADC Channel 2.

Bits 0 to 3 of each register are fixed at outlined in Table 3.10. Bits 4 through 7 correspond to each clock's output delay setting. The following bits 8 to 15 relate to the final divider prior to the clock output. Bit 16 is a clock enable. Bits 17 and 18 determine if the output from the PLL is divided, delayed, or both per the Delay and Divide values. Refer to the LMK03000C Datasheet for further information.

Note that these register are not affected by a standard board reset. These registers are only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of these registers is logic low unless otherwise stated in the Table 3.10.

Reading or writing to these register is possible via 32-bit data transfers only. After writing to a register, the corresponding register of the LMK03000C will be programmed serially. Serial programming is indicated by bit 0 of the Clock Conditioner Control Register at Base Address + 8110H. Do not write to any other Clock Conditioner Register until serial programming of the previous register is complete.

CLOCK CONDITIONER REGISTERS

Table 3.10 *Clock Conditioner CLK Control Registers*

Note: In this table, X is a placeholder corresponding to either the R0, R1, R3, or R4 Register.

BIT	FUNCTION	
3-0	Address Reference Bits: These bits are fixed for each register as detailed blow.	
	R0	"0000"
	R1	"0001"
	R3	"0011"
	R4	"0100"
7-4	CLKoutX_DLY: These bits control delay stage for each clock output. The delay added is equal to 150ps times this binary value here plus 400ps.	
15-8	CLKoutX_DIV: These bits control the clock output divider value. The actual clock divide value is equal to twice the binary value of these bits. The allowable values are binary 01H to FFH corresponding to divide values of 2 through 510. The default value of these bits is 01H.	
16	CLKoutX_EN: This bit is a Local Output Enable. Setting this bit to one will enable a specific clock output. Note that this bit must be set in addition to the Global Output Enable bit in the Clock Conditioner Control Register.	
18-17	CLKoutX_MUX: These bits control the Clock Output Multiplexer for each clock output.	
	Logic "00"	Bypassed (Default)
	Logic "01"	Divided (Adds 100ps delay)
	Logic "10"	Delayed
	Logic "11"	Divided and Delayed (Adds 100ps delay)
30-19	Not Used	
31	Clock Conditioner RESET bit – R0 Only. This bit is only in register R0. Setting this bit to '1' forces all Clock Conditioner registers to their reset condition and automatically will clear this bit. Note that the reset procedure requires up to 10us to complete. After setting this bit, R0 will have to be programmed again. For all other registers this bit is not used.	

CLOCK CONDITIONER REGISTERS

Clock Conditioner R11 PLL Control Registers (Read/Write) – (Base Addr + 8124H)

This registers controls the PLL input divider. It corresponds directly to the R11 Register as described in the LMK03000C Data sheet. Bits 0 to 3 are fixed address bits. Bit 15 is the PLL DIV4 bit. For stability purposes, this bit must be set if the frequency of the phase detector (Input Frequency / R) within the PLL is greater then 20MHz. All other bits in this register are fixed as outline in Table 3.11.

Note that this register is not affected by a standard board reset. This register is only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of this register is logic low unless otherwise stated in Table 3.11.

Reading or writing to this register is possible via 32-bit data transfers only. After writing to a register, the corresponding register of the LMK03000C will be programmed serially. Serial programming is indicated by bit 0 of the Clock Conditioner Control Register at Base Address + 8110H. Do not write to any other Clock Conditioner Register until serial programming of the previous register is complete.

Table 3.11 *Clock Conditioner R11 PLL Control Register*

BIT	FUNCTION
3-0	Address Reference Bits: These bits are fixed for each register as detailed blow.
	R11 "1011"
14-4	Not Used.
15	DIV4: These bits must be set to 1 if the phase detector frequency (Input Freq. / R) is greater then 20MHz.
31-16	Not Used. Default "0000000010000010"

Clock Conditioner R13 PLL Control Registers (Read/Write) – (Base Addr + 8128H)

This registers controls the internal VCO filter options and defines the input frequency. It corresponds directly to the R13 Register as described in the LMK03000C Data sheet. Bits 0 to 3 are fixed address bits. Bits 4 through 13 select resistor and capacitor values for the VCO internal loop filter. These bits should be programmed to "0000000101". Varying from these values may induce noise and/or cause clock instability. Bits 14 to 21 are the input frequency in MHz. This value should be set to 100 if you are using the on board oscillator. Otherwise they should be set to the external clock or FPGA clock input frequency. If the input frequency is not a multiple of 1MHz, then round to the closet value.

CLOCK CONDITIONER REGISTERS

Note that this register is not affected by a standard board reset. This register is only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of this register is logic low unless otherwise stated in Table 3.12.

Reading or writing to this register is possible via 32-bit data transfers only. After writing to a register, the corresponding register of the LMK03000C will be programmed serially. Serial programming is indicated by bit 0 of the Clock Conditioner Control Register at Base Address + 8110H. Do not write to any other Clock Conditioner Register until serial programming of the previous register is complete.

Table 3.12 *Clock Conditioner R13 PLL Control Register*

BIT	FUNCTION
3-0	Address Reference Bits: These bits are fixed for each register as detailed blow.
	R13 "1101"
7-4	VCO_C3_C4_LF: These bits control the capacitor value for the internal loop filter. Default value "0000". Acromag recommended value"0101".
10-8	VCO_R3_LF: These bits control the R3 resistor value in the internal loop filter. Default value "000". Acromag recommended value "0000".
13-11	VCO_R4_LF: These bits control the R4 resistor value in the internal loop filter. Default value "000". Acromag recommended value "0000".
21-14	OSCin_FREQ: These bits define the clock input frequency (in MHz). Default "00000000". Use "01100100" for on board oscillator (100MHz).
31-22	Not Used. Default "0000001010".

Clock Conditioner R14 PLL Control Registers (Read/Write) – (Base Addr + 812CH)

This registers controls PLL_R Divider value, the functionality of the Lock Detect pin, plus Power down and global output enables. It corresponds directly to the R14 registers as described in the LMK03000C Datasheet. Bits 0 to 3 are fixed address bits. Bits 8 to 19 is the value for the PLL R divider. Note that the PLL R divider cannot be set to 0 (illegal divide). This value can be calculated using "AXM_A30_Clock_Cal.exe" program provided in the EDK. Bits 20 through 23 determine the functionality of the lock detect pin and should be set to "0011". This sets the lock detect pin as an active high digital lock detect. Device power down can be enabled via bit 26. There is an additional clock output global enable on Bit 27. Bit 28 determined the functionality of the Fout pin and should always be disabled (logic '0').

Note that this register is not affected by a standard board reset. This register is only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of this register is logic low unless otherwise stated in Table 3.13.

Reading or writing to this register is possible via 32-bit data transfers only. After writing to a register, the corresponding register of the LMK03000C will be programmed serially. Serial programming is indicated by bit 0 of the Clock Conditioner Control Register at Base Address + 8110H. Do not write to any other Clock Conditioner Register until serial programming of the previous register is complete.

Table 3.13 *Clock Conditioner R14 PLL Control Register*

BIT	FUNCTION
3-0	Address Reference Bits: These bits are fixed for each register as detailed blow.
	R14 | "1110"
7-4	Not Used. Default "0000".
19-8	PLL_R[1]: These bits control the PLL R Divider. Default value "000000001010".
23-20	PLL_MUX: These bits control the functionality of the Lock Detect output pin. This pin can be read from Bit 1 of the Clock Condition Control/Status Register at Base Address 8110H. Default value "0000". Acromag recommended value "0011.
25-24	Not Used. Default "00".
26	POWERDOWN: Setting this bit to logic '1' will power down the entire device regardless of other settings. This bit must be reset to "0" to continue normal operations.
27	EN_CLKout_Global[2]: This bit overrides the individual CLKoutX_En bits. When this bit is set to 0 all clock outputs are disable. Default '1' (Enabled).
28	EN_Fout: This bit must be set to logic '0' to disable the Fout pin.
31-29	Not Used. Default "000".

1. Refer to the Acromag "AXM_A30_Clock_Cal.exe" program to determine the value to write to PLL_R.

2. Acromag recommends that you set this bit to '1' and use the local clock enables plus the global output enable pin accessible from the Clock Conditioner Control/Status Register as Base Address +

Clock Conditioner R15 PLL Control Registers (Read/Write) – (Base Addr + 8130H)

WARNING: *The clock (external or internal) must be active and enabled prior to writing to the Clock Conditioner R15 PLL Control Register.*

This registers controls the PLL_N divider value, the VCO Divider Value and the charge pump gain. It corresponds directly to the R15 Register as described in the LMK0300C Datasheet. Bits 0 to 3 are fixed address bits. The PLL_N divider encompasses bit 8 through 25. The PLL N divider cannot be set to 0 (illegal divide). Bits 26 to 29 contain the VCO divider value. The only valid VCO divider values are 2 through 8. The VCO divider cannot be bypassed. The charge pump gain is set via bits 30 and 31. To determine the PLL_N, VCO divider, and charge pump gain refer to "AXM_A30_Clock_Cal.exe" program provided in the EDK. Writing to this register will cause the LMK03000C device to active the frequency calibration routine. As such an input clock must be applied to the clock conditioner part prior to writing to this register.

Note that this register is not affected by a standard board reset. This register is only reset at power-up and when logic '1' is written to bit 31 of Clock Conditioner R0 CLK Control Register at Base Address + 8114H. The default power-up state of this register is logic low unless otherwise stated in Table 3.14.

Reading or writing to this register is possible via 32-bit data transfers only. After writing to a register, the corresponding register of the LMK03000C will be programmed serially. Serial programming is indicated by bit 0 of the Clock Conditioner Control Register at Base Address + 8110H. Do not write to any other Clock Conditioner Register until serial programming of the previous register is complete.

Table 3.14 *Clock Conditioner R15 PLL Control Register*

BIT	FUNCTION
3-0	Address Reference Bits: These bits are fixed for each register as detailed blow.
	R15 | "1111"
7-4	Not Used. Default "0000".
25-8	PLL_N[1]: These bits control the PLL N Divider. Default value "00000001011111000" (760).
29-26	VCO_DIV[1]: These bits program the divide value for the VCO Divider. Default value "0010".
31-30	PLL_CP_GAIN[1]: These bits set the charge pump gain of the PLL. Default "00".

1. Refer to the Acromag "AXM_A30_Clock_Cal.exe" program to determine these values.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the board. A description of the basic functionality of the circuitry used on the board is also provided. Note that each section does not necessarily apply to every model. Refer to table below to determine the appropriate sections.

SMA FIELD CONNECTORS

The field I/O interface to the board is provided through four front SMA connectors (refer to Table 2.1). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operational errors, and with extreme abuse, possible circuit damage.

TWO ADC CHANNELS

The board contains two high performance ADCs that operate on a 3.2V peak to peak single-ended bipolar input signal. The ADC paths are independent. Each of the ADC's paths consist of a SMC connector, 50Ω resistor to ground, differential ADC driver, lowpass filter, series resistor. The positive and negative outputs of the differential ADC driver connect to the respective inputs of the ADC via an LC lowpass filter. The lowpass filter limits the output noise of the ADC driver into the ADC input. In addition, the positive and negative outputs of the differential driver connect to a pair of series resistors to minimize the effects of transient currents that arise due to overshoot of the LC filter and because of the switched-capacitive front end of the ADC . Also a shunt capacitor is placed across the ADC inputs to provide dynamic charging currents.

The ADA4937-1 differential ADC driver is designed to give low harmonic distortion as an ADC driver. The circuit operates from a +5 volt supply. A 3.4V peak to peak bipolar single-ended input signal produces a 1.6V peak to peak differential signal at the output of the ADA4937, centered around a Common Mode voltage of 3.2V.

Sampling of the ADC occurs on the rising edge for ADC Channel 1 and the falling edge for ADC Channel 2 of the ADC clock. The clock signal alternatively switches the sample and hold amplifier between sample mode and hold mode. The ADC clock signal is driven by a clock conditioner IC. The conditioner circuit is used to minimize the jitter and noise passed on the ADC. The conditioner is driven by either a low jitter crystal oscillator, the FPGA, or directly driven by the SMA ADC clock input. The clock conditioner will synchronize the rising edge of the clock output to that of the input. Acromag recommends using the crystal oscillator for best ADC performance. Use of the FPGA clock should be avoided at high frequencies due to its large jitter (200ps).

THEORY OF OPERATION CONTINUED

An input clock duty cycle stabilizer for each ADC is available on the PMC-AX1065, PMC-AX2065, and PMC-AX3065 models. Input clock rates of over 40MHz can use the duty cycle stabilizer. The duty cycle stabilizer provides an ADC clock with a nominal 50% duty cycle.

The board is configured to use the ADC internal 1.6 volt fixed reference. The input span of the ADC will be twice the value of the reference voltage.

PMC BASE BOARD CONNECTION

The AXM-A30 expansion I/O modules are attached to the PMC base board via a high speed 150 pin header. The connector provides power to the extension board and multiple logic connections to the base board. Note that any PMC base board with a re-configurable FPGA will require the pin definitions provided in the EDK to properly operate the AXM-A30 boards. Refer to the AXM Board Design Guide for further information on the interconnection between the AXM-A30 module and the PMC base board.

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

SERVICE AND REPAIR ASSISTANCE

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

www.acromag.com

Acromag's application engineers can also be contacted directly for technical assistance via telephone or email. Contact information is located at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Single AXM Board

Height	11.5 mm (0.453 in)
Stacking Height	5.0 mm (0.197 in)
Depth	31.0 mm (1.220 in)
Width	74.0 mm (2.913 in)
Board Thickness	1.6 mm (0.062 in)

Unit Weight (Including all mounting hardware)
AXM-A30: 41.3g (1.46oz)

Connectors

- **AXM-A30 Front Field I/O:** 4 SMA Connectors

Table 6.1: Power Requirements for Example Design

Power Requirements			
		TYP[2]	**MAX**
3.3V (±5%)[1]	AXM-A30	460mA	900mA
5V (±5%)[1]	AXM-A30	600mA	800mA

1. Power source is the base board. Current draw is for AXM module only.
2. Typical assumes 1 ADC in operation at 105MHz with one clock output enabled from the LMK03000C.

ENVIRONMENTAL

The AXM-A30 requires adequate air circulation. Still air will cause the module to exceed its maximum allowable temperature!

Operating Temperature: 0°C to +70°C
Relative Humidity: 5-95% Non-Condensing.
Storage Temperature: -55°C to 150°C.
Non-Isolated: Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI): Complies with EN61000-4-3 (3V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no register upsets.

Conducted R F Immunity (CRFI): Complies with EN61000-4-6 (3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.

SPECIFICATIONS

Electromagnetic Interference Immunity (EMI): No register upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity: Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient (EFT) Immunity: Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.

Electrostatic Discharge (ESD) Immunity: Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) Level 2 (4KV enclosure port contact discharge) Level 1 (2KV I/O terminals contact discharge) and European Norm EN50082-1.

Radiated Emissions: Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

Reliability Prediction

Mean Time Between Failure: MIL-HDBK-217F, Notice 2, at 25°C
AXM-A30: 1,972,542 Hours

ADC Specifications

Channel Configuration: 2 Single-ended via SMA connectors into 50Ω.

ADC: Analog Devices AD9460-105

Analog Input

- **Input Range**: Bipolar 3.2Vp-p (+/-1.6Volts)
- **Input Gain**: 0.9V/V
- **ADC Resolution**: 16-Bits
- **Data Format**: 2's Complement (DFS High) or Offset Binary (DFS Low)
- **No Missing Codes**: 16-bits
- **ADC Integral Linearity Error**:+/-30 LSB, Typ
- **DC Offset Error**: 0.2V +/-1% FSR
- **Gain Error**: +/-1% FSR
- **Input Signal Type**: Voltage (Non-isolated)
- **Pipeline Delay:** Thirteen Clock Cycles
- **Signal to Noise Ratio (SNR):** 65 dB Min
- **Analog Input Memory FIFO Buffer:** 8191 Sample Memory

ADC Driver: Analog Devices ADA4937-1

Differential ADC Driver

- **Input Range**: 3.2 p-p Min
- **Offset Voltage**: Min 0V, Max 0.2V
- **Bandwidth**: 190Mhz (@ 3dB)
- **Common-Mode Voltage**: 3.3V
- **Gain**: 0.9Min, 1 Max
- **Input Impedance**: 55Ω ±10%

Internal Clock

- **Crystal Oscillator:** 100 MHz On board crystal 2ps Jitter Max.
- **FPGA Clock:** 16.66MHz. 200ps Jitter Typ.

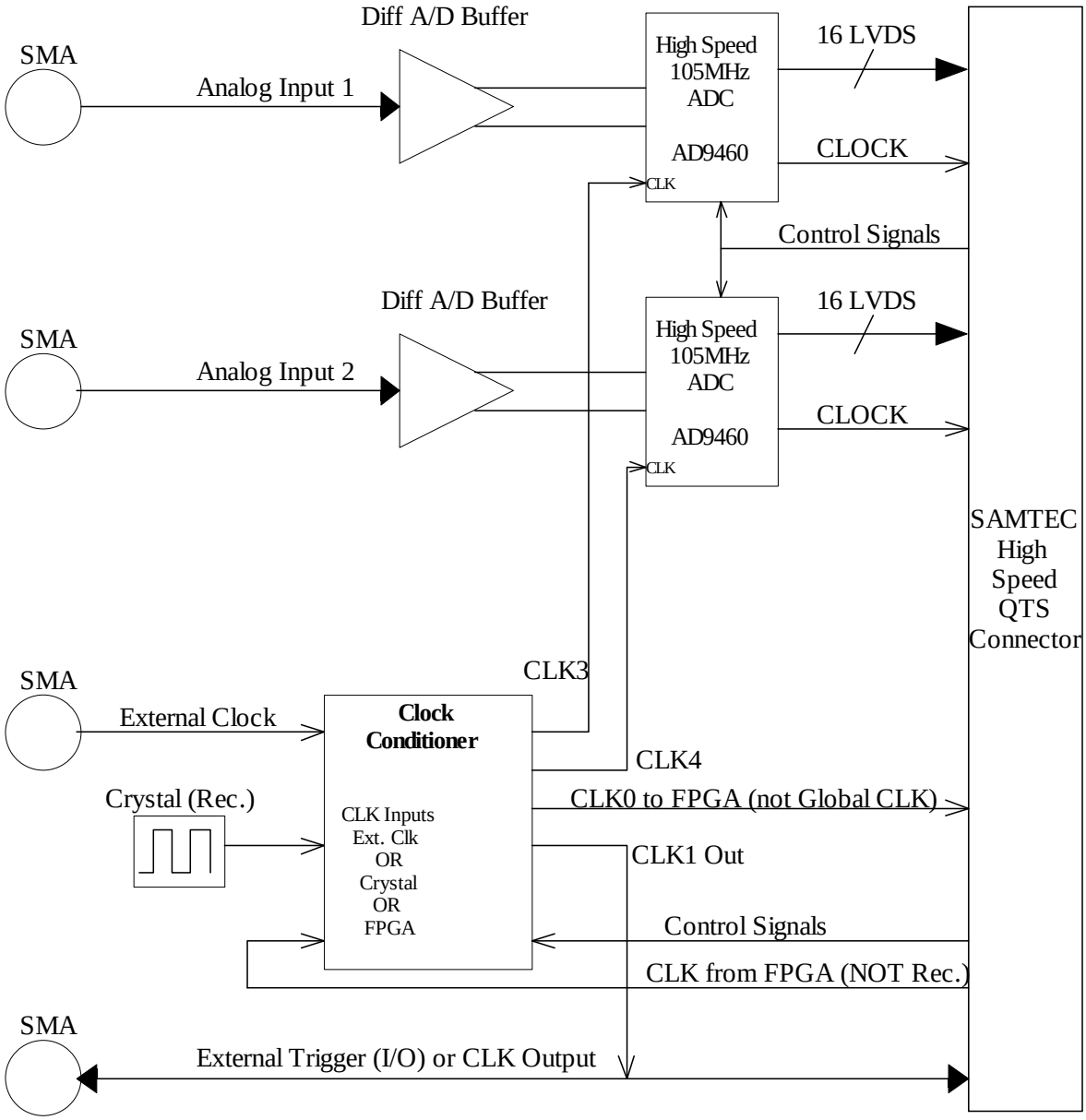
External Clock

- **Channel Configuration:** 1 Single-ended via SMA capacitively coupled
- **External Clock Frequency**: 1MHz minimum, 100MHz maximum

- **External Clock Voltage Buffer**: 1.6V $_{p-p}$ minimum, 3.3V $_{p-p}$ maximum. Note that external clock is buffered prior to the LMK03000C.

DRAWINGS

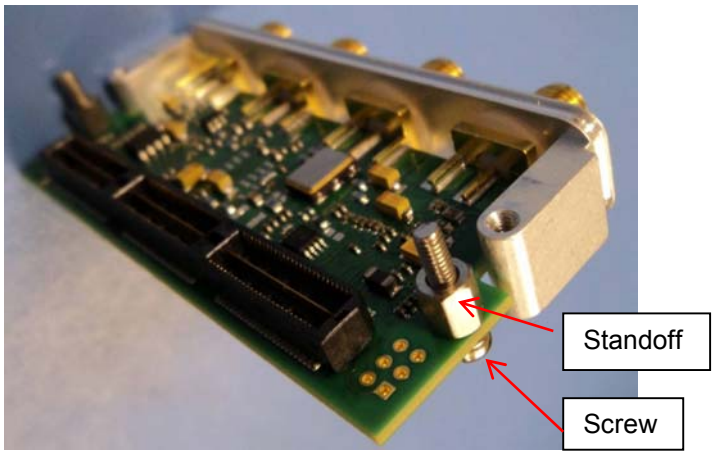
AXM-A30 BLOCK DIAGRAM



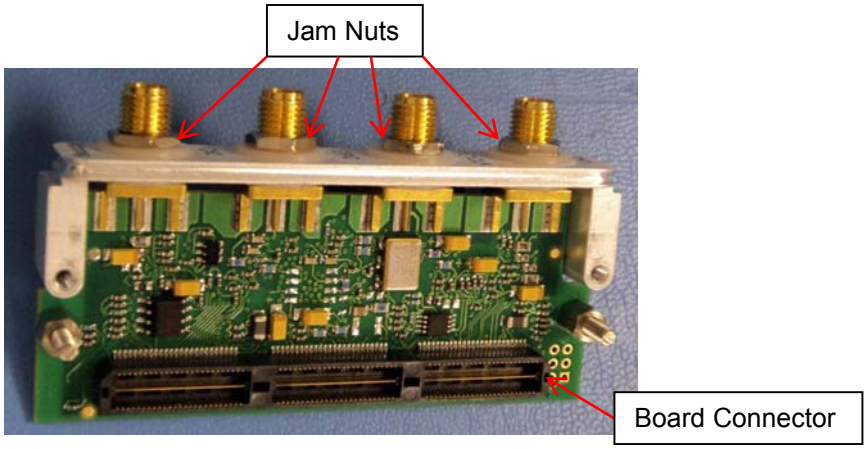
Assembly Procedure for AXM-A30 onto PMC Module:

DRAWINGS

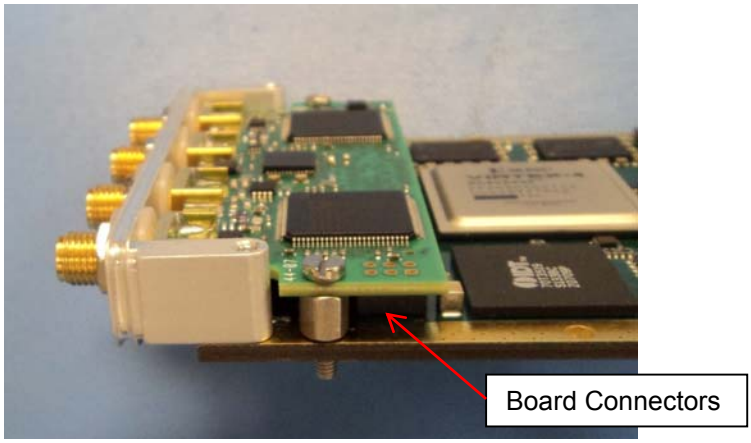
1) Install two M2.5 x 12mm Cheese Head Screws and two M2.5 x 5mm Hex Standoffs as shown, and then tighten.



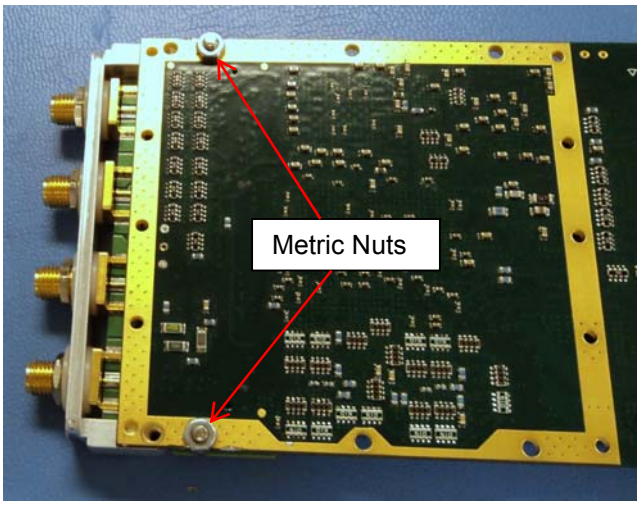
2) Loosen all four Jam Nuts on SMA connectors (3 to 4 turns) as shown.



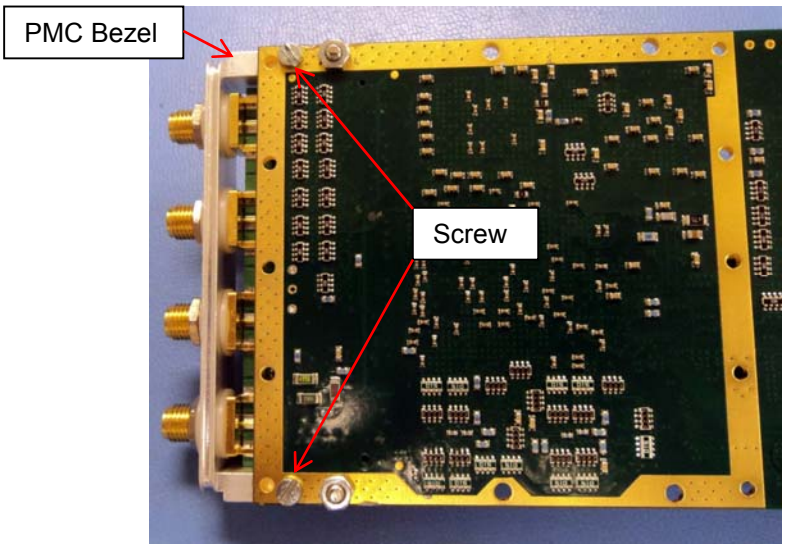
3) Attached AXM-A30 module to PMC module, making sure that the board connectors are properly seated.



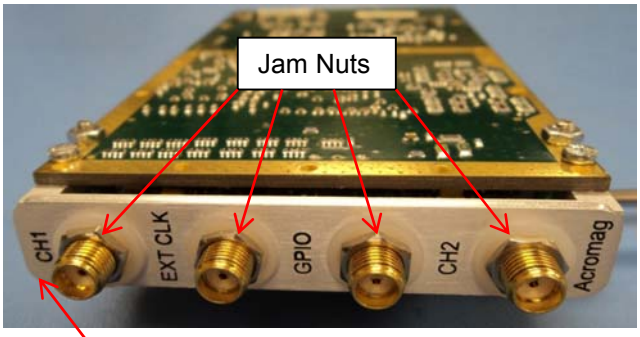
4) Then install two Metric Nuts as shown, and then tighten.



5) Install two M2.5 x 5mm Cheese Head Screws to PMC Bezel as shown, and then tighten.



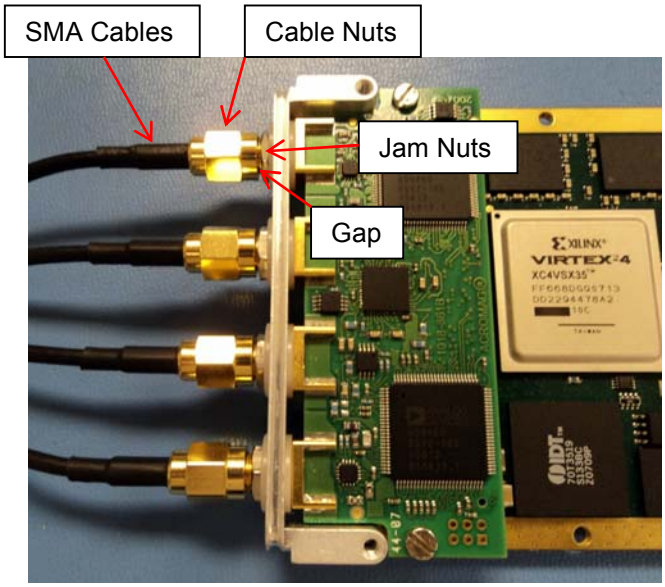
6) Then snuggly tighten the four Jam Nuts on the SMA connectors as shown. DO NOT OVER TIGHTEN.



Note: PMC Bezel O-ring already installed, but not shown.

7) Assembly is complete.

The following picture shows what the SMA Cables should look like when installed on the AXM-A30 module. Notice there will be a gap between the Cable Nuts and Jam Nuts on the SMA connectors when the SMA Cables are securely fasten. This indicates that the SMA Cables are fully inserted into the SMA connectors (no loose connections).



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