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Acromag®

# Series IP220 Industrial I/O Pack
# 12-Bit High-Density Analog Output Board

# USER'S MANUAL

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**8500-486-E98M015**

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**Table of Contents**


| | | Page |
|---|---|---|
| 1.0 | **GENERAL INFORMATION** | 2 |
| | KEY IP220 FEATURES | 2 |
| | INDUSTRIAL I/O PACK INTERFACE FEATURES | 3 |
| | SIGNAL INTERFACE PRODUCTS | 3 |
| | INDUSTRIAL I/O PACK SOFTWARE LIBRARY | 3 |
| | INDUSTRIAL I/O PACK OLE CONTROL SOFTWARE | 3 |
| 2.0 | **PREPARATION FOR USE** | 3 |
| | UNPACKING AND INSPECTION | 3 |
| | CARD CAGE CONSIDERATIONS | 3 |
| | BOARD CONFIGURATION | 4 |
| | Default Hardware Jumper Configuration | 4 |
| | Power Supply Hardware Jumper Configuration | 4 |
| | Programmable Register Configuration | 4 |
| | Analog Output Data Format | 4 |
| | CONNECTORS | 4 |
| | IP Field I/O Connector (P2) | 4 |
| | Analog Output Noise and Grounding Considerations | 5 |
| | IP Logic Interface Connector (P1) | 5 |
| 3.0 | **PROGRAMMING INFORMATION** | 5 |
| | ADDRESS MAPS | 6 |
| | IP Identification PROM | 6 |
| | DAC Channel Registers | 6 |
| | Transparent Mode | 7 |
| | Simultaneous Mode | 7 |
| | Simultaneous Output Trigger | 7 |
| | Channel Offset/Gain Error Coefficients | 8 |
| | IP220 PROGRAMMING CONSIDERATIONS | 8 |
| | Using the Transparent Mode | 8 |
| | Using the Simultaneous Mode | 8 |
| | USE OF CALIBRATION DATA | 8 |
| | Uncalibrated Performance | 8 |
| | Calibrated Performance | 9 |
| 4.0 | **THEORY OF OPERATION** | 10 |
| | ANALOG OUTPUTS | 10 |
| | LOGIC/POWER INTERFACE | 10 |
| 5.0 | **SERVICE AND REPAIR** | 10 |
| | SERVICE AND REPAIR ASSISTANCE | 10 |
| | PRELIMINARY SERVICE PROCEDURE | 10 |
| 6.0 | **SPECIFICATIONS** | 11 |
| | GENERAL SPECIFICATIONS | 11 |
| | ANALOG OUTPUTS | 11 |
| | INDUSTRIAL I/O PACK COMPLIANCE | 11 |
| | **APPENDIX** | 12 |
| | CABLE: MODEL 5025-550 | 12 |
| | CABLE: MODEL 5025-551 | 12 |
| | TERMINATION PANEL: MODEL 5025-552 | 12 |
| | TRANSITION MODULE: MODEL TRANS-GP | 12 |

**DRAWINGS** **Page**

| | | |
|---|---|---|
| 4501-441 | IP220 JUMPER LOCATIONS | 13 |
| 4501-434 | IP MECHANICAL ASSEMBLY | 13 |
| 4501-440 | ANALOG OUTPUT CONNECTIONS | 14 |
| 4501-439 | IP220 BLOCK DIAGRAM | 14 |
| 4501-462 | CABLE 5025-550 (NON-SHIELDED) | 15 |
| 4501-463 | CABLE 5025-551 (SHIELDED) | 15 |
| 4501-464 | TERMINATION PANEL 5025-552 | 16 |
| 4501-465 | TRANSITION MODULE TRANS-GP | 16 |


**IMPORTANT SAFETY CONSIDERATIONS**

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

## 1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP220 module is a 12-bit, high-density, single-size IP, analog output board with the capability to drive up to 16 analog voltage output channels. The IP220 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for many industrial control and scientific applications that require high-density, high-reliability, and high-performance at a low cost.

| MODEL | # OUTPUTS | OPERATING TEMPERATURE RANGE |
|---|---|---|
| IP220-16 | 16 | 0 to 70°C |
| IP220-8 | 8 | 0 to 70°C |
| IP220-16E | 16 | -40 to 85°C |
| IP220-8E | 8 | -40 to 85°C |

**KEY IP220 FEATURES**

- **High Channel Count** - Individual control of up to 16 analog voltage output channels is provided. Four units mounted on a carrier board provide up to 64 output channels in a single system slot.
- **12-Bit Accuracy** - Each channel contains its own 12-bit, Digital to Analog Converter (DAC) with an 8uS output settling time.
- **Bipolar Outputs** - Provides bipolar voltage range outputs: -10 to +10 Volts.
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration of the module.
- **Individual Output Control** - Output channels can be individually selected and updated with a single channel data write command when using the "transparent" output mode.
- **Simultaneous Output Control** - All output channels can be simultaneously updated with a single software trigger command when using the "simultaneous" output mode (DAC's are double-buffered which allows new data to be written to each channel before the simultaneous trigger updates the outputs).

- **Easy Mode Selection** - Selection of transparent and simultaneous output modes is easily done via software commands.
- **Reset is Failsafe** - Outputs reset to 0 volts following a power up or reset.

**INDUSTRIAL I/O PACK INTERFACE FEATURES**

- **High density** - Single-size, industry standard, IP module footprint. Up to four units may be mounted on a carrier board.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **16-bit I/O** - Control register writes, DAC writes, and calibration coefficient reads are performed through 16-bit data transfer cycles in the IP module Input/Output space.
- **High Speed** - This IP model does not generate any "wait" states. Thus, all data transfers proceed at maximum speed with 0 wait states.
- **Hold State Support** - This IP module supports "Hold" states, if generated by the carrier board.

**SIGNAL INTERFACE PRODUCTS**

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent carrier boards). Additionally, PC carrier boards are also supported (See Acromag Model APC8610). Consult the documentation of your carrier board to ensure compatibility with the following interface products (since all connections to field signals are made through the carrier board which passes them to the individual IP modules).

**Cables:**

Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with this module and for precision analog I/O applications.

**Termination Panel:**

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

**Transition Module:**

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/ 9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

**INDUSTRIAL I/O PACK SOFTWARE LIBRARY**

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO220.TXT" file in the "IP220" subdirectory on the diskette for more details.

**INDUSTRIAL I/O PACK OLE CONTROL SOFTWARE**

Acromag provides a software diskette of Industrial I/O Pack Object Linking and Embedding (OLE) drivers for Windows 95 and Windows NT compatible application programs (Model IPSW-DVR-OLE-PC, MSDOS format). This software provides individual drivers that allow Acromag I/O Packs and the APC8610 carrier to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, etc. The OLE controls provide a high-level interface to Acromag I/O Packs, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers--all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with the Acromag APC8610 ISAbus (PC/AT) carrier and consist of a Carrier Configuration Program, and APC8610 OLE control, and an OLE control for each Acromag I/O Pack model.

## 2.0 PREPARATION FOR USE

**UNPACKING AND INSPECTION**

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.




The board utilizes static sensitive components and should only be handled at a static-safe workstation.

**CARD CAGE CONSIDERATIONS**

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

**IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.**

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature

rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

### BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible jumper settings will be discussed in the following sections. The jumper locations are shown in Drawing 4501-441.

Power should be removed from the board when configuring hardware jumpers, installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions.

#### Default Hardware Jumper Configuration

A board is shipped from the factory configured as follows:

- Internal ±12 Volt power supplies are used (sourced from P1).
- Analog output range is -10 to +10 Volts and is not configurable.
- Programmable software register bits are undefined at reset, but the board defaults to 0 Volts on all analog outputs and the Simultaneous Channel Update Mode (see Section 3).

#### Power Supply Hardware Jumper Configuration

Hardware jumpers J1 & J2 allow the selection of internal or external analog power supplies. J1 (J2) controls the selection of either the internal +12 (-12) Volt supply sourced from the P1 connector, or the external +15 (-15) Volt supply sourced from the P2 connector. The IN/OUT configuration of the jumpers for the different supplies is shown in the following table. "IN" means that the pins noted are shorted together with a shorting clip. "OUT" means that the clip has been removed.

**Table 2.1: Power Supply Selections (Pins of J1 and J2)**

| Power Supply Selection* | J1 (1&2) | J1 (2&3) | J2 (1&2) | J2 (2&3) |
|---|---|---|---|---|
| ±12 Volt (Internal, P1) | IN | OUT | IN | OUT |
| ±15 Volt (External, P2) | OUT | IN | OUT | IN |

* Do not mix internal and external supplies (e.g. do not use +12V internal with -15V external). Note that the IP220 module can achieve rated output using either internal or external supplies.

#### Programmable Register Configuration

Programmable registers are software configurable. That is, there are no hardware jumpers associated with them. Registers must be accessed to select the desired mode of operation and to update analog outputs (refer to Section 3 for details).

#### Analog Output Data Format

The bipolar output range (-10 to +10 Volts) is programmed with Bipolar Offset Binary (BOB) data to the Digital-to-Analog-Converter (DAC). The following table indicates the relationship between the data format and the ideal analog output voltage from the module.

**Table 2.2: Bipolar Offset Binary (BOB) Output Data Format***

| Analog Output Voltage (Volts) | BOB Data (Hex) |
|---|---|
| 9.9951 | FFF0 |
| 9.9902 | FFE0 |
| . | . |
| . | . |
| 0.0049 | 8010 |
| 0.0000 | 8000 |
| -0.0049 | 7FF0 |
| . | . |
| . | . |
| -9.9951 | 0010 |
| -10.0000 | 0000 |

* The BOB, 12-bit data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are shown as zero in the table, but actually it does not matter what is written to them.

### CONNECTORS

#### IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin receptacle female header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly. P2 Pin assignments are unique to each IP (see Table 2.3) and normally correspond to the pin numbers of the front panel, field I/O interface connector on the carrier board (you should verify this for your carrier board). In Table 2.3, channel designations are abbreviated to save space (i.e. channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively). Further, note the output signals all have the same ground reference ("-CH00" and the minus leads of all other channels are connected to analog common on the module).

**Table 2.3: IP220 Field I/O Pin Connections (P2)**

| Pin Description | Number | Pin Description | Number |
|---|---|---|---|
| +CH00 | 1 | -CH12[1] | 26 |
| -CH00[1] | 2 | +CH13 | 27 |
| +CH01 | 3 | -CH13[1] | 28 |
| -CH01[1] | 4 | +CH14 | 29 |
| +CH02 | 5 | -CH14[1] | 30 |
| -CH02[1] | 6 | +CH15 | 31 |
| +CH03 | 7 | -CH15[1] | 32 |
| -CH03[1] | 8 | *RESERVED* | 33 |
| +CH04 | 9 | *RESERVED* | 34 |
| -CH04[1] | 10 | *RESERVED* | 35 |
| +CH05 | 11 | *RESERVED* | 36 |
| -CH05[1] | 12 | *RESERVED* | 37 |
| +CH06 | 13 | *RESERVED* | 38 |
| -CH06[1] | 14 | *RESERVED* | 39 |
| +CH07 | 15 | *RESERVED* | 40 |
| -CH07[1] | 16 | *RESERVED* | 41 |
| +CH08 | 17 | *RESERVED* | 42 |
| -CH08[1] | 18 | COMMON[1] | 43 |
| +CH09 | 19 | COMMON[1] | 44 |
| -CH09[1] | 20 | *RESERVED* | 45 |
| +CH10 | 21 | *RESERVED* | 46 |
| -CH10[1] | 22 | -15V DC | 47 |
| +CH11 | 23 | *RESERVED* | 48 |
| -CH11[1] | 24 | +15V DC | 49 |
| +CH12 | 25 | SHIELD | 50 |

**Note**: 1. The minus leads of all channels are connected to analog common on the module.

**Analog Output Noise and Grounding Considerations**

All output channels are referenced to analog common on the module (See Drawing 4501-440 for analog output connections), but each channel has a separate return (minus lead) to maintain accuracy and reduce noise. Still, the accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads > 100KΩ) provide the best accuracy. For low impedance loads, the IP220 can source up to 5mA, but the effects of source and cabling resistance should be considered.

Output common is electrically connected to the IP module ground. As such, the IP220 is non-isolated between the logic and field I/O grounds. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog outputs when a high level of accuracy/resolution is needed (e.g. 12-bits or more). Refer to Drawing 4501-440 for example output and grounding connections. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to provide isolated voltage or current outputs when used in conjunction with the IP220 output module.

**IP Logic Interface Connector (P1)**

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.4). Note that the IP220 does not utilize all of the logic signals defined for the P1 connector. Logic lines NOT USED used by this model are indicated in ***BOLD ITALICS***.

**Table 2.4: Standard Logic Interface Connections (P1)**

| Pin Description | Number | Pin Description | Number |
|---|---|---|---|
| GND | 1 | GND | 26 |
| CLK | 2 | +5V | 27 |
| Reset* | 3 | R/W* | 28 |
| D00 | 4 | IDSEL* | 29 |
| D01 | 5 | ***DMAReq0**** | 30 |
| D02 | 6 | MEMSEL* | 31 |
| D03 | 7 | ***DMAReq1**** | 32 |
| D04 | 8 | IntSel* | 33 |
| D05 | 9 | ***DMAck0**** | 34 |
| D06 | 10 | IOSEL* | 35 |
| D07 | 11 | ***RESERVED*** | 36 |
| D08 | 12 | A1 | 37 |
| D09 | 13 | ***DMAEnd**** | 38 |
| D10 | 14 | A2 | 39 |
| D11 | 15 | ***ERROR**** | 40 |
| D12 | 16 | A3 | 41 |
| D13 | 17 | ***INTReq0**** | 42 |
| D14 | 18 | A4 | 43 |
| D15 | 19 | ***INTReq1**** | 44 |
| ***BS0**** | 20 | A5 | 45 |
| ***BS1**** | 21 | ***STROBE**** | 46 |
| -12V | 22 | A6 | 47 |
| +12V | 23 | ACK* | 48 |
| +5V | 24 | ***RESERVED*** | 49 |
| GND | 25 | GND | 50 |

Asterisk (*) is used to indicate an active-low signal.
***BOLD ITALIC*** Logic Lines are NOT USED by this IP Model.

## 3.0 PROGRAMMING INFORMATION

This board is addressable in the Industrial Pack I/O space to control the level of analog outputs in the field and to read offset and gain calibration coefficients. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6. The IP220 uses this address space for enabling control signals for DAC functions and addressing offset and gain calibration coefficients used by the software to adjust the accuracy of the output range. The calibration coefficients are accessed via reads from PROM in the I/O space. The I/O space address map for the IP220 is shown in Table 3.1 below. Note the base addresses for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on a 16-bit word basis (D0..D15).

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on an ISAbus (PC/AT) carrier board will require the use of the even address locations to access the data, while a VMEbus carrier will require the use of odd address locations.

## ADDRESS MAPS

**Table 3.1: IP220 I/O Space Address Memory Map**

| Base Address + (Hex) | Even Byte D15 D08 | Odd Byte D07 D00 |
|---|---|---|
| 00 | (W) - DAC Channel 0 | |
| 02 | (W) - DAC Channel 1 | |
| 04 | (W) - DAC Channel 2 | |
| 06 | (W) - DAC Channel 3 | |
| 08 | (W) - DAC Channel 4 | |
| 0A | (W) - DAC Channel 5 | |
| 0C | (W) - DAC Channel 6 | |
| 0E | (W) - DAC Channel 7 | |
| 10 | (W) - DAC Channel 8[2] | |
| 12 | (W) - DAC Channel 9[2] | |
| 14 | (W) - DAC Channel 10[2] | |
| 16 | (W) - DAC Channel 11[2] | |
| 18 | (W) - DAC Channel 12[2] | |
| 1A | (W) - DAC Channel 13[2] | |
| 1C | (W) - DAC Channel 14[2] | |
| 1E | (W) - DAC Channel 15[2] | |
| 20 | (W) - Transparent Mode | |
| 22 | (W)- Simultaneous Mode | |
| 24 | (W) - Simultaneous Output Trigger | |
| 26 ↓ 3E | NOT USED[1] | |
| 40 | | (R)-CH0 Offset Error |
| 42 | | (R)-CH0 Gain Error |
| 44 | | (R)-CH1 Offset Error |
| 46 | | (R)-CH1 Gain Error |
| 48 | | (R)-CH2 Offset Error |
| 4A | | (R)-CH2 Gain Error |
| 4C | | (R)-CH3 Offset Error |
| 4E | | (R)-CH3 Gain Error |
| 50 | | (R)-CH4 Offset Error |
| 52 | | (R)-CH4 Gain Error |
| 54 | | (R)-CH5 Offset Error |
| 56 | | (R)-CH5 Gain Error |
| 58 | | (R)-CH6 Offset Error |
| 5A | | (R)-CH6 Gain Error |
| 5C | | (R)-CH7 Offset Error |
| 5E | | (R)-CH7 Gain Error |
| 60 | | (R)-CH8 Offset Error[2] |
| 62 | | (R)-CH8 Gain Error[2] |
| 64 | | (R)-CH9 Offset Error[2] |
| 66 | | (R)-CH9 Gain Error[2] |
| 68 | | (R)-CH10 Offset Error[2] |
| 6A | | (R)-CH10 Gain Error[2] |
| 6C | | (R)-CH11 Offset Error[2] |
| 6E | | (R)-CH11 Gain Error[2] |
| 70 | | (R)-CH12 Offset Error[2] |
| 72 | | (R)-CH12 Gain Error[2] |
| 74 | | (R)-CH13 Offset Error[2] |
| 76 | | (R)-CH13 Gain Error[2] |
| 78 | | (R)-CH14 Offset Error[2] |
| 7A | | (R)-CH14 Gain Error[2] |
| 7C | | (R)-CH15 Offset Error[2] |
| 7E | | (R)-CH15 Gain Error[2] |

**Notes (Table 3.1):**

1. The IP will not respond to addresses that are "Not Used".
2. Channels 8-15 are present in the IP220-16 Model, only.

The following sections give details on the function of each location in the I/O space noted above.

### IP Identification PROM - (Read Only, 32 odd-byte addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP220 ID PROM bytes are addressed using only the odd addresses in a 64-byte block. The IP220 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 0 wait states.

**Table 3.2: IP220 ID Space Identification (ID) PROM**

| Hex Offset From ID PROM Base Address | ASCII Character Equivalent | Numeric Value (Hex) | Field Description |
|---|---|---|---|
| 01 | I | 49 | All IP's have 'IPAC' |
| 03 | P | 50 | |
| 05 | A | 41 | |
| 07 | C | 43 | |
| 09 | | A3 | Acromag ID Code |
| 0B | | 22 IP220-16<br>23 IP220-8 | IP Model Code |
| 0D | | 00 | Not Used (Revision) |
| 0F | | 00 | Reserved |
| 11 | | 00 | Not Used (Driver ID Low Byte) |
| 13 | | 00 | Not Used (Driver ID High Byte) |
| 15 | | 0C | Total Number of ID PROM Bytes |
| 17 | | 55 IP220-16<br>34 IP220-8 | CRC |
| 19 to 3F | | yy | Not Used |

### DAC Channel Registers- (Write, Base + 00H to Base + 1EH)

The IP220 contains sixteen (16) DAC Channel Registers in the I/O space. Writing to the address of the specific register enables the 12-bit input buffer, of the 12-bit input double buffer, to latch the data existing on the data bus. The 12-bit DAC registers are written (will not respond to reads) with 16-bit words (D16) with the four least significant bits (D3 to D0) being non-functional during a digital to analog conversion cycle. Execution of a DAC Channel Write command requires 0 wait states.

The twelve bits of data are left-justified within the 16-bit word (D16). The four LSB's are undefined (typically passive pull-ups on the carrier board will cause undriven bits to be high). The data format is Bipolar Offset Binary (BOB, see Section 2 for details).

| MSB | | | | | | | | | | | LSB | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ← | | | | | | | DATA | | | | → | X | X | X | X |

"X" means "Don't Care" - the bit value does not matter.

RESET CONDITION: All output channels are set to "0 Volts".

**Note:** The reset function resets only the D/A output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before a DAC output update by enabling the Transparent Mode, or enabling the Simultaneous Output Trigger. Otherwise, old data or unknown data present in the input latches will be transferred to the D/A output latch producing an undesired analog output.

**Transparent Mode - (Write, Base + 20H)**

The Transparent Mode is a write-only register in the I/O space that is used to select and enable the transparent type of data transfer (it will not respond to reads). Once the Transparent Mode is selected, 12-bit digital data written to the address specific channel's input latch will automatically be converted and transferred to the board's field connector. The data is transferred from the input latch, through the D/A latch (transparent in this mode), to the analog output field connector until a reset, Simultaneous Mode, or Simultaneous Output Trigger is enabled. Execution of a Transparent Mode write command requires 0 wait states. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

| D15...D00 |
|---|
| X...X |

"X" means "DON'T CARE" - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

**Note:** The reset function resets only the D/A output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old or unknown data present in the input latches will be transferred to the D/A output latch producing an undesired analog output.

In the Transparent Mode, the Simultaneous Mode can be activated by a write to the Simultaneous Output Trigger register.

**Simultaneous Mode - (Write, Base + 22H)**

The Simultaneous Mode is a write-only register (will not respond to reads) in the I/O space that is used to select the simultaneous type of data transfer. Once the Simultaneous Mode is selected, 12-bit digital data written to the address specific channel's input latch will continue to be held until the Simultaneous Output Trigger register is written, before digital data is transferred to the output latch (and the updated analog output appears at the board's field connector). The data, of all the channels, is simultaneously transferred, **once per simultaneous trigger,** from the D/A input latch to the output latch (and analog output updated) **only** when the Simultaneous Output Trigger register is enabled. Execution of a Simultaneous Mode Write command requires 0 wait states. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

| D15...D00 |
|---|
| X...X |

"X" means "Don't Care" - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

**Note:** The reset function resets only the D/A output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the D/A output latch producing an undesired analog output.

The Simultaneous Mode can also be activated while in Transparent Mode if a write occurs to the Simultaneous Output Trigger register.

**Simultaneous Output Trigger - (Write, Base + 24H)**

The Simultaneous Output Trigger is a write-only register (will not respond to reads) in the I/O space that produces the pulse needed to trigger the simultaneous type of data transfer. The Simultaneous Output Trigger register works in conjunction with the Simultaneous Mode register to simultaneously transfer all the channels' digital data from the D/A input latch to the output latch (and update the analog output) at a specific time. The Simultaneous Mode register must be written to first. Then, writing to the Simultaneous Output Trigger register creates the trigger for digital data to be converted and transferred to the board's field connector. The 12-bit digital data written to the address specific channel's input latch will continue to be held until the Simultaneous Output Trigger register is written. This will trigger the transfer of digital data from the D/A input latch to the output latch and the digital to analog conversion producing the updated analog output. Execution of a Simultaneous Output Trigger Write command requires 0 wait states. The data written to this location (D16) is immaterial, since the write is sufficient to complete the action.

| D15...D00 |
|---|
| X...X |

"X" means "Don't Care" - the bit value does not matter.

RESET CONDITION: Defaults to Simultaneous Mode. All register bits are undefined. All analog output channels are set to "0 Volts".

**Note:** The reset function resets only the D/A output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the D/A output latch producing an undesired analog output.

The Simultaneous Mode can also be activated while in Transparent Mode if a write occurs to the Simultaneous Output Trigger register.

**Channel Offset/Gain Error Coeff. - (Read, Base + 41 to 7FH)**

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in a PROM. These coefficients can be retrieved (read-only) by accessing the last 32 odd bytes (41H to 7FH) of the I/O space (D08 - or using the lower 8 bits for D16 accesses). The offset and gain calibration coefficients read from the PROM are stored with 1/4-LSB resolution. Thus, it is necessary to divide each coefficient by four to correctly use them when calibrating the bipolar outputs. Each is stored as a two's-complement (i.e. signed) eight-bit number. This number has a range of -128 to +127, which represents the offset or gain adjustments from -32 to +31.75 LSB's. Execution of a Channel Offset or Gain Error Read command requires 0 wait states.

| EVEN BYTE | | | | | | | ODD BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | MSB | | | | | | | LSB |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | ←——— DATA ———→ | | | | | | | |

**PROGRAMMING CONSIDERATIONS FOR ANALOG OUTPUTS**

The IP220 provides two methods of analog output programming for maximum flexibility with different applications. The following paragraphs describe the features of each and how to best use them.

**Using the Transparent Mode**

Use of the Transparent Mode provides the quickest method of updating the desired analog output. This method is geared for those applications that require maximum speed without the need for updating all channels simultaneously. In Transparent Mode, each analog output channel is updated as soon as it is written to. Multiple channels may be written to separately, resulting in the analog outputs being updated one channel at a time. Functionally, the input latch is written to, and the D/A latch is automatically updated, providing more speed by eliminating a separate write instruction.

**Transparent Mode Programming Example**

1. Write to the Transparent Mode register to setup the transparent type of data transfer.
2. Read the PROM to acquire the channel's unique offset and gain calibration coefficient data. This data is necessary to adjust, by software, the accuracy of the involved channel's analog output. See USE OF CALIBRATION DATA.
3. Write the 16-bit (corrected 12-bit, left-justified) digital data to the desired DAC Channel Register.
4. (OPTIONAL) Observe or monitor that the specific DAC channel reflects the results of the digital data converted to an analog output voltage at the field connector.
5. Repeat steps 1-4 until all the desired channels reflect the updated analog output voltage at the field connector.

**Using the Simultaneous Mode**

Use of the Simultaneous Mode provides a method of distributing data simultaneously and synchronously to produce desired analog outputs. This method is useful for applications that require updating all the channels simultaneously and synchronously. Each channel is written to with the required 16-bit (12-bit, left-justified) data. When all the required channels contain the desired digital data, then a write to the Simultaneous Output Trigger register will produce a pulse to simultaneously trigger each channel's digital to analog converter. Thus, all the analog outputs are updated simultaneously. Functionally, each input latch is written to separately. When all input latches contain the desired digital data, then all channels are pulsed simultaneously and synchronously to convert to the updated analog output voltage.

**Simultaneous Mode Programming Example**

1. Write to the Simultaneous Mode register to setup the simultaneous type of data transfer.
2. Read the PROM to acquire the channel's unique offset and gain calibration coefficient data. This data is necessary to adjust, by software, the accuracy of the involved channel's analog output. See USE OF CALIBRATION DATA.
3. Write the 16-bit (corrected 12-bit, left-justified) digital data to the desired DAC Channel Register.
4. Repeat steps 2-3 to write new digital data to the DAC Channel Registers for all other channels requiring update.
5. Write to the Simultaneous Output Trigger register to produce a pulse to simultaneously trigger digital to analog conversions for all channels, resulting in updated analog output voltages at the field connector.
6. (OPTIONAL) Observe or monitor that DAC channels reflect the results of the digital data converted to an analog output voltage at the field connector.
7. Repeat steps 2-6 for continued simultaneous and synchronous triggered updates of all desired channels.

**USE OF CALIBRATION DATA**

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in the PROM. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Software calibration uses some fairly complex equations. Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code. The functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO220.TXT" file in the "IP220" subdirectory on the diskette for details.

**Uncalibrated Performance**

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset

and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). The maximum uncalibrated error is summarized as follows:

**DAC4813AP @ 25°C:**

Linearity Error is +/- 0.012% maximum (i.e. 1/2 LSB).
Bipolar Offset Error is +/- 0.4% FSR (i.e. 20V SPAN) maximum.
Gain Error is +/- 0.2% FSR maximum.

Table 3.3 summarizes the maximum uncalibrated error combining the linearity, offset and gain errors:

**Table 3.3: Maximum Overall Uncallbrated Error**

| Max. Linearity Error (%) | Max. Offset Error (%) | Max. Gain Error (%) | Max. Total Error* (%) |
|---|---|---|---|
| +/-0.012 | +/-0.4 | +/-0.2 | +/-0.612 |

* This represents the worst case error with all errors summed. Typically, each error component is much less than its maximum and all error components do not reinforce each other. Thus, typical errors are much less than that shown in the table above.

**Calibrated Performance**

Accurate calibration of the IP220 can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in the PROM as 1/4 LSB's for each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage.

Table 3.4 summarizes the maximum calibrated error combining the linearity and adjusted offset and gain errors:

**Table 3.4: Maximum Overall Calibrated Error**

| Max. Linearity Error LSB | Max. Offset Error LSB | Max. Gain Error LSB | Max. Total Error LSB (%) |
|---|---|---|---|
| +/-0.5 | +/-0.25 | +/-0.25 | +/-1.0 (0.025) |

Thus, correcting the value programmed to the DAC Channel Register using the stored calibration coefficients provides the means to obtain excellent accuracy.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (ideal_count) written to the 12-bit DAC to achieve a specified voltage within the -10 to +10 Volt output range assuming Bipolar Offset Binary (BOB) data format (see Section 2 for details).

**Ideal_Count = [(Count_Span / Ideal_Volt_Span) * Desired_Voltage] + Ideal_Zero_Count** (1)

where,
**Count_Span** = 4096 (a 12-bit converter has $2^{12}$ possible levels)
**Ideal_Volt_Span** = 20 Volts (for the bipolar -10 to +10 Volt range)
**Ideal_Zero_Count** = 2048 (count for an ideal output of 0 Volts)

Equation (1) can be simplified using the above constants, since the range and DAC are fixed on the IP220. Equation (2) results:

**Ideal_Count = [(4096 / 20) * Desired_Voltage] + 2048** (2)

Using equation (2), one can determine the ideal count for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts, equation (2) returns the result 3072 for Ideal_Count. If this value is used to program the DAC output (following conversion to Hex and left-justification), the output value will approach +5 Volts to within the uncalibrated error specified in Table 3.3. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal_Count into the Corrected_Count required to accurately produce the output voltage. This is illustrated in equation (3):

**Corrected_Count = [(Ideal_Gain + Gain_Correction) * (Ideal_Count - Ideal_Zero_Count)] + (Ideal_Zero_Count + Offset_Correction)** (3)

where,
**Ideal_Gain** = 1
**Gain_Correction** = PROM_Gain_Error / 4 / 4096 = PROM_Gain_Error / 16384
**Offset_Correction** = PROM_Offset_Error / (4)

Ideal_Count is determined from equation (2) and Ideal_Zero_Count remains 2048. PROM_Gain_Error and PROM_Offset_Error are obtained from the PROM on the IP220 on a per channel basis. Equation (3) can be written as (4) by making the listed substitutions:

**Corrected_Count = [(1 + (PROM_Gain_Error / 16384)) * (Ideal_Count - 2048)] + (2048 + (PROM_Offset_Error / 4))** (4)

Using equation (4), you can determine the corrected count from the ideal count. For the previous example, equation (2) returned a result 3072 for the Ideal_Count to produce an output of +5 Volts. Assuming that a gain error of +13 and an offset error of -25 are read from the PROM on the IP220 for the desired channel, substitution into equation (4) yields:

**Corrected_Count = [(1 + (13 / 16384)) * (3072 - 2048)] + (2048 + (-25 / 4)) = 3066.56**

If this value (rounded to 3067) is used to program the DAC output (following conversion to Hex and left-justification), the output value will approach +5 Volts to within the calibrated error specified in Table 3.4 (+/-1 LSB). Note that the quantization error (up to 0.5 LSB) introduced by rounding to 3067 is not included in the overall accuracy specification.

**Calibration Programming Example**

The available bipolar range, centered around 0 Volts is -10 to +10 Volts. Assume it is necessary to program channel 0 with an output of -2.5 Volts.

1. Write to the Transparent Mode register @BASE + 20H with data of FFFFH to select the Transparent Mode. In this mode, data written to the Channel Register will be automatically transferred from the input latch to the output latch and converted to the desired output.
2. Read the PROM to retrieve the channel's unique offset calibration error data. For channel 0, read byte @BASE + 41H. An 8 bit two's compliment number is read (assume 20H). This corresponds to a PROM_Offset_Error of +32 decimal.

3. Read the PROM to retrieve the channel's unique gain calibration error data. For channel 0, read byte @BASE + 43H. An 8 bit two's compliment number is read (assume F1H). This corresponds to a PROM_Gain_Error of -15 decimal.
4. Calculate the Ideal_Count required to provide an uncorrected output of the desired value (-2.5 Volts) by using equation (2). **Ideal_Count** = [(4096 / 20) * -2.5] + 2048 = 1536.0
5. Calculate the Corrected_Count required to provide an accurate output of the desired value (-2.5 Volts) by using equation (4). **Corrected_Count** = [(1 + (-15 / 16384)) * (1536.0 - 2048)] + (2048 + (32 / 4)) = 1544.47
6. Write to the DAC Channel 0 Register @BASE + 00H with the desired data (6080H - data is determined by rounding 1544.47 decimal to 1544, then converting to Hex 608 and left justifying as 6080H).
7. (OPTIONAL) Observe or monitor that the specific DAC channel (0) reflects the results of the digital data converted to an analog output voltage at the field connector.
8. Repeat steps 2-7 to adjust the unique calibration characteristic and update each channel used, or repeat steps 4-7 to update the value of a single channel.

Error checking should be performed on the calculated count values to insure that calculated values below 0 or above 4095 decimal are restricted to those end points. Note that the software calibration cannot generate outputs near the endpoints of the range which are clipped off due to the uncalibrated hardware (i.e. the DAC).

## 4.0 THEORY OF OPERATION

This section describes the basic functionality of the IP220 circuitry. Review the block diagram shown in Drawing 4501-439 as you study the following paragraphs.

### ANALOG OUTPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). Field analog outputs are NON-ISOLATED. This means that the field return, output channel minus, and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops and excessive output loading (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-440 for example analog output and grounding connections.

The fully populated board contains sixteen 12-bit DAC's (IP220-16), one per channel. This allows each channel to be independently programmed for maximum speed and accuracy and avoids the problems associated with designs using sample and hold amplifiers multiplexed to a single DAC. Each DAC may source up to 5mA of output current without requiring separate buffer amplifiers. DAC calibration is done via software to avoid the mechanical drawbacks of hardware potentiometers for each DAC channel. This also conserves board space and helps to achieve high channel density. Calibration parameters are stored in PROM on a per channel basis.

DAC inputs are double-buffered. This allows channels to be programmed by either of two modes (software register selectable). The Transparent Mode allows channels to be updated quickly on an individual basis, since data written to the input latch is immediately transfered to the output latch and converted to an updated analog output voltage. Selection of the Simultaneous Mode allows many or all channels to be updated at once. In this mode, the data for channels is written to their associated input latch, but does not get transfered to the output latch until a Simultaneous Trigger command is sent. All channels update synchronously and simultaneously upon receipt of the trigger command.

The logic interface provides ±12 Volt supplies to the analog circuitry. If desired, the user has the option of providing ±15 Volt external supplies. However, supplies cannot be mixed (do not use +12V with -15V). Rated outputs are achieved using either internal or external supplies and this is selected via hardware jumpers J1 & J2 prior to powering the unit (see Section 2).

### LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.4). Not all of the IP logic P1 pin functions are used. P1 also provides ±12V and +5V to power the module.

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces, and produces the chip selects, control signals, and timing required by the DAC's, software registers, and ID PROM, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also controls the mode selection and triggering to start DAC conversions for the Transparent and Simultaneous Modes.

The ID PROM (read only) installed on the IP module provides the identification for the individual module per the IP specification. The Calibration PROM (same physical device as the ID PROM, but mapped into the I/O space) contains channel specific calibration coefficients to correct both offset and gain errors. The coefficients must be used to trim the outputs to within their accuracy specification. The PROM, software registers, and DAC's are all accessed through the 16-bit data bus interface to the carrier board.

## 5.0 SERVICE AND REPAIR

### SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

### PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

**CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS**

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

## 6.0 SPECIFICATIONS

### GENERAL SPECIFICATIONS

Operating Temperature.....0 to +70°C
.....-40°C to +85°C (E Versions)
Relative Humidity.....5-95% Non-Condensing
Storage Temperature.....-55°C to +100°C
Physical Configuration.....Single Industrial I/O Pack Module
Length.....3.900 in. (99.0 mm)
Width.....1.800 in. (45.7 mm)
Board Thickness.....0.062 in. (1.59 mm)
Max Component Height.....0.314 in. (7.97 mm)
Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%).....150mA Typical, 200mA Maximum.
+12 Volts (±5%) from P1 or....200mA Typical, 300mA Maximum
+15 Volts (±5%) from P2.....(See Notes 1 & 2 Below)
-12 Volts (±5%) from P1 or.....80mA Typical, 180mA Maximum
-15 Volts (±5%) from P2.....(See Notes 1 & 2 Below)
Non-Isolated.....Logic and field commons have a direct electrical connection.

Notes (Power):

1. The ±12 volt power supplies are normally supplied through P1 (logic interface connector). Optionally (jumper selectable on the IP), the user may connect external ±15 volt supplies through the field I/O interface connector, P2.
2. The maximum current draw assumes that the rated current of 5mA per channel is drawn. Current draw will be reduced proportionately for high impedance output loads.

### ANALOG OUTPUTS

Output Channels (Field Access).....IP220-16: 16 Single-Ended.
IP220-8: 8 Single-Ended.
Output Type.....Voltage (Non-Isolated).
Output Range.....Bipolar -10V to +10V (See Notes 3 & 4).
Output Current.....-5mA to +5mA (Maximum); this corresponds to a minimum load resistance of 2KΩ with a 10V output (See Notes 3 & 4).
Data Format (left-justified).....Bipolar Offset Binary (BOB).
DAC Programming.....Immediate (transparently programmed to DAC output); Simultaneous (input latches of multiple DAC's are loaded with new data before simultaneously updating DAC outputs).
Resolution.....12-bits.
Monotonicity over Temperature.....12-bits.
Linearity Error.....± 1/2 LSB (Maximum).
Differential Linearity Error.....± 1 LSB (Maximum).
System Accuracy.....±0.025% of 20V SPAN Maximum corrected error (i.e. calibrated) at 25°C (See Note 5) with the output unloaded.
Settling Time.....8uS to within 0.012% for a 20V step change (load of 5KΩ in parallel with 470 pf).
Output at Reset.....Bipolar Zero Volts (See Note 6).
Output Noise.....2mV rms in a 20MHz bandwidth, Typical.
Output Impedence.....1Ω Maximum at 25°C (a load of 10KΩ will introduce 0.01% output error).
Short Circuit Protection.....Indefinite at 25°C.
Output Load Stability.....Maximum recommended capacitive load is 500pf. Capacitive loads above 500pf can be tolerated, but with additional overshoot.
Gain Drift.....±30ppm/per °C Maximum.
Bipolar Zero Drift (Maximum).....±15ppm of 20V SPAN per °C.
Resistance to RFI.....Error is < ± 0.25% of a 20V span for RFI field strengths up to 10V/m at 27MHz, 159MHz, and 460MHz.

Notes (Analog Outputs):

3. Maximum output current (±5mA) can be achieved at the range endpoints using the internal ±12 volt power supplies sourced through P1. The external ±15 volt power supplies, sourced through P2, are not required to achieve rated output.
4. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.
5. Offset and gain calibration coefficients stored in the ID PROM must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error. Follow the output connection recommendations of Section 2, because non-ideal grounds can degrade overall system accuracy.
6. The reset function resets only the D/A (i.e. output) latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before a simultaneous DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the D/A output latch, producing an undesired analog output.

### INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications for Type I modules per ANSI/VITA 4-1995.
Electrical/Mechanical Interface.....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).....16-bit word write of 12-bit left-justified channel data; 16-bit write to control registers; 16-bit read of 8-bit right-justified DAC offset and gain calibration coefficients.
ID Read (IDSel*).....32x8 ID PROM read on D0..D7.

Access Times (8MHz Clock):
ID PROM Read.....0 wait states (250ns cycle).
DAC Channel Data Write.....0 wait states (250ns cycle).
DAC Offset/Gain Coeff. Read...0 wait states (250ns cycle).
Control Register Writes.....0 wait states (250ns cycle).

## APPENDIX

**CABLE: MODEL 5025-550-x (Non-Shielded)**
**MODEL 5025-551-x (Shielded)**

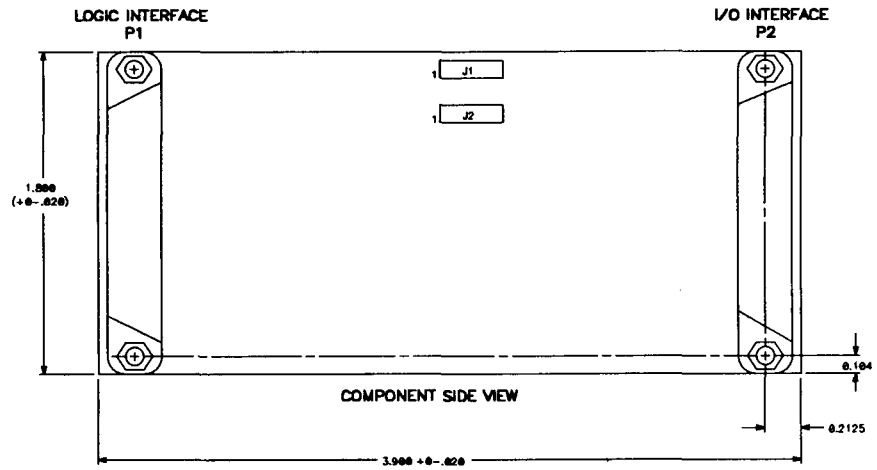
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (Both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg), packed.

**TERMINATION PANEL: MODEL 5025-552**

Type: Termination Panel For AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packed.

**TRANSITION MODULE: MODEL TRANS-GP**

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.

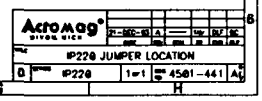


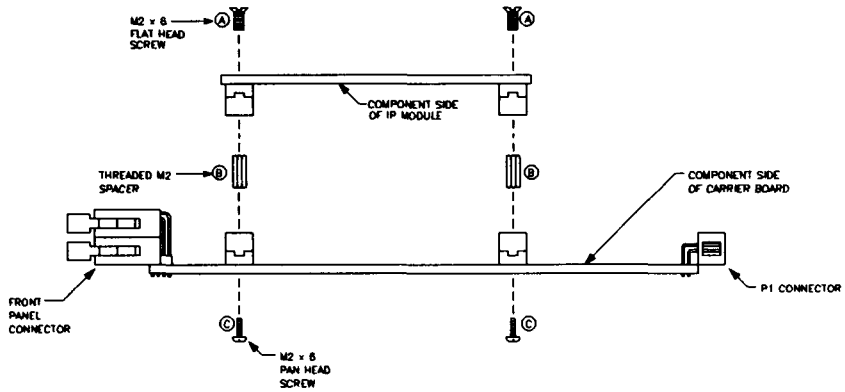

**POWER SUPPLY SELECTIONS (PINS OF J1 AND J2)**

| POWER SUPPLY SELECTION* | J1 (1 & 2) | J1 (2 & 3) | J2 (1 & 2) | J2 (2 & 3) |
|---|---|---|---|---|
| +/-12 VOLT (INTERNAL, P1) | IN | OUT | IN | OUT |
| +/-15 VOLT (EXTERNAL, P2) | OUT | IN | OUT | IN |

* INTERNAL AND EXTERNAL SUPPLIES SHOULD NOT BE MIXED (E.G. DO NOT USE +12 VOLTS WITH -15 VOLTS.)

## IP220 JUMPER LOCATIONS

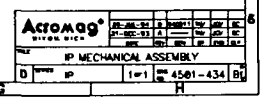


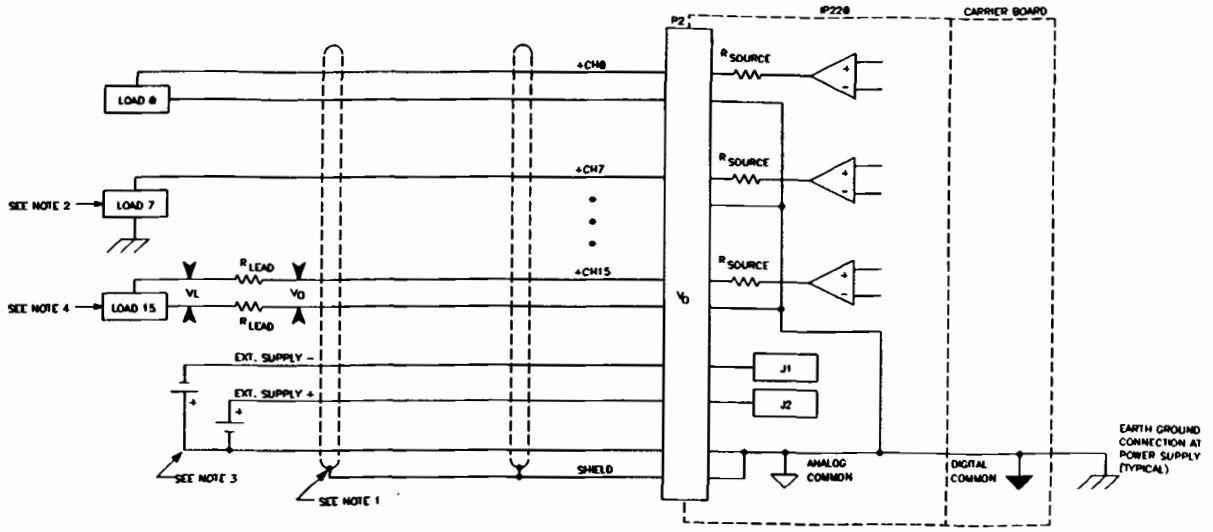




ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9680 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

## IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

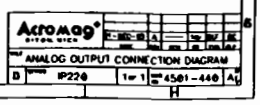


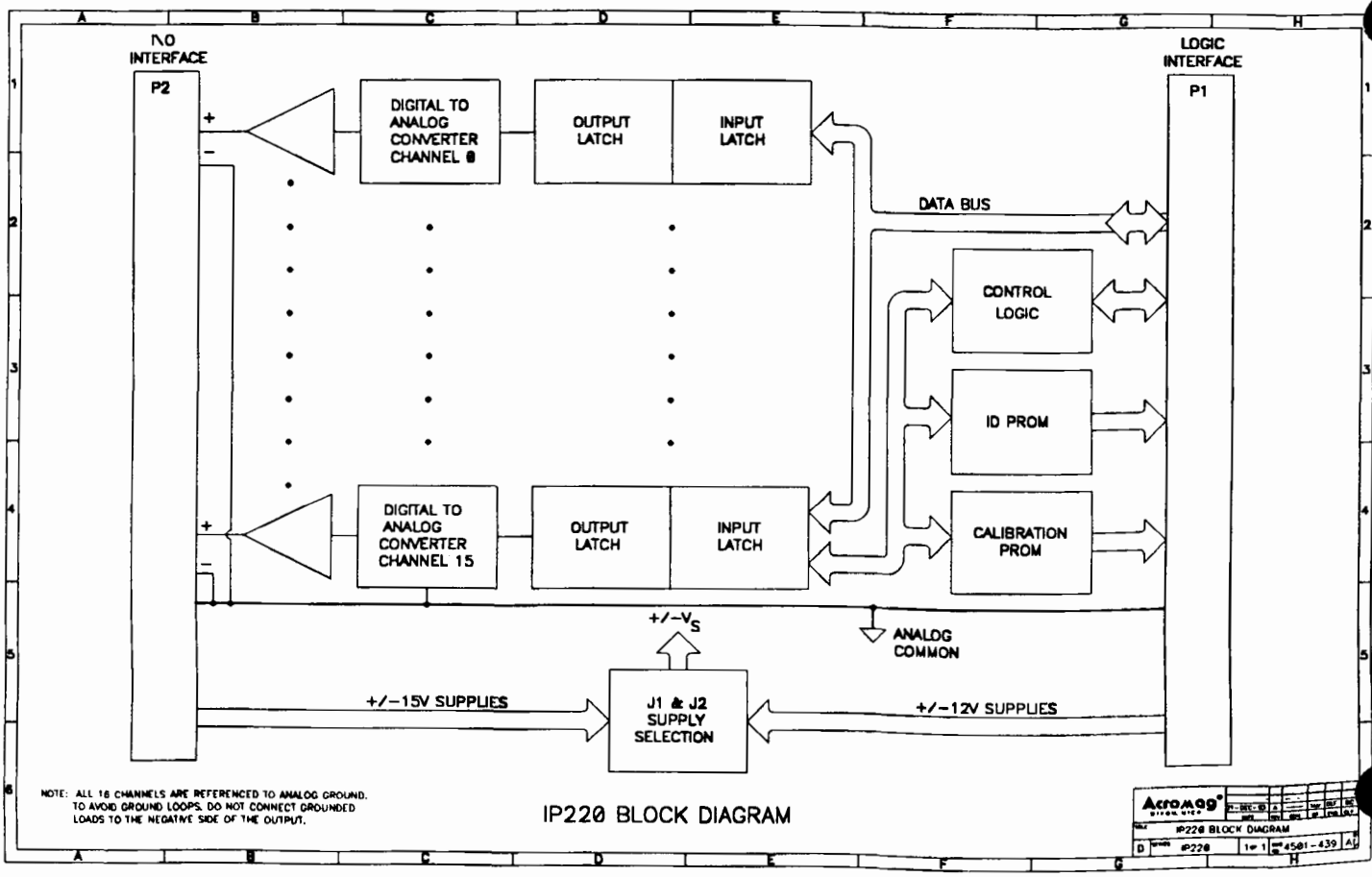



NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONLY ONE END TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. ALL 16 CHANNELS ARE REFERENCED TO ANALOG COMMON AT THE IP220. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED CHANNELS TO THE NEGATIVE SIDE OF THE OUTPUT.
3. EXTERNAL SUPPLIES CAN BE USED BY JUMPERING. IT IS RECOMMENDED THAT THE SUPPLY COMMONS BE CONNECTED TO ANALOG COMMON.
4. VL < VO DUE TO VOLTAGE DROPS ACROSS THE LEAD RESISTANCE OF THE WIRE. IT IS RECOMMENDED THAT A HIGH RESISTANCE LOAD WITH A SHORT WIRE RUN BE CONNECTED AT THE OUTPUT TO REDUCE THE EFFECTS OF LEAD AND SOURCE RESISTANCE VOLTAGE DROPS IN THE WIRE.

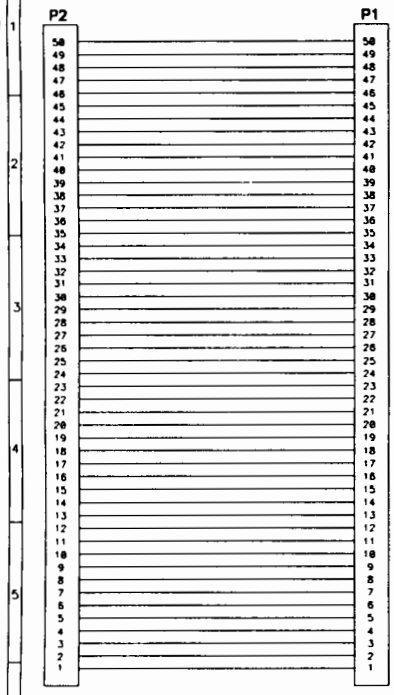
## IP220 ANALOG OUTPUT CONNECTION DIAGRAM



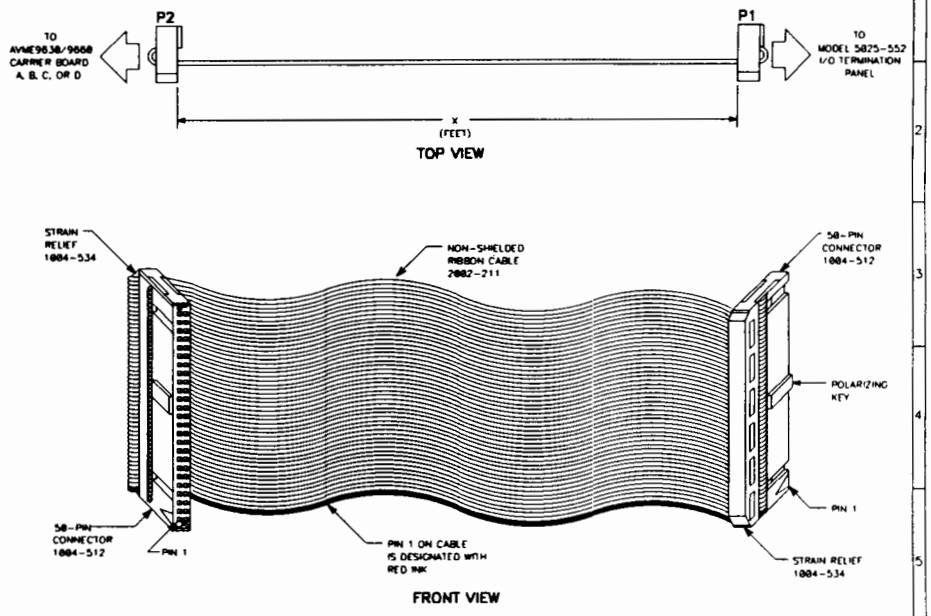




NOTE: ALL 16 CHANNELS ARE REFERENCED TO ANALOG GROUND. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED LOADS TO THE NEGATIVE SIDE OF THE OUTPUT.

## IP220 BLOCK DIAGRAM



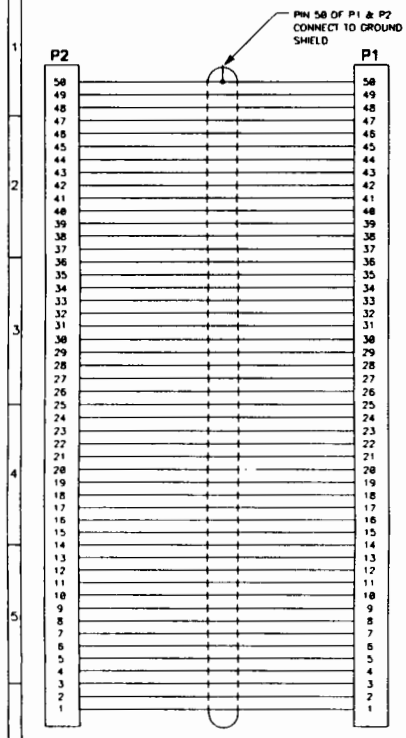

MODEL 5025-550-x SCHEMATIC



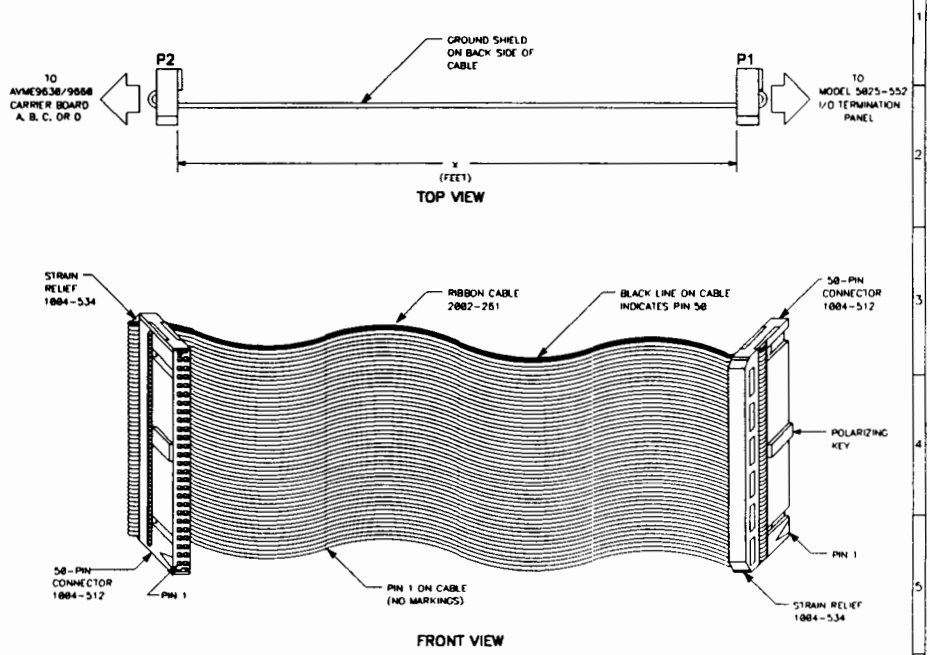

NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

Acromag
CABLE 5025-550-x, NON-SHIELDED
4501-462




MODEL 5025-551-x SCHEMATIC

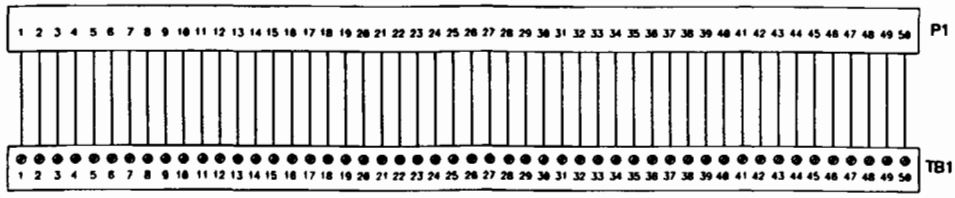


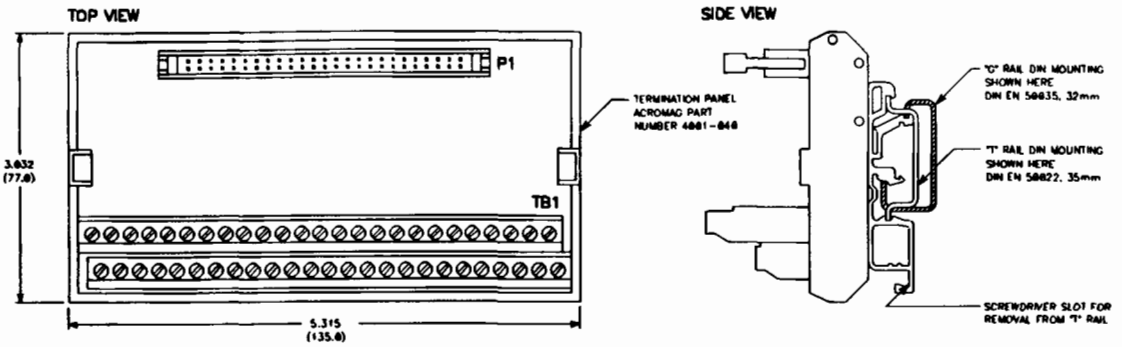

NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX-XXX).

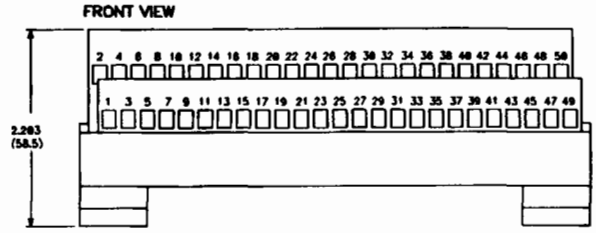
MODEL 5025-551-x SIGNAL CABLE, SHIELDED

Acromag
CABLE 5025-551-x, SHIELDED
4501-463

## MODEL 5025–552 SIMPLIFIED SCHEMATIC



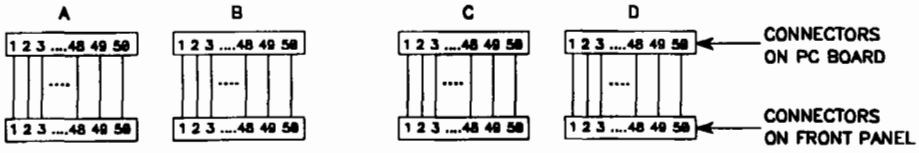



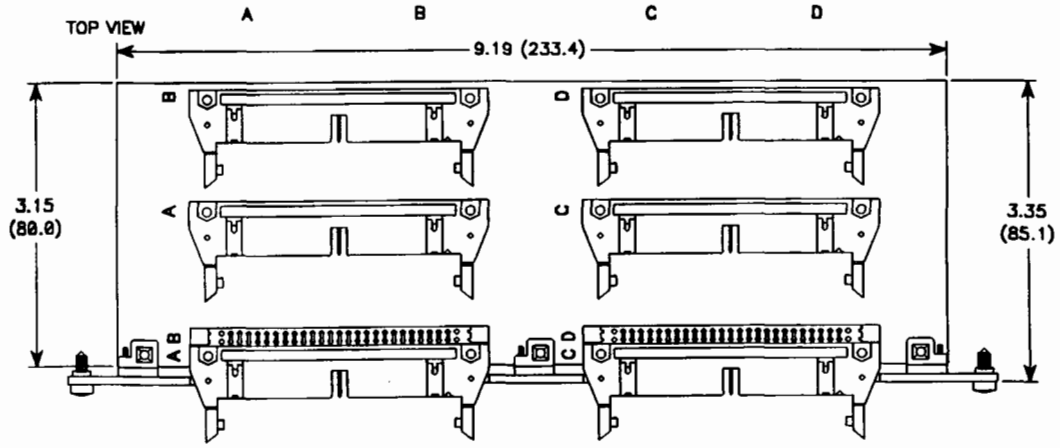

## MODEL 5025–552 TERMINATION PANEL MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

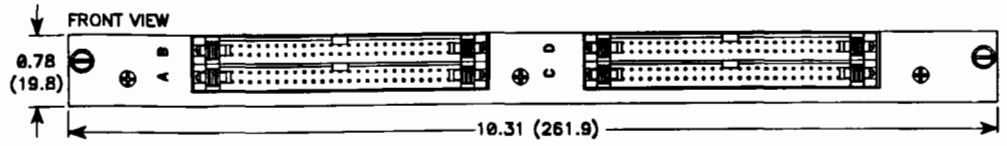
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: +/-0.020 (+/-0.5).

Acromag — MODEL 5025-552 TERMINATION PANEL — 4501-484

## MODEL TRANS–GP MODULE SCHEMATIC




## TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

Acromag — MODEL TRANS-GP TRANSITION MODULE — 4501-465

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