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Acromag®

Series IP235 and IP230 Industrial I/O Pack
16-Bit High Density Analog Output Module

USER'S MANUAL

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Table of Contents **Page**

1.0 GENERAL INFORMATION 2
KEY IP235 and IP230 FEATURES 3
INDUSTRIAL I/O PACK INTERFACE FEATURES 3
SIGNAL INTERFACE PRODUCTS 3
INDUSTRIAL I/O PACK SOFTWARE LIBRARY 4
2.0 PREPARATION FOR USE 4
UNPACKING AND INSPECTION 4
CARD CAGE CONSIDERATIONS 4
BOARD CONFIGURATION 4
Default Hardware Jumper Configuration 4
Analog Output Ranges & Corresponding Digital Codes 4
Analog Output Range Hardware Jumper Configuration 5
Software Configuration 5
CONNECTORS 5
IP Field I/O Connector (P2) 5
Analog Outputs: Noise and Grounding Considerations .. 5
External Trigger Input/Output 5
IP Logic Interface Connector (P1) 6
3.0 PROGRAMMING INFORMATION 6
IP IDENTIFICATION SPACE 6
I/O SPACE ADDRESS MAP 6
Control Register 7
Timer Prescaler Register 8
Conversion Timer Register 8
Waveform Memory Data Register 8
Waveform Memory Address Register 9
Calibration Coefficient Access Register 9
Calibration Coefficient Status Register 9
Start Convert Register 10
DAC Channel Registers 10
Interrupt Vector Register 10
DAC MODES OF CONVERSION 10
Single Convert From DAC Register 10
Single Convert From Waveform Memory 11
Cycle Once Through Waveform Memory and Stop 11
Continuous Cycle Through Waveform Memory 11
Convert On External Trigger Only 11
PROGRAMMING CONSIDERATIONS 11
Single Conversion From DAC Register Example 11
Single Conversion From Waveform Memory Example ... 11
Cycle Once Through Waveform Memory & Stop 12
Cycle Once and Interrupt Example 12
USE OF CALIBRATION DATA 13
Uncalibrated Performance 13
Calibrated Performance 13
Calibrated Programming Example 13
4.0 THEORY OF OPERATION 14
FIELD ANALOG OUTPUTS 14
LOGIC/POWER INTERFACE 14
IP INTERFACE LOGIC 14
CONTROL LOGIC 15
DATA TRANSFER FROM FPGA To INDIVIDUAL DACs 15
INTERVAL TIMER 15
EXTERNAL TRIGGER 15
INTERRUPT CONTROL LOGIC 15
CALIBRATION MEMORY CONTROL LOGIC 15
5.0 SERVICE AND REPAIR 15
SERVICE AND REPAIR ASSISTANCE 15
PRELIMINARY SERVICE PROCEDURE 16
6.0 SPECIFICATIONS 16
GENERAL SPECIFICATIONS 16
ANALOG OUTPUT 16
INDUSTRIAL I/O PACK COMPLIANCE 17
APPENDIX 18
CABLE: MODEL 5025-551 18
TERMINATION PANEL: MODEL 5025-552 18
TRANSITION MODULE: MODEL TRANS-GP 18

DRAWINGS **Page**

4501-434 IP MECHANICAL ASSEMBLY 19
4501-619 IP235 and IP230 JUMPER LOCATION 20
4501-620 ANALOG OUTPUT CONNECTION 21
4501-621 IP235 and IP230 BLOCK DIAGRAM 22
4501-463 CABLE 5025-551 (SHIELDED) 23
4501-464 TERMINATION PANEL 5025-552 24
4501-465 TRANSITION MODULE TRANS-GP 24

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP235 and IP230 modules are precision 16-bit, high density, single size IP, analog output boards with up to eight analog voltage output channels. Each of the output channels on both the IP235 and IP230 has a dedicated register from which digital values are read and simultaneously transferred to its corresponding Digital-to-Analog-Converter (DAC). Each of the eight output channels of the IP235 also has a dedicated 2K deep RAM buffer from which digital values can be read and simultaneously transferred to the (DAC).

The IP235 and IP230 are available with cost effective four or eight 16-bit analog output channels. The IP235 and IP230 are available in standard and extended temperature range modules as follows:

Model	Analog Output Channels	Waveform Memory	Temperature Range
IP235-4	4	Yes	0 to +70°C
IP235-4E	4	Yes	-40°C to +85°C
IP235-8	8	Yes	0 to +70°C
IP235-8E	8	Yes	-40°C to +85°C
IP230-4	4	No	0 to +70°C
IP230-4E	4	No	-40°C to +85°C
IP230-8	8	No	0 to +70°C
IP230-8E	8	No	-40°C to +85°C

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The IP235 and IP230 utilize state of the art Surface Mounted Technology (SMT) to achieve their high channel density. Four units may be mounted on a carrier board to provide up to 32 analog output channels per 6U-VMEbus system slot or ISA bus (PC/AT) system slot. The IP235 and IP230 offer a variety of features which make them an ideal choice for many industrial and scientific applications as described below.

KEY IP235 and IP230 FEATURES

- **DAC 16-Bit Resolution** - 16-bit monolithic DAC with bipolar voltage output ranges of ±10V, ±5V, and an unipolar output range of 0 to 10V.
- **10μsec Conversion Time** - A maximum recommended conversion rate of 100KHz, for specified accuracy, is supported. The absolute maximum conversion rate of 150KHz is also supported.
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration for both gain and offset correction for each of the channels of the module.
- **Reset is Failsafe For Bipolar Output Ranges -** When the module is jumpered for bipolar operation, the analog outputs are reset to 0 volts upon power up or issue of a software or hardware reset. This eliminates the problem of applying random output voltages to actuators during power on sequences.
- **Individual Output Control -** Output channels can be individually updated. Other channels not updated maintain their previous analog output values.
- **Simultaneous Output Control -** All output channels are simultaneously updated upon issue of a software or external trigger.
- **Hardware Jumper Setting For Selection of DAC Ranges** - Both bipolar (±5V, ±10V) and unipolar (0 to 10V) ranges are available. The ranges can be selected on a per channel basis.
- **External Trigger Scan Mode** - All channels simultaneously implement a new conversion with each external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Output** - The external trigger is assigned to a field I/O line. The external trigger may be configured as an output signal to provide a means to synchronize other IP235 or IP230 devices to a single IP235 or IP230 module.

KEY IP235 FEATURES

- **User Programmable Interval Timer** - A user programmable interval timer is provided to control the delay between conversions. All channels are simultaneously converted. Then after a delay specified by the interval timer, new digital values are read from memory and all channels are simultaneously converted. This feature supports a minimum interval of 6.7μsec and a maximum interval of 2.09 seconds.
- **Single Step Mode** - On each new software or external trigger, all output channels are simultaneously updated with a new digital value read from their 2K deep waveform memory.
- **One Cycle Output Mode -** Each of the output channels is simultaneously updated with the digital value from its corresponding waveform memory. Conversions start with the first digital value in memory and continue at the rate set by the interval timer until one cycle through waveform memory has completed. Conversions are initiated by issue of a software or external trigger.
- **Continuous Output Mode -** All output channels are simultaneously updated with a new digital value from their corresponding waveform memory. Continuous conversions are implemented by continuously cycling through the waveform memory until halted by software. The interval between conversions is controlled by the interval timer. Conversions are initiated by issue of a software or external trigger.
- **Interrupt Upon Conversion Complete Mode** - The IP235 can be programmed to interrupt after completion of one cycle through waveform memory has completed.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 32 DAC channels in a single system slot. Both VMEbus and ISA bus (PC/AT) carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID signature which can be read via access to the ID space.
- **16-bit and 8-bit I/O** - Port register Read/Write is performed through data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 1 wait state is required for reading all control registers and ID values. Interrupt select cycles also require 1 wait state for reading the interrupt vector. All write cycles require 1 wait state except for the IP230-8 where 0 wait state writes are implemented. Read or write of the waveform memory buffers requires 4 wait states.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board. Acromag's AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards and Acromag's APC8610 ISA bus (PC/AT) carrier board are supported. A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the 16-bit IP235 and IP230 analog output modules, use of the shortest possible length of shielded output cable is recommended.

Cables

Model 5025-551-X (Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, APC8610, or other compatible carrier boards, to Model 5025-552 termination panels. The "-X" suffix of the model number is used to indicate the length in feet. The shielded cable is highly recommended for optimum performance with the IP235 and IP230 analog output module.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, APC8610, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them).

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It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both VMEbus and ISA bus (PC/AT) applications. All functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO235.TXT" or "INFO230.TXT" file in the appropriate "IP235" or "IP230" subdirectory "\VMEIP" or "\PCIP", according to your carrier.

INDUSTRIAL I/O PACK OLE CONTROL SOFTWARE

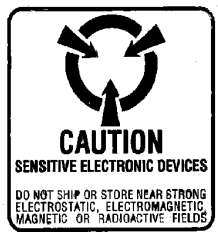
Acromag provides a software diskette of Industrial I/O Pack Object Linking and Embedding (OLE) drivers for Windows 95 and Windows NT compatible application programs (Model IPSW-DVR-OLE-PC, MSDOS format). This software provides individual drivers that allow Acromag I/O Packs and our personal computer carriers to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, etc. The OLE controls provide a high-level interface to Acromag I/O Packs, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a Carrier Configuration Program, and carrier OLE control, and an OLE control for each Acromag I/O Pack model.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.



This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. Jumper settings are discussed in the following sections. The jumper locations are shown in Drawing 4501-619.

Remove power from the board when configuring hardware jumpers, installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following paragraphs for configuration and assembly instructions.

Default Hardware Jumper Configuration

The board is shipped from the factory, configured as follows:

- Each analog output range is configured for a bipolar output with a 20 volt span (i.e. a DAC output range of -10 to +10 Volts).
- The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired mode before starting DAC analog output conversions.

Analog Output Ranges and Corresponding Digital Codes

The IP235 and IP230 are designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. Table 2.1 indicates the relationship between the data format and the ideal analog output voltage for each of the analog output ranges. Selection of an analog output range is implemented via the jumper setting given in Table 2.2.

Table 2.1: Full-Scale Ranges and Ideal Analog Output

DESCRIPTION	Digital Input Code	ANALOG OUTPUT		
Output Range		±10V	0 to 10V	±5V
LSB (Least Significant Bit) Weight		305µV	153µV	153µV
+ Full Scale Minus One LSB	$7FFF_H$	9.999695 Volts	9.999847 Volts	4.999847 Volts
Midscale	0000_H	0V[1]	5V[1]	0V[1]
One LSB Below Midscale	$FFFF_H$	-305µV	4.999847 Volts	-153µV
- Full Scale	8000_H	-10V	0V	-5V

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Notes (Table2.1):

1. Upon power-up or software reset the bipolar ranges will output 0 volts while the unipolar range will output 5 volts.

Analog Output Range Hardware Jumper Configuration

The output range of the DACs are individually programmed via hardware jumpers J1 to J8. Jumpers J1 to J8 are used to control channels 0 to 7, respectively. The jumpers control the output voltage span and the selection of unipolar or bipolar output ranges. J1 to J8 pins 1 and 2 control the selection of unipolar or bipolar output ranges. J1 to J8 pins 3 and 4 control the selection of output voltage span. The configuration of the jumpers for the different ranges is shown in Table 2.2. "ON" means that the pins are shorted together with a shorting clip. "OFF" means that the clip has been removed. The individual jumper locations are shown in Drawing 4501-619.

Table 2.2: Analog Output Range Selections/Jumper Settings

Desired ADC Output Range (VDC)	Output Span (Volts)	Required Output Type	J1 to J8 Pins (1&2)	J1 to J8 Pins (3&4)
-5 to +5	10	Bipolar	ON	ON
-10 to +10**	20	Bipolar	ON	OFF
0 to +10	10	Unipolar	OFF	ON

** The board is shipped with the default jumper setting for the ±10 volt DAC output range.

Software Configuration

Software configurable control registers are provided for control of external trigger mode, conversion mode, timer control, and interrupt mode selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as desired before starting DAC analog output conversions. Refer to section 3 for programming details.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.3) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board). When reading Table 2.3 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively. Further, note that the output signals all have the same ground reference ("-CH00" and the minus leads of all other channels are connected to analog common on the module).

Table 2.3: IP235[2] and IP230[2] Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
+CH00	1	COMMON[1]	26
-CH00[1]	2	COMMON[1]	27
COMMON[1]	3	COMMON[1]	28
+CH01	4	COMMON[1]	29
-CH01[1]	5	COMMON[1]	30
COMMON[1]	6	COMMON[1]	31
+CH02	7	COMMON[1]	32
-CH02[1]	8	COMMON[1]	33
COMMON[1]	9	COMMON[1]	34
+CH03	10	COMMON[1]	35
-CH03[1]	11	COMMON[1]	36
COMMON[1]	12	COMMON[1]	37
+CH04	13	COMMON[1]	38
-CH04[1]	14	COMMON[1]	39
COMMON[1]	15	COMMON[1]	40
+CH05	16	COMMON[1]	41
-CH05[1]	17	COMMON[1]	42
COMMON[1]	18	COMMON[1]	43
+CH06	19	COMMON[1]	44
-CH06[1]	20	COMMON[1]	45
COMMON[1]	21	COMMON[1]	46
+CH07	22	COMMON[1]	47
-CH07[1]	23	COMMON[1]	48
COMMON[1]	24	EXT TRIGGER*	49
COMMON[1]	25	SHIELD	50

Notes:

1. The minus leads of all channels are connected to analog common on the module.
2. Channels 04 through 07 are only present on 8 channel models.

Analog Outputs: Noise and Grounding Considerations

All output channels are referenced to analog common on the module (See Drawing 4501-620 for analog output connections), but each channel has a separate return (minus lead) to maintain accuracy and reduce noise. Still, the accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads > 100KΩ) provide the best accuracy. For low impedance loads, the IP235 and IP230 can source up to 5mA, but the effects of source and cabling resistance should be considered.

Output common is electrically connected to the IP module analog ground which connects to logic ground of the module at the DAC's. As such, the IP235 and IP230 are non-isolated between the logic and field I/O grounds. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog outputs when a high level of accuracy/resolution is needed. Refer to Drawing 4501-620 for example output and grounding connections.

External Trigger Input/Output

The external trigger signal on pin 49 of the P2 connector can be programmed to accept a TTL compatible external trigger input signal, or output hardware timer generated triggers to allow synchronization of multiple IP235 or IP230 modules.

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As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The trigger pulse must be low for a minimum of 250n seconds to guarantee acquisition. It must not stay low for more than 6μ seconds, or additional, unwanted conversions may be triggered. The actual conversion is triggered within 6.25μ seconds of the falling edge of the external trigger signal. This type of conversion triggering can be used to synchronize generation of analog output signals to external events.

As an output an active-low TTL signal can be driven to additional IP235s, thus providing a means to synchronize the conversions of multiple IP235s. The additional IP235s must program their external trigger for signal input and convert on external trigger only mode. The trigger pulse generated is low for typically 125n seconds. See section 3.0 for programming details to make use of this signal.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.4).

Table 2.4: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

IP IDENTIFICATION - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP235 and IP230 ID information space does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC ISA bus. The IP235 and IP230 ID space contents are shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 1 wait state.

Table 3.1: IP235 ID Space Identification (ID)

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		12(IP235-8) 13(IP235-4) 18(IP230-8) 19(IP230-4)	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		D8 IP235-8 B9 IP235-4 96 IP230-8 F7 IP230-4	CRC
19 to 3F		yy	Not Used

Notes (Table 3.1):

1. The IP model number is represented by a two-digit code within the ID space (for example the IP235-8 model is represented by 12 Hex).

I/O SPACE ADDRESS MAP

This board is addressable in the Industrial Pack I/O space to control the conversion of analog outputs to the field. As such, three types of information are stored in the I/O space: control, status, and data.

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The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IP235 and IP230 use only a portion of this space. The I/O space address map for the IP235 and IP230 is shown in Table 3.2. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space.

Table 3.2: IP235 & IP230 I/O Space Address Memory Map[2]

Hex Base Adr+	MSB D15 D08	LSB D07 D00	Hex Base Adr+
00	Control Register		01
02	Not Used	Timer Prescaler[3]	03
04	Conversion Timer[3]		05
06	Waveform Memory Data Register[3]		07
08	Waveform Memory Address Register[3]		09
0A	Rd Wr~ / Calibration Coefficient Address	Calibration Coefficient Write Data	0B
0C	Calibration Coefficient Read Data	Wr Busy / Rd Comp	0D
0E	Not Used Bits15 to Bit 01	Start Convert Bit-0	0F
10	DAC Channel 0		11
12	DAC Channel 1		13
14	DAC Channel 2		15
16	DAC Channel 3		17
18	DAC Channel 4[4]		19
1A	DAC Channel 5[4]		1B
1C	DAC Channel 6[4]		1D
1E	DAC Channel 7[4]		1F
20	Not Used[1]	Interrupt Vector[3]	21
22	Reserved[5]	Not Used[1]	23
24	Not Used[1] ⇓		25
7E	Not Used[1]		7F

Notes (Table 3.2):

1. The IP will not respond to addresses that are "Not Used".
2. All Reads are 1 wait state (except read or write of the waveform memory which requires 4 wait states). Writes are 1 wait state except for the IP230-8 which has 0 wait states.
3. These registers are not used on the IP230 since the IP230 does not include waveform memory or interrupt capability.
4. Channels 4-7 are only present on 8 channel models.
5. This byte is reserved for use at the factory to enable writing of the calibration coefficients.

This memory map reflects byte accesses using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, installation of this module on a PC carrier board will require the use of the even address locations to access the lower 8-bit data while on a VMEbus carrier use of odd address locations are required.

Control Register, (Read/Write) - (Base + 00H)

This read/write register is used to: individually select a waveform memory buffer for read or write, control the external trigger, select one of the digital-to-analog conversion modes, enable interrupts, and issue a software reset.

The function of each of the control register bits are described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.3: Control Register

BIT	FUNCTION
2,1,0[2]	Waveform Memory Select for Read or Write 000 = Channel 0 001 = Channel 1 010 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7
3	Not Used[1]
4[2]	Automatic Increment of Memory Address 0 = Automatic Increment Disabled 1 = Automatic Increment Enabled This bit when set will automatically increment the value of the address used to access waveform memory. After completion of a memory read or write cycle the address is automatically incremented for the next access.
6, 5	External Trigger Control 00 = External Trigger Input: External, Software, and Internal Timer triggers are all enabled 01 = External Trigger Input: External triggers are only enabled. Software and Internal Timer triggers are disabled. 10 = External Trigger Output: Software and Internal Timer triggers are output on the External trigger pin of the field I/O connector. It is possible to synchronize the conversion of multiple IP235 or IP230 modules. A single master IP235 or IP230 must be selected to output the external trigger signal (bit 6 and 5 set to "10") while all other modules are selected to input the external trigger signal (bit 6 and 5 set to "01"). The external trigger signals (pin 49 of the field I/O connector) of all modules to be synchronized must be wired together.

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BIT	FUNCTION
7	Not Used[1]
10, 9, 8	DAC Conversion Mode 000 = Disabled 001 = Single Conversion from DAC registers 010^2 = Single Conversion from Waveform Memory 011^2 = Cycle Once through Waveform Memory 100^2 = Cycle Once through Waveform Memory then Generate Interrupt 101^2 = Continuously Cycle through Waveform Memory 110, 111 = Not Defined All modes require either the software start convert or an external trigger to initiate DAC conversions.
11 to 14	Not Used[3]
15	Perform Software Reset when Set[3]

Notes (Table 3.3):

1. All bits labeled "Not Used" will return the last value written on a read access.
2. These bits are not used on the IP230 since the IP230 does not include waveform memory or interrupt capability.
3. Bits 11 to 15 will return random values when read.

Timer Prescaler Register (Read/Write, 03H)

The Timer Prescaler register is an 8-bit register that can be written with an 8-bit or 16-bit data transfer to control the interval time between conversions. This register is defined for the IP235 module only since the IP230 does not include an internal timer.

Timer Prescaler Register							
MSB							LSB
07	06	05	04	03	02	01	00

This 8-bit number divides the 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 35 hex or 53 decimal. A Timer Prescaler value of less then 53 (decimal) will result in unpredictable operation. This minimum value corresponds to a conversion interval of 6.625μ seconds which translates to the maximum conversion rate of about 150KHz. Although the board will operate at the 150KHz conversion rate, conversion accuracy will be sacrificed. To achieve specified conversion accuracy a maximum conversion rate of 100KHz is recommended (see the specification chapter for details regarding accuracy).

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows.

Reading or writing to this register is possible via 16-bit or 8-bit data transfers. The Timer Prescaler register contents are cleared upon reset.

Conversion Timer Register (Read/Write, 04H)

The Conversion Timer Register can be written to control the interval time between conversions. Read or writing to this register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset. This register is defined for the IP235 module only since the IP230 does not include an internal timer.

Conversion Timer Register															
MSB								LSB							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

This 16-bit number is the second divisor of the 8MHz clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by the 8MHz clock signal. The output of this clock is input to the second counter, the Conversion Timer, whose output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{8} = \text{T in } \mu \text{ seconds}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 53 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval which can be programmed to occur is (53 * 1) ÷ 8 = 6.625μ seconds. This minimum of 6.625μ seconds is defined by the minimum conversion time of the hardware but does sacrifice conversion accuracy. To achieve specified conversion accuracy a minimum conversion time of 10μ seconds is recommended (see the specification chapter for details regarding accuracy).

Waveform Memory Data Register (Read/Write, 06H)

The Waveform Memory Data register is used to provide read or write access to waveform memory. Reading or writing to this register is possible via 16-bit data transfers only. This register is defined for the IP235 module only since the IP230 does not include waveform memory.

In order to properly access the waveform memory, which constitutes 2048 words for each of the DAC channels, an address pointer to a single word in memory must first be specified. The address is specified via the least significant 3-bits of the control register and the Waveform Memory Address register. The first three bits of the control register are used to select a specific channel's waveform memory block. The Waveform Memory Address register is used to point to one of the 2048 words corresponding to the selected channel.

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All read or write accesses to the Waveform Memory Data register will in turn implement an access to waveform memory at the address specified by the control register and the Waveform Address register.

The address specified in the Waveform Memory Address register will be automatically incremented after the read or write cycle is completed if bit-4 of the control register is set to "1". Thus, when consecutive locations within the waveform memory are accessed the Waveform Memory Address register need not be manually updated by software.

Read or write accesses to this register require four wait states. A software or hardware reset has no affect on this register.

Waveform Memory Address Register (Write Only, 08H)

The Waveform Memory Address register is used to point to one of 2048 words in waveform memory. Bits 1 to 11 are used to specify one of 2048 words that can be accessed via a read or write to the Waveform Memory Data register. Writing to this register is possible via 16-bit data transfers only. This register is defined for the IP235 module only since the IP230 does not include waveform memory.

Waveform Memory Address Register		
Unused	Address Value	Unused
15, 14, 13, 12	11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1	0

In order to properly access the waveform memory, which constitutes 2048 words for each of the DAC channels, an address pointer to a single word in memory must be first specified. The address is specified via the least significant 3-bits of the Control register and 11-bits of this Waveform Memory Address register. The first three bits of the control register are used to select the channel to be accessed while the Waveform Memory Address register is used to point to one of 2048 words. After the address is programmed, an access to the Waveform Memory Data register is required to implement the actual memory access.

The address specified in the Waveform Memory Address register will be automatically incremented after the read or write cycle to the Waveform Memory Data register is completed if bit-4 of the control register is set to "1". Thus, when consecutive locations within the waveform memory are accessed the Waveform Memory Address register need not be manually incremented by software.

A write access to this register requires one wait state. A software or hardware reset will clear this register to zero.

Calibration Coefficient Access Register (Write, 0AH)

This register configures access to the calibration coefficient memory. Calibration data is provided so that software can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in this memory. These coefficients can be retrieved using this register.

The Calibration Coefficient Access Register is a write-only register and is used to configure and initiate a read cycle to the calibration coefficient memory. Setting bit-15 of this register high, to a "1'', initiates a read cycle.

The address of the calibration coefficient to be read must be specified on bits 14 to 8 of Calibration Coefficient Access register. The address location of each of the gain and offset coefficient is given in table 3.4.

Most Significant Byte of Calibration Coefficient Access Reg	
Read or Write~	Calibration Coefficient Address
15	14, 13, 12, 11, 10, 9, 8

Write accesses to the Calibration Coefficient Access register require one wait state and are possible via 16-bit data transfers only. A software or hardware reset has no affect on this register.

The address location of each of the gain and offset coefficients is given in table 3.4. The address corresponding to each of the offset and gain coefficients for each of the channels and ranges is given in hex. The coefficients are 16-bit values with the most significant byte at the even addresses and the least significant bytes at the odd addresses for big endian systems. The calibration coefficients are stored as 1/4 LSB's. For additional details on the use of the calibration coefficients, refer to the "Use of Calibration Data" section.

Table 3.4: Offset and Gain Address Memory Map

Channel		Offset Coefficient Address (Hex)		Gain Coefficient Address (Hex)	
		MSB	LSB	MSB	LSB
±10 Volt Range	0	00	01	02	03
	1	04	05	06	07
	2	08	09	0A	0B
	3	0C	0D	0E	0F
	4	10	11	12	13
	5	14	15	16	17
	6	18	19	1A	1B
	7	1C	1D	1E	1F
±5 Volt Range	0	20	21	22	23
	1	24	25	26	27
	2	28	29	2A	2B
	3	2C	2D	2E	2F
	4	30	31	32	33
	5	34	35	36	37
	6	38	39	3A	3B
	7	3C	3D	3E	3F
0 to 10 Volt Range	0	40	41	42	43
	1	44	45	46	47
	2	48	49	4A	4B
	3	4C	4D	4E	4F
	4	50	51	52	53
	5	54	55	56	57
	6	58	59	5A	5B
	7	5C	5D	5E	5F

Calibration Coefficient Status Register (Read, 0CH)

The Calibration Coefficient Status register is a read-only register and is used to access the calibration coefficient read data and determine the status of a read cycle initiated by the Calibration Coefficient Access register. In addition this register is used to determine the status of a write cycle to the coefficient memory. Bit-1

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of this register when set indicates the coefficient memory is busy completing a write cycle.

All read accesses to this Calibration Coefficient Status register initiate an approximately 1m second access to the coefficient memory. **Thus, you must wait 1m second after reading this status register before a new read or write cycle to the coefficient memory can be initiated.**

A read request of the coefficient memory, initiated through the Calibration Coefficient Access register, will provide the addressed byte of the calibration coefficient on data bits 15 to 8 of the Calibration Coefficient Status register. Although the read request via the Calibration Coefficient Access register is accomplished in less then 800n seconds, typically, the calibration coefficient will not be available in the Calibration Coefficient Status register for approximately 2.5m seconds.

Bit-0 of the Calibration Coefficient Status register is the read complete status bit. This bit will be set high to indicate that the requested calibration coefficient is available on data bits 15 to 8 of this status register. This bit is cleared upon initiation of a new read access of the coefficient memory or upon issue of a software or hardware reset.

Writes to calibration coefficient memory required a special enable code. Writes to coefficient memory are normally only performed at the factory. The module should be returned to Acromag if recalibration is needed.

A write operation to the calibration coefficient memory, initiated via the Calibration Coefficient Access register, will take approximately 5m seconds. Bit-1 of the Calibration Coefficient Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation, and bit-1 will remain high until the requested write operation has completed. New read or write accesses to the coefficient memory, via the Calibration Coefficient Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A software or hardware reset of the IP module will also clear this bit to 0.

Read accesses to Calibration Coefficient Status register require one wait state and are possible via 16-bit data transfers only. A software or hardware reset will clear all bits to 0.

Start Convert Register (Write Only, 0FH)

The Start Convert register is a write-only register and is used to trigger conversions by setting data bit-0 to a logic one. The desired mode of conversion must first be configured by setting the following registers to the desired values and modes: Control, Interrupt Vector, Timer Prescaler, and Conversion Timer.

This register can be written with either a 16-bit or 8-bit data value. Data bit-0 must be a logic one to initiate data conversions.

When External Trigger Only mode is selected via bits 6 and 5 of the control register (set to “01”), the Software Start Convert bit is disabled from starting data conversions.

Start Convert Register							
Not Used							Start Convert
07	06	05	04	03	02	01	00

The actual conversion will be initiated 6.625μ seconds after setting the Start Convert Bit. Thus in single conversion mode, you cannot reload the DAC registers with new data until at least 6.625μ seconds after a start convert.

DAC Channel Registers (Write Only, 10H to 1EH)

The DAC Channel registers are write only registers and are used to hold the 16-bit digital values that are to be output to the Digital-to-Analog-Converter’s (DAC’s). The contents of the DAC registers are simultaneously transferred to their corresponding converter upon issue of a software or external trigger.

Table 3.2 lists each of the DAC Channel registers with their corresponding hex address in I/O space memory.

Writing this register requires one wait state for all but the IP230-8 which requires 0 wait states and is possible via 16 or 8 bit data transfers. Software or hardware resets will clear the contents of the DAC Channel registers to 0.

Interrupt Vector Register (Read/Write, 21H)

The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL* cycle. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

This register is defined for the IP235 module only since the IP230 does not include interrupt capability.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

Interrupts are released on an interrupt acknowledge cycle. Reading the interrupt vector during an interrupt acknowledge cycle signals the IP235 to remove its interrupt request. Issue of a software or hardware reset will clear the contents of this register to 0.

DAC MODES OF CONVERSION

The IP235 provides four methods of analog output operation for maximum flexibility with different applications. The IP230 provides a single method of analog output operation. The following sections describe the features of each and how to best use them.

Single Conversion from DAC Register-Mode

This mode of operation can be used on the IP235 and IP230 modules. It can be used to update from a single DAC channel to all DAC channels with a new analog output voltage. With each conversion, initiated by a software or external trigger, the digital values in each of the DAC Channel registers are simultaneously moved to their corresponding converter for update of their analog output signal. It is possible to keep a given channel’s analog voltage unchanged by simply keeping the digital value in the channel’s DAC register unchanged. Only those channels with updated digital values

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in their corresponding DAC Channel registers will result in different analog output voltages.

Each of the DAC Channel register's digital values is moved to its corresponding converter for simultaneous conversion upon issue of a software or external trigger.

Single Conversion from Waveform Memory-Mode

In Single Conversion from Waveform Memory mode of operation, one value for each of the channels is moved from waveform memory to its corresponding converter. All channels are simultaneously updated. This mode of operation is only available on the IP235 modules.

To initiate this mode of operation the control register must be set with the DAC conversion mode "010" on bits 10 to 8. The address of the word moved from waveform memory to the DAC must also be specified via the Waveform Memory Address register. Then, issuing a software start convert or external trigger will initiate the simultaneous update of all channels. The interval timer is not used in this mode of operation.

Cycle Once Through Waveform Memory and Stop-Mode

In Cycle Once Through Waveform Memory mode of operation, one pass through waveform memory for each of the channels is implemented. That is, 2048 values for each of the channels are converted. The first value converted for each of the channels corresponds to address zero while the last value corresponds to address 2047. All channels are simultaneously updated at an interval controlled by the interval timer or external trigger signal. This mode of operation also includes an option to issue an interrupt upon conversion of the last digital value in waveform memory. This conversion mode is only available on the IP235 modules.

To initiate this mode of operation the control register must be set with the DAC conversion mode "011", or "100" (interrupt enabled) on bits 10 to 8. Then, issuing a software start convert or external trigger will initiate the simultaneous update of all channels.

Continuously Cycle Through Waveform Memory - Mode

In the Continuous Cycle mode of operation, the hardware controls the continuous cycling through waveform memory for each of the channels. Digital data from each channel's corresponding waveform memory is simultaneously transferred and converted at the rate specified by the interval timer or external trigger. This mode of operation is ideal for waveform generation. This conversion mode is only available on the IP235 modules.

To initiate this mode of operation the control register must be set with DAC conversion mode "101" on bits 10 to 8. Then, issuing a software start convert or external trigger will initiate the simultaneous and continuous update of all channels.

Convert On External Trigger Only

When bit-6 and 5 of the control register are set to digital code "01", each conversion is initiated by an external trigger only (logic low pulse) input to the EXT TRIGGER* signal of the P2 connector. Conversions are performed for each channel simultaneously with each external trigger pulse. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation.

The external trigger signal is configured as an input for this mode of operation.

External Trigger Only mode of operation can be used to synchronize multiple IP235 modules to a single module running in a continuous cycle mode. The external trigger, of the IP235 "master", must be programmed as an output. The external trigger signal of that IP235 must then be connected to the external trigger signal of all other IP235 modules, programmed for external trigger input, that are to be synchronized. These other IP235 modules must be programmed for External Trigger Input only mode. Data conversion can then be started by writing high to the Start Convert bit of the master IP235 configured for continuous cycle mode.

PROGRAMMING CONSIDERATIONS FOR GENERATION OF ANALOG OUTPUTS

The IP235 and IP230 provide different methods of analog output generation to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion from DAC Register Example

This mode of operation is available on both the IP235 and IP230 modules.

1. Execute Write of 0100H to Control Register at Base Address + 00H.
   a) External, Software, and Hardware timer genterated triggers are all enabled.
   b) Single Conversion from DAC registers is enabled.

2. Execute Write of 7FFFH to each DAC Channel Register starting at Base Address + 10H. This will drive each analog output to plus full scale minus one least significant bit.

3. Execute Write 0001H to the Start Convert Bit at Base Address + 0EH. This starts the simultaneous transfer of the digital data in each DAC Channel register to its corresponding converter for analog conversion.

Single Conversion from Waveform Memory Example

This mode of operation is only available on the IP235 module. In this example, only channel 0 and 1's analog outputs are to be updated to minus full scale and mid-scale, respectively. This example assumes the waveform memory corresponding to channels 2 to 7 has previously been loaded with their desired digital values.

1. Execute Write of 0200H to Control Register at Base Address + 00H.
   a) Channel 0's Waveform Memory bank is selected.
   b) External, Software, and Hardware triggers are all enabled
   c) Single Conversion from waveform memory is enabled.

2. Execute Write of 0H to the Waveform Memory Address Register at Base Address + 08H. The first location in the waveform memory bank is selected.

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3. Execute Write of 8000H to Waveform Memory Data Register at Base Address + 06H. Channel 0's first Waveform Memory location is written with digital value 8000H. This digital value will provide a minus full scale analog output on channel 0 when converted.

4. Execute Write of 0201H to Control Register at Base Address + 00H. Channel 1's Waveform Memory bank is selected.

5. Execute Write of 0H to Waveform Memory Data Register at Base Address + 06H. Channel 1's first Waveform Memory location is written with digital value 0H. This digital value will provide a mid-scale analog output on channel 1 when converted.

6. Execute Write of 0001H to the Start Convert Bit at Base Address + 0EH. This starts the simultaneous transfer of digital data from each of the waveform memories to its corresponding converter for analog conversions.

Cycle Once Through Waveform Memory and Stop Example

This mode of operation is only available on the IP235 module. This example assumes the Waveform memory corresponding to each of the channels has previously been loaded with the desired digital values, with the exception of channel 7's first two digital values in memory which are to be updated to minus full scale and mid-scale, respectively. In addition, the interval timer will be set for an 80μ second interval.

1. Execute Write of 0317H to Control Register at Base Address + 00H.
   a) Channel 7's Waveform Memory bank is selected.
   b) Automatic increment of memory address is selected.
   c) External, Software, and Hardware timer generated triggers are all enabled.
   d) Cycle once through waveform memory mode is selected.

2. Execute Write of 0H to the Waveform Memory Address Register at Base Address + 08H. The first location in the waveform memory corresponding to channel 7 is selected.

3. Execute Write of 8000H to Waveform Memory Data Register at Base Address + 06H. Channel 7's first Waveform Memory location is written with digital value 8000H. This digital value will provide a minus full scale analog output when converted.

4. Execute Write of 0H to Waveform Memory Data Register at Base Address + 06H. Channel 7's second Waveform Memory location is written with digital value 0H. This digital value will provide a mid-scale analog output when converted. Note that the waveform memory address was automatically incremented to point to this second location in waveform memory.

5. Execute Write of 50H to the Timer Prescaler Register at Base Address + 02H. This sets the Timer Prescaler to 80 decimal.

6. Execute Write of 08H to the Conversion Timer Register at Base Address + 04H. The conversion timer in conjunction with the Timer Prescaler sets the interval time between conversions to (80 ∗ 8) ÷ 8 = 80μ seconds.

7. Execute Write of 0001H to the Start Convert Bit at Base Address + 0EH. This starts the simultaneous transfer of digital data from each of the waveform memories to its corresponding converter for analog conversions. Conversions will continue until one cycle through waveform memory for all of the channels is completed.

Cycle Once Through Waveform Memory with Interrupt Example

An interrupt can be enabled for generation after completion of one cycle through waveform memory. Interrupts generated by the IP235 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism is Release On Acknowledge (ROAK) type. That is, the IP235 will release the INTREQ0* signal during an interrupt acknowledge cycle from the carrier.

The IP235 Interrupt Vector register can be used as a pointer to an interrupt handling routine. The vector is an 8-bit value and can be used to point to any one of 256 possible locations to access the interrupt handling routine.

This example assumes that the IP235 is installed onto an Acromag AVME9630/60 carrier board (consult your carrier board documentation for compatibility details).

1. Clear the global interrupt enable bit in the carrier board status register by writing a "0" to bit 3.
2. Write the interrupt vector to the IP235 Module at base address + 21H.
3. Write to the carrier board interrupt Level Register to program the desired interrupt level per bits 2,1, & 0.
4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the desired IP interrupt request being configured.
5. Write "1" to the carrier board IP Interrupt Enable Register bit corresponding to the IP interrupt request to be enabled.
6. Enable interrupts for the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the carrier board's Status Register.
7. Execute Write of 0400H to the IP235 Control Register at Base Address + 00H. This enables the IP235 to interrupt after one cycle through waveform memory.
8. Interrupts can now be generated after conversions are started via a software or external trigger.

General Sequence of Events for Processing an Interrupt

1. The IP235 asserts the Interrupt Request 0 Line (INTREQ0*) in response to an interrupt condition.
2. The AVME9630/60 carrier board acts as an interrupter in making the VMEbus interrupt request (IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/60, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*).
5. The IP235 puts the interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.

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6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
   a) Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.
   b) Service the interrupt.
   c) Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/60 IP Interrupt Clear register.
   d) Enable the interrupting IP by writing "1" to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.

USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in memory. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs.

Software calibration uses some fairly complex equations. **Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.** The functions are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO235.TXT" or "INFO230.TXT" file in the "IP235" or "IP230" subdirectory on the diskette for details.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). See the specification chapter for details regarding maximum uncalibrated error.

Calibrated Performance

Accurate calibration of the IP235 and IP230 can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in memory as (1/4 LSB's) for each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage. See the specification chapter for details regarding maximum calibrated error.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (Ideal_count) written to the 16-bit DAC to achieve a specified voltage within the selected output range.

Equation (1):

$$\text{Ideal_ Count} = \left[\frac{\text{Count_ Span} * \text{Desired_ Voltage}}{\text{Ideal_ Volt_ Span}} \right]$$

where,
Count_Span = 65,536 (a 16-bit converter has 2^{16} possible levels)
Ideal_Volt_Span = 20 Volts (for the bipolar -10 to +10 Volt range)
= 10 Volts (for the bipolar ±5 or unipolar 0 to 10 volt ranges).

Using equation (1), one can determine the ideal count for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts for the bipolar ±10 volt range, the Ideal_Count of 16,384 results. If this value is used to program the DAC output, the output value will approach +5 Volts to within the uncalibrated error. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal_Count into the Corrected_Count required to accurately produce the output voltage. This is illustrated in the next equation.

Equation (2):

$$\text{Corrected_ Count} = \text{Ideal_ Count} * \left[1 + \text{Gain_ Correction} \right] + \text{Offset_ Correction} + \text{Ideal_ Zero_ Count}$$

where,
Gain_Correction = Stored_Gain_Error / (4*65,536)
Offset_Correction = Stored_Offset_Error / 4
Ideal_Zero_Count = 0 for bipolar ±5 and ±10 volt ranges
-32,768 for unipolar 0 to 10 volt range

Ideal_Count is determined from equation (1) given above. Stored_Gain_Error and Stored_Offset_Error are written at the factory and are obtained from memory on the IP235 or IP230 on a per channel basis. The Stored_Gain_Error and Stored_Offset_Error are stored in memory as two's complement numbers. Refer to the "Calibration Coefficient Access Register" section for details on how to read the coefficients from memory.

Using equation (2), you can determine the corrected count from the ideal count. For the previous example, equation (1) returned a result 16,384 for the Ideal_Count to produce an output of +5 Volts. Assuming that a gain error of -185 and an offset error of -43 are read from memory on the IP235 or IP230 for the desired channel, substitution into equation (2) yields:

$$\text{Corrected_ Count} = 16{,}384 * \left[1 + \frac{-185}{4*65536} \right] - \frac{43}{4} = 16{,}361.6875$$

If this value (rounded to 16,362) is used to program the DAC output, the output value will approach +5 Volts to within the calibrated error (see the specification chapter for details regarding maximum calibrated error).

Calibration Programming Example

Assume it is necessary to program channel 0 with an output of -2.5 Volts. Also assume the bipolar range centered around 0 Volts is -10 to +10 Volts.

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The Single Conversion from DAC Register mode of operation, which is available on both the IP235 and IP230 modules, is used in this example.

1. Execute Write of 0100H to Control Register at Base Address + 00H.
   a) External, Software, and Internal Hardware timer generated triggers are all enabled.
   b) Single Conversion from DAC registers is enabled.

2. Read the calibration memory to retrieve channel 0's unique offset coefficient. To obtain the 16-bit offset coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8000H at Base Address + 0AH. The offset coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contain the most significant byte of the offset coefficient.

To initiate a read of channel 0's least significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8100H at Base Address + 0AH. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the offset coefficient.

3. Read the calibration memory to retrieve channel 0's unique 16-bit gain coefficient. To obtain the 16-bit gain coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8200H at Base Address + 0AH. The gain coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contains the most significant byte of the gain coefficient.

To initiate a read of channel 0's least significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8300H at Base Address + 0AH. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the gain coefficient.

4. Calculate the Ideal_Count required to provide an uncorrected output of the desired value (-2.5 Volts) by using equation (1). **Ideal_Count =** [65,536×(-2.5)]/20 = -8,192.0

5. Calculate the Corrected_Count required to provide an accurate output of the desired value (-2.5 Volts) by using equation (2). Assume the offset and gain coefficients are -43 and -185 respectively.

Corrected_Count = -8,192.0×[1 + -185/(4×65,536)] - 43/4 = -8,196.9687. This value is rounded to -8,197 and is equivalent to DFFB hex as a 2's complement value.

6. Execute Write of DFFB hex to the DAC Channel 0 Register at Base Address + 10H.

7. Execute Write 0001H to the Start Convert Bit at Base Address + 0EH. This starts the simultaneous transfer of the digital data in each DAC Channel register to its corresponding converter for analog conversions. This will drive channel 0's analog output to -2.5 volts.

8. (OPTIONAL) Observe or monitor that the specific DAC channel (0) reflects the results of the digital data converted to an analog output voltage at the field connector.

Error checking should be performed on the calculated count values to insure that calculated values below 0 or above 65535 decimal are restricted to those end points. Note that the software calibration cannot generate outputs near the endpoints of the range which are clipped off due to hardware limitations(i.e. the DAC).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the IP235 and IP230. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-621 as you review this material.

FIELD ANALOG OUTPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-620 for example wiring and grounding connections.

Jumpers on the board control the range selection for the DACs (-5 to +5, -10 to +10, and 0 to 10 Volts) as detailed in chapter 2. Jumper selection should be made prior to powering the unit. Channels may use different ranges.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.4). The P1 interface also provides +5V and ±12V power to the module. Note that the DMA control, INTREQ1∗, ERROR∗, and STROBE∗ signals are not used.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The interface to the carrier board allows complete control of all IP235 and IP230 functions.

IP INTERFACE LOGIC

IP interface logic of the IP235 or IP230 is imbedded within the FPGA. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID storage implementation.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobes BS0∗ and BS1∗ are decoded to identify low byte, high byte, or double byte data transfers.

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The carrier to IP module interface implements access to both ID and I/O space via 16 or 8-bit data transfers. Read only access to ID space provides the identification for the individual module (as given in Table 3.1) per the IP specification. Read and write accesses to the I/O space provide a means to control the IP235 or IP230.

Access to both ID and I/O spaces are implemented with one wait state read or write data transfers. There is one exception; however, read or write access to waveform memory via the Waveform Memory Data register requires four wait states.

CONTROL LOGIC

All logic to control data conversions is imbedded in the IP module's FPGA. The control logic of the IP235 and IP230 is responsible for controlling the operation of a user specified mode of data conversions. Once the IP module has been configured, the control logic performs the following:

- Controls serial transfer of data from the FPGA to the individual DAC registers based on the selected mode of operation.
- Provides external or internal trigger control.
- Controls read and write access to calibration memory.
- Controls issue of interrupt requests to the carrier (IP235 only).

DATA TRANSFER FROM FPGA To INDIVIDUAL DACs

A 16-bit serial shift register is implemented in the IP module's FPGA for each of the supported channels. These serial shift registers are referred to as the individual DAC registers in the memory map. To control transfer of digital data to the individual converters, internal FPGA counters are used to synchronize the simultaneous transfer of serial shift register data to their corresponding converter.

The DACs can be updated with new digital values or left unchanged. The DACs are updated by first writing the individual DAC registers, resident in the FPGA. Then, upon issue of a trigger (software or external), the contents of the DAC registers are simultaneously transferred to the DACs.

In addition, the FPGA of an IP235 module contains control logic that can implement transfer of digital values from waveform memory to the individual converters. There are three modes by which digital data from waveform memory can be transferred to the converters. Using the first mode, single convert from memory, each channel is updated with a single value from waveform memory. In the second mode, cycle once through memory and stop, each of the channels can be updated with a sequence of 2048 digital values. After the last of the 2048 digital values has been converted the FPGA halts further conversions and, optionally, can issue an interrupt. The last mode of update implements the continuous DAC update operation. In this mode the FPGA controls a continuous sequencing through waveform memory.

INTERVAL TIMER (IP235 only)

The DAC update interval is controlled by an interval timer. This interval timer is a 24-bit counter implemented in the FPGA. The timer is implemented via two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by the 8MHz. board clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 6.6μ seconds to 2.0889 seconds. The output of this interval counter is used to trigger the start of new conversions. Triggers generated by the interval counter are also referenced as hardware timer generated triggers in chapter 3 of this manual.

EXTERNAL TRIGGER

The external trigger connection is made via pin 49 of the P2 Field I/O Connector. For all modes of operation, when external trigger input is enabled via bits 6 and 5 of the control register, the falling edge of the external trigger will start the simultaneous conversion of all channels. For External Trigger Only mode (bits 6 and 5 set to "01"), each falling edge of the external trigger causes a conversion at the DAC. Once the external trigger signal has been driven low, it should remain low for minimum of 250n seconds and a maximum of 6μ seconds, or additional unwanted conversions may be triggered.

INTERRUPT CONTROL LOGIC

The IP235 can be configured to generate an interrupt after completion of conversion of one cycle through waveform memory. IP interrupt signal INTREQ0* is issued to the carrier to request an interrupt. An 8-bit interrupt service routine vector is provided during an interrupt acknowledge cycle on data lines D0 to D7. The interrupt release mechanism employed is ROAK (Release On AcKnowledge). The IP235 will release the INTREQ0* signal during an interrupt acknowledge cycle from the carrier.

CALIBRATION MEMORY CONTROL LOGIC

The FPGAs of the IP235 and IP230 modules contain control logic that implements read and write access to calibration memory. The calibration memory (EEPROM) contains offset and gain coefficients for each of the ranges and channels. Calibration of the individual DACs is implemented via software to avoid the mechanical drawbacks of hardware potentiometers.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Annual return of the IP235 or IP230 to Acromag for re-determination of the calibration coefficients is highly recommended. Corrected data accuracies depend heavily on the calibration coefficients being within specification. Field determination of calibration coefficients requires precision test equipment. Contact Acromag for technical assistance if field recalibration is needed.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

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PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....Standard units are 0 to +70°C.
"E" suffixed units -40°C to +85°C

Note:
The extended temperature grade version of the DAC714 is no longer available from the manufacturer. Acromag has performed operational tests of sampled commercial grade components over the extended temperature range without failure. All DAC714s' used on the -E version of the IP23x have been functionally tested by an independent third party laboratory for use in extended temperature applications, except for verification of analog output specifications.

Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-55°C to +125°C.

Physical Configuration.....Single Industrial I/O Pack Module.
Length.....3.880 inches (98.5 mm).
Width.....1.780 inches (45.2 mm).
Board Thickness.....0.062 inches (1.59 mm).
Max Component Height.....0.314 inches (7.97 mm).

Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).

Power Requirements		IP235 -8/8E	IP235 -4/4E	IP230 -8/8E	IP230 -4/4E
5V (±5%)	Typical	70mA	62mA	22mA	22mA
	Max.	100mA	82mA	30mA	30mA
+12V (±5%)	Typical	130mA	65mA	125mA	62mA
	Max.	170mA	85mA	165mA	82mA
-12V (±5%)	Typical	160mA	82mA	160mA	78mA
	Max.	210mA	115mA	210mA	110mA

Non-Isolated.....Logic and field commons have a direct electrical connection.

Resistance to RFI[1].....Designed to comply with IEC1000-4-3 Level 3 (10V/m, 27 to 500MHz.) and European Standard EN50082-1 with error less than ±0.25% of FSR.

Resistance to EMI[1].....Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.

ESD Protection.....Designed to comply with IEC1000-4-2 Level 1 (2KV direct contact discharge at input/output terminals) and European Standard EN50082-1.

EFT Protection.....Complies with IEC1000-4-4 Level 2 (0.5KV at input and output terminals) and European Standard EN50082-1.

Radiated Emissions.....Designed to comply with European Standard EN55022 for class B equipment with a shielded enclosure port.

Note:
1. Reference Test Conditions: All output ranges, Temperature 25°C, 100K conversions/second, using Acromag's AVME9660 VMEbus IP carrier with a 1 meter shielded cable length connection to the field analog output signals unloaded.

ANALOG OUTPUTS

Output Channels (Field Access)..8 Single Ended IP235-8 & IP230-8
4 Single Ended IP235-4 & IP230-4
Output Signal Type.....Voltage (Non-isolated).
Output Ranges[2] .....Bipolar -5 to +5 Volts
(Jumper selected): Bipolar -10 to +10 Volts
Unipolar 0 to +10 Volts

Note:
2. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.

Output Current.....-5mA to +5mA (Maximum); this corresponds to a minimum load resistance of 2KΩ with a 10V output.

DAC Data Format.....Positive-true binary two's complement (BTC) input codes.

DAC Programming.....Simultaneous; Input registers of multiple DAC's are directly loaded or loaded from waveform memory (IP235) with new data before simultaneously updating DAC outputs.

Resolution.....16-bits.

Monotonicity over Temperature...16-bits (IP235 or IP230)
15-bits (IP235E or IP230E)

Linearity Error.....± 2 LSB (Maximum).

Differential Linearity Error.....± 1 LSB (Maximum).

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Maximum Overall Calibrated Error[3,4]

Max. Linearity Error LSB	Max. Offset Error LSB	Max. Gain Error LSB	Max. Total Error LSB (%)
± 2	± 1	± 1	± 4 (0.0061)

Note:

3. Offset and gain calibration coefficients stored in the coefficient memory must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error and are with outputs unloaded. Follow the output connection recommendations of Chapter 2, to keep a non-ideal grounds from degrading overall system accuracy.
4. The maximum uncalibrated error combining the linearity, offset and gain errors is ± 0.453%.

DAC714HL @ 25°C:

Linearity Error is ± 0.003% maximum (i.e. ± 2 LSB).
Bipolar Offset Error is ± 0.2% FSR (i.e. 20V SPAN) max.
Gain Error is ± 0.25% maximum.

Settling Time.....10uS to within 0.003% of FSR for a 20V step change (load of 5KΩ in parallel with 500pF).
Conversion Rate (per channel)....150KHz Maximum, 100KHz recommended for specified accuracy.
Maximum Throughput……8 X conversion rate (IP23X-8/8E)
8 X 150KHz=1.2MHz. maximum
8 X 100KHz=0.8MHz spec accur.
4 X conversion rate (IP23X-4/4E)
4 X 150KHz=0.6MHz. maximum
4 X 100KHz=0.4MHz spec accur.
Output Noise……120 nV/√Hz typical
Output at Reset.....Bipolar Zero Volts.
Unipolar 5 Volts (See Note 5)
Board Warm-up Time.....8 minutes minimum

Note:

5. The reset function resets the DAC analog output and the FPGA's internal DAC registers. Therefore, the DAC outpust will remain in their reset state after simultaneous DAC output updates until the DAC registers are overwritten with new data.

Output Impedence.....0.1Ω Typical at 25°C
Short Circuit Protection .....Indefinite at 25°C.
Waveform Memory…….....2048 samples per channel
Interrupt…….....Vectored interrupt on end of single cycle through waveform memory.

External Trigger Input/Output

As An Input:.....Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered within 6.4μ seconds of the falling edge. Minimum pulse width 250n sec. Maximum pulse width 6μ seconds, otherwise, an additional trigger is produced.

As An Output:.....Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for 125n seconds, typical. A maximum of 4 loads are allowed.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995, for Type 1 Modules.
Electrical/Mechanical Interface....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).....D16 or D08 read/write of data.
ID Read (IDSel*).....32 x 8 ID space read on D0..D7. as D16 or D08.
Interrupt Select (INTSel*).....8-bits (D08) Interrupt Vector Register contents.
Access Times (8MHz Clock):
ID Space Read.....1 wait state (375ns cycle).
I/O Space Read.....1 wait state (375ns cycle).
Waveform Memory……4 wait states typical (750ns cycle)
I/O Space Write.....1 wait state (375ns cycle).
0 wait states (250ns cycle) IP230-8 only.
Interrupt Select Read.....1 wait state (375ns cycle).

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APPENDIX

CABLE: MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded cable according to model number. The shielded cable is highly recommended for optimum performance with IP235 and IP230 analog output modules.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 or APC8610 non-intelligent carrier board connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

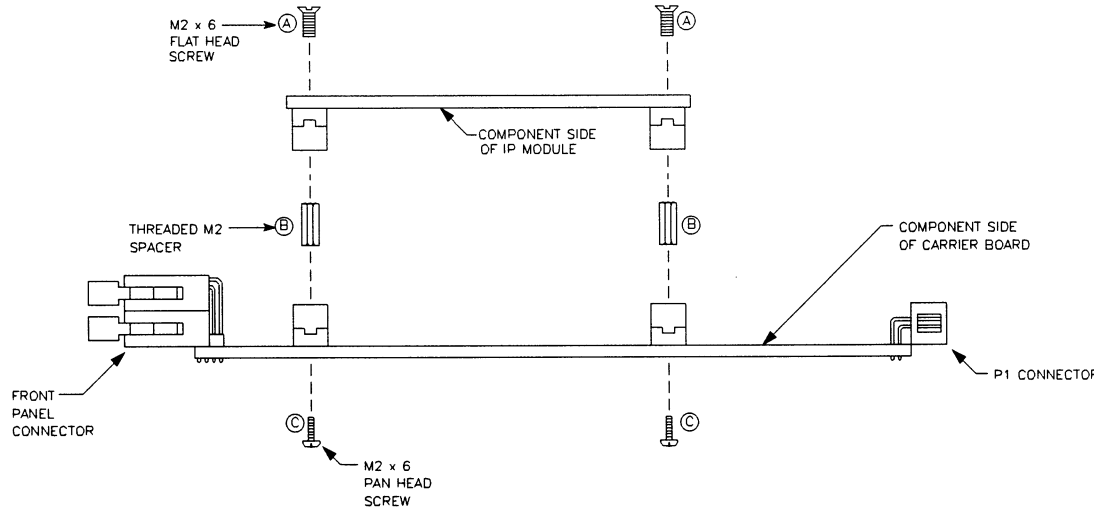
TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 or APC8610 Boards Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U or APC8610 non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660 or APC8610: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.

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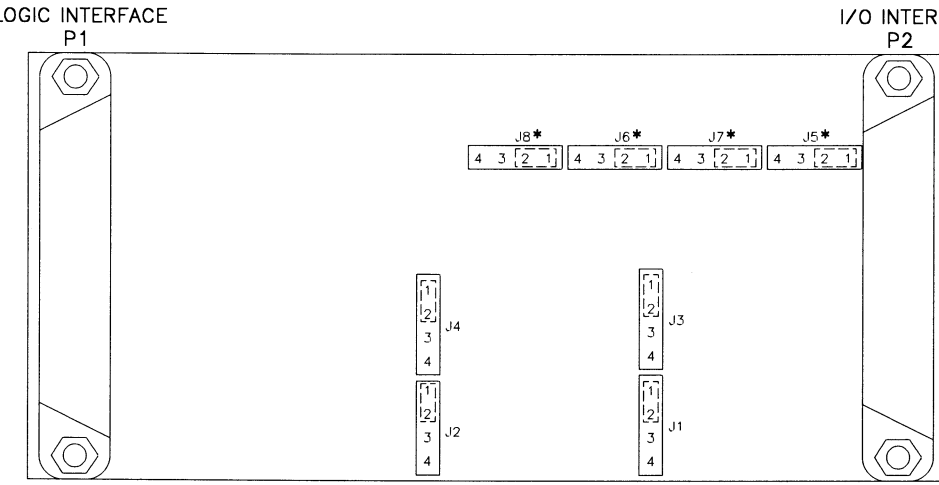
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

Acromag WIXOM, MICH.	DATE	REV	ECN	DR	ENG	CLP
	29-JUL-94	B	940811	TAV	JQV	BC
	21-DEC-93	A	——	TAV	JQV	BC
TITLE: IP MECHANICAL ASSEMBLY						
D SERIES: IP	1 OF 1	DWG NO. 4501-434				B REV

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COMPONENT SIDE VIEW

NOTE: Dashed lines inside jumper blocks represent installed jumpers.

ANALOG OUTPUT RANGE SELECTION (Jumper Settings)

DESIRED ADC OUTPUT RANGE (VDC)	OUTPUT SPAN (VOLTS)	OUTPUT TYPE	J1 to J8 PINS (1&2)	J1 to J8 PINS (3&4)
−5 TO +5	10	Bipolar	ON	ON
−10 TO +10**	20	Bipolar	ON	OFF
0 TO +10	10	Unipolar	OFF	ON

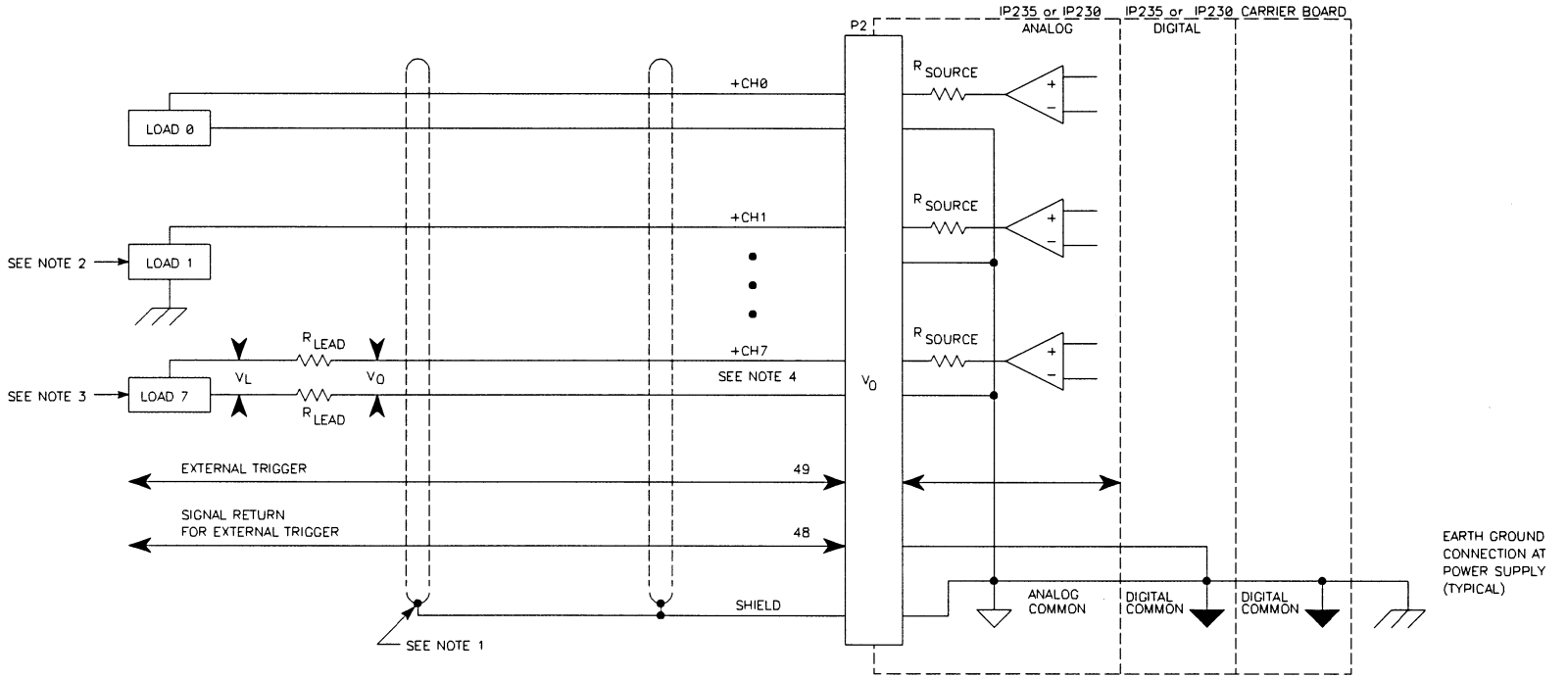
* Jumper blocks not present on the IP235−4 and IP230−4 models.

** THE BOARD IS SHIPPED WITH THE DEFAULT JUMPER SETTING FOR THE −10 TO +10 VOLT DAC OUTPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

IP235 & IP230 JUMPER LOCATIONS

Acromag® WIXOM, MICH. | 3-SEPT-98 DATE | A REV | ECN | RS DR | LMP ENG | GL CLP
TITLE: IP235 & IP230 JUMPER LOCATION
D | SERIES: IP235 & 230 | 1 OF 1 | DWG NO. 4501-619 | A REV

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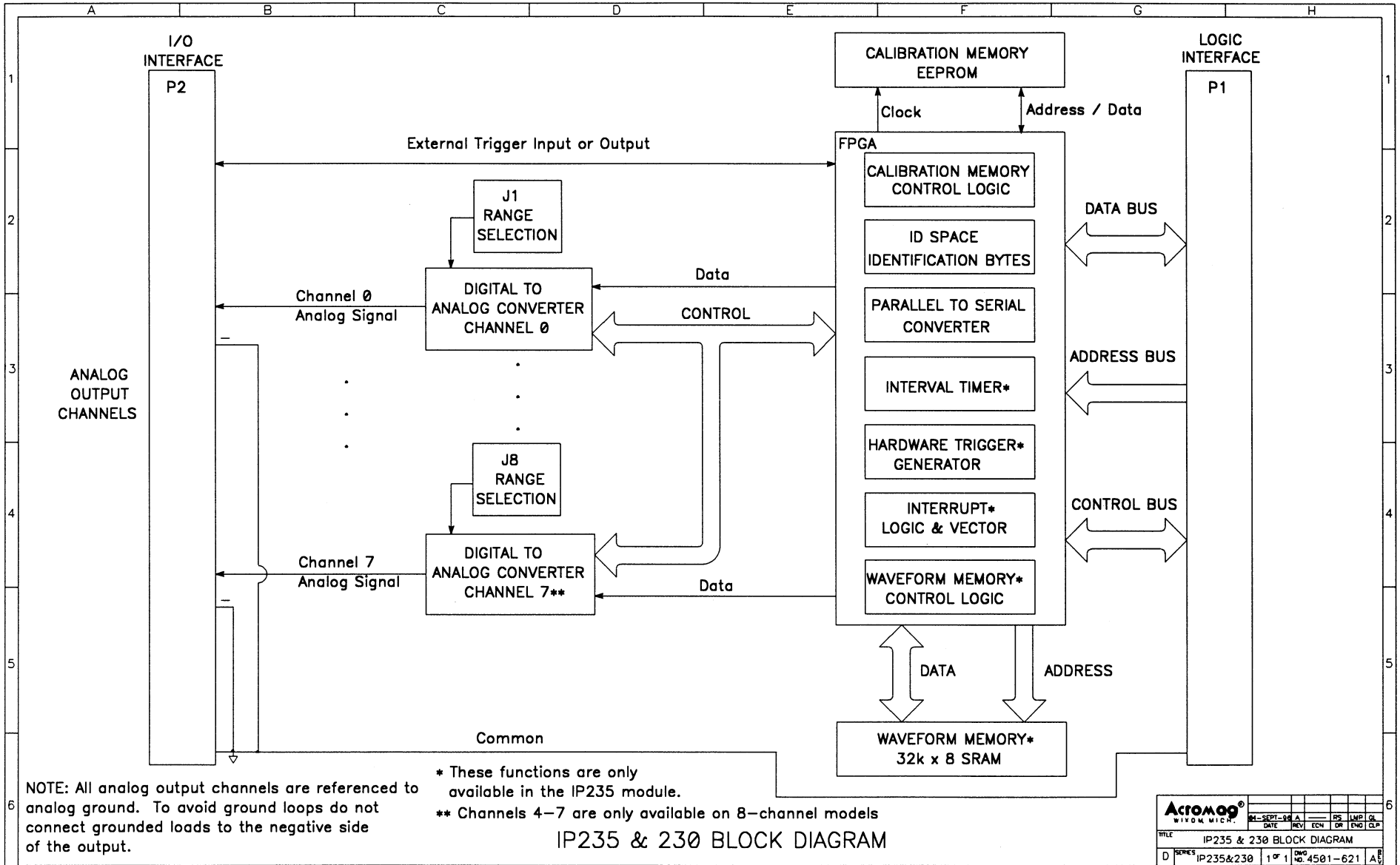
NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONLY ONE END TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. ALL 8 CHANNELS ARE REFERENCED TO ANALOG COMMON AT THE IP235 OR IP230. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED CHANNELS TO THE NEGATIVE SIDE OF THE OUTPUT.
3. VL < VO DUE TO VOLTAGE DROPS ACROSS THE LEAD RESISTANCE OF THE WIRE. IT IS RECOMMENDED THAT A HIGH RESISTANCE LOAD WITH A SHORT WIRE RUN BE CONNECTED AT THE OUTPUT TO REDUCE THE EFFECTS OF LEAD AND SOURCE RESISTANCE VOLTAGE DROPS IN THE WIRE.
4. CHANNELS 4–7 ARE ONLY AVAILABLE ON 8–CHANNEL MODELS.

IP235 & IP230 ANALOG OUTPUT CONNECTION DIAGRAM

Acromag WIXOM, MICH.								
	3-SEPT-96	A	——	RS	LWP	GL		
	DATE	REV	ECN	DR	ENG	CLD		
TITLE: ANALOG OUTPUT CONNECTION DIAGRAM								
D	SERIES: IP235 & IP230	1 OF 1	DWG NO. 4501-620	A				

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NOTE: All analog output channels are referenced to analog ground. To avoid ground loops do not connect grounded loads to the negative side of the output.

* These functions are only available in the IP235 module.

** Channels 4–7 are only available on 8–channel models

IP235 & 230 BLOCK DIAGRAM

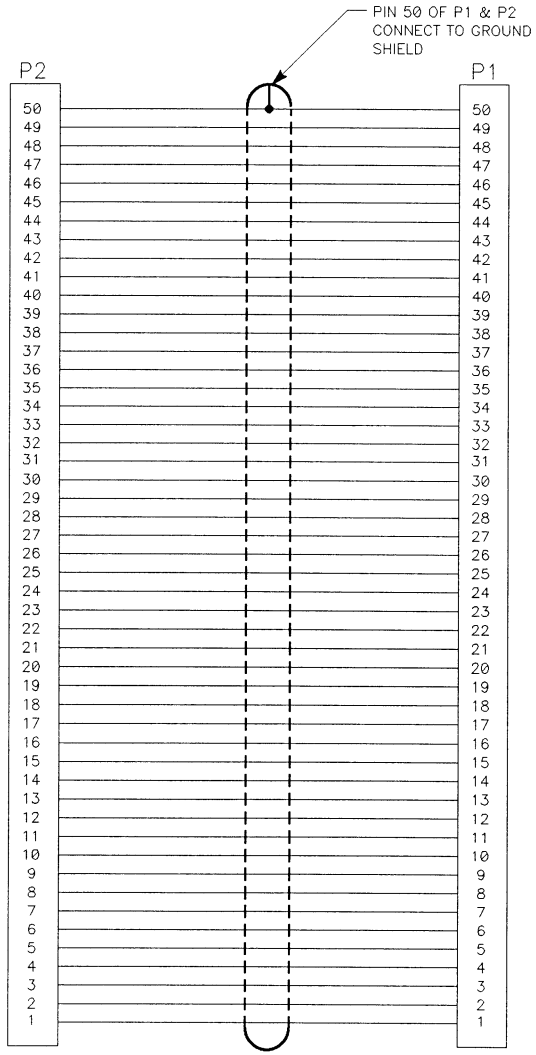
Acromag® WIXOM, MICH.

6H-SEPT-98 DATE	A REV	— ECN	RS DR	LMP ENG	GL CLP

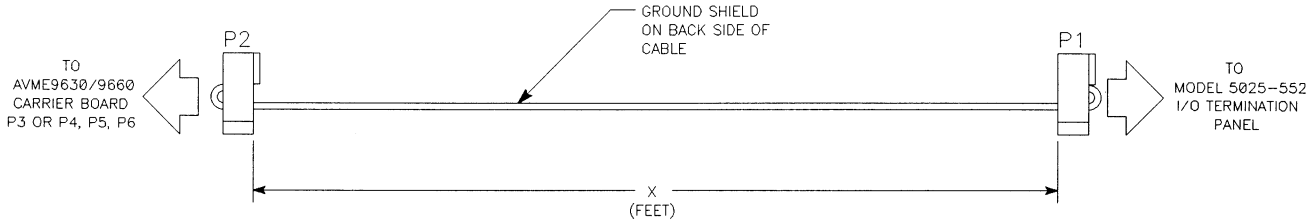
TITLE: IP235 & 230 BLOCK DIAGRAM

D | SERIES IP235&230 | 1 OF 1 | DWG NO. 4501-621 | A REV

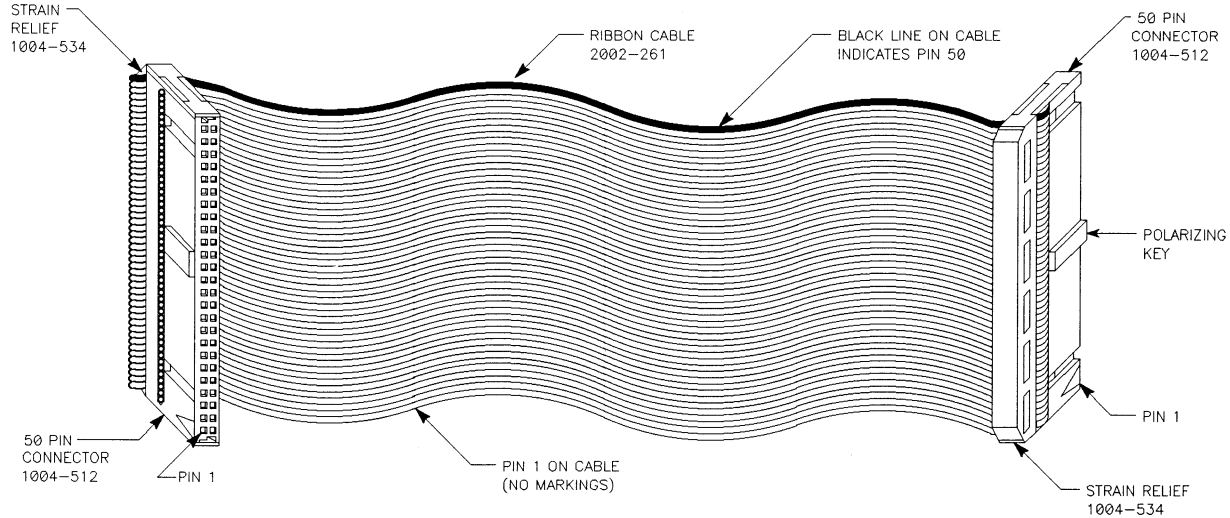
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MODEL 5025-551-x SCHEMATIC



TOP VIEW



FRONT VIEW

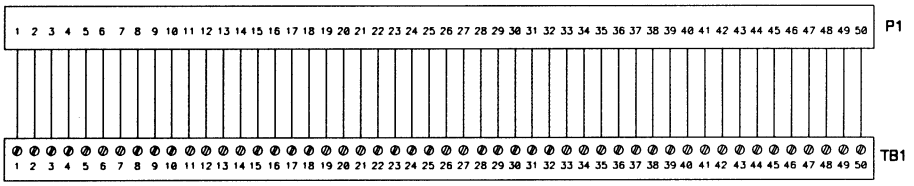
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-551-x SIGNAL CABLE, SHIELDED

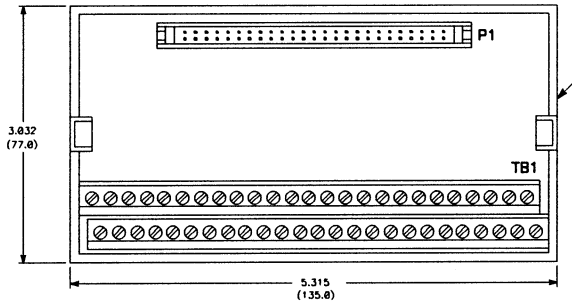
Acromag® WIXOM, MICH					TAV	CAP	BC
	09 FEB 94	A	——		DR	ENG	CLP
	DATE	REV	ECN				
TITLE: CABLE 5025-551-x, SHIELDED							
D	SERIES		1 OF 1	DWG NO. 4501-463		A	REV

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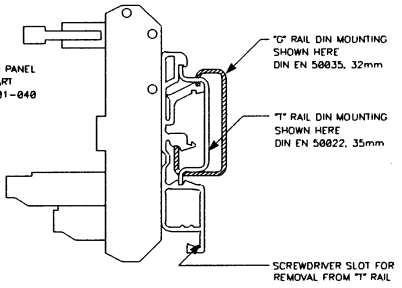
MODEL 5025–552 SIMPLIFIED SCHEMATIC



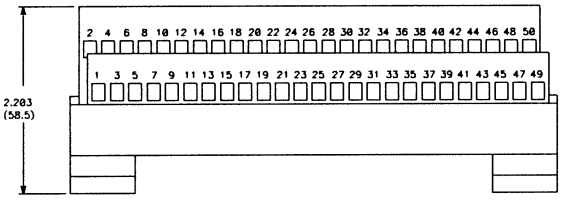
TOP VIEW



SIDE VIEW



FRONT VIEW

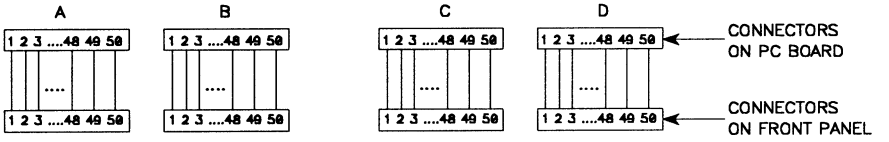


MODEL 5025–552 TERMINATION PANEL MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

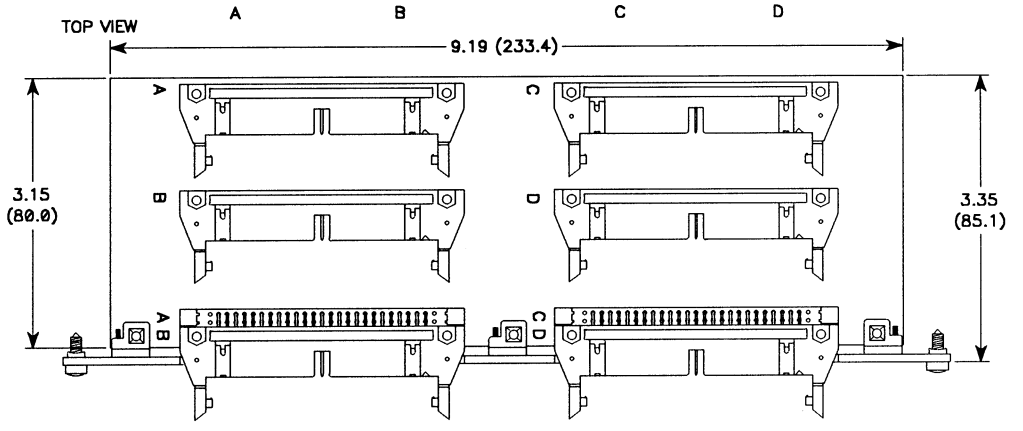
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: +/–0.020 (+/–0.5).

MODEL 5025–552 TERMINATION PANEL
D 1 OF 1 4501–464 A

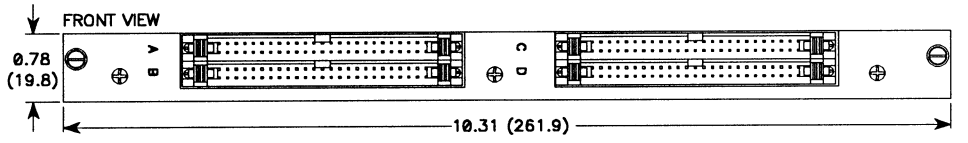
MODEL TRANS–GP MODULE SCHEMATIC



TOP VIEW



FRONT VIEW



TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

MODEL TRANS–GP TRANSITION MODULE
D AVME 1 OF 1 4501–465 A

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