



**Series IP400 Industrial I/O Pack
40-Channel Digital Input Board**

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP400 module is a 40-channel digital input board. This model accepts forty 0 to 60V DC inputs, providing up to 160 inputs per 6U-VMEbus system slot. When mated with the Acromag IP405 Digital Output Module, this model can be used for direct "loopback" monitoring of the output states. The IP400 can be programmed to generate Change-Of-State (COS), Low, or High level transition interrupts. The input threshold is TTL compatible with hysteresis included. The IP400 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitoring applications that require high-density, high-reliability, and high-performance at a low cost.

Model	Operating Temperature Range
IP400	0 to 70°C
IP400E	-40 to 85°C

KEY IP400 FEATURES

- **High Channel Count** - Interfaces with up to 40 inputs. Four units mounted on a carrier board provide up to 160 input channels in a single system slot.
- **TTL Input Threshold** - Input threshold is at TTL levels and includes hysteresis.
- **Input Hysteresis** - Buffered inputs include hysteresis for increased noise immunity.
- **Programmable Change-of-State/Level Interrupts** - Interrupts are software programmable for any bit change of state or level match on up to 12 channels (channels 0-11 only).
- **Loopback Compatible with IP405** - The P2 pin assignments of the IP400 input module correspond with those of the IP405 output module. This provides direct interface "loopback" capability between these models.
- **High Voltage Inputs** - Inputs are rated to 60VDC. Input channels are non-isolated and share a common connection.
- **High Impedance Inputs** - High impedance inputs minimize loading of the input source and minimize input current.
- **No Configuration Jumpers or Switches** - All configuration is performed through software command with no internal jumpers to configure or switches to set.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density** - Single-size, industry standard, IP module footprint. Up to four units may be mounted on a 6U VMEbus carrier board.
- **Local ID** - Each IP module has its own 32-byte ID PROM which is accessed via data transfers in the "ID Read" space.

- **Supports 16-bit & 8-bit I/O** - Channel register Read/Write is performed through 16-bit (D16) or 8-bit (D08[EO]) data transfer cycles in the IP module I/O space.
- **High Speed** - Acquisition times for all data transfer cycles are described in terms of "wait" states - 1 wait state is required for reading the inputs, 1 wait state for write operations (see specifications for detailed information).

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent carrier boards). Consult the documentation of your carrier board to ensure compatibility with the following interface products (since all connections to field signals are made through the carrier board which passes them to the individual IP modules).

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The "X" of Model denotes the length in feet. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module, with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO400.TXT" file in the "IP400" subdirectory on the diskette for more details.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be

present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.



The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP400 Input Boards have no jumpers or switches to configure--interrupts are configured through software command.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the front-panel, field I/O interface connector on the carrier board (you should verify this for your carrier board). The IP400 P2 connector shares the same signal pinouts with Acromag Model IP405 40-Channel Output Boards, making it directly compatible for “loopback” monitoring of the IP405 output states.

Table 2.1: IP400 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
IN00	1	IN25	32
IN01	2	IN26	33
IN02	3	IN27	34
IN03	4	IN28	36
IN04	6	IN29	37
IN05	7	IN30	38
IN06	8	IN31	39
IN07	9	IN32	41
IN08	11	IN33	42
IN09	12	IN34	43
IN10	13	IN35	44
IN11	14	IN36	46
IN12	16	IN37	47
IN13	17	IN38	48
IN14	18	IN39	49
IN15	19	COMMON	5
IN16	21	COMMON	10
IN17	22	COMMON	15
IN18	23	COMMON	20
IN19	24	COMMON	25
IN20	26	COMMON	30
IN21	27	COMMON	35
IN22	28	COMMON	40
IN23	29	COMMON	45
IN24	31	COMMON	50

Input Noise and Grounding Considerations

This model is non-isolated between the logic and field input grounds since input common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. Refer to Drawing 4501-518 for example input and grounding connections.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). Note that the IP400 does not utilize all of the logic signals defined for the P1 connector and these are indicated in **BOLD ITALICS**.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	<i>DMAReq0*</i>	30
D02	6	MEMSEL*	31
D03	7	<i>DMAReq1*</i>	32
D04	8	IntSel*	33
D05	9	<i>DMAAck0*</i>	34
D06	10	IOSEL*	35
D07	11	RESERVED	36
D08	12	A1	37
D09	13	<i>DMAEnd*</i>	38
D10	14	A2	39
D11	15	ERROR*	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	<i>INTReq1*</i>	44
BS0*	20	A5	45
BS1*	21	STROBE*	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	RESERVED	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal. **BOLD ITALIC** Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the acquisition of digital inputs from the field. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP400 only uses a portion of this space. The I/O space address map for the IP400 is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Accesses can be performed on an 8-bit (D08[EO]), or 16-bit word (D16) basis.

Table 3.1: IP400 I/O Space Address (Hex) Memory Map⁴

EVEN Base Addr.+	EVEN Byte D15 D08		ODD Byte D07 D00		ODD Base Addr.+
00	READ- Digital Input Channel Register A CH15 ↔ CH08		READ- Digital Input Channel Register A CH07 ↔ CH00		01
02	READ- Digital Input Channel Register B CH31 ↔ CH24		READ- Digital Input Channel Register B CH23 ↔ CH16		03
04	(FF) Not Driven ¹		READ- Digital Input Channel Register C CH39 ↔ CH32		05
06	(OFFF) NOT USED ³				07
08	Driven LOW ² 15.....12	R/W - Interrupt Enable Register ² CH11 ↔ CH00			09
0A	Driven LOW ² 15.....12	R/W -Interrupt Type Config. Register ² CH11 ↔ CH00			0B
0C	Driven ² LOW 15.....12	R/W - Interrupt Polarity Register ² CH11 ↔ CH00			0D
0E	Driven ² LOW 15.....12	R/W - Interrupt Status Register ² CH11 ↔ CH00			0F
10	Driven ² LOW 15.....12	(F) Driven HIGH	R/W - Interrupt Vector Register ¹		11
12 ↓ 7E	(OFFF) NOT USED ³				13 ↓ 7F

Notes (Table 3.1):

1. These bits of this register are not driven. Pull-ups on the carrier board data bus will cause these bits to always read High (1's).
2. The upper 4 bits of these 16-bit registers are driven low (0's).
3. These registers have no function. The upper 4 bits of these 16-bit registers are driven low (0's) and pullups on the data bus will cause the lower 12-bits to read high (1's). Embedded "Not Used" addresses occur due to the IP400's use of the same register architecture as Acromag Model IP408.
4. All Read and Write operations require 1 wait state.

IP Digital Input Registers A, B, & C (Read Only)

When the Digital Input Channel Data Registers are read, the value read corresponds to the actual state of the input channels at the time of the read. A "0" bit means that the corresponding input signal is below TTL threshold, a "1" bit means that the corresponding input signal is at or above the TTL threshold (approximately 1.6V, typical).

40 Input channels numbered 0 through 39 may be read. Channel Read operations use 8-bit (D08[E0]), or 16-bit (D16) words with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A monitors input channels 0 through 15. Register B monitors input channels 16 through 31. Register C monitors input channels 32 through 39. Pullups on the carrier board data bus will cause the upper 8 bits of Register C to read back as high (1's).

REGISTER A (INPUT CHANNELS 0 THROUGH 15):																
<u>MSB</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	<u>LSB</u>
CH15.....	CH8						CH7.....	CH0								

REGISTER B (INPUT CHANNELS 16 THROUGH 31):																
<u>MSB</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	<u>LSB</u>
CH31.....	CH24						CH23.....	CH16								

REGISTER C (INPUT CHANNELS 32 THROUGH 39):																
<u>MSB</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	<u>LSB</u>
1	1	1	1	1	1	1	1	1	CH39.....	CH32						

It is recommended that unused input points not be left floating, but pulled high or low. The unused upper 8 bits of Register C are "Don't Care" and will always read high (1's) for D16 accesses.

Interrupt Enable Register (R/W)

The digital input channel Interrupt Enable Register provides a mask bit for each of the 12 possible interrupt channels (channels 0-11 only). A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding input channel to generate an interrupt.

INTERRUPT ENABLE REGISTER:																
<u>MSB</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	<u>LSB</u>
0	0	0	0	0	CH11.....	CH0										

All input channel interrupts are masked ("0") following a reset. The unused upper 4 bits of this 16-bit register are always driven low (0's) for D08(E) or D16 accesses.

Interrupt Type Configuration (COS or H/L) Register (R/W)

The Interrupt Type Configuration Register determines the type of input channel transition that will generate an interrupt for each of the 12 possible interrupt channels (channels 0-11 only). A "0" bit means that an interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-of-State (COS) occurs at the corresponding input channel (i.e. any state transition). Note that interrupts will not occur unless they are enabled (see the Interrupt Enable Register).

INTERRUPT TYPE (COS or H/L) CONFIGURATION REGISTER:																
<u>MSB</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	<u>LSB</u>
0	0	0	0	0	CH11.....	CH0										

All bits are set to "0" following a reset which means that the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register. The unused upper 4 bits of this 16-bit register are always driven low (0's) for D08(E) or D16 accesses.

Interrupt Polarity Register (R/W)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the 12 possible interrupt channels (channels 0-11 only). A "0" bit specifies that an interrupt will occur when the corresponding input channel is *BELOW* TTL threshold (i.e. a "0" in the digital input channel data register). A "1" bit means that an interrupt will occur when the input channel is *ABOVE* TTL threshold (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

INTERRUPT POLARITY (HIGH/LOW) REGISTER:															
MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CH11	CH0

All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold. The unused upper 4 bits of this 16-bit register are always driven low (0's) for D08(E) or D16 accesses.

Interrupt Status Register (R/W)

The Interrupt Status Register reflects the status of the 12 possible interrupt channels (channels 0-11 only). A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). This is known as the "Release On Register Access" (RORA) method, as defined in the VME system architecture specification. However, if the condition which caused the interrupt to occur remains (in the case of a level interrupt), the interrupt will be generated again (unless disabled via the Interrupt Enable Register).

Note that interrupts are prioritized via hardware within the card. Channel 11 has the highest priority, channel 0 the lowest priority. If multiple input channel interrupts become pending at the same time, the vector corresponding to the highest numbered channel will be delivered first. After the highest numbered channel's interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority channel with an interrupt pending. Note that the input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel, this could happen if multiple changes occur before the channel's interrupt is serviced.

INTERRUPT STATUS REGISTER:															
MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CH11	CH0

All interrupts are cleared following a reset. The unused upper 4 bits of this 16-bit register are always driven low (0's) for D08(E) or D16 accesses.

Interrupt Vector Register (R/W)

The Interrupt Vector Register maintains an 8-bit interrupt pointer for each of the 12 digital input channel interrupt lines (channels 0-11 only). The lower 4 bits of the Interrupt Vector Register (odd-byte address) contain the channel number that originated the interrupt. The upper 4 bits of the odd-addressed byte are user-programmable and contain a pointer to the interrupt service routine. Interrupts are served on a priority basis with the higher numbered channels having higher priority (i.e. channel 11 has the highest priority, channel 0 the lowest). The appropriate interrupt vector is given to the VMEbus Interrupt Handler when an interrupt is being serviced. As such, it is a pointer to 12 possible interrupt handling routines. This allows each digital input channel to be serviced by its own software handler.

INTERRUPT VECTOR REGISTER:															
MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	X	X	X	X	User-Programmable	Channel No.

All bits of this register are set to "0" following a reset. The upper 4 bits (even byte address) of this 16-bit register are driven low (0's). The lower 4 bits of the upper byte are driven high (1's).

IP ID PROM (Read Only, 32 Odd-Byte Addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP400 ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block (see Table 3.2).

Table 3.2: IP400 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		02	IP Model Code ¹
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		A3	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP400 model is represented by 02 Hex).

The IP400 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read operation requires 1 wait state.

IP400 PROGRAMMING CONSIDERATIONS

To make programming and communicating with the board easier, Acromag provides you with the Industrial I/O Pack Software Library diskette. The functions provided are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO400.TXT" file in the "IP400" subdirectory on the diskette for details.

The following sections give some pointers for programming interrupts.

Programming Interrupts

Digital input channels can generate interrupts for the following conditions (channels 0-11 only):

- Any Change-of-State (COS) at selected channels.
- Input level (polarity) match at selected input channels.

Interrupts generated by the IP400 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism employed is the Release On Register Access (RORA) type. This means that the interrupter will release the Industrial I/O Pack interrupt request line (INTREQ0) after the interrupt has been cleared by writing a "1" to the appropriate bit position in the input channel Interrupt Status Register.

The Interrupt Vector Register contains a pointer to an interrupt handling routine. The lower 4 bits of this 8-bit number contain the channel number of the interrupting channel. The upper 4 bits of this 8-bit number contain a user-programmable pointer to complete the vector. As such, the vector may point to any one of 12 possible locations to access the interrupt handling routine. If each of these 8 locations contain the same address (the address of a single interrupt handling routine), one interrupt handling routine may be used to service all possible channel interrupts.

Interrupt service is prioritized with the higher numbered channel having a higher priority over the lower numbered channels. Thus, Channel 11 has the highest priority and channel 0 the lowest. As such, if multiple channel interrupts become pending at the same time, the pointer corresponding to the highest numbered channel will be delivered first. After the highest numbered channel interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority (pending) interrupt.

When using interrupts, input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a given input channel, this could happen if multiple changes occur before the channel's interrupt is serviced. The response time of the input channels should also be considered when figuring this bandwidth. The total response time is the sum of the input buffer response time, plus the interrupt logic circuit response time, and this time must pass before another interrupt condition will be recognized.

The following programming examples assume that the IP400 is installed onto an Acromag AVME9630/9660 carrier board (consult your carrier board documentation for compatibility details).

Programming Example for AVME9630/9660 Carrier Boards:

1. Clear the Global Interrupt Enable Bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Perform Specific IP Module Programming - see the Change-of-State or Level Match programming examples that follow, as required for your application.
3. Write to the carrier board Interrupt Level Register to program the desired interrupt level per bits 2, 1, & 0.
4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the desired IP interrupt request(s) being configured.
5. Write "1" to the carrier board IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the Carrier Board Status Register.

IP Programming Example for Change-of-State Interrupts:

1. Program the upper 4 bits of the odd-addressed byte of the Interrupt Vector Register with the user specified portion of the interrupt vector. These 4 bits combined with the lower 4 bits (the interrupting channel number) form a pointer to one of 12 possible locations in memory that contain the address of the interrupt handling routine for the interrupting channel.
2. Select Change-of-State interrupts for channels by writing a "1" to each channel's respective bit in the Interrupt Type Register for channels that are to generate interrupts.
3. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register.
4. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

Change-of-State Interrupts may now be generated by the input channels programmed above for any Change-Of-State transition.

IP Programming Example for Level (Polarity) Match Interrupts:

1. Program the upper 4 bits of the odd-addressed byte of the Interrupt Vector Register with the user specified portion of the interrupt vector. These 4 bits combined with the lower 4 bits (the interrupting channel number) form a pointer to one of 12 possible locations in memory that contain the address of the interrupt handling routine for the interrupting channel.
2. Select Polarity interrupts for channels by writing a "0" to each channel's respective bit in the Interrupt Type Register for channels that are to generate interrupts.
3. Select the desired polarity (High/Low) level for interrupts by writing a "0" (Low) or "1" (High) level to each channel's respective bit in the Interrupt Polarity Register.
4. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register.
5. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

Interrupts can now be generated by matching the input level with the selected polarity for programmed interrupt channels.

General Sequence of Events for Processing an Interrupt

1. The IP400 asserts the Interrupt Request 0 Line (IREQ0*) in response to an interrupt condition at one or more inputs.
2. The AVME9630/9660 carrier board acts as an interrupter in making the VMEbus interrupt request (asserts IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/9660, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the IntSel* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0*; A1 high corresponds to IntReq1*).
5. The IP400 puts the appropriate interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.
6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
 - A. Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
 - B. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the IP400 Interrupt Enable Register.
 - C. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the IP400 Interrupt Status Register.
 - D. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the IP400 Interrupt Enable Register.
 - E. Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Clear Register.
 - F. Enable the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
8. If the IP400 interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is complete (i.e. the carrier board negates its interrupt request, IRQ*).
 - A. If the IP400 interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, then the IP400 interrupt enable bit should be disabled or reconfigured.
 - B. If other IP modules have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Drawing 4501-519 as you review this material.

INPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field inputs are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-518 for example input and grounding connections.

A Field Programmable Gate Array (FPGA) is used to generate all the logic necessary to operate the board. It is driven by 16 individual input buffers (channels 0-15). The balance of the input buffers selectively drive the 16-bit data bus directly. Field input signals are tied to the buffer inputs via 100KΩ series connected resistors to limit input current. Additionally, the buffer inputs are clamped to +4.7V (generated from the +12V supply to minimize +5V loading). The input signal threshold is TTL compatible. The typical threshold is 1.5V DC with about 200mV of hysteresis.

Digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) or input level (polarity) match conditions for selected input channels (channels 0-11 only). Interrupt service is prioritized with the higher numbered channel having a higher priority over the lower numbered channels. An 8-bit interrupt service routine vector is provided during interrupt acknowledge cycles on data lines D0...D7. The interrupt release mechanism employed is RORA (Release On Register Access).

Since IP400 40-channel input boards use the same field I/O pin assignments (P2) as Model IP405 40-channel output boards, these units are directly compatible for loopback monitoring of the IP405 output states.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V and +12V to power the module (-12V is not used).

All I/O, address decoding, control signals, interrupt handling, and ID access logic, is done through a programmable gate array installed on the IP module. The program for the gate array is stored in separate PROM memory and loaded upon reset. The FPGA also returns the acknowledgement signal required by the carrier board per the IP specification.

The ID PROM (read only) installed on the IP module provides the identification for the individual module per the IP specification. The ID PROM, input and interrupt registers are all accessed through the 16-bit data bus interface to the carrier board (D0..D15).

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

- Operating Temperature.....0 to +70°C.
-40 to +85°C (E Version)
- Relative Humidity.....5-95% Non-Condensing.
- Storage Temperature.....-25 to +85°C.
-55 to +125°C (E Version)
- Physical Configuration.....Single Industrial I/O Pack Module.
Length.....3.880 in. (98.5 mm).
Width.....1.780 in. (45.2 mm).
Board Thickness.....0.062 in. (1.59 mm).
Max Component Height.....0.314 in. (7.97 mm).
- Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header
(AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header
(AMP 173279-3 or equivalent).
- Power:
+5 Volts (±5%).....15mA Typical; 30mA Maximum.
+12 Volts (±5%) from P1.....7.3mA Typical; 8.5mA Maximum.
-12 Volts (±5%) from P1.....0mA (Not Used).
- Non-Isolated.....Logic and field I/O common have a direct electrical connection.

DIGITAL INPUTS

- Input Channel Configuration.....40 non-inverting buffered inputs with a common connection. For DC voltage applications only, observe proper polarity. Channels 0-11 can be configured to generate interrupts.
- Input Signal Voltage Range.....0 to +60V DC, Maximum.
- Input Signal Threshold.....TTL compatible. 1.5VDC with 200mV of hysteresis, typical. Thus, Low-to-High threshold is 1.6VDC, High-to-Low is 1.4VDC, typical. Limited to TTL levels of 0.8VDC (maximum LOW level) and 2.0VDC (minimum HIGH level).
- Input Resistance.....100KΩ, Typical.
- Input Hysteresis.....200mVDC centered at a 1.5VDC threshold, Typical.
- Input Current.....560uA, Typical at 60V DC.

- Interrupt Input Response Time.....250nS minimum to 375nS maximum, depending on when the input transition occurs with respect to the 8MHz clock. Measured from input transition to INTREQ0 line assertion.
- Resistance to RFI.....No digital upsets occur for field strengths up to 10V per meter at 27MHz, 151MHz, & 460MHz per SAMA PMC 33.1 test procedures.
- Resistance to EMI.....Unit has been tested with no digital upsets under the influence of EMI from switching solenoids, commutator motors, and drill motors.
- ESD Protection.....Inputs exhibit no degradation of performance with repeated ESD induced voltages to ± 6KV per DOD-STD-1686.

INDUSTRIAL I/O PACK COMPLIANCE

- Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.
- Electrical/Mechanical Interface.....Single-Size IP Module.
- IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).....16-bit (D16) word or 8-bit (D08[EO]) read of data on D0..15.
ID Read (IDSel*).....32 x 8 ID PROM read on D0..D7.
- Access Times (8MHz Clock):
ID PROM Read.....1 wait state (375ns cycle).
Channel Registers Read.....1 wait state (375ns cycle).
Interrupt Registers Read.....1 wait state (375ns cycle).
Interrupt Registers Write.....1 wait state (375ns cycle).
- Interrupts:
Handling Format.....12 interrupt channels are supported (channels 0-11 only). An 8-bit vector is provided during interrupt acknowledge cycles on D0...D7. The release mechanism is RORA type (Release On Register Access).

APPENDIX**CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)**

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).

Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).

Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).

Keying: Headers at both ends have polarizing key to prevent improper installation.

Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.

Shipping Weight: 1.0 pound (0.5Kg), packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards

Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel*: Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

Mounting: Termination panel is snapped on the DIN mounting rail.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

Storage Temperature: -40°C to +100°C.

Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.

Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Schematic and Physical Attributes: See Drawing 4501-465.

Field Wiring: 50-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C).

Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

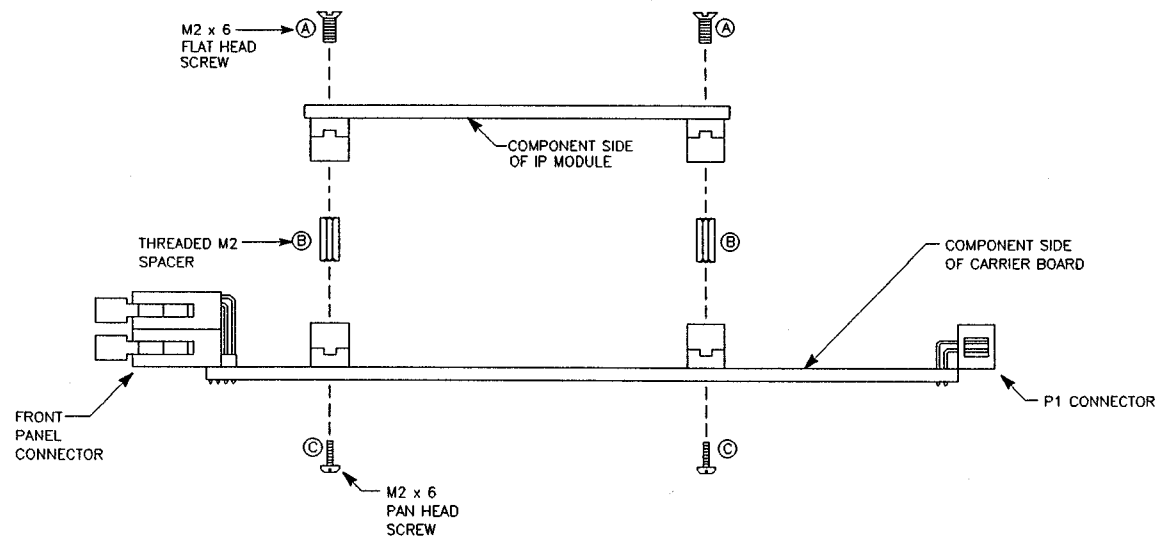
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.

Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +105°C.

Shipping Weight: 1.25 pounds (0.6Kg) packaged.

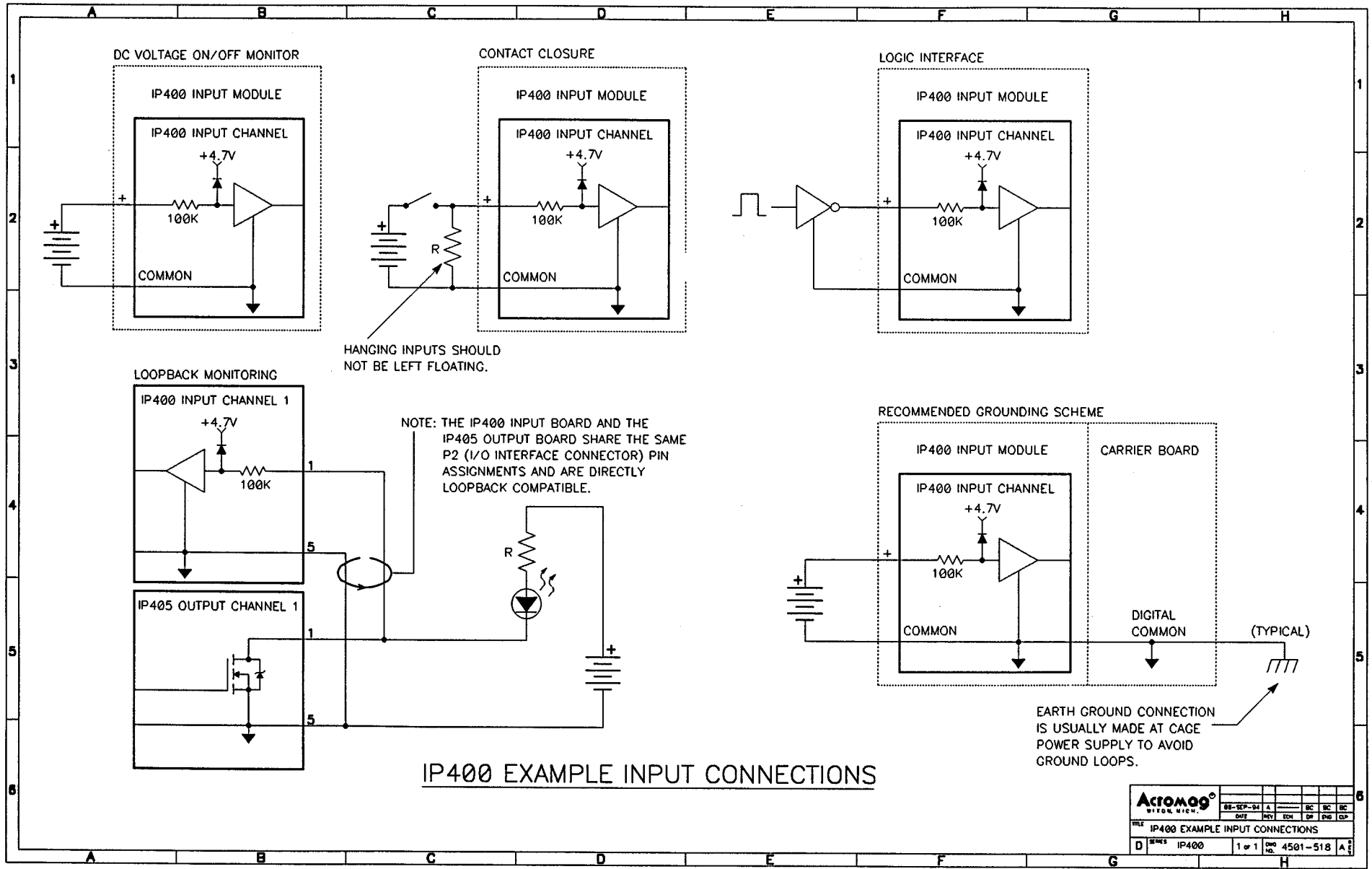


ASSEMBLY PROCEDURE:

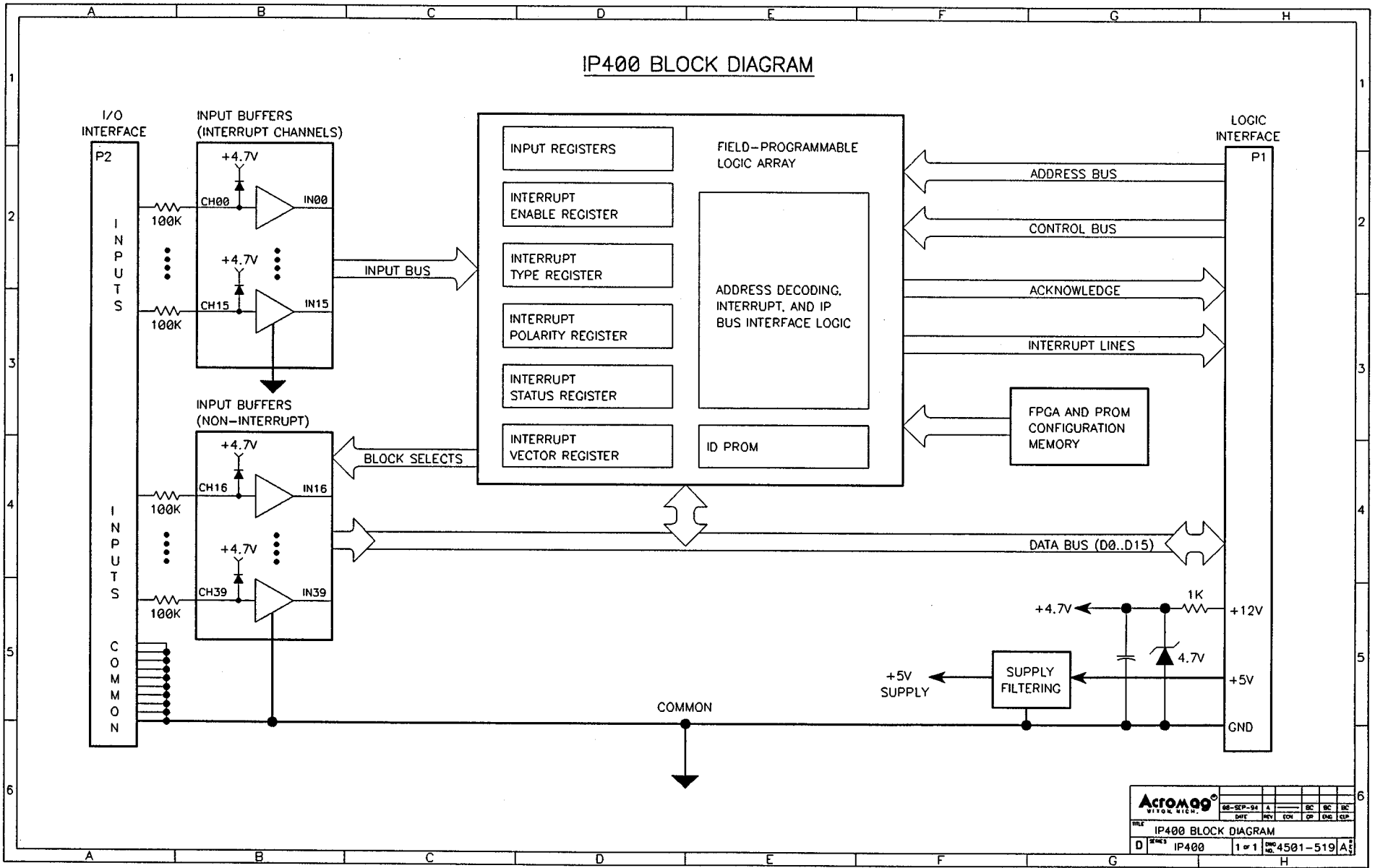
1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

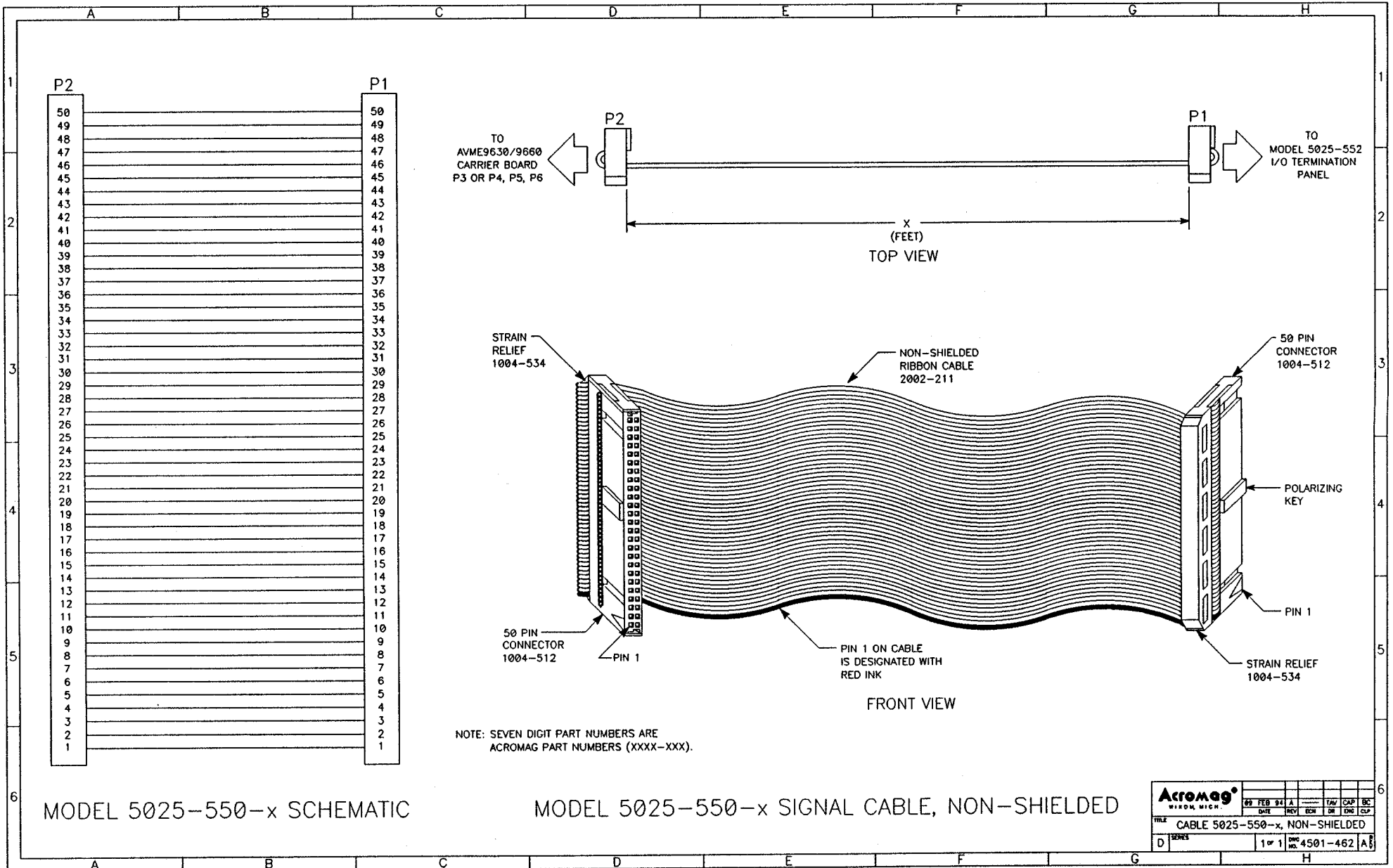
Acromag WINDMILL MICH.		20 JUL 94	B	040811	TAV	JGV	BC
		21 DEC 93	A		TAV	JGV	BC
TITLE		DATE	REV	ENH	DR	ENG	CLP
IP MECHANICAL ASSEMBLY							
D	SERIES	IP	1 of 1	DOC NO.	4501-434	B	



IP400 BLOCK DIAGRAM



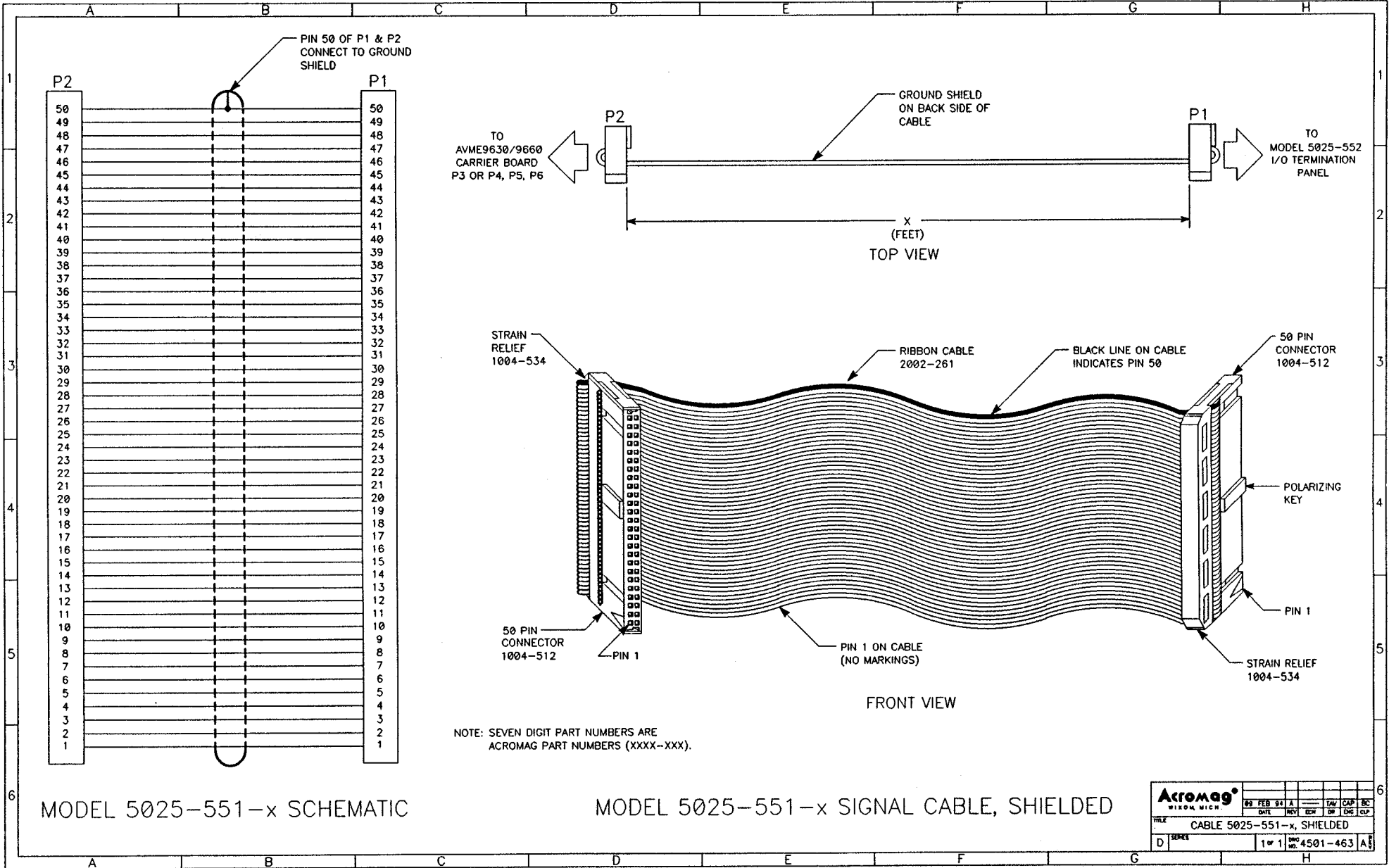
Acromag <small>WITON WISE</small>		02-SEP-84	4	EC	EC	EC
		DATE	REV	ECN	OP	ENG
FILE IP400 BLOCK DIAGRAM						
D	REV 3	IP400	1 of 1	NO 4501-519 A		

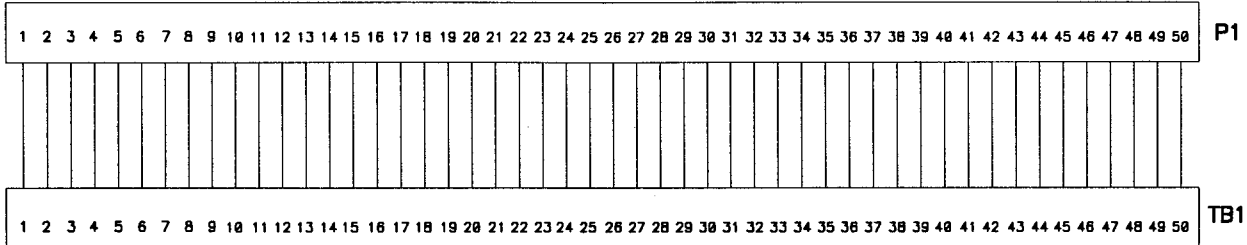


MODEL 5025-550-x SCHEMATIC

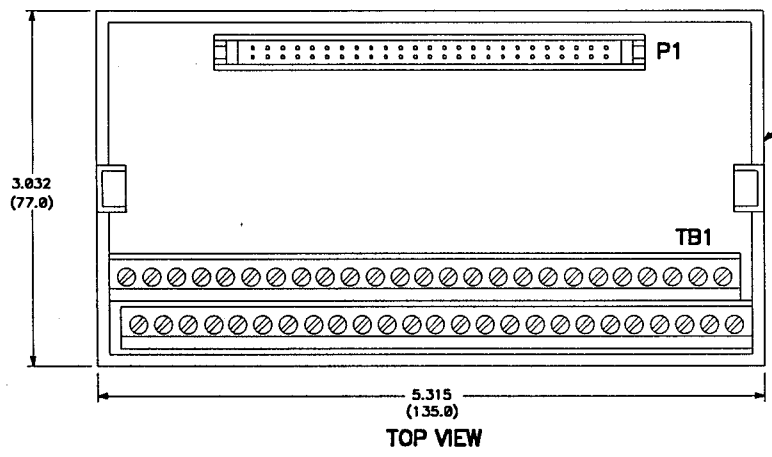
MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

Acromag WINDON, MICH.		89 FEB 94	A						
DATE	REV	ECN	TRV	CAP	BC				
TITLE: CABLE 5025-550-x, NON-SHIELDED									
D	SERIES	1 of 1	ENC	NO.	4501-462	A			

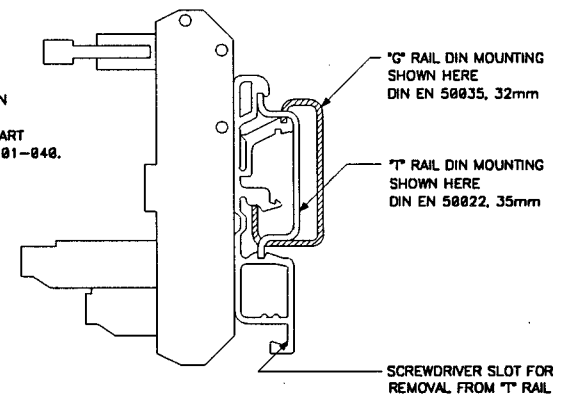




MODEL 5025-552 TERMINATION PANEL SCHEMATIC



TOP VIEW



SIDE VIEW

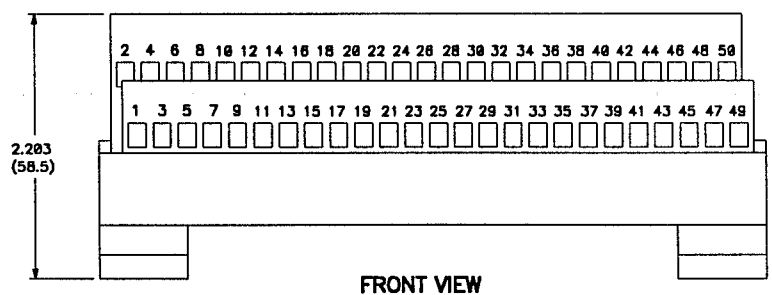
TERMINATION
PANEL
ACROMAG PART
NUMBER 4001-040.

"G" RAIL DIN MOUNTING
SHOWN HERE
DIN EN 50035, 32mm

"T" RAIL DIN MOUNTING
SHOWN HERE
DIN EN 50022, 35mm

SCREWDRIVER SLOT FOR
REMOVAL FROM "T" RAIL

NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ± 0.020 (± 0.5).



FRONT VIEW

MODEL 5025-552 TERMINATION PANEL

Acromag®						
WIXOM, MICH.		09 FEB 94	A	---	TAV	CAP
		DATE	REV	ECN	DR	ENG
TITLE MODEL 5025-552 TERMINATION PANEL						
D	SERIES	1 of 1	DWG NO.	4501-464	A	BC

