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Series IP521-64 Industrial I/O Pack
Octal EIA/TIA-422B Communication Module

USER'S MANUAL

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Table of Contents **Page**

1.0 **GENERAL INFORMATION**..... 2
KEY IP521 FEATURES..... 2
INDUSTRIAL I/O PACK INTERFACE FEATURES..... 3
SIGNAL INTERFACE PRODUCTS..... 3
INDUSTRIAL I/O PACK SOFTWARE LIBRARY..... 4
IP MODULE OLE CONTROL SOFTWARE..... 4
IP MODULE VxWORKS SOFTWARE..... 4
2.0 **PREPARATION FOR USE**..... 4
UNPACKING AND INSPECTION..... 4
CARD CAGE CONSIDERATIONS..... 4
BOARD CONFIGURATION..... 4
CONNECTORS..... 4
IP Field I/O Connector (P2)..... 4
Noise and Grounding Considerations..... 5
IP Logic Interface Connector (P1)..... 5
3.0 **PROGRAMMING INFORMATION**..... 6
ADDRESS MAPS..... 6
RBR - Receiver Buffer Register..... 7
THR - Transmitter Holding Register..... 7
DLL & DLM - Divisor Latch Registers..... 7
IER - Interrupt Enable Register..... 8
ISR - Interrupt Status Register..... 9
FCR - FIFO Control Register..... 9
LCR - Line Control Register..... 9
MCR - Modem Control Register..... 10
LSR - Line Status Register..... 11
MSR - Modem Status Register..... 12
SCR - Scratch Pad/Interrupt Vector Register 12
Enhanced Register Set..... 12
EFR - Enhanced Feature Register..... 12
XON/XOFF - 1,2 Registers..... 13
Identification Space..... 13
THE EFFECT OF RESET..... 13
IP521 PROGRAMMING CONSIDERATIONS..... 14
FIFO Polled-Mode..... 14
FIFO Interrupt Mode..... 14
Loopback Mode Operation..... 15
Interrupt Generation..... 15
Software Flow Control..... 15
Programming Example..... 16
4.0 **THEORY OF OPERATION**..... 17
EIA/TIA-422B SERIAL INTERFACE..... 17
IP521 OPERATION..... 18
LOGIC/POWER INTERFACE..... 18
5.0 **SERVICE AND REPAIR**..... 18
SERVICE AND REPAIR ASSISTANCE..... 18
PRELIMINARY SERVICE PROCEDURE..... 18
6.0 **SPECIFICATIONS**..... 19
PHYSICAL..... 19
ENVIRONMENTAL..... 19
UART..... 19
RS422/RS485 PORTS..... 19
RS422/RS485 TRANSMITTER OUTPUTS..... 19
RS422/RS485 RECEIVERS INPUTS..... 19
INDUSTRIAL I/O PACK COMPLIANCE..... 20

APPENDIX..... 20
CABLE: MODEL 5025-550-X. & 5025-551-X..... 20
TERMINATION PANEL: MODEL 5025-552..... 20
TRANSITION MODULE: MODEL TRANS-GP..... 20

DRAWINGS **Page**
4501-434 IP MECHANICAL ASSEMBLY..... 21
4501-713 IP521 BLOCK DIAGRAM..... 22
4501-714 RS422/RS485 INTERFACE DIAGRAM..... 23
4501-715 RESISTOR SOCKET LOCATION DIAGRA.. 24
4501-462 CABLE 5025-550 (NON-SHIELDED)..... 25
4501-463 CABLE 5025-551 (SHIELDED)..... 26
4501-464 TERMINATION PANEL 5025-552..... 27
4501-465 TRANSITION MODULE TRANS-GP..... 28

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

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1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP521 module provides eight EIA/TIA-422B serial communication ports for interfacing to the VMEbus, PCIbus, or ISAbus, according to your carrier board. Up to five units may be mounted on the PCIbus carrier board to provide up to 40 asynchronous serial ports per PCI system slot.

The IP521 can also be used to implement an EIA-485 interface operating in full-duplex. In this mode more than one transmitter is connected to differential pair and only one transmitter can be enabled at any given time.

The transmit and receive paths of each channel include generous 64-byte FIFO buffers to minimize CPU interaction. Character size, stop bits, parity, and baud rate are software configurable. Prioritized interrupt generation is also supported for transmit, receive, line status, and data set conditions. The IP521 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial communication interface applications that require a highly reliable, high-performance interface at a low cost.

The IP521 is available in standard and extended temperature range modules. The IP521-64 model is the standard temperature range (0 to 70°C) version. The IP521-64E model is the extended temperature range (-40°C to +85°C) version.

KEY IP521 FEATURES

- **High Density** - Provides programmable control of eight EIA/TIA-422B serial ports. Four units mounted on a VMEbus or ISAbus carrier board provide 32 serial channels in a single system slot. On the PCIbus carrier, up to five units may be mounted to provide up to 40 asynchronous serial ports per PCI system slot.
- **64-Character FIFO Buffers -** Both the transmit and receive channels of each serial port provide 64-byte data buffering to reduce CPU interactions and interrupts. This allows the external processor to handle more tasks within a given time.
- **Programmable Character Size -** Each serial port is software programmable for 5, 6, 7, or 8 bit character sizes.

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- **Programmable Stop Bits -** Each serial port allows 1, 1-1/2, or 2 stop-bits to be added to, or deleted from, the serial data stream**.**
- **Programmable Parity Generation & Detection** - Even, Odd, or No Parity generation and detection is supported**.**
- **Line-Break Generation & Detection -** provision for sending and detecting the line break character is provided.
- **False Start Bit Detection -** Prevents the receiver from assembling false data characters due to low-going noise spikes on the RxD input line.
- **Programmable Baud Rate -** The internal baud rate generator allows the 921.6K maximum baud rate to be divided by any divisor between 1 and $2^{(16-1)}$, providing support for all standard baud rates.
- **Interrupt Support -** Individually controlled transmit empty, receive ready, line status, data set, & flow control interrupts may be generated. Unique interrupts can be assigned to each port. Interrupts use a priority shifting scheme based on the last interrupt serviced, preventing the continuous interrupts of one port from blocking the interrupts of another port.
- **Socketed Termination and Bias Resistors** - The network termination and bias resistors are installed in sockets on the board and may be easily inserted or removed where required.
- **Failsafe Receivers** - The receivers employed in this model include a fail-safe feature which guarantees a high output state when the inputs are left open or floating.
- **Internal Diagnostic Capabilities** - Loopback controls for communication link fault isolation are included. Break, parity, overrun, and framing error simulation are also possible.
- **Compatible with Industry Standard UARTs** - The UART of this IP module is compatible with the industry standard ST16C554/654, ST68C554/654, and TL16C544. Additionally, this device can operate in a 16C450 UART family software compatible mode. The transmit and receive channels are double-buffered in this mode. Hold and shift registers eliminate the need for precise synchronization between the host CPU and the serial data.
- **Software Flow Control** - One or two sequential receive data characters are compared to a programmed Xon or Xoff character value. Data transmission can be suspended or resumed via software flow control.
- **Sleep Mode** -The UART can be set via register control to a special sleep mode to reduce power consumption when the chip is not being used.
- **Extended Temperature Performance Option -** Model IP521-E units support operation from -40°C to +85°C.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four/five units mounted on a carrier board provide up to 32/40 serial ports in a single system slot.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID Read" space.
- **8-bit I/O** - Port register Read/Write is performed through 8-bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 1 wait state is required for reading/writing channel data, 2 wait states for interrupt select cycles, and 0 wait states for reading the ID space (see the Specifications section for detailed information).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, PC/AT carrier boards are also supported (see the Acromag Model APC8620 PCIbus carrier board). A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

Note: Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, APC8610, or APC8620 carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The "-X" suffix of the model number is used to indicate the length in feet.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, APC8610, or APC8620 carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

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INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette to simplify communication with the board (Model IPSW-LIB-M03, MSDOS format). Example software functions are provided. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO521.TXT" file in the "IP521" subdirectory on the diskette for more details.

IP MODULE OLE CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module OLE (Object Linking and Embedding) drivers for Windows 95®, and Windows NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow Acromag IP modules and our personal computer carriers to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a Carrier OLE Control, and an OLE control for each Acromag IP module as well as a generic OLE control for non-Acromag IP modules.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module VxWorks® drivers. This software (Model IPSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9660/9630, APC8610, and APC8620. The software is implemented as a library of "C" functions which when linked with existing user code makes possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be



This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following discussion for configuration and assembly instructions. Model IP521 communication boards have no hardware jumpers or switches to configure.

CONNECTORS

Connectors of the IP521 module consist of one IP module field I/O connector, and one IP module logic connector. These interface connectors are discussed in the following sections.

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

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P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: IP521 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
COMMON	1	COMMON	26
TXD-_A	2	TXD-_F	27
TXD+_A	3	TXD+_F	28
RXD-_A	4	RXD-_F	29
RXD+_A	5	RXD+_F	30
COMMON	6	COMMON	31
TXD-_B	7	TXD-_G	32
TXD+_B	8	TXD+_G	33
RXD-_B	9	RXD-_G	34
RXD+_B	10	RXD+_G	35
COMMON	11	COMMON	36
TXD-_C	12	TXD-_H	37
TXD+_C	13	TXD+_H	38
RXD-_C	14	RXD-_H	39
RXD+_C	15	RXD+_H	40
COMMON	16	COMMON	41
TXD-_D	17	No Connection	42
TXD+_D	18	No Connection	43
RXD-_D	19	No Connection	44
RXD+_D	20	No Connection	45
COMMON	21	No Connection	46
TXD-_E	22	No Connection	47
TXD+_E	23	No Connection	48
RXD-_E	24	No Connection	49
RXD+_E	25	No Connection	50

In Table 2.1, a suffix of "_A", "_B", "_C", to "_H" is appended to each pin label to denote its port association. A brief description of each of the serial port signals at P2 is included below. A complete functional description of all P2 pin functions is included in Section 4.0 (Theory Of Operation).

P2 Pin Signal Descriptions

SIGNAL	DESCRIPTION
RxD_A to RxD_H	Receive Data Line Input - This is the receive data input line. During Loopback Mode, the RxD input is disabled from the external connection and connected to the TxD output internally.
TxD_A to TxD_H	Transmit Data Line Output - This is the transmit output data line. In the idle state, this signal line is held in the mark (logic 1) state. During Loopback Mode, the TxD output is internally connected to the RxD input.

Noise and Grounding Considerations

The serial channels of this module are non-isolated and share a common signal ground connection. Further, the IP521 is non-isolated between the logic and field I/O grounds since signal common is electrically connected to the IP module ground. Consequently, the field interface connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

The signal ground connection at the communication ports are common to the IP interface ground, which is typically common to safety (chassis) ground when mounted on a carrier board and inserted in a backplane. As such, be careful not to attach signal ground to safety ground via any device connected to these ports, or a ground loop will be produced, and this may adversely affect operation.

The communication cabling of the P2 interface carries digital data at a high transfer rate. For best performance, increased signal integrity, and safety reasons, you should isolate these connections away from power and other wiring to avoid noise-coupling and crosstalk interference. EIA/TIA-422B communication distances are generally limited to less then 4000 feet. Always keep interface cabling and ground wiring as short as possible for best performance.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details).

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). Note that the IP521 does not utilize all of the logic signals defined for the P1 connector and these are indicated in ***BOLD ITALICS***.

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3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the interface configuration, data transfer, and steering logic of eight EIA/TIA-422B serial ports. As such, three types of information are stored in the I/O space: control, status, and data. These registers are listed below along with their mnemonics used throughout this manual.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP521 uses 64 lower byte locations of this space. The I/O space address map for the IP521 is shown in Table 3.1. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on an 8-bit word basis (D0..D7).

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PC carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier requires the use of odd address locations.

SERIAL DATA REGISTERS (Per Serial Port):	
RBR	Receiver Buffer Register
THR	Transmitter Holding Register
SERIAL STATUS REGISTERS (Per Serial Port):	
LSR	Line Status Register
MSR	Modem Status Register
ISR	Interrupt Status Register
SERIAL CONTROL REGISTERS (Per Serial Port):	
LCR	Line Control Register
FCR	FIFO Control Register
MCR	Modem Control Register
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
IER	Interrupt Enable Register
SCR	Scratch Pad/Interrupt Vector Register
EFR	Enhanced Feature Register
XON-1	XON-1 Low Byte
XON-2	XON-2 High Byte
XOFF-1	XOFF-1 Low Byte
XOFF-2	XOFF-2 High Byte

Shaded registers are accessible only after writing "BF" to the line Control Register (LCR).

Note that some functions share the same register address. For these items, the address lines are used along with the LCR (Line Control Register) and/or the read and write signals to determine the function required. The DLL and DLM registers are only accessible when LCR bit-7 is set to "1". The EFR, Xon 1,2, and Xoff 1,2 locations are accessible only when the LCR is set to "BF" hex.

The IP521 is an eight port RS422 module. Memory map Table 3.1 lists the addresses and registers corresponding to Port A. Detailed register maps for Ports B to H are not given. Since all registers corresponding to all Ports are listed in the same order, it is possible to determine the address for Ports B to H by using Port A and adding the offset given in the table below. For example, Port E's LCR can be accessed at word address 40 + 06 or 46 hex which is Port A LCR at 06 hex plus Port E Offset at 40 hex.

PORT	ADDRESS SPACE OFFSET
A	00
B	10
C	20
D	30
E	40
F	50
G	60
H	70

Table 3.1: IP521 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR	Base Addr+
Serial Port A Registers:				
00	Not Driven[1]	READ - RBR Port A Receiver Buffer Register	Bit7 0	**01**
00	Not Driven[1]	WRITE - THR Port A Transmitter Holding Register	Bit7 0	**01**
00	Not Driven[1]	R/W - DLL Port A Divisor Latch LSB	Bit7 1	**01**
02	Not Driven[1]	R/W - IER Port A Interrupt Enable Register	Bit7 0	**03**
02	Not Driven[1]	R/W - DLM Port A Divisor Latch MSB	Bit7 1	**03**
04	Not Driven[1]	READ - ISR Port A Interrupt Status Reg	N/A	**05**
04	Not Driven[1]	WRITE - FCR Port A FIFO Control Reg.	N/A	**05**
04	Not Driven[1]	R/W - EFR Port A Enhanced Feature Register	BF Hex	**05**
06	Not Driven[1]	R/W - LCR Port A Line Control Register	N/A	**07**
08	Not Driven[1]	R/W - MCR Port A Modem Control Reg	N/A	**09**
08	Not Driven[1]	R/W - Xon-1 Low Byte	BF Hex	**09**
0A	Not Driven[1]	R/W - LSR Port A Line Status Register	N/A	**0B**
0A	Not Driven[1]	R/W - Xon-2 High Byte	BF Hex	**0B**

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Table 3.1 Continued: IP521 I/O Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR	Base Addr+
0C	Not Driven[1]	R/W - MSR Port A Modem Status Reg.	N/A	0D
0C	Not Driven[1]	R/W - Xoff-1 Low Byte	BF Hex	0D
0E	Not Driven[1]	R/W - SCR Port A Scratch Pad, Interrupt Vector, FIFO Count	N/A	0F
0E	Not Driven[1]	R/W - Xoff-2 High Byte	BF Hex	0F
10 ↓ 1E	Not Driven[1]	Port B Registers Organized as Port A[3]		11 ↓ 1F
20 ↓ 2E	Not Driven[1]	Port C Registers Organized as Port A[3]		21 ↓ 2F
30 ↓ 3E	Not Driven[1]	Port D Registers Organized as Port A[3]		31 ↓ 3F
40 ↓ 4E	Not Driven[1]	Port E Registers Organized as Port A[3]		41 ↓ 4F
50 ↓ 5E	Not Driven[1]	Port F Registers Organized as Port A[3]		51 ↓ 5F
60 ↓ 6E	Not Driven[1]	Port G Registers Organized as Port A[3]		61 ↓ 6F
70 ↓ 7E	Not Driven[1]	Port H Registers Organized as Port A[3]		71 ↓ 7F

Notes (Table 3.1):

1. The upper 8 bits of these registers are not driven. Pullups on the carrier data bus will cause these bits to read high (1's).
2. All Reads/Writes to IO space are 1 wait state, Interrupt select cycle is 2 wait states, and ID space reads are 0 wait states.
3. To save user manual space the registers corresponding to ports B to H have not been individually shown. The registers of ports B to H are in the address space shown above. To access a register in port H, for example, the offset of 70 hex is added to the address of the corresponding register given in table 3.1. All ports require a 16 byte memory block.

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UART's and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions. Two FIFO modes are possible: FIFO Interrupt Mode and FIFO Polled Mode. Some registers operate differently between the available modes and this is noted in the following paragraphs.

RBR - Receiver Buffer Register, Ports A-H (READ Only)

The Receiver Buffer Register (RBR) is a serial port input data register that receives the input data from the receiver shift register. Note that the RBR will only receive data if the transceiver is first enabled to receive data. **The transceiver is enabled to receive data by setting bit-0 of the MCR (Modem Control Register) to a logic "1".**

The RBR holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register (LCR bits 0 & 1). If less than 8 bits are transmitted, then data is right-justified to the LSB. If parity is used, then LCR bit 3 (parity enable) and LCR bit 4 (type of parity) are required. Status for the receiver is provided via the Line-Status Register (LSR). When a full character is received (including parity and stop bits), the data-received indication bit (bit 0) of the LSR is set to 1. The host CPU then reads the Receiver Buffer Register, which resets LSR bit 0 low. If the character is not read prior to a new character transfer between the receiver shift register and the receiver buffer register, the overrun-error status indication is set in LSR bit 1. If there is a parity error, the error is indicated in LSR bit 2. If a stop bit is not detected, a framing error indication is set in bit 3 of the LSR.

Serial asynchronous data is input to the receiver shift register via the receive data line (RxD). From the idle state, this line is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x clock to 7-1/2 (which is the center of the start bit). The start bit is judged valid if RxD is still low at this point. This is known as false start-bit detection. By verifying the start bit in this manner, it helps to prevent the receiver from assembling an invalid data character due to a low-going noise spike on RxD. If the data on RxD is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center (providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

THR - Transmitter Holding Register, Ports A-H (WRITE Only)

The Transmitter Holding Register (THR) is a serial output data register that shifts the data to the transmit data line (TxD). However, the THR data will not pass to the TxD line unless the tranceiver is first enabled. **The transceiver must be enabled to transmit data by setting bit-1 of the MCR (Modem Control Register) to a logic "1".**

The Transmitter Holding Register (THR) is a serial port output data register that holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register. If less than 8 bits are transmitted, then data is entered right-justified to the LSB. This data is framed as required, then shifted to the transmit data line (TxD). In the idle state, TxD is held high. In Loopback Mode, this data is looped back into the Receiver Buffer Register.

The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, provided that at least one FIFO location is available. The THR empty flag in the LSR register will be set to a logic 1 when at least one FIFO location is available.

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DLL & DLM - Divisor Latch Registers, Ports A-H (R/W)

The Divisor Latch Registers form the divisor used by the internal baud-rate generator to divide the 14.7456MHz clock to produce an internal sampling clock suitable for synchronization to the desired baud rate. The output of the baud generator (RCLK) is sixteen times the baud rate. Two 8-bit divisor latch registers per port are used to store the divisors in 16-bit binary format. The DLL register stores the low-order byte of the divisor, DLM stores the high-order byte. **These registers must be loaded during initialization.**

Note that bit 7 of the LCR register must first be set high to access the divisor latch registers (DLL & DLM).

Upon loading either latch, a 16-bit baud counter is immediately loaded (this prevents long counts on initial load). The clock may be divided by any divisor from 1 to $2^{(16-1)}$. The relationship between the baud rate, the divisor, and the 14.7456MHz clock can be summarized in the following equations:

$$\text{Divisor} = 14.7456\text{MHz} \Big/ (16 \times \text{Baud Rate} \times \text{MCRDIV})$$

$$\text{Baud Rate} = 14.7456\text{MHz} \Big/ (16 \times \text{Divisor} \times \text{MCRDIV})$$

The MCRDIV term represents the state of bit-7 of the MCR (Mode Control Register) as follows:

MCRDIV = 1 If MCR bit-7=0
MCRDIV = 4 If MCR bit-7=1

The following table shows the correct divisor to use for generation of some standard baud rates (based on the 14.7456MHz clock). A different external crystal can replace the 14.7456MHz crystal on the circuit board to obtain unique clock rates. You may contact Acromag Applications Engineering to explore options in this area.

Table 3.2: Baud Rate Divisors (14.7456MHz Clock)

BAUD RATE		DIVISOR (N)		
MCR Bit-7=1	MCR Bit-7=0	Decimal	DLM (HEX)	DLL (HEX)
50	200	4608	12	00
300	1200	768	03	00
600	2400	384	01	80
1200	4800	192	00	C0
2400	9600	96	00	60
3600	14,400	64	00	40
4800	19,200	48	00	30
7200	28,800	32	00	20
9600	38,400	24	00	18
19,200	76,800	12	00	0C
28,800	115,200	8	00	08
38,400	153,600	6	00	06
57,600	230,400	4	00	04
230,400	921,600	1	00	01

With respect to this device, the baud rate may be considered equal to the number of bits transmitted per second (bps). The bit rate (bps), or baud rate, defines the bit time. This is the length of time a bit will be held on before the next bit is transmitted. A receiver and transmitter must be communicating at the same bit rate, or data will be garbled. A receiver is alerted to an incoming character by the start bit, which marks the beginning of the character. It then times the incoming signal, sampling each bit as near to the center of the bit time as possible.

To better understand the asynchronous timing used by this device, note that the receive data line (RxD) is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x sampling clock to 7-1/2 (the center of the start bit). The receiver then counts from 0 to 15 to sample the next bit near its center, and so on, until a stop bit is detected, signaling the end of the data stream. Use of a sampling rate 16x the baud rate reduces the synchronization error that builds up in estimating the center of each successive bit following the start bit. As such, if the data on RxD is a symmetrical square wave, the center of each successive data cell will occur within ±3.125% of the actual center (this is 50% ÷ 16, providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

IER - Interrupt Enable Register, Ports A-H (R/W)

The Interrupt Enable Register is used to independently enable/ disable the serial port interrupt sources. Each of the eight ports have seven unique interrupt sources which are all mapped to INTREQ0* of the IP module.

Interrupts are disabled by resetting the corresponding IER bit low (0), and enabled by setting the IER bit high (1). Disabling the interrupt system (IER bits 7-5 and 3-0 low) also inhibits the Interrupt Status Register (ISR) and the interrupt request line (INTREQ0*). **In addition to enabling the desired bits in the IER, bit-3 of the Modem Control Register (MCR) must be set to a logic "1" to enable interrupts.**

Interrupt Enable Register

IER BIT	INTERRUPT ACTION
0	0 = Disable Interrupt 1 = Enable Interrupt This interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation. Note that the receive FIFO must also be enabled via bit-0 of the FCR for a receive interrupt to be issued.
1	0 = Disable Interrupt 1 = Enable Interrupt This interrupt will be issued whenever the THR is empty and is associated with bit-1 in the LSR.
2	0 = Disable Interrupt 1 = Enable Interrupt This interrupt will be issued whenever a fully assembled receive character is available.
3	0 = Disable Interrupt 1 = Enable Interrupt Modem Status Interrupt. Since the modem input signals are not used on this module, this interrupt should always be disabled.
4[1]	0 = Disable Sleep Mode 1 = Enable Sleep Mode The clock/oscillator circuit is disabled in sleep mode. The UART will not lose the programmed bits when sleep mode is activated or deactivated. The UART will not enter sleep mode if any interrupts are pending.
5[1]	0 = Disable the Receive Xoff Interrupt 1 = Enable the Receive Xoff Interrupt When software flow control in enabled, and one or two sequential receive data characters match the preprogrammed Xoff 1-2 values an interrupt will be issued.

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IER BIT	INTERRUPT ACTION
6[1]	0 = Disable RTS Interrupt 1 = Enable RTS Interrupt. This Interrupt is generated when the RTS pin transitions from a logic 0 to a logic 1. RTS is not output by this module. Instead RTS is used to enable the transmitter of the port. This interrupt should always be disabled.
7[1]	0 = Disable CTS Interrupt 1 = Enable CTS Interrupt. This interrupt will be issued when the CTS pin transitions from a logic 0 to a logic 1. Since CTS is not used on this module, this interrupt should always be disabled.

Notes (Interrupt Enable Register):

1. Bits 4 to 7 are only programmable when the EFR bit 4 is set to "1".

A power-up or system reset sets all IER bits to 0 (bits 7-0 forced low).

ISR - Interrupt Status Register, Ports A-H (READ Only)

The Interrupt Status Register is used to indicate that a prioritized interrupt is pending and the type of interrupt that is pending. Six levels of prioritized interrupts are provided to minimize software interaction. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. Note, only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits.

The eight individual ports share the IP module INTREQ0* signal. Each port has an opportunity to issue an interrupt in a round robin fashion. That is, interrupt vectors are served according to a shifting priority scheme that is a function of the last interrupting port served.

The following interrupt source table shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

PRIORITY LEVEL	ISR BITS Bit5 to Bit0	Source of the Interrupt
1	000110	Receiver Line Status (see LSR bits 1-4)
2	000100	Received Data Ready or Trigger Level reached.
2	001100	Receive Data Time Out.
3	000010	Transmitter Holding Register Empty
4	000000	MSR (Modem Status Register)
5	010000	Received Xoff signal special character
6	100000	CTS, RTS change of state

Note that ISR bit 0 can be used to indicate whether an interrupt is pending (bit 0 low when interrupt is pending). ISR bits 1 & 2 are used to indicate the highest priority interrupt pending. ISR bit 3 is always logic 0 in the 16C450 mode. ISR bit 3 is set along with bit 2 when in the FIFO mode and a timeout interrupt is pending. Bit 4 set indicates a Xoff/special character detected interrupt pending. Bit 5 indicates a pending interrupt due to a change of state on the CTS or RTS signals.

Bits 6 and 7 are set when bit 0 of the FIFO Control Register is set to 1. A power-up or system reset sets ISR bit 0 to logic "1", and bits 1 to 7 to logic "0".

FCR - FIFO Control Register, Ports A-H (WRITE Only)

This write-only register is used to enable and clear the FIFO buffers, set the transmit/receive FIFO trigger levels, and select the type of DMA signaling (DMA is NOT supported by this model).

FIFO Control Register

FCR BIT	FUNCTION
0	When set to "1", this bit enables both the Tx and Rx FIFO's. All bytes in both FIFO's can be cleared by resetting this bit to 0. Data is cleared automatically from the FIFO's when changing from FIFO mode to the alternate (16C450) mode and visa-versa. This bit must be a "1" when other FCR bits are written to or they will not be programmed.
1	When set to "1", this bit clears all bytes in the Rx-FIFO and the resets counter logic to 0 (this does not clear the shift register).
2	When set to "1", this bit clears all bytes in the Tx-FIFO and resets the counter logic to 0 (this does not clear the shift register).
3	When set to "1", this bit sets DMA Signal from Mode 0 to Mode 1, if FIFO Control Register Bit 0 = 1 (DMA Not Supported)
5,4[1]	These bits are used to set the trigger level for the transmit FIFO interrupt. An interrupt will be issued when the number of characters in the FIFO drops below the selected trigger level. One of four trigger levels can be selected. bit 5 bit 4 Trigger Level 0 0 08 0 1 16 1 0 32 1 1 56
7,6	These bits are used to set the trigger level for the receiver FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. One of four trigger levels can be selected. bit 7 bit 6 Trigger Level 0 0 08 0 1 16 1 0 56 1 1 60

Notes (FIFO Control Register):

1. Bits 4 and 5 are only programmable when the EFR bit 4 is set to "1".

A power-up or system reset sets all FCR bits to 0.

LCR - Line Control Register, Ports A-H (Read/Write)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the

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number of stop bits, and the parity are selected by writing the appropriate bits in this register.

The individual bits of this register control the format of the data character as follows:

Line Control Register

LCR Bit	FUNCTION	PROGRAMMING
1,0	Word Length Sel.	0 0 = 5 Data Bits 0 1 = 6 Data Bits 1 0 = 7 Data Bits 1 1 = 8 Data Bits
2	Stop Bit Select	0 = 1 Stop Bit 1 = 1.5 Stop Bits if 5 data bits; 2 Stop Bits if 6, 7, or 8 data bits selected.
3	Parity Enable	0 = Parity Disabled 1 = Parity Enabled A parity bit is generated and checked for between the last data word bit and the stop bit.
4	Even-Parity Select	0 = Odd Parity 1 = Even Parity
5	Stick Parity	0 = Disabled, 1 = Enabled When parity is enabled, stick parity causes the transmission and reception of a parity bit to be in the opposite state from the value selected via bit 4. This is used as a diagnostic tool to force parity to a known state and allow the receiver to check the parity bit in a known state.
6	Break Control	0 = Break Disabled, 1 = Break Enabled When break is enabled, the serial output line (TxD) is forced to the space state (low). This bit acts only on the serial output and does not affect transmitter logic. For example, if the following sequence is used, no invalid characters are transmitted due to the presence of the break. 1. Load a zero byte in response to the Transmitter Holding Register Empty (THRE) status indication. 2. Set the break in response to the next THRE status indication. 3. Wait for the transmitter to become idle when the Transmitter Empty status signal is set high (TEMT=1); then clear the break when normal transmission has to be restored.
7	DLL/DLM and EFR Enable Bit	0 = Access Receiver Buffer 1 = Allow Access to Divisor Latches (DLL & DLM) and Enhanced Feature Register enabled (EFR).

Note that bit 7 must be set high to access the divisor latch registers DLL & DLM of the baud rate generator or access the Enhanced Feature Register (EFR). Bit 7 must be low to access the Receiver Buffer Register (RBR), the Transmitter Holding Register (THR), or the Interrupt Enable Register (IER). A power-up or system reset sets all LCR bits to 0.

A detailed discussion of word length, stop bits, parity, and the break signal is included in Section 4.0 (Theory of Operation).

MCR - Modem Control Register, Ports A-H (R/W)

The Modem Control register controls the interface with the modem or data set as described below. For this model, DTR is used to enable the receiver to enable input of RxD. RTS is used to enable its corresponding transmitter for output of the TxD signal. The four modem control inputs (CTS, DSR, DCD, and RI) are disconnected from their receiver input paths. In addition, the four modem control outputs (DTR, RTS, OUT1, and OUT2) do not have transmitter output paths.

Bit-3 of this register must be set to a logic "1" to enable the corresponding port to issue an interrupt.

Modem Control Register

MCR Bit	FUNCTION	PROGRAMMING
0	Data Terminal Ready Output Signal (DTR)	0= DTR* Not Asserted (Inactive) 1= DTR* Asserted (Active) A DTR signal path is NOT SUPPORTED by this model. Instead, this output is used to enable the receiver of the port RxD.
1	Ready to Send Output Signal (RTS)	0 = RTS* Not Asserted (Inactive) 1 = RTS* Asserted (Active) A RTS signal path is NOT SUPPORTED by this model. Instead, the output is used to enable the transmitter of the port TxD.
2	Not Used	No Effect on External Operation
3	Port Interrupt Disable/Enable	0 = Interrupt Disabled for this port. 1 = Interrupt Enabled for this port.
4	Loop-back[1]	0 = Loop-back Disabled 1 = Loop-back Enabled
5[2]	Xon Control	0 = Disable Xon 1 = Enable any Xon function. In this mode any RX character received will enable Xon.
6[2]	Not Used	Must be logic 0
7[2]	Divide by Four	0 = Divide by one. The crystal frequency is unchanged. 1 = Divide by four. After the crystal frequency is divided by 16 it is further divided by 4 (see Table 3.2).

Notes (Modem Control Register):

1. MCR Bit 4 provides a local loopback feature for diagnostic testing of the UART channel. When set high, the UART serial output (connected to the TXD driver) is set to the marking (logic 1 state), and the UART receiver serial data input is disconnected from the RxD receiver path. The output of the UART transmitter shift register is then looped back into the receiver shift register input. The control output (RTS) is internally connected to the control input DSR (while its associated pin is forced to its high/inactive state). Thus, in the loopback diagnostic mode, transmitted data is immediately received, permitting the host processor to verify the transmit and receive data paths of the selected serial channel. In this mode, interrupts are generated by controlling the state of the four lower order MCR bits

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internally, instead of by the external hardware paths. However, no interrupt requests or interrupt vectors are actually served in loopback mode, and interrupt pending status is only reflected internally.

2. Bits 5-7 are only programmable when the EFR bit 4 is set to "1". The programmed values for these bits are latched when EFR bit 4 is cleared, preventing existing software from inadvertently overwriting the extended functions. However, these MCR bits can not be set if the LCR is set to BF hex.

A power-up or system reset sets all MCR bits to 0.

LSR - Line Status Register, Ports A-H (Read/Write-Restricted)

The Line Status Register (LSR) provides status indication corresponding to the data transfer. LSR bits 1-4 are the error conditions that produce receiver line-status interrupts (a priority 1 interrupt in the Interrupt Identification Register). The line status register may be written, but this is intended for factory test and should be considered read-only by the application software.

Line Status Register

LSR Bit	FUNCTION	PROGRAMMING
0	Data Ready (DR)	0 = Not Ready (reset low by CPU Read of RBR or FIFO) 1 = Data Ready (set high when character received and transferred into the RBR or FIFO).
1	Overrun Error (OE)	0 = No Error 1 = Indicates that data in the RBR is not being read before the next character is transferred into the RBR, overwriting the previous character. In the FIFO mode, it is set after the FIFO is filled and the next character is received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred into the FIFO, but is overwritten. This bit is reset low when the CPU reads the LSR.
2	Parity Error (PE)	0 = No Error 1 = Parity Error - the received character does not have the correct parity as configured via LCR bits 3 & 4. This bit is set high on detection of a parity error and reset low when the host CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO (LSR Bit 2 reflects the error when the character is at the top of the FIFO).
3	Framing Error (FE)	0 = No Error 1 = Framing Error - Indicates that the received character does not have a valid stop bit (stop bit following last data bit or parity bit detected as a zero/space bit). This bit is reset low when the CPU reads the contents of the LSR. In FIFO mode, the framing error is associated with a particular character in the FIFO (LSR Bit 3 reflects the error when the character is at the top of the FIFO).

Line Status Register...continued

LSR Bit	FUNCTION	PROGRAMMING
4	Break Interrupt (BI)	0 = No Break 1 = Break the received data input has been held in the space (logic 0) state for more then a full-word transmission time (start bits+ data+ parity bit+ stop bits). Reset upon read of LSR. In FIFO mode, this bit is associated with a particular character in the FIFO and reflects the Break Interrupt when the break character is at the top of the FIFO. It is detected by the host CPU during the first LSR read. Only one "0" character is loaded into the FIFO when BI occurs.
5	Transmitter Holding Register Empty (THRE)	0 = Not Empty 1 = Empty - indicates that the channel is ready to accept a new character for transmission. Set high when character is transferred from the THR into the transmitter shift register. Reset low by loading the THR (It is not reset by a host CPU read of the LSR). In FIFO mode, this bit is set when the Tx FIFO is empty and cleared when one byte is written to the Tx FIFO. When a Transmitter Holding Register Empty interrupt is enabled by IER bit 1, this signal causes a priority 3 interrupt in the ISR. If the ISR indicates that this signal is causing the interrupt, the interrupt is cleared by a read of the ISR.
6	Transmitter Empty (TEMT)	0 = Not Empty 1 = Transmitter Empty - set when both the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. Reset low when a character is loaded into the THR and remains low until the character is transmitted (it is not reset low by a read of the LSR). In FIFO mode, this bit is set when both the transmitter FIFO and shift register are empty.
7	Receiver FIFO Error	0 = No Error in FIFO (it is always 0 in 16C450 mode--FCR bit 0 low). 1 = Error in FIFO - set when one of the following data errors is present in the FIFO: parity error, framing error, or break interrupt indication. Cleared by a host CPU read of the LSR if there are no subsequent errors in the FIFO. FIFO read of offending character is also required.

Note that LSR Bits 1-4 (OE, PE, FE, BI) are the error conditions that produce a receiver-line-status interrupt (a priority 1 interrupt in the ISR register when any one of these conditions are detected). This interrupt is enabled by setting IER bit 2 to "1".

A power-up or system reset sets all LSR bits to 0, except bits 5 and 6 which are high.

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MSR - Modem Status Register, Ports A-H (Read/Write)

The Modem Status Register (MSR) provides the host CPU with an indication on the status of the modem input line from a modem or other peripheral device. However for this model, the four modem control inputs (CTS, DSR, DCD, and RI) are disconnected from their receiver input paths.

Modem Status Register

MSR BIT	FUNCTION
0	ΔCTS - NOT SUPPORTED
1	ΔDSR - NOT SUPPORTED
2	ΔRI - NOT SUPPORTED.
3	ΔDCD - NOT SUPPORTED
4	CTS - If the channel is in the loopback mode (MCR bit 4 = 1), then the state of RTS in the MCR is reflected.
5	DSR - NOT SUPPORTED
6	RI - NOT SUPPORTED
7	DCD - NOT SUPPORTED

An Asterisk (*) is used to indicate an active-low signal.

Note that reading MSR clears the delta-modem status indication (bit 0), but has no effect on the bit-4 status bit. For both the LSR & MSR, the setting of the status bits during a status register read operation is inhibited (the status bit will not be set until the trailing edge of the read). However, if the same status condition occurs during a read operation, that status bit is cleared on the trailing edge of the read instead of being set again.

Note that not all UART signal paths are used by this model and their corresponding UART pins are tied high (+5V). This includes, CTS (Clear To Send), RI (Ring Indicator), DSR (Data Set Ready), and DCD (Data Carrier Detect).

A power-up or system reset sets MSR bit-0 to “0” (bit 4 is determined by the corresponding input signal). All other bits are not used.

SCR - Scratch Pad/Interrupt Vector Register, Ports A-H (Read/Write)

This 8-bit read/write register has no effect on the operation of either serial channel. It is provided as an aide to the programmer to temporarily hold data. Alternately, it stores the interrupt vector for the port.

In response to an interrupt select cycle, the IP module will execute a read of this register for the interrupting port (see Interrupt Generation section for more details).

Enhanced Register Set, Ports A-H

The Enhanced Register Set is unique to the EXAR® UART provided on the IP521 IP module. The EXAR® UART maintains compatibility with the industry standard 16C554/654 and 68C554/654 UARTs and provides new features to enhance serial communication operation.

The new features provided by the EXAR 16C654 UART are summarized in the following register descriptions and includes software flow control via Xon and Xoff.

The Enhanced Register Set includes the following registers.

- Enhanced Feature Register (EFR)
- Xon-1, Xon-2
- Xoff-1, Xoff-2

In order to access the Enhanced Registers the LCR must be set to “BF” hex. Each of these registers will be described in the following.

EFR - Enhanced Feature Register, Ports A-H (Read/Write)

The Enhanced Feature register is used to enable or disable enhanced features, including software flow control. This register is also used to unlock access to programming the extended register functionality of IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7.

Enhanced Feature Register

EFR Bit	FUNCTION	PROGRAMMING
3-0	Software Flow Control	00XX = No Transmit Flow Control 10XX = Transmit Xon1/Xoff1 01XX = Transmit Xon2/Xoff2 11XX = Transmit Xon1 and Xon2, Xoff1 and Xoff2 XX00 = No receive Flow Control XX10 = Receiver Compares Xon1/Xoff1 XX01 = Receiver Compares Xon2/Xoff2 1011 = Transmit Xon1/Xoff1, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2. 0111 = Transmit Xon2/Xoff2. Receiver compares Xon1 and Xon2, Xoff1 and Xoff2. 1111 = Transmit Xon1 and Xon2, Xoff1 and Xoff2; Receiver compares Xon1 and Xon2, Xoff1 and Xoff2. 0011 = No transmit flow control. Receiver compares Xon1 and Xon2, Xoff1 and Xoff2.
4	Enhanced Function Control	0 = Disable and latch the Enhanced Functions: the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7. This feature prevents existing software from altering or overwriting the enhanced functions. 1 = Enables the enhanced functions. Allows the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified.
5	Special Character Detect Control	0 = Disable special character detect. 1 = Enable special character detect. Incoming receive characters are compared with Xoff-2 data. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Bit-0 of the Xoff/Xon registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR bits 0-3 must be set to a logic “0”).

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EFR Bit	FUNCTION	PROGRAMMING
6	RTS[1] Hardware Flow Control	0 = Disable Automatic RTS flow control. 1= Enable Automatic RTS flow control. The RTS pin can be automatically controlled to indicate local buffer overflows to remote buffers. When automatic hardware flow control is enabled, an interrupt will be generated when the receive FIFO is filled to the program trigger level and RTS will go to a logic "1" at the next trigger level. RTS will return to a logic "0" when data is unloaded below the next lower trigger level. RTS functions normally when hardware flow control is disabled. FCTR bits0-1 are used to set the RTS delay timer/trigger level.
7	CTS[2] Hardware Flow Control	0 = Disable Automatic CTS flow control. 1 = Enable Automatic CTS flow control.

Notes :

1. For this model RTS is used to enable its corresponding transmitter for output of the TxD signal. The RTS signals do not have transmitter output paths on this model.
2. The CTS signals do not have a receiver input path on this model.

A power-up or system reset sets all EFR bits to 0.

XON/XOFF-1,2 Registers, Ports A-H (R/W)

These registers hold the programmed XON and XOFF characters for software flow control. XON or XOFF characters may be 1 or 2 bytes long. The UART compares incoming data to these values and restarts (XON) or suspends (XOFF) data transmission when a match is detected. Note that access to these registers is granted only after writing "BF" to the Line Control Register (LCR). All XON/XOFF bits are set to 0 upon power-up or system reset.

Identification Space (Read Only, 32 odd-byte addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP521 ID Space does not contain any variable (e.g. unique calibration) information. ID Space bytes are addressed using only the odd addresses in a 64 byte block (on the "Big Endian" VMEbus). Even addresses are used on the "Little Endian" PC ISA or PCI buses.

The IP521 ID Space contents are shown in Table 3.3. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID information. Execution of an ID Space Read operation requires 0 wait states.

Table 3.3: IP521 ID Space Identification (ID)

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		25	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		11	CRC
19 to 3F		yy	Not Used

Notes (Table 3.3):

1. The IP model number is represented by a two-digit code within the ID space (the IP521 model is represented by 25 Hex).

THE EFFECT OF RESET

A software or hardware reset puts the serial channels into an idle-mode until initialization (programming). A reset initializes the receiver and transmitter clock counters. It also clears the Line-Status Register (LSR), except for the transmitter shift-register empty (TEMT) and transmit holding-register empty (THRE) bits which are set to 1 (note that when interrupts are subsequently enabled, an interrupt will occur due to THRE being set). The Modem Control Register (MCR) is also cleared. All of the discrete signal lines, memory elements, and miscellaneous logic associated with these register bits are cleared, de-asserted, or turned off. However, the Line Control Register (LCR), divisor latches, Receiver Buffer Register (RBR), and Transmitter Holding Register (THR) are not affected. The following table summarizes the effect of a reset on the various registers and internal and external signals:

REG/SIGNAL	RESET CTRL	STATE/EFFECT
REGISTERS:		
IER	Reset	All Bits low
ISR	Reset	Bit 0 high, Bits 1-7 low
LCR	Reset	All bits low
MCR	Reset	All bits low
FCR	Reset	All bits low
LSR	Reset	All bits low, except bits 5 & 6 are high
MSR	Reset	Bits 0-3 low, bit 4 corresponds to input signal
EFR	Reset	All bits low
XON-1,2	Reset	All bits low
XOFF-1,2	Reset	All bits low
TRG	Reset	All bits low

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SIGNALS (INTERNAL & EXTERNAL):		
TxD	Reset	High
Interrupt (RCVR errors)	Read LSR/ Reset	Low
Interrupt (RCVR data ready)	Read RCVR Buffer Register/ Reset	Low
Interrupt (THRE)	Read ISR/Write THR/Reset	Low
Interrupt (Modem Status Changes)	Read MSR/ Reset	Low
RTS*	Reset	High

IP521 PROGRAMMING CONSIDERATIONS

Each serial channel of this module is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. The control registers can be written in any order, but the IER register should be written last since it controls the interrupt enables. The contents of these registers can be updated any time the serial channel is not transmitting or receiving data.

The complete status of each channel can be read by the host CPU at any time during operation. Two registers are used to report the status of a particular channel: the Line Status Register (LSR) and the Modem Status Register (MSR).

Serial channel data is read from the Receiver Buffer Register (RBR), and written to the Transmitter Holding Register (THR). Writing data to the THR initiates the parallel-to-serial transmitter shift register to the TxD line. Likewise, input data is shifted from the RxD pin to the Receiver Buffer Register as it is received.

The Scratch Pad Register is used to store the interrupt vector for the port. In response to an interrupt select cycle, the IP module will provide a read of this port. As such, each port may have a unique interrupt vector assigned. Interrupts are served in a shifting-priority fashion as a function of the last interrupting port serviced to prevent continuous interrupts from a higher-priority interrupt channel from freezing out service of a lower priority channel.

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UART's, and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions.

Two FIFO modes of operation are possible: FIFO Interrupt Mode and FIFO Polled Mode. In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating time-out conditions. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached. The transmit and the receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

To make programming and communicating with the board easier, Acromag provides you with the Industrial I/O Pack Software Library diskette. The functions provided are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO521.TXT" file in the "IP521" subdirectory on the diskette for details.

Acromag also provides a software diskette of IP module Object Linking and Embedding (OLE) drivers for Windows 95®/NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow all IP modules and the APC8620 carrier to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a carrier OLE control, and an OLE control for each Acromag IP module as well as a generic OLE control for non-Acromag IP modules.

In addition, Acromag provides a software product (sold separately) consisting of IP module VxWorks® drivers. This software (Model IPSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9660/9630, APC8610, and APC8620. The software is implemented as a library of "C" functions which when linked with existing user code makes possible simple control of all Acromag IP modules and carriers.

FIFO Polled-Mode

Resetting all Interrupt Enable Register (IER) bits to 0, with FIFO Control Register (FCR) Bit 0 =1, puts the channel into the polled-mode of operation. The receiver and transmitter are controlled separately and either one or both may be in the polled mode. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached, the transmit and the receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

FIFO-Interrupt Mode

In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating a time-out condition. Please note the following with respect to this mode of operation.

When the receiver FIFO and receiver interrupts are enabled, the following receiver status conditions apply:

1. LSR Bit 0 is set to 1 when a character is transferred from the shift register to the receiver FIFO. It is reset to 0 when the FIFO is empty.
2. The receiver line-status interrupt (ISR=06) has a higher priority than the received data-available interrupt (ISR=04).
3. The receive data-available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. It is cleared when the FIFO drops below its programmed trigger level. The receive data-available interrupt indication

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(ISR=04) also occurs when the FIFO reaches its trigger level, and is cleared when the FIFO drops below its trigger level.

When the receiver FIFO and receiver interrupts are enabled, the following receiver FIFO character time-out status conditions apply:

1. A FIFO character time-out interrupt occurs if:
   - A minimum of one character is in the FIFO.
   - The last received serial character is longer than four continuous prior character times ago (if 2 stop bits are programmed, the second one is included in the time delay).
   - The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud, and with 12-bit characters (including start, stop, and parity bits), the FIFO time-out interrupt causes a latency of 160ms maximum from received character to interrupt issued.
2. From the clock signal input, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

When the transmit FIFO and transmit interrupts are enabled (FCR Bit 0 = 1 and IER=01), a transmitter interrupt will occur as follows:

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (ISR=02) occurs. The interrupt is cleared when the Transmitter Holding Register (THR) is written to or the Interrupt Status Register (ISR) is read. One to 128 characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmit FIFO empty indications are delayed one character time minus the last stop bit time when the following occurs: Bit 5 of the LSR (THRE) is 1 and there is not a minimum of two bytes at the same time in the transmit FIFO since the last time THRE=1. The first transmitter interrupt after changing FCR Bit 0 is immediate, assuming it is enabled.

The receiver FIFO trigger level and character time-out interrupts have the same priority as the received data-available interrupt. The Transmitter Holding-Register Empty interrupt has the same priority as the Transmitter FIFO-Empty interrupt.

Loopback Mode Operation

This device can be operated in a “loopback mode”, useful for troubleshooting a serial channel without physically wiring to the channel. Bit 4 of the Modem Control Register (MCR) is used to program the local loopback feature for the UART channel. When set high, the UART channel’s serial output line (Transmit Data Path) is set to the marking (logic 1 state), and the UART receiver serial data input lines are disconnected from the RxD receiver path. The output of the UART transmitter shift register is then looped back into the receiver shift register input. Thus, a write to the Transmitter Holding Register is automatically looped back to the corresponding Receiver Buffer Register. The RTS modem control output (of the MCR Register) is internally connected to the corresponding modem control input (monitored via the Modem Status Register), while their associated pins are forced to their high/inactive state. Thus, in loopback diagnostic mode, transmitted data is immediately received permitting the host processor to verify the transmit and receive data paths of the selected serial channel. Further, modem status interrupt generation is controlled manually in loopback mode by controlling the state of CTS internally.

Interrupt Generation

This model provides individual control for generation of transmit, receive, line status, and data set interrupts on each of eight channels. Each channel shares interrupt request line 0 (INTREQ0) according to a unique priority shifting scheme that prevents the continuous interrupts of one channel from freezing out another channels’ interrupt requests.

After pulling the INTREQ0 line low and in response to an Interrupt Select cycle, the current highest priority interrupt channel will serve its interrupt vector first. Interrupt serving priority will shift as a function of the last port served. A unique interrupt vector may be assigned to each communication port and is loaded into the Scratch Pad Register (SCR) for the port. The IP module will thus execute a read of the scratch pad register in response to an interrupt select cycle. Two wait states are required to complete this cycle.

Interrupt priority is assigned as follows. Initially, with no prior interrupt history, Port A has the highest priority and will be served first, followed by port B, followed by port C etc. to Port H. However, if port A was the last interrupt serviced, then port B will have the highest priority, followed by port C, etc. to Port H, then port A, in a last-serviced last-out fashion. Priority continues to shift in the same fashion if Port B or Port C was the last interrupt serviced. This is useful in preventing continuous interrupts on one channel from freezing out interrupt service for other channels.

Software Flow Control

Model IP521-64 modules include support for software flow control. Software flow control utilizes special XON & XOFF characters to control the flow of data, for more efficient data transfer and to minimize overrun errors.

Software flow control (sometimes called XON/XOFF pacing) sends a signal from one node to another by adding flow control characters to the data stream. The receiving node will detect the XON or XOFF character and respond by suspending transmission of data (XOFF turns the data flow off), or resuming transmission of data (XON turns the data flow on). Flow control is used frequently in data communications to prevent overrun errors or the loss of data. For example, a node might transmit the XOFF character to the host computer if the host is sending data too quickly to be processed or buffered, thus preventing the loss of data.

The flow control characters are stored in the XON-1,2 and XOFF-1,2 registers. Two XON & XOFF registers are provided because the flow control character may be 1 or 2 bytes long. The contents of the XON-1,2 and XOFF-1,2 registers are reset to “0” upon power-up or system reset, and may be programmed to any value for software flow control. Different conditions may be set to detect the XON/XOFF characters or start/stop the transmission.

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When software flow control is enabled, the UART of this model will compare two sequential received data bytes with preprogrammed XOFF-1,2 characters. When an XOFF match is detected, the UART will halt transmission after completing the transmission of the current character. The receive ready flag of the Interrupt Status register will be set (ISR bit 4 is set to "1" when the XOFF character has been detected), only if enabled via bit 5 of the Interrupt Enable register (IER bit 5 is used to enable the received XOFF interrupt) and bit-3 of the MCR. An interrupt will then be generated. After recognition of the XOFF characters, the UART will compare the next two incoming characters with the preprogrammed XON-1,2 characters. If a match is detected, the UART will resume transmission and clear the received XOFF interrupt flag (Interrupt Status Register bit 4). After more data has been received, the UART will automatically send XOFF-1,2 characters as soon as the received data passes the programmed FIFO trigger level, causing the host to suspend transmission. The UART will then transmit the programmed XON-1,2 characters as soon as the received data reaches the next lowest trigger level, thus causing the host to resume transmission (received data trigger levels are 8, 16, 56, and 60).

When single XON/XOFF characters are selected, the UART compares the received data to these values and controls the transmission accordingly (XON=restart transmission, XOFF=suspend transmission). These characters are not stacked in the data buffer or FIFO. When the *ANY* XON function is enabled (MCR bit 5 is set), the UART will automatically resume transmission after receiving *ANY* character after having recognized XOFF and suspended transmission. Note that the UART will automatically transmit the XON character(s) after the flow control function is disabled, if the XOFF character(s) had been sent prior to disabling the software flow control function. Special cases are provided to detect the special character and stack it into the data buffer or FIFO and these conditions are configured via bits 0-3 of the Enhanced Feature Register (EFR).

Programming Example

The following example will demonstrate data transfer between one channel of the host IP521 and another node. Both nodes will use the FIFO Mode of operation with a FIFO threshold set at 60 bytes. The data format will use 8-bit characters, odd-parity, and 1 stop bit.

Please refer to Table 3.1 for address locations. The "H" following data below refers to the Hexadecimal format.

1. Write 80H to the Line Control Register (LCR).

   This sets the Divisor Latch Access bit to permit access to the two divisor latch bytes used to set the baud rate. These bytes share addresses with the Receive and Transmit buffers, and the Interrupt Enable Register (IER).

2. Write 00H to the Divisor Latch MSB (DLM). Write 60H to the Divisor Latch LSB (DLL).

   This sets the divisor to 96 for 9600 baud (i.e. 9600 = 14.7456MHz ÷ [16*96]).

3. Write 0BH to the Line Control Register (LCR).

   This first turns off the Divisor Latch Access bit to cause accesses to the Receiver and Transmit buffers and the Interrupt Enable Register. It also sets the word length to 8 bits, the number of stop bits to one, and enables odd-parity.

4. (OPTIONAL) Write xxH to the Scratch Pad Register.

   This has no effect on the operation, but is suggested to illustrate that this register can be used as a 1-byte memory cell. Optionally, this register is also used to store the interrupt vector for the port. A read of this register will be performed in response to an interrupt cycle.

5. Write 07H to the Interrupt Enable Register (IER).

   This is the first step to enable the receiver line status interrupt. Note bit-3 of the MCR must also be set to logic "1" to enable interrupts. The line status interrupt is used to signal error cases, such as parity or overrun errors. The received data available and transmit holding buffer empty interrupts have also been enabled to aide control by the host CPU in moving data back and forth.

6. Write C7H to the FIFO Control Register (FCR).

   This enables and initializes the transmit and receive FIFO's, and sets the trigger level of the receive FIFO interrupt to 60 bytes.

7. Read C1H from the Interrupt Status Register (ISR).

   This is done to check that the device has been programmed correctly. The upper nibble "C" indicates that the FIFO's have been enabled and the lower nibble "1" indicates that no interrupts are pending.

8. Write 0AH to the Modem Control Register (MCR).

   This enables interrupts and sets the Ready-To-Send bit and asserts the RTS* signal line. It is used to enable transmit data output for the port. Note the modem control lines, either input or output, have no effect on the parallel-to-serial output data or serial-to-parallel input data. These lines interact only through CPU control to provide the handshaking necessary for this data transfer protocol.

9. The host should begin writing data repeatedly to the Transmitter Holding Register.

   This loads the transmit FIFO and initiates transmission of serial data on the TxD line. The first serial byte will take about 100us to transmit, so it is likely that the transmit FIFO will fill before the first byte has been sent.

10. Read data repeatedly from the Receiver Buffer Register.

    After 60 bytes have been received (or fewer bytes with a timeout), an interrupt will be generated. INTREQ0* will go active to signal the host CPU that it can begin reading the receive FIFO.

11 The host should acknowledge the interrupt

   To acknowledge and clear it, an interrupt select cycle should be executed. Then begin reading the receive FIFO data.

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4.0 THEORY OF OPERATION

This section contains information regarding theTIA/EIA-422B serial data interface. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-713 as you review this material.

EIA/TIA-422B SERIAL INTERFACE

The Electronic Industries Association (EIA) in conjunction with the Telecommunication Industries Association (TIA) introduced TIA/EIA-422B as a balanced (differential) serial data transmission interface standard between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). By definition, DTE is commonly used to represent the data source, data sink, or both. DCE is used to represent the devices used to establish, maintain, and terminate a connection, and to code/decode the signals between the DTE and the transmission channel. Most computers are considered DTE devices, while modems are DCE devices.

The EIA/TIA-422B interface is the second revision of this standard and specifies a balanced driver with balanced receivers. Balanced data transmission refers to the fact that only two conductors are switched per signal and the logical state of the data is referenced by the difference in potential between the two conductors, not with respect to signal ground. The differential method of data transmission makes EIA-422B ideal for noisy environments since it minimizes the effects of coupled noise and ground potential differences. That is, since these effects are seen as common-mode voltages (common to both lines), not differential, they are rejected by the receivers. Additionally, balanced drivers have generally faster transition times and allow operation at higher data rates over longer distances.

The EIA/TIA-422B standard defines a unidirectional, terminated, single driver and multiple receiver configuration. By providing a separate data path for transmit and receive, full-duplex operation is accomplished. The maximum data transmission cable length is generally limited to 4000 feet without a signal repeater installed.

EIA/TIA-422B is electrically similar to EIA-485, except that EIA-485 supports multiple driver operation. Consequently, this board may be used to implement a full-duplex EIA-485 interface (see Drawing 4501-714). However, for true half-duplex EIA-485 operation, please see the Acromag Model IP502.

With respect to EIA/TIA-422B, logic states are represented by differential voltages from 2V to 10V. The polarity of the differential voltage determines the logical state. A logic 0 (the ‘space’ or OFF state) is represented by a positive differential voltage between the terminals (measured A to B, or + to -). A logic 1 (the ‘mark’ or ON state) is represented by a negative differential voltage between the terminals (measured A to B, or + to -). Note that at the interface, a logic ‘0’ is represented by a positive voltage, and a logic ‘1’ by a negative voltage. The line receivers convert these signals to the conventional TTL level associations.

EIA/TIA-422B	BINARY 0 (SPACE/OFF)	BINARY 1 (MARK/ON)
SIGNAL A to B (+) to (-)	Positive Differential Voltage	Negative Differential Voltage

Start and stop bits are used to synchronize the DCE to the asynchronous serial data of the DTE. The transmit data line is normally held in the mark state (logical 1). The transmission of a data byte requires that a start bit (a logical 0 or a transition from mark to space) be sent first. This tells the receiver that the next bit is a data bit. The data bits are followed by a stop bit (a logical 1 or a return to the mark state). The stop bit tells the receiver that a complete byte has been received. Thus, 10 bits make up a data byte if the data character is 8 bits long (and no parity is assumed). Nine bits are required if only standard ASCII data is being transmitted
(1 start bit + 7 data bits + 1 stop bit). The character size for this module is programmable between 5 and 8 bits.

Parity is a method of judging the integrity of the data. Odd, even, or no parity may be configured for this module. If parity is selected, then the parity bit precedes transmission of the stop bit. The parity bit is a 0 or 1 bit appended to the data to make the total number of 1 bits in a byte even or odd. Parity is not normally used with 8-bit data. Even parity specifies that an even number of logical 1’s be transmitted. Thus, if the data byte has an odd number of 1’s, then the parity bit is set to 1 to make the parity of the entire character even. Likewise, if the transmitted data has an even number of 1’s, then the parity bit is set to 0 to maintain even parity. Odd parity works the same way using an odd number of logical 1’s.

Thus, both the DTE & DCE must have the same parity. If a byte is received that has the wrong parity, an error is assumed and the sending system is typically requested to retransmit the byte. Two other parity formats not supported by this module are mark and space parity. Mark parity specifies that the parity bit will always be a logical 1, space parity requires that the parity bit will always be 0.

The most common asynchronous serial data format is 1 start bit, 8 data bits, and 1 stop bit, with no parity. The following table summarizes the available data formats:

START BIT	Binary 0 (a shift from “Mark” to “Space”)
DATA BITS	5,6,7, or 8 Bits
PARITY	Odd, Even, Stick, or None
STOP BIT	Binary 1 (1, 1-1/2, or 2 Bit times)

With start, stop, and parity in mind, for an asynchronous data byte, note that at least one bit will be a 1 (the stop bit). This defines the break signal (all 0 bits with a 1 stop bit lasting longer than one character). A break signal is a transfer from “mark” to “space” that lasts longer than the time it takes to transfer one character. Because the break signal doesn’t contain any logical 1’s, it cannot be mistaken for data. Typically, whenever a break signal is detected, the receiver will interpret whatever follows as a command rather than data. The break signal is used whenever normal signal processing must be interrupted. In the case of a modem, it will usually precede a modem control command. Do not confuse the break signal with the ASCII Null character, since a break signal is longer than one character time. That is, it is any

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"space" condition on the line that lasts longer than a single character (including its framing bits) and is usually 1-1/2 to 2 character times long.

The baud rate is a unit of transmission speed equal to the number of electrical signals (signal level changes) sent on a line in one second. It is thus, the electrical signaling rate or frequency at which electrical impulses are transmitted on a communication line. The baud rate is commonly confused with the bit transfer rate (bits-per-second), but baud rate does not equate to the number of bits transmitted per second unless one bit is sent per electrical signal. However, one electrical signal (change in signal level) may contain more than one bit (as is the case with most phone modems). While bits-per-second (bps) refers to the actual number of bits transmitted in one second, the baud rate refers to the number of signal level changes that may occur in one second. Thus, 2400 baud does not equal 2400 bits per second unless 1 bit is sent per electrical signal. Likewise, a 1200bps or 2400bps modem operates at a signaling rate of only 600 baud since they encode 2 and 4 bits, respectively, in one electrical impulse (through amplitude, phase, and frequency modulation techniques). However, for this device, the baud rate is considered equivalent to the bit rate.

Pins 1-40 of the field I/O connector P2 provide connectivity to serial Ports A-H of this module (Refer to Table 2.1 for pin assignments). Note that a suffix of '_A', '_B', '_C', to '_H' is appended to the signal names to indicate their port association. The receive and transmit signals are described in detail below.

EIA/TIA-422B Signal Descriptions

SIGNAL	DESCRIPTION
RxD_A RxD_B to RxD_H	Receive Data Line (DCE-to-DTE) - This is the receive data line from the modem to the DTE. The signals on this line are in serial form. For data to be received the DTR signal is used to enable the receiver of the port.
TxD_A TxD_B to TxD_H	Transmit Data Line (DTE-to-DCE) - This is the transmit data line from the DTE to the modem. When no data is being transmitted, the signal line is held in the mark state. For data to be transmitted RTS must all be in the on state (asserted).

An Asterisk (*) is used to indicate an active-low signal.

IP521 OPERATION

Connection to each serial port is provided through connector P2 (refer to Table 2.1). These pins are tied to the inputs and outputs of EIA/TIA-422B line receivers and drivers. The function of the line receivers is to convert the required EIA/TIA-422B signals to the TTL levels required by the UART (Universal Asynchronous Receiver/Transmitter). The line drivers convert the UART TTL levels to the EIA/TIA-422B voltage levels. The UART provides the necessary conversion from serial-to-parallel (receive) and parallel-to-serial (transmit) for interfacing to the data bus. Additionally, it provides data buffering and data formatting capabilities. A programmable logic device is used to control the interface between the UART and the IP bus.

Note that the field serial interface to the carrier board provided through connector P2 (refer to Table 2.1) is NON-ISOLATED. This means that the field signal return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause errors in operation, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-714 for example communication wiring connections.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V to power the module.

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces and produces the chip selects, control signals, and timing required by the communication registers, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also prioritizes the serving of port interrupts.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Application Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

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6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration..... Single Industrial Pack Module.
- Length..... 3.880 in. (98.5 mm).
- Width..... 1.780 in. (45.2 mm).
- Board Thickness..... 0.062 in. (1.59 mm).
- Max Component Height..... 0.290 in. (7.37 mm).

Connectors:
- P1 (IP Logic Interface)..... 50-pin female receptacle header (AMP 173279-3 or equivalent).
- P2 (Field I/O)..... 50-pin female receptacle header (AMP 173279-3 or equivalent).

Power:
- +5 Volts (±5%)..... 285mA, Typical 340mA Maximum.

ENVIRONMENTAL

Operating Temperature..... Standard Unit 0 to +70°C. "E" suffixed units -40°C to +85°C.

Relative Humidity..... 5-95% Non-Condensing.

Storage Temperature..... -55°C to 125°C.

Non-Isolated..... Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI).. Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1.

Electromagnetic Interference Immunity (EMI)..... There shall be no loss of functionality (occasional corruption of communication packets is permitted) under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge (ESD) Immunity..... Complies with IEC1000-4-2, Level 3 (8KV/4KV air/direct discharge) to the enclosure port and European Norm EN50082-1.

Surge Immunity..... Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity EFT..... Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions..... Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

UART

EXAR..... XR16C654

RS422/RS485 PORTS

Channel Configuration..... Eight independent, non-isolated EIA/TIA-422B serial ports with a common signal return connection.

Data Rate..... 921.6K bits/sec, Maximum. (Limited by 14.7456MHz crystal).

Interface..... Asynchronous serial only.

Cable Length..... 4000 feet (1200M), typical

Character Size..... Software Programmable 5 to 8 bits.

Parity..... Software Programmable odd, even, or no parity.

Stop Bits..... Software Programmable 1, 1-1/2, or 2 bits.

Data Register Buffers..... The data registers are double buffered (16C450 mode), or 64-byte FIFO buffered (FIFO mode).

Interrupts..... Receiver Line Status Interrupt (i.e. Overrun, Parity, or Framing error, or Break Interrupt); Received/Transmit FIFO level reached or Character Time-Out; or Xon/Xoff/Special Character Detect.

Termination Resistors..... 120Ω Termination Resistors are installed in sockets on the module and may be removed if required (see Drawing 4501-715 for location). For an RS422 network install a terminating resistor at the end of the network only. For an RS422/RS485 network, transmitting and receiving channels may have terminating resistors (RT) at both ends of the network (see interface Drawing 4501-714).

Bias Resistor..... 560Ω pullup to +5V on (+) output lines, 560Ω pull-down to GND on (-) lines, installed in sockets on board and may be removed if required (see Drawing 4501-715 for location).

RS422/RS485 Transmitter Outputs

Differential Output..... 2.0V Minimum (Loaded 50Ω).

Common-Mode Output Voltage 3V Max

Propagation Delay ..... 60ns Max, R_{DIFF} = 54Ω, C_L = 100pF

Driver Rise and Fall Time..... 40ns Max, R_{DIFF} = 54Ω, C_L = 100pF

RS422/RS485 Receiver Inputs

Data Rate..... Up to 2.5 Mbps.

Input Voltage Range..... -8V to +12.5V DC Maximum.

Input High Threshold..... 2..0V Minimum

Input Low Threshold..... 0.8V Maximum

Input Resistance..... 12KΩ.

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INDUSTRIAL I/O PACK COMPLIANCE

Specification..... This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz operation for Type I Modules.
Electrical/Mechanical Interface..... Single-Size IP Module.
I/O Space..... 16-bit, 8-bit:
ID Space..... 16-bit, 8-bit; Supports Type 1, 32 bytes per IP (consecutive odd byte addresses).
Memory Space..... Not Used.
Interrupts..... Generates INTREQ0* interrupt request per IP and interrupt acknowledge cycles via access to IP INT space. 8-bit read of Scratch Pad/Interrupt Vector Register contents.
Access Times (8MHz Clock):
ID Space Read..... 0 wait state (250ns cycle).
Channel Registers Read..... 1 wait state (375ns cycle).
Channel Registers Write..... 1 wait state (375ns cycle).
Interrupt Registers Read..... 2 wait states (500ns cycle).
Interrupt Registers Write..... 2 wait states (500ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

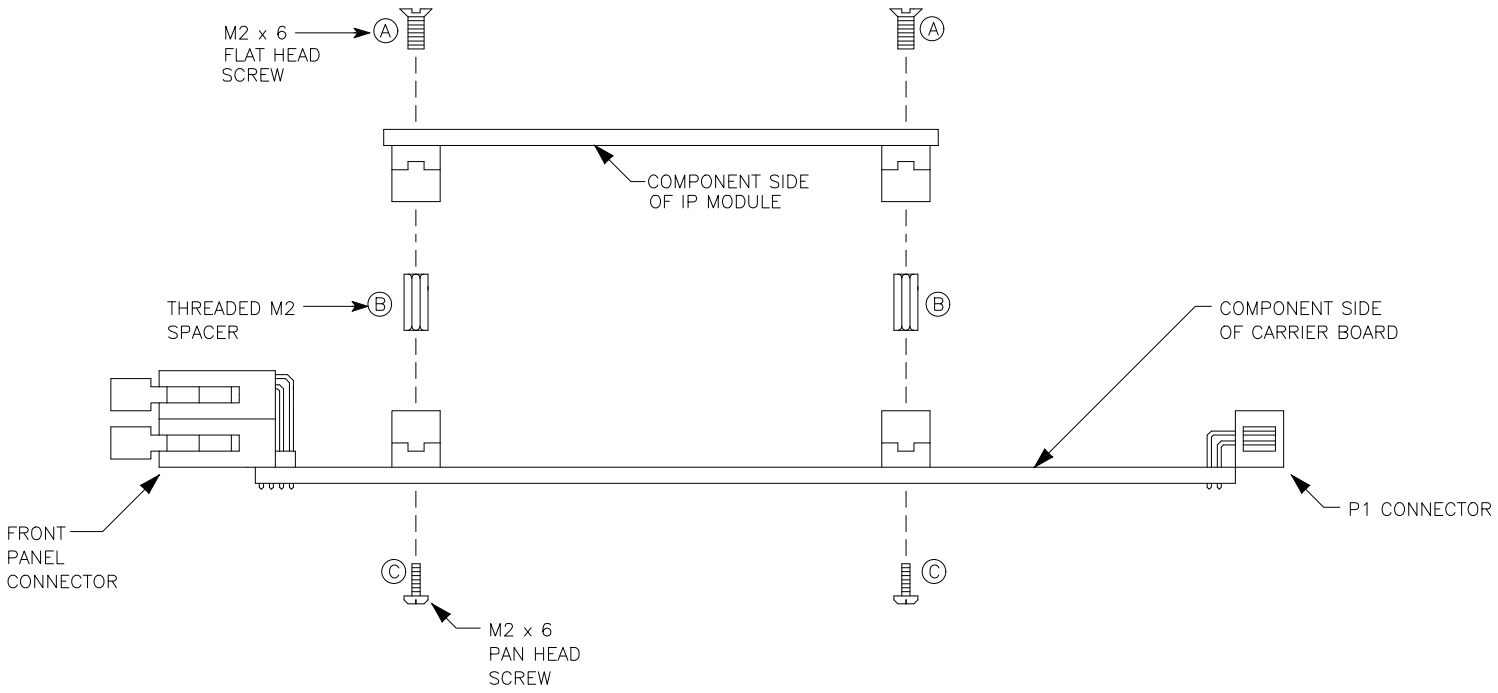
TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660, APC8610, or APC8620 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U, APC8610, or APC8620 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660, APC8610, or APC8620: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.

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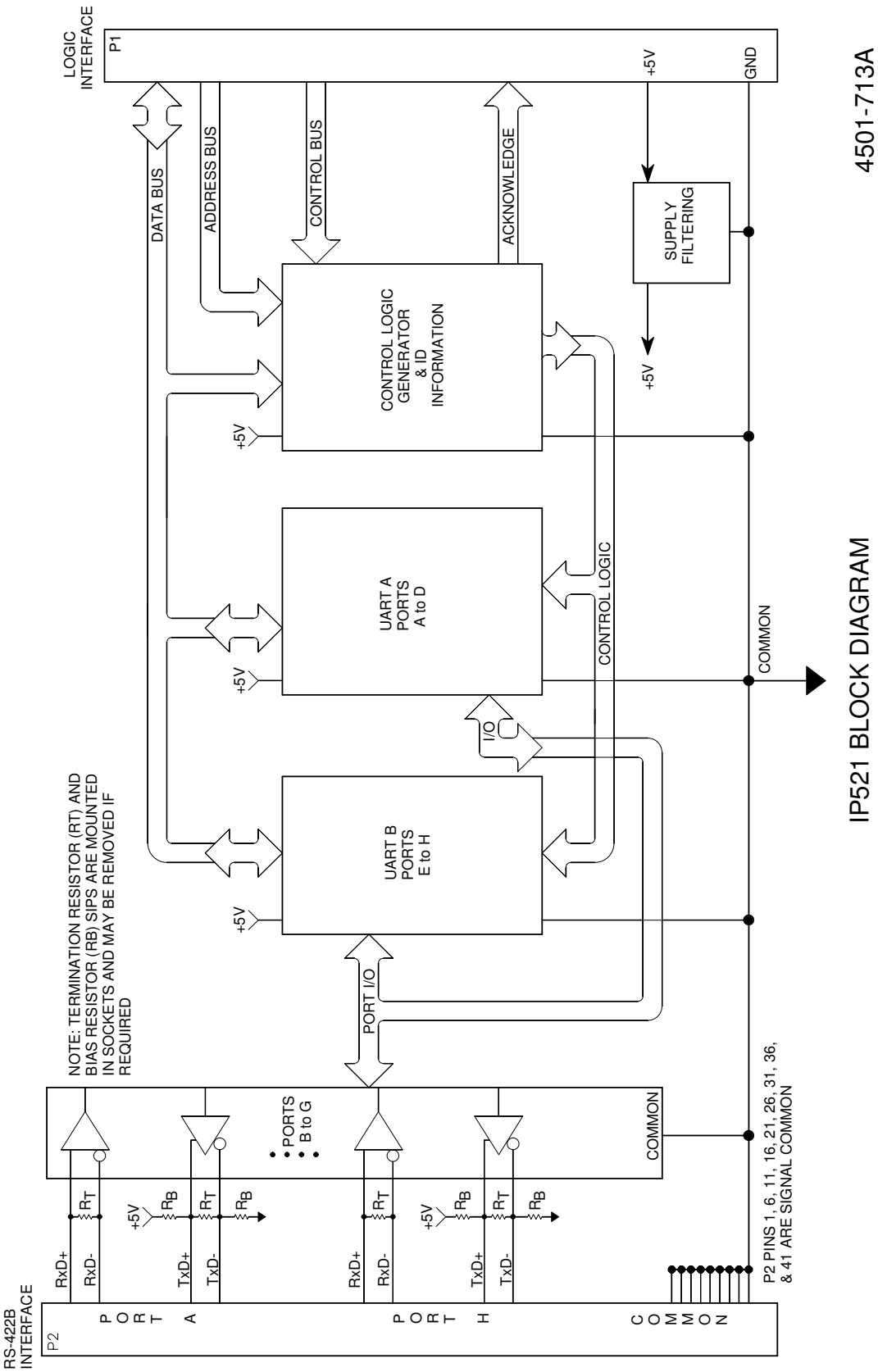
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

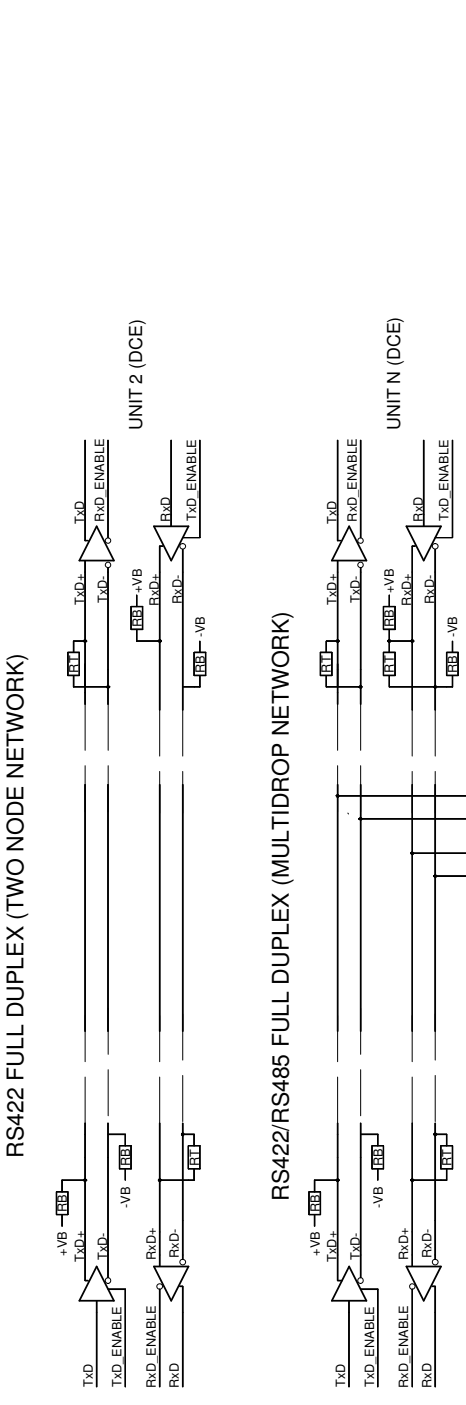
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434C

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NOTES CONCERNING RESISTOR PLACEMENT AND REMOVAL FOR RT AND RB:

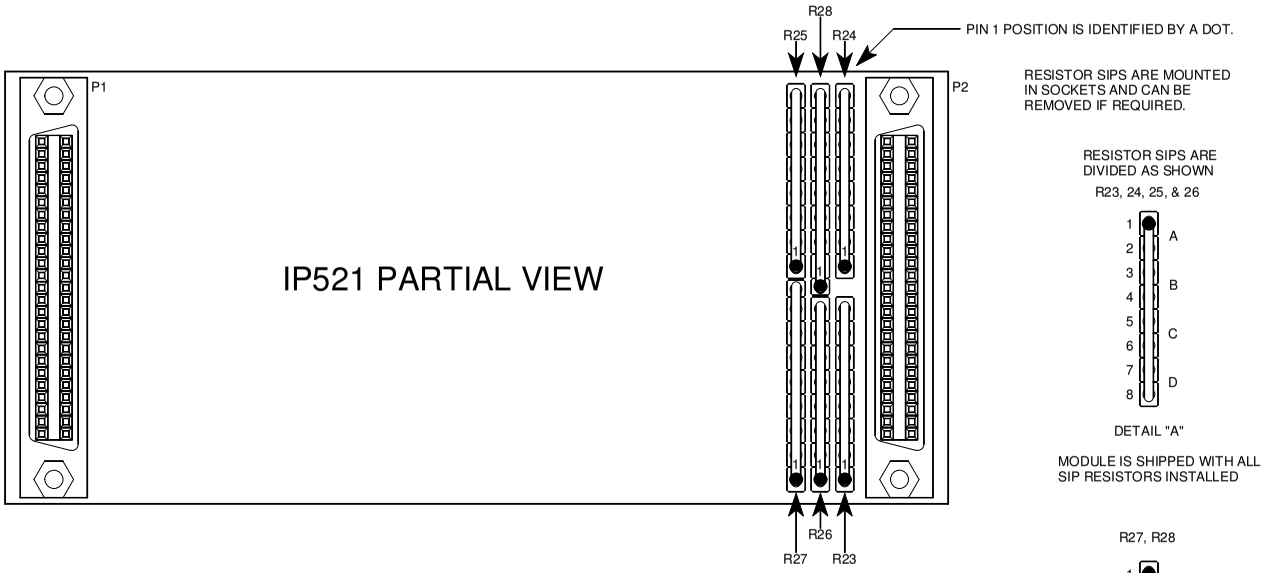
1. FOR AN RS422 NETWORK, INSTALL A TERMINATING RESISTOR AT THE RECEIVING END OF THE NETWORK ONLY
2. ALL RS422/RS485 TRANSMITTING AND RECEIVING CHANNELS MAY HAVE TERMINATING RESISTORS (RT) AT BOTH ENDS OF THE NETWORK. THE IP521 HAS THESE RESISTORS (120 OHM) INSTALLED IN SOCKETS AND THEY MAY BE REMOVED AS REQUIRED.
3. THERE MUST BE AT MOST, ONE SET OF BIAS RESISTORS ASSOCIATED WITH EACH PAIR OF SIGNAL WIRES TO KEEP THE NETWORK FROM FLOATING WHEN NO UNITS ARE TRANSMITTING.
4. THE TxD LINE SOURCED FROM A PORT CAN BE PERMANENTLY ENABLED VIA SOFTWARE. IF SO, THE NETWORK BIAS RESISTORS ASSOCIATED WITH EACH PAIR OF SIGNAL WIRES WILL NOT BE NEEDED. THESE RESISTORS ARE INSTALLED IN SOCKETS AND CAN BE REMOVED IF THESE DRIVERS ARE ALWAYS ENABLED.
5. THE IDLE STATE OF THE TxD & RxD DATA PAIRS ARE HIGH ON TxD+ & RxD+. THIS CORRESPONDS TO A MARK (1) ON THE DATA LINE.
6. RS-422 IS CONSIDERED A BALANCED (DIFFERENTIAL) TRANSMISSION STANDARD BECAUSE THE VOLTAGE OF ONE SIGNAL LINE IS TAKEN WITH RESPECT TO ANOTHER TO DETERMINE THE SIGNAL LEVEL.

IP521 RS-422/485 INTERFACE DIAGRAM

4501-714A

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IP521 TERMINATION AND BIAS SIP RESISTOR LOCATION DRAWING FOR REMOVAL AND REPLACEMENT WHERE REQUIRED (SEE DRAWING 4501-714)



NOTES CONCERNING RESISTOR PLACEMENT AND REMOVAL:

1. ALL TRANSMITTING AND RECEIVING CHANNELS MAY HAVE TERMINATING RESISTORS (RT) AT BOTH ENDS OF THE NETWORK. THE IP521 HAS USER-REMOVEABLE PLUG-IN SIP TERMINATION RESISTORS (120 OHM).

2. THERE MUST BE AT MOST, ONE SET OF BIAS RESISTORS ASSOCIATED WITH EACH PAIR OF SIGNAL WIRES TO KEEP THE NETWORK FROM FLOATING WHEN NO UNITS ARE TRANSMITTING.

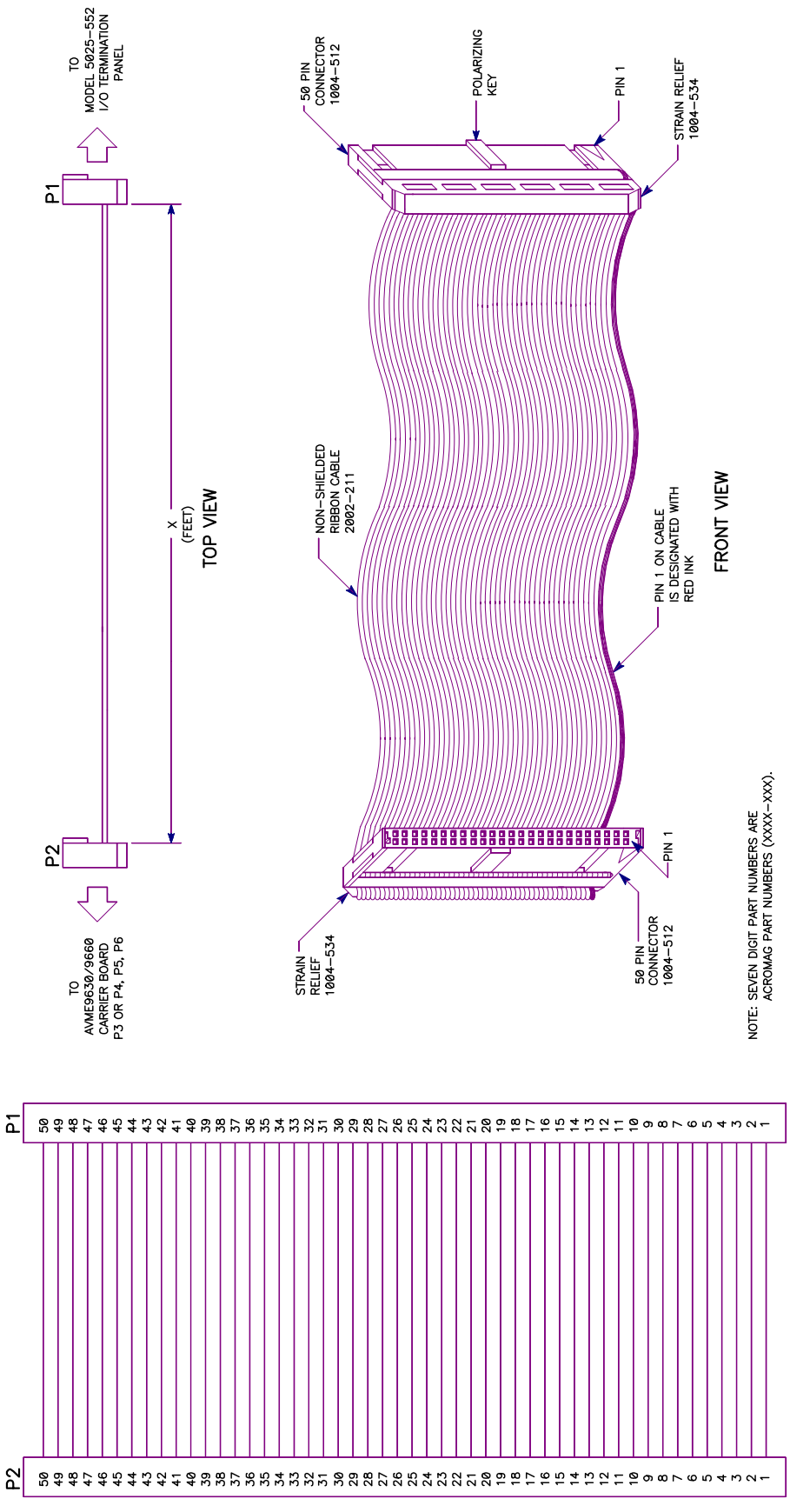
3. THE TxD AND RTS LINES SOURCED FROM A PORT CAN BE ENABLED VIA SOFTWARE. IF SO, THE NETWORK BIAS RESISTORS ASSOCIATED WITH EACH PAIR OF SIGNAL WIRES WILL NOT BE NEEDED. THESE RESISTORS ARE INSTALLED IN SOCKETS AND CAN BE REMOVED IF THESE DRIVERS ARE ALWAYS ENABLED.

RESISTOR IDENTIFICATION

SIP	VALUE	FUNCTION	PORT	
R23:A	120 OHM	TxD-A TERMINATION	PORT A	TERMINATION
R23:B	120 OHM	RxD-A TERMINATION	PORT A	
R23:C	120 OHM	TxD-B TERMINATION	PORT B	
R23:D	120 OHM	RxD-B TERMINATION	PORT B	
R24:A	120 OHM	TxD-D TERMINATION	PORT D	
R24:B	120 OHM	RxD-D TERMINATION	PORT D	
R24:C	120 OHM	TxD-E TERMINATION	PORT E	
R24:D	120 OHM	RxD-E TERMINATION	PORT E	
R25:A	120 OHM	TxD-H TERMINATION	PORT H	
R25:B	120 OHM	RxD-H TERMINATION	PORT H	
R25:C	120 OHM	TxD-C TERMINATION	PORT C	
R25:D	120 OHM	RxD-C TERMINATION	PORT C	
R26:A	120 OHM	TxD-F TERMINATION	PORT F	
R26:B	120 OHM	RxD-F TERMINATION	PORT F	
R26:C	120 OHM	TxD-G TERMINATION	PORT G	
R26:D	120 OHM	RxD-G TERMINATION	PORT G	
R27:A	560 OHM	TxD-A+ BIAS +5V	PORT A	+5V AND GND BIAS
R27:B	560 OHM	TxD-F+ BIAS +5V	PORT F	
R27:C	560 OHM	TxD-B+ BIAS +5V	PORT B	
R27:D	560 OHM	TxD-G+ BIAS +5V	PORT G	
R27:E	560 OHM	TxD-C+ BIAS +5V	PORT C	
R27:F	560 OHM	TxD-H+ BIAS +5V	PORT H	
R27:G	560 OHM	TxD-D+ BIAS +5V	PORT D	
R27:H	560 OHM	TxD-E+ BIAS +5V	PORT E	
R28:A	560 OHM	TxD-A- BIAS GND	PORT A	
R28:B	560 OHM	TxD-F- BIAS GND	PORT F	
R28:C	560 OHM	TxD-B- BIAS GND	PORT B	
R28:D	560 OHM	TxD-G- BIAS GND	PORT G	
R28:E	560 OHM	TxD-C- BIAS GND	PORT C	
R28:F	560 OHM	TxD-H- BIAS GND	PORT H	
R28:G	560 OHM	TxD-D- BIAS GND	PORT D	
R28:H	560 OHM	TxD-E- BIAS GND	PORT E	

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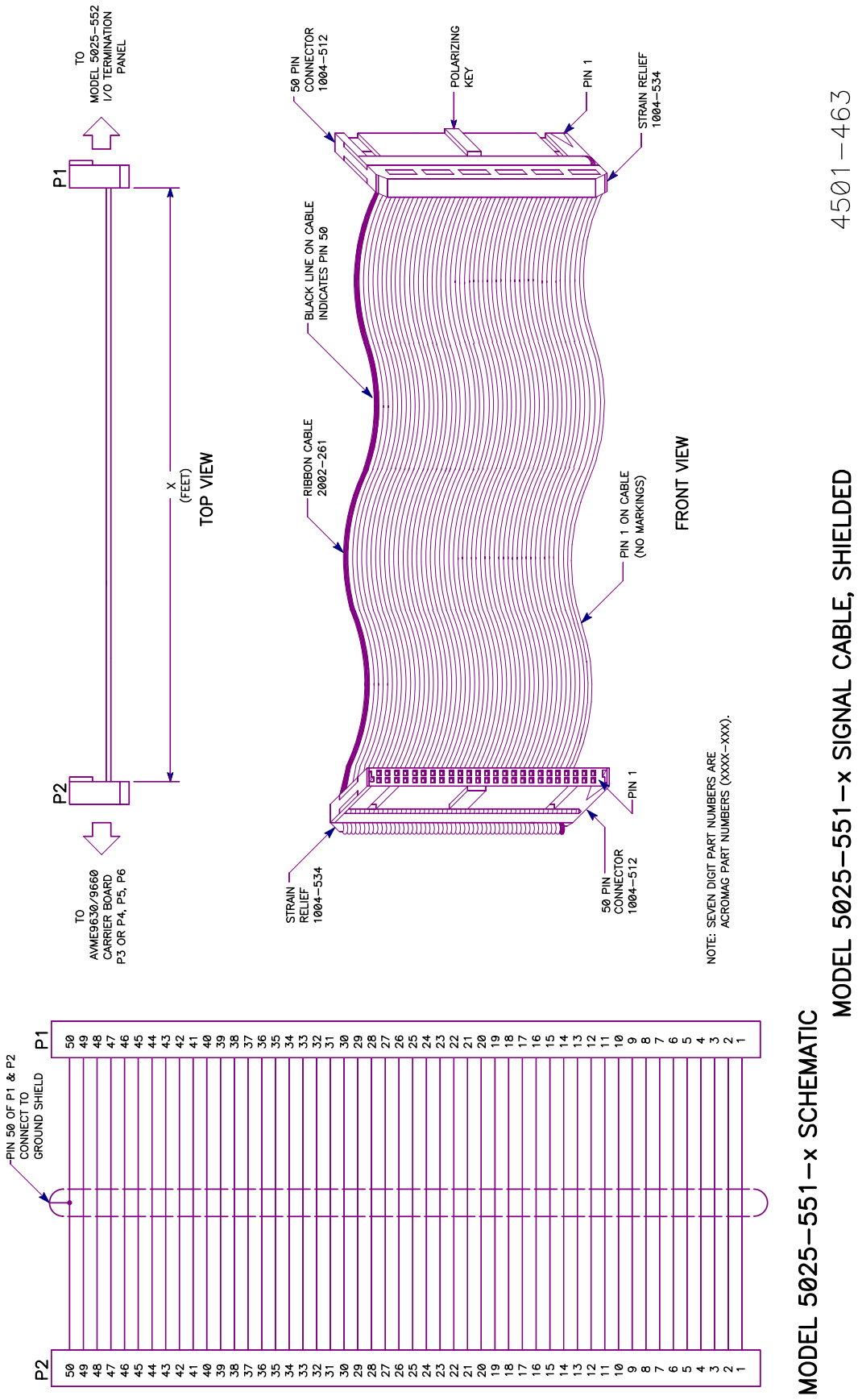


MODEL 5025-550-x SCHEMATIC

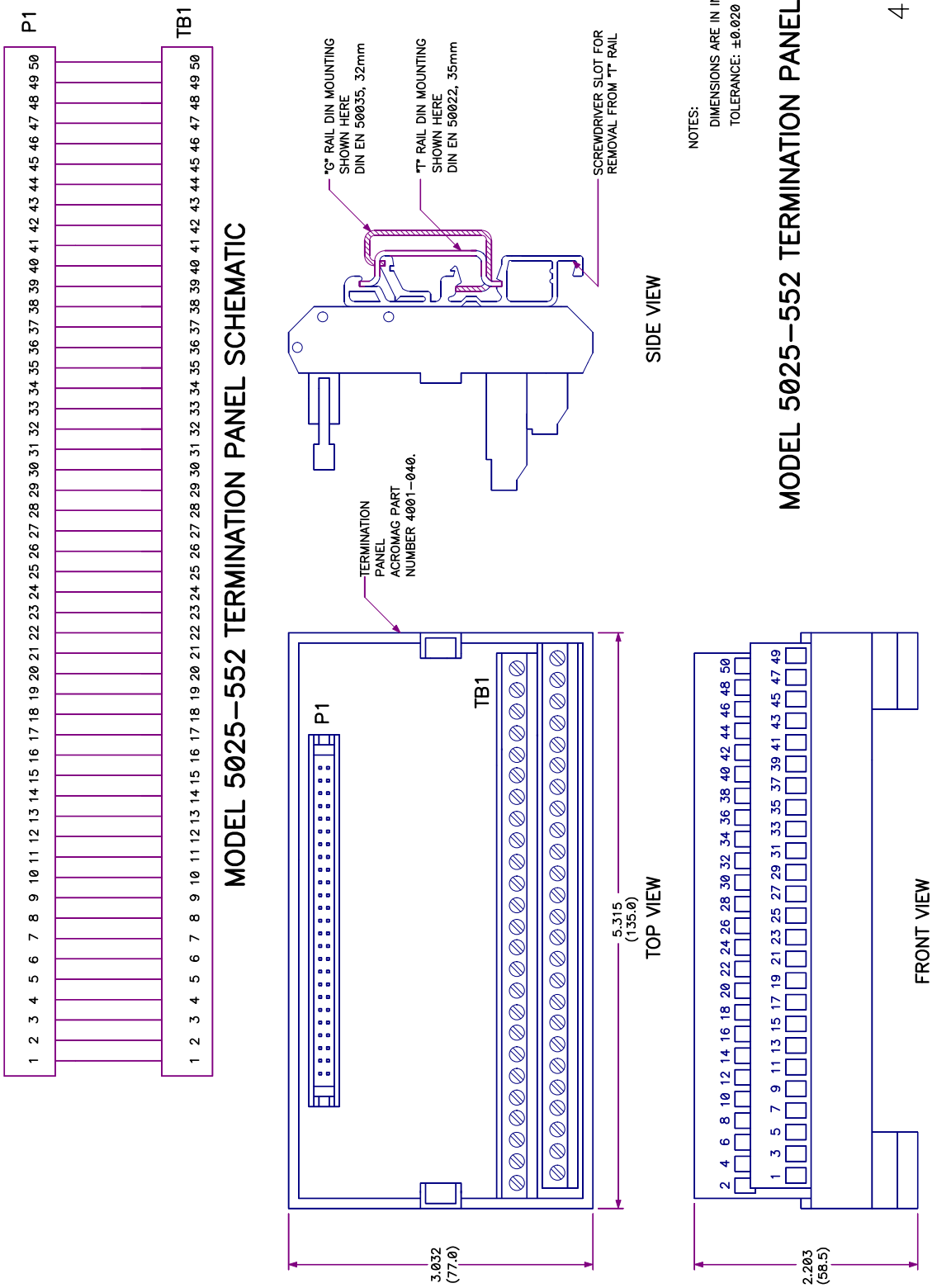
MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

4501-462

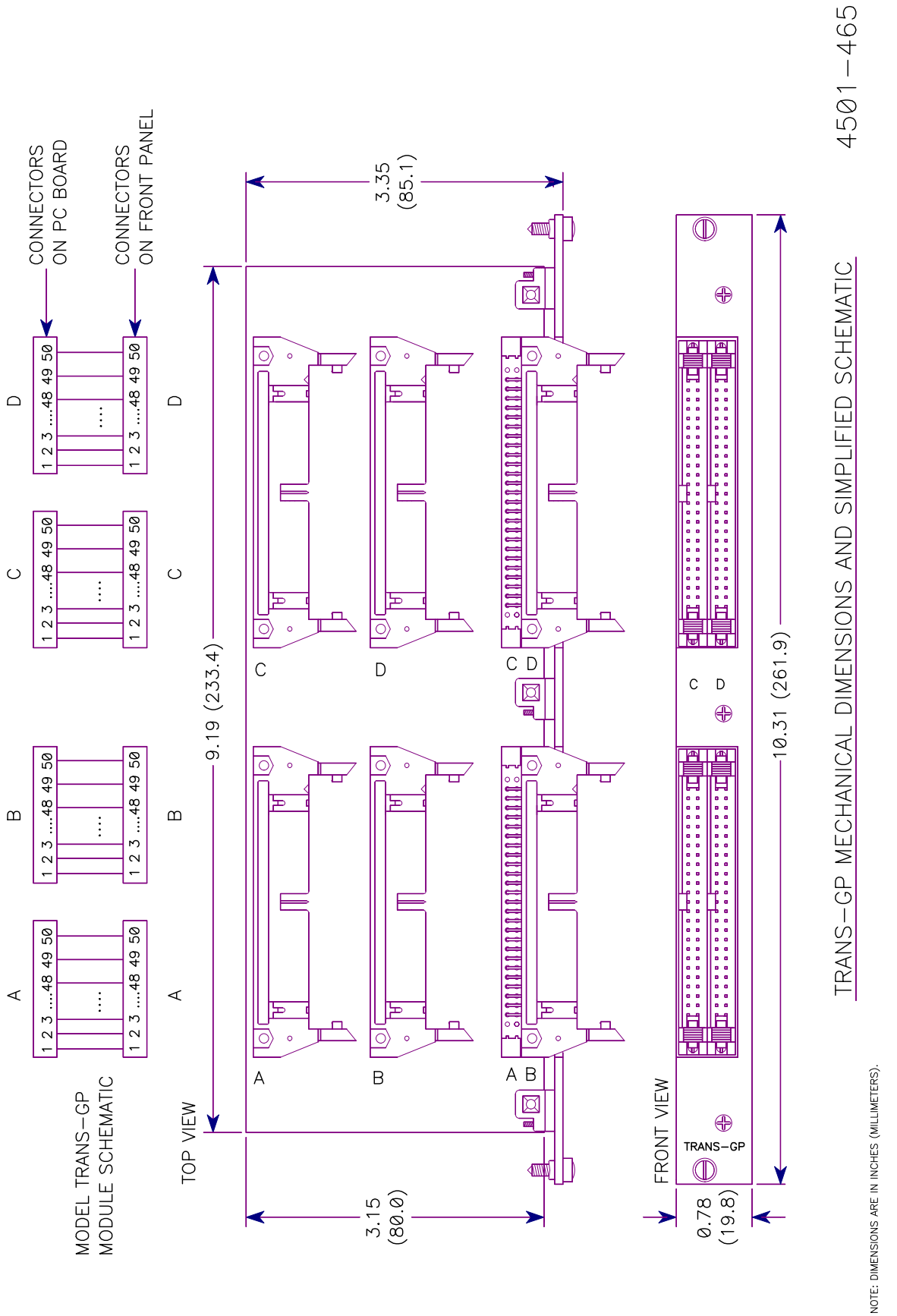
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