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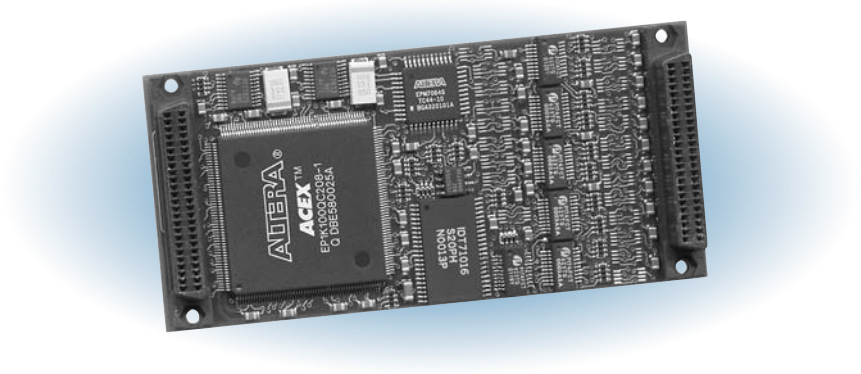
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Find the *Acromag IP-1K100-0024* at our website: ***Click HERE***

IP-1K100 User-Programmable FPGA Modules



These modules support adaptive computing applications with an FPGA running custom programs to control system communication.

This series of plug-in mezzanine modules provides a user-customizable FPGA on an Industry Pack (IP) module. The module allows users to develop and store their own instruction set in the FPGA for adaptive computing applications. Typical uses include specialized communication systems over EIA-422/485 networks, test fixture simulation of signals over TTL-switched lines, and analysis of acquired data using specialized mathematical formulas such as those developed with MathWorks's MatLab® software.

The FPGA on Acromag's IP-1K100 modules can control up to 48 TTL or 24 EIA-485 I/O signals or a mix of both types. User application programs are downloaded through the IP bus directly into the FPGA. A pre-programmed internal CPLD facilitates initialization by acting as the bus controller during power-up and while the program is downloading. This bus controller is limited to functions necessary for power-up and downloading. After the program downloads, the FPGA takes control of the IP bus and the CPLD is disabled.

Features

- Altera® EP1K100 FPGA
- Three models available:
  IP-1K100-0024: 24 differential EIA-485 lines
  IP-1K100-2412: 24 TTL lines and 12 EIA-485
  IP-1K100-4800: 48 TTL lines
- FPGA programmable via the IP bus
- Local static RAM (64K x 16) under FPGA control
- Programmable PLL-based clock synthesizer
- Supports 8MHz and 32MHz IP bus
- User-programmable interval timer
- Example FPGA design code provided as VHDL
  - 8MHz IP bus interface
  - Digital I/O control register
  - others
- Hardware support for DMA and memory space

Specifications

FPGA

FPGA: Altera EP1K100.

FPGA configuration: Downloadable via IP bus.

Clock: Programmable PLL-based clock synthesizer.

Input/output signals:
IP-1K100-0024: 24 differential EIA-485 lines
IP-1K100-2412: 24 TTL lines and 12 EIA-485
IP-1K100-4800: 48 TTL lines

IP bus clock frequency: Supports 8 and 32MHz clocks.

ID space: 8-bit data.

I/O space: 8 or 16-bit data.

Memory space: Wired to FPGA but not supported with example FPGA design firmware.

Interrupt support: Two IP request levels.

DMA support: Wired to FPGA but not supported with example FPGA design firmware.

IP logic interface: EPLD maintains ID space and two locations in IO space for FPGA configuration. Remaining IO space and INT space are defined by the configured FPGA.

Example FPGA program: VHDL provided implements IP bus interface to IO, ID, and INT space. Requires user proficiency with VHDL and Altera MAX+PLUS® II or Quartus® software tools. See Engineering Design Kit.

IP Compliance (ANSI/VITA 4)

Meets IP specifications per ANSI/VITA 4-1995.

IP data transfer cycle types supported: Input/output (IOSel*), ID read (IDSel*), Interrupt select (INTSel*).

Access times (8MHz or 32MHz clock):
ID space read: 0 wait states (250ns cycle).
Registers read/write: 1 wait states (500ns cycle).
Interrupt read/write: 0 wait states (250ns cycle).

Environmental

Operating temperature: 0 to 70°C.

Storage temperature: -55 to 125°C.

Relative humidity: 5 to 95% noncondensing.

MTBF: 5,554,167 hrs. at 25°C, MIL-HDBK-217F, notice 2

Engineering Design Kit

Engineering Design Kit: Provides user with basic information required to develop a custom FPGA program for download to the Altera FPGA. This kit must be ordered with the first purchase of a IP-1K100.
Kit on CD-ROM includes:
Schematics (.pdf)
Parts List (.pdf)
Part Location drawing (.pdf)
Example VHDL Source File (.vhd)
Example Pin Definition File (.acf)
Example VHDL Object code (.hex)
Readme file (.txt)

Only one Design Kit purchase is required. User should be fluent in the use of Altera MAX+PLUS or Quartus design tools. Additionally, user should also purchase either the IPSW-API-VXW (VxWorks source code library) or the IPSW-ATX-PCI (ActiveX driver package). These programs include important driver support programs to assist in transferring developed code between user's processor and Altera 1K100.

Ordering Information

Industry Pack Modules

IP-1K100-0024
24 differential EIA-485 lines

IP-1K100-2412
24 TTL lines and 12 EIA-485

IP-1K100-4800
48 TTL lines

IP-1K100-EDK
Engineering Design Kit (one kit required)

For Industry Pack Carrier Cards, see Page 5.

Software*

IPSW-API-VXW: VxWorks® software support package

IPSW-API-QNX: QNX® software support package

IPSW-ATX-PCI: ActiveX®/OLE Controls 2.0 software package

IPSW-LINUX: Linux support (website download only)

** For software information, see Page 65.*
For accessories information, see Page 71.

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