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Series IP-EP201/202/203/204 Industrial I/O Pack
Cyclone II Based Reconfigurable FPGA
Digital I/O Modules

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS
You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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RELATED PUBLICATIONS

The following manuals and part specifications provide the necessary information for in depth understanding of the IP-EP2 Series board.

IP-EP2 FPGA Programming Guide	**Acromag IP-EP2-EDK**
71V016SA SRAM Specifications	**http://www.idt.com**
Cyclone II Data Book	**http://www.altera.com**
CY22150 Specification	**http://www.cypress.com**
IP Specification ANSI/VITA 4-1995	**http://www.vita.com**

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1.0 GENERAL INFORMATION

The Industrial I/O Pack EP2 Series module is a reconfigurable digital input/output board. The modules use an Altera Cyclone II® Field Programmable Gate Array (FPGA). This allows designers to implement logic functions unique to their application. Furthermore, the FPGA can be configured in-system using either the industry-standard JTAG interface or directly through the IP bus.

An example Altera FPGA configuration file and its corresponding VHDL source are provided with the IP-EP2 Series Engineering Design Kit. The example design includes an IP bus interface to ID space, IO space and Interrupt space. IO space is used to access a 64K x 16 RAM array, control field data I/O, and configure a clock generation chip. To take advantage of the example VHDL program, the user must be proficient in the use of VHDL and the Altera Quartus II software tools.

The IP-EP2 Series provides several different interface options which allow a mix of differential digital and TTL digital input/output channels. The models and their corresponding combination of channels are given in the table below. All models use the EP2C20 Cyclone II FGPA.

Table 1.1: *The IP-EP2 Series models.*

MODEL	TTL Channels	EIA-485/422 Channels	LVDS Channels	Operating Temperature Range
IP-EP201	48	0	0	0 to 70°C
IP-EP201E	48	0	0	-40 to 85°C
IP-EP202	0	24	0	0 to 70°C
IP-EP202E	0	24	0	-40 to 85°C
IP-EP203	24	12	0	0 to 70°C
IP-EP203E	24	12	0	-40 to 85°C
IP-EP204	0	0	24	0 to 70°C
IP-EP204E	0	0	24	-40 to 85°C

KEY FEATURES

- **Reconfigurable Altera FPGA** – In system configuration of the FPGA is implemented via a standard JTAG interface or the IP bus. This provides a means for implementation of custom user defined designs.
- **High Channel Count Digital Interface** – RS485, LVDS and TTL interface options are available. Models with up to 24 RS485, 24 LVDS, a mix of 12 RS485 and 24 TTL, or up to 48 TTL digital input/output channels are available.
- **External Clock** – An LVTTL external clock input is available on all models. The external clock is connected directly to a global clock pin on the Altera FPGA.
- **5V Tolerance** – All TTL I/O are 5V tolerant.
- **Channel Input/Output Control** – The direction of the TTL digital channels is controlled in groups of 8 channels. The direction of the differential digital signals is controlled in groups of 4 channels.
- **Long Distance Data Transmission** – Data transmission with RS485/RS422 Transceivers allow up to 32 nodes and up to 4000 feet of transmission cable.

KEY FEATURES

- **64K x 16 SRAM –** A 64K x 16 static random access memory (SRAM) is directly accessed by the Altera device. Custom user defined design logic for the Altera FPGA will permit use of the SRAM as FIFO memory, or single port memory as required by the application.
- **Example Design Provided –** An example VHDL design which includes implementation of the IP bus interface and control of digital I/O with software programmable Interrupts is provided.
- **Programmable Clock Generator –** A clock generator IC is provided for applications requiring a custom user specified clock frequency. The clock generator can be programmed to any desired frequency value between 250KHz and 100MHz.
- **Power Up & System Reset is Failsafe** – For safety, all channels are configured as inputs upon power-up and after a system reset.
- **Hardware Program Disable –** JTAG and IP bus reconfiguration of the FPGA can be hardware disabled by the removal of zero ohm resistors on the board.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **Clock Speed –** Supports an 8 or 32 MHz IP bus clock speed.
- **High density -** Single-size, industry-standard, IP module footprint. Up to four units may be mounted on a 6U VMEbus carrier board or five units may be mounted on a PCI carrier board.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID" space.
- **16-bit & 8-bit I/O** - Channel register Read/Write is performed through 16 bit or 8 bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states. For the supplied IP module example, wait states are minimized for all read and write operations (see specifications for detailed information).

SIGNAL INTERFACE PRODUCTS

Refer to the Appendix for more information about these products.

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9668 VMEbus, APC8620A/21A PCI bus, and ACPC8625/30/35 Compact PCI bus non-intelligent carrier boards). A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, represent some of the accessories available from Acromag. Each Acromag carrier has its own unique accessories. They are not all listed in this document. Consult your carrier board documentation for the correct interface product part numbers to ensure compatibility with your carrier board.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to all Acromag carriers (or other compatible carrier boards) via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

ENGINEERING DESIGN KIT

Acromag provides an engineering design kit for the IP-EP2 Series boards (sold separately), a "must buy" for first time IP-EP2 module purchasers. The design kit (model IP-EP2-EDK) provides the user with the basic information required to develop a custom FPGA program for download to the Altera FPGA. The design kit includes a CD containing: schematics, parts list, part location drawing, example VHDL source, and other utility files. The IP-EP2 modules are intended for users fluent in the use of Altera FPGA design tools.

IP MODULE DLL CONTROL SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (2000/XP/Vista/7®) applications accessing Acromag Industry Pack models installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments including Visual C++™, Visual Basic®, Borland C++ Builder® and others. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and Carriers, PCI I/O Cards, and CompactPCI I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PCI boards.

IP MODULE QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of board QNX® software. This software (Model IPSW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software supports X86 PCI bus only and is implemented as library of "C" functions. These functions link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

CARD CAGE CONSIDERATIONS

IMPORTANT: *Adequate air circulation or conduction cooling must be provided to prevent a temperature rise above the maximum operating temperature.*

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to the IP Mechanical Assembly Drawing located in the *Drawings* Section of this manual and the following discussion for configuration and assembly instructions.

Default Hardware Configuration

Default Hardware Jumper Configuration

There is one jumper on the board that is used to select the method for loading the FPGA, either from FLASH or direct from the IP bus. The jumper is set at the factory to load from IP bus. Refer to the JTAG Interface/Jumper Location diagram in the *Drawings* Section of this manual for the jumper location and settings.

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header which mates to the male connector of the carrier board. This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing in the *Drawings* Sections of this manual). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field-I/O interface connector on the carrier board (you should verify this for your carrier board). When reading Table 2.1 notice that Differential input/output channels as well as digital TTL input/output channels are listed with their corresponding connector pin number. Furthermore each Differential I/O point could be either RS485 or LVDS defined by the IP-EP2 model. Table 2.2 lists the channels dedicated to each of the IP-EP2 models.

Pin Description		Pin	Pin Description		Pin
DIFF[1]	TTL	Number	DIFF[1]	TTL	Number
I/O00+	I/O00	1	I/O12-	I/O25	26
I/O00-	I/O01	2	I/O13+	I/O26	27
I/O01+	I/O02	3	I/O13-	I/O27	28
I/O01-	I/O03	4	I/O14+	I/O28	29
I/O02+	I/O04	5	I/O14-	I/O29	30
I/O02-	I/O05	6	I/O15+	I/O30	31
I/O03+	I/O06	7	I/O15-	I/O31	32
I/O03-	I/O07	8	I/O16+	I/O32	33
I/O04+	I/O08	9	I/O16-	I/O33	34
I/O04-	I/O09	10	I/O17+	I/O34	35
I/O05+	I/O10	11	I/O17-	I/O35	36
I/O05-	I/O11	12	I/O18+	I/O36	37
I/O06+	I/O12	13	I/O18-	I/O37	38
I/O06-	I/O13	14	I/O19+	I/O38	39
I/O07+	I/O14	15	I/O19-	I/O39	40
I/O07-	I/O15	16	I/O20+	I/O40	41
I/O08+	I/O16	17	I/O20-	I/O41	42
I/O08-	I/O17	18	I/O21+	I/O42	43
I/O09+	I/O18	19	I/O21-	I/O43	44
I/O09-	I/O19	20	I/O22+	I/O44	45
I/O10+	I/O20	21	I/O22-	I/O45	46
I/O10-	I/O21	22	I/O23+	I/O46	47
I/O11+	I/O22	23	I/O23-	I/O47	48
I/O11-	I/O23	24	External Clock Input[2]		49
I/O12+	I/O24	25	GND		50

Table 2.1: IP-EP2 Series Field I/O Pin Connections (P2).

1. Differential refers to either RS485 or LVDS channels. Refer to Table 2.2 for I/O assignments per module.

2. The External Clock Input is routed directly to an global input on the Cyclone II FPGA.

WARNING: THE EXTERNAL CLOCK INPUT PIN IS NOT 5V TOLERANT. IT REQUIRES LVTTL (3.3V) SIGNALING. APPLYING 5V TO FIELD I/O PIN 49 MAY DAMAGE THE BOARD.

Table 2.2: IP-EP2 Model Channel Assignments

1. Refer to Table 2.1 for I/O pin assignments.

Model	I/O Register Bits[1]	
IP-EP201	TTL Channels 0 to 47	
IP-EP202	Differential/RS485 Channels ±0 to ±23	
IP-EP203	TTL Channels 0 to 23	Differential /RS485 Channels ±12 to ±23
IP-EP204	Differential/LVDS Channels ±0 to ±23	

The external clock pin is an LVTTL ***(NOT 5V TOLERANT)*** input that connects directly to a global clock input on the Altera FPGA. In addition, several buffered I/O are routed to global input clock pins. Table 2.3 summarizes the buffered I/O are can be used for global input signals for each IP-EP2 Series model. *Note that modification of the example vhdl file is required to utilize the additional global inputs.*

Table 2.3: IP-EP2 Model Global Clock Signals

1. These buffered I/O are connected to global input pins on the FPGA. Modification of the Example Design is required to use the global inputs.

Model	Buffered Global Inputs[1]	
IP-EP201	TTL Channels 18, 22, & 46	
IP-EP202	RS485 Channels ±9, ±11, & ±23	
IP-EP203	TTL Channels 18 & 22	RS485 Channel ±23
IP-EP204	LVDS Channels ±9, ±11, & ±23	

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header which mates to the male connector of the carrier board. This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Mechanical Assembly Drawing in the Drawings sections of this manual for details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.4). However some logic signals not used for the IP interface are reserved for factory programming.

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset#	3	R/W#	28
D00	4	IDSEL#	29
D01	5	DMAReq0#	30
D02	6	MEMSEL#	31
D03	7	DMAReq1#	32
D04	8	IntSel#	33
D05	9	DMAck0#	34
D06	10	IOSEL#	35
D07	11	Reserved[2]	36
D08	12	A1	37
D09	13	DMAEnd#	38
D10	14	A2	39
D11	15	Reserved[2]	40
D12	16	A3	41
D13	17	INTReq0#	42
D14	18	A4	43
D15	19	INTReq1#	44
BS0#	20	A5	45
BS1#	21	STROBE#	46
-12V[1]	22	A6	47
+12V[1]	23	ACK#	48
+5V	24	Reserved[2]	49
GND	25	GND	50

Table 2.4: Standard Logic Interface Connections (P1).

1. Not Used by this IP Module.

2. Reserved for Factory Programming.

The pound sign (#) is used to indicate an active-low signal.

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the board.

The IP-EP2 Series Module has two distinct operating modes. The first is the Configuration Mode. In this mode, the board has limited functionality since the FPGA is not yet configured. The second is the User (operation) mode where the FPGA is programmed. Board operation in this mode is determined by the FPGA programming. To determine the current mode, read the Identification Space (Refer to Table 3.2).

CONFIGURATION MODE

The I/O space address map for the IP-EP2 Series when in configuration mode is as shown in Table 3.1. The module is always in configuration mode upon system power up when the direct IP programming method is selected or when the EnableCPLD line on pin L3 of the Altera FPGA is a logic high. The EnableCPLD line is a signal that communicates to the IP-EP2 Series hardware the status (configured vs. non-configured) of the FPGA. This signal must be held low by the Altera FPGA after successful configuration to disable configuration mode.

If you have a configured FPGA and then wanted to re-configure the FPGA, you must enable the configuration mode. This is accomplished by driving pin L3 of the FPGA to a logic high level via control register bit-0. If you change your mind and want to return control back to the FPGA an IP bus reset can be used to clear or drive pin L3 to a logic low level (see example VHDL file). Note that the Altera FPGA must not drive the IP bus data lines or the ACK# signal after you return to configuration mode from a pre-configured FPGA. Also, IP bus write cycles must be disabled from changing the registers of your configured FPGA while in configuration mode.

Configuration Address Maps

The I/O space address map used to configure the FPGA is shown in Table 3.1. 16 or 8-bit register accesses are permitted.

Table 3.1: IP-EP2 Series I/O Space Configuration Address Map

1. The IP module will return 0 for all addresses that are "Not Used".

2. The IP module will not respond to read/write operations at these addresses.

Base Addr+	D15 D08	D07 D00	Base Addr+
00	Not Used[1]	Control/Status Register	01
02	Not Used[1]	Configuration Data Register	03
04 ↓ 7E	Not Acknowledged[2]		05 ↓ 7F

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PC carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier requires the use of odd address locations.

CONFIGURATION REGISTERS

Configuration Control/Status Register (Read/Write) Base Addr + 1H

This read/write register is used to initiate the reprogramming of the Cyclone II FPGA and to monitor the status of the FPGA during configuration. Bit 0 of this register is used to trigger FPGA programming. Writing a logic "1" to bit 0 will enable a pulse on the FPGA nConfig signal. If the IP carrier is providing a 32MHz clock, the pulse length will be 40uS. If the carrier provides a 8MHz clock, the pulse length will be 160uS. Bit-1 monitors the Altera nSTATUS signal which must remain high during configuration. Bit-2 of the Status register reflects the status of the Altera FPGA CONF_DONE signal. The CONF_DONE signal must remain at a logic low until configuration has completed. Writing to either bits 1 or 2 will have no effect. Bits 4 is the CRC_ERROR signal from the FPGA. This function is disabled in the example program must be enabled within the Quartus II software. Refer to the Cyclone II Manual for information on this signal. Bit 5 is the value of MSEL0 as determined by the configuration jumper. A logic high on this bit indicates that configuration will occur over the IP bus. A logic low indicates that the configuration data is loaded from Flash. Bits 3, and 6 to 7 are not used and will return logic "0" when read.

Configuration Data Register (Write Only) Base Addr + 3H

This write only register is a conduit for the programming data file, when configuring the IP-EP2 module over the IP bus. Prior to configuration the user must write a logic "1" to bit zero of the Configuration Control/Status Register. Then after bit 0 of the Configuration Control/Status register reads logic low again (up to 160mS), the programming file is written to this register one byte at a time. The data is transferred serially to the FPGA, therefore a write to this register requires 8 wait states.

CONFIGURATION METHODOLOGIES

The IP-EP2 module has three methods of configuration. The first is configuring the Altera FPGA directly over the IP Bus. This method uses the passive serial scheme to directly program the FPGA. Note that this scheme requires the FPGA to be reprogrammed after every power-up. The second method is to configure the part directly using a JTAG interface. The JTAG interface will automatically over-write any existing configuration and can be completed at any time using a standard Altera JTAG download cable such as the ByteBlaster 2®. This cable is NOT provided by Acromag. Once again all programming is lost at power-down using the direct JTAG configuration approach. Finally the IP-EP2 Series module contains a Flash Configuration Device (Altera EPCS4 or equivalent) that can be programmed indirectly through the JTAG interface using the Altera Serial Flash Loader. The Serial Flash Loader creates a logic bridge between the Cyclone II JTAG interface and the controls of the FLASH device. This bridge allows the user to program the Flash via the JTAG interface. The FLASH device cannot be programmed through the IP interface. This method is recommended for debugged designs since the Flash device programs the Altera FPGA at power-up. The programming procedures for each of the three methods are below.

IP-EP2 IP Direct Configuration Procedure

The IP-EP2 Series can implement configuration of the Altera FPGA over the IP bus interface. The IP-EP2 module uses the Altera passive serial scheme with the IP bus serving as the download path. Thus, download and configuration are implemented with no special hardware or cables.

An example program written in C and available from Acromag, implements configuration of the IP-EP2 Series module over the IP bus. The program requires the configuration file to be in the Intel Hex format. For information on generating hex files refer to the documentation supplied with the EDK.

IP-EP2 IP Direct Configuration Procedure

1. Prior to power-up set the Configuration Jumper to "IP BUS" as shown in the JTAG Interface/Jumper Location drawing at the end of this manual.
2. Start in the configuration mode. Upon system power-up, the IP-EP2 module is in configuration mode. If the Altera FPGA is currently configured and operational, configuration mode can be entered by driving pin L3 of the Altera FPGA to a logic high via the control register bit-0. Pin L3 is the EnableCPLD signal which upon system power-up is held high by a pull-up resistor.
3. You can verify that you are in configuration mode by reading ID space at base address + 0BH. The byte read will be 48H when in configuration mode and 49H when in user mode.
4. Configuration is started by setting bit-0 of the control register, at base address + 01H, to a logic high.
5. This same register bit-0 must be read next. When read as a logic high software can proceed to the data transfer phase. A polling method should be used since this bit may not be read high for up to 160μ seconds after the control bit is set high.
6. The status of the Altera FPGA during configuration can be monitored via the Status register at base address + 01H. Bit-1 monitors the Altera nStatus signal which must remain high during configuration. Bit-2 of the Status register reflects the Altera FPGA CONF_DONE signal. The CONF_DONE signal must remain at a logic low until configuration has completed.
7. Write program data, one byte at a time, to the Configuration Data register at base address + 03H.
8. Upon successful configuration, control of the IP bus will automatically be switched to user mode and the Altera FPGA will have control of the IP bus interface. It is good practice to issue a software reset prior to operating the board.

Refer to the documentation provided with the IP-EP2 EDK for further information on programming methodologies.

IP-EP2 Direct JTAG Configuration Procedure

The IP-EP2 module can also implement configuration using a standard JTAG interface. The JTAG interface can either program the FPGA directly or program the FLASH configuration memory. When programming the FPGA directly, the programming jumper may be in either position. Note that the FPGA will require reprogramming after power down.

The following is the general procedure for direct programming of the Altera FPGA using the JTAG interface.

1. Connect the 10-pin Altera JTAG cable (not included) to the board.
2. Power-up the carrier board.
3. Download the Configuration .sof file to the FPGA via JTAG using Altera Quartus II software.
4. Upon successful configuration the board will be in User mode with the Altera FPGA in control of the IP bus interface. It is good practice to issue a software reset prior to operating the board.

Refer to the documentation provided with the IP-EP2-EDK for further instructions on JTAG configuration.

IP-EP2 FLASH Configuration Procedure

The configuration FLASH can be programmed using the JTAG interface. The JTAG interface can either program the FPGA directly or program the FLASH configuration memory. When programming the FLASH, the Altera FPGA acts as a logic bridge between the JTAG interface and the configuration device. Once the FLASH is programmed, the Altera FPGA will load that program at power-up.

The following is the general procedure for programming the FLASH using the JTAG interface.

1. Connect the 10-pin Altera JTAG cable (not provided) to the board.
2. Set the programming jumper to the FLASH position.
3. Power-up the carrier board.
4. Download the Configuration file to the FPGA using Altera Quartus II software. An indirect FLASH configuration requires a jic file.
5. After download, the board must be reset to load the proper configuration. Either power down the board or write 01H to the configuration control register at address 01H.
6. Upon successful configuration the board will be in User mode with the Altera FPGA in control of the IP bus interface.

Refer to the documentation provided with the IP-EP2-EDK for further instructions on JTAG configuration.

IP IDENTIFICATION SPACE (Read Only)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains at most 32 bytes of information. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAH" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP-EP2 Series ID space does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the "Big Endian" Motorola or VME bus). Even addresses are used on the "Little Endian" PCI bus.

The IP-EP2 Series ID space will read differently in configuration mode than it does in user mode. In configuration mode the IP model code at base address + 0BH will read a 48H, while in user mode the same byte will read 49H. In addition, the CRC byte at base address + 17H will read a BAH in configuration mode and read a DBH in user mode. All other ID space bytes will read the same in both configuration mode and user mode.

In user mode, the ID space must be defined in the internal logic of the FPGA. In order for Acromag software to properly identify the model, this ID space must remain as defined in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID information. Execution of an ID Space Read operation requires 1 wait state.

Table 3.2: IP-EP2 Series ID Space Identification (ID)

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All 32MHz IP's have 'IPAH'
03	P	50	
05	A	41	
07	H	48	
09		A3	Acromag ID Code
0B		 48 49	IP Model Code[1] Configuration Mode = 48 User Mode = 49
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		 BA DB	CRC Configuration Mode = BA User Mode = DB
19 to 3F		00	Not Used

1. The IP model number is represented by a two-digit code within the ID space. The IP-EP2 Series models are represented by 48 Hex in Configuration Mode and 49 Hex in User Mode.

USER MODE

Example Altera FPGA Design

The example design provided with the IP-EP2-EDK consists of IP bus interface logic, Altera interface to 64K x 16 static RAM, Altera interface to the clock generator chip, and I/O interface to differential or TTL I/O.

The IP-EP2 Series hardware supports a direct connection to all IP bus signals as listed in Table 2.4. As such, hardware will support all IP bus cycles including: ID, I/O, Interrupt, Memory, and DMA. The example design provided uses all but the Memory and DMA cycle types.

The I/O space address map for this example design is given in Table 3.3. The differential or TTL I/O, clock generator chip, and 64K x 16 static RAM can be controlled and accessed through I/O space.

The base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown in Table 3.3 to properly access the I/O space. Accesses can be performed on an 8-bit or 16-bit basis.

This memory map reflects byte accesses using the "Big Endian" byte ordering format. Big Endian uses odd-byte addresses to store the low-order byte. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. The Intel x86 family of microprocessors uses "Little Endian" byte ordering. In Little Endian, the lower-order byte is stored at even-byte addresses.

Base Addr+	D15 D08	D07 D00	Base Addr+
00	Control Register		01
02	Input/Output Register[1] Channels 15 ↔00		03
04	Input/Output Register[1] Channels 31 ↔ 16		05
06	Input/Output Register[1] Channels 47 ↔ 32		07
08	Direction Control Register		09
0A	Not Used[2]	Interrupt Enable Register	0B
0C	Not Used[2]	Interrupt Type Register	0D
0E	Not Used[2]	Interrupt Status Register	0F
10	Not Used[2]	Interrupt Polarity Register	11
12	Not Used[2]	Interrupt Vector Register	13
14	Memory Data Register		15
16	Memory Address Register		17
18	Clock Control Register 1		19
1A	Clock Control Register 2		1B
1C	Not Used[2]	Clock Control Register 3	1D
1E	Not Used[2]	Clock Generator Trigger Register	1F
20 ↓ 7E	Not Used[2]		21 ↓ 7F

Table 3.3: IP-EP2 Series FPGA Address Map (IO Space) for Example Design

1. Refer to the Input/Output Register Description for I/O mapping for the various IP-EP2 series models.

2. The board will return 0 for all addresses that are "Not Used".

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Control Register (Read/Write) - (Base Addr + 01H)

This read/write register is used to transfer control back to configuration mode when in user mode, set your specific model of the IP-EP2, and issue a software reset.

Bit-0 controls operation of the IP-EP2 module in user mode and configuration mode via control of pin L3 of the Altera FPGA. When bit-0 is set to logic low the IP-EP2 module will be in user mode. Setting bit-0 to a logic high places the IP-EP2 Series in configuration mode. Upon issue of an IP bus reset, this register bit will be clear placing the IP-EP2 in user mode. Also, initial configuration of the Altera FPGA sets bit-0 to a logic low holding the FPGA in user mode.

Bits 10 to 8 are used to set the IP-EP2 model corresponding to your I/O mix. This will allow the Altera FPGA to properly map Input/Output registers to the I/O transceivers present on your module. Bits 10 to 8 should be set as identified in the following table to identify the model corresponding to your IP-EP2.

Table 3.4: Control Register Identification Bits

Control Register Bits 10, 9, and 8			
IP Model	Bit-10	Bit-9	Bit-8
Disabled	0	0	0
IP-EP201	1	1	1
IP-EP202	0	0	1
IP-EP203	1	0	0
IP-EP204	0	0	1

Bit-11 is reserved for factory testing. For normal operation this bit should always be logic low.

Bit-15 can be used to issue a software reset. When bit-15 is set to a logic high a software reset will occur.

Reading this register will return logic low on all data lines/bits except for bits 11 to 8 which will reflect their last written state.

Input/Output Registers
(Read/Write) - (Base Addr + 03H to 07H)

Forty-eight possible input/output channels numbered 0 through 47 may be individually accessed via these registers. The Input/Output Channel registers are used to monitor/read or set/write channels 0 through 47. The first eight channels are accessed at the carrier base address +03H via the low data byte. The next eight channels are accessed at the carrier base address +02H via the high data byte. The remaining 32 channels are accessed similarly at the carrier base address + offsets shown in Table 3.3.

If the Input/Output port is to be used as an output, you should first set the output register bit as desired before setting the Direction Control register. Note: if you select as an output port before setting this Input/Output register, the output port will be logic low as this is the power-up/reset state of the output register bits.

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Table 3.5 shows all channels and their corresponding I/O data register bit for each of the IP-EP2 models. The register bits not listed will not be used. See the memory map to identify the addresses required to control I/O registers.

Table 3.5: Input/Output Register Module Mapping

Used Input/Output Channel Register Bits		
Model	*I/O Register Bits* See Table 2.1 for Pin Assignments	
IP-EP201	*TTL Channels 0 to 47* Register Bits 0 to 47	
IP-EP202	*Differential/RS485 Channels ±0 to ±23* Register Bits 0 to 23	
IP-EP203	*TTL Channels 0 to 23* Register Bits 0 to 23	*Diff./RS485 Channels ±12 to ±23* Register Bits 32 to 43
IP-EP204	*LVDS Channels ±0 to ±23* Register Bits 0 to 23	

Channel read/write operations use 8-bit, or 16-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs on a power-on or software reset. The unused upper bits of these registers will always read logic "0".

Direction Control Register (Read/Write) - (Base Addr +09H)

The data direction (input or output), of the digital I/O channels, is selected via this register. The data direction of all differential channels are set as a group of two or four channels while data direction of all TTL channels is controlled as a group of 8 channels. Setting a bit high configures the data direction, for the identified channels, as output. Setting the control bit low configures the corresponding channel's data direction for input. Refer to Table 3.6 for the corresponding channels for each bit in the Direction Control Register.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs on system reset or power-up. All not used bits will read low logic. See Table 2.1 for field I/O pin assignments corresponding to each of the Differential and TTL channels listed below.

Table 3.6: Direction Control Register

Bit(s)	Function by Model			
	I/O Type	IP-EP201	IP-EP202/ IP-EP204	IP-EP203
0	**Diff.**	Not Used	Ch 0, 1, 12, 13	Ch 12, 13
1		Not Used	Ch 2, 3, 14, 15	Ch 14, 15
2		Not Used	Ch 4, 5, 16, 17	Ch 16, 17
3		Not Used	Ch 6, 7, 18, 19	Ch 18, 19
4		Not Used	Ch 8, 9, 20, 21	Ch 20, 21
5		Not Used	Ch 10, 11, 22, 23	Ch 22, 23
6	**TTL**	Ch 0 – Ch 7	Not Used	Ch 0 – Ch 7
7		Ch 8 – Ch 15	Not Used	Ch 8 – Ch 15
8		Ch 16 – Ch 23	Not Used	Ch 16 – Ch 23
9		Ch 24 – Ch 31	Not Used	Not Used
10		Ch 32 – Ch 39	Not Used	Not Used
11		Ch 40 – Ch 47	Not Used	Not Used
15 – 12	Not Used			

Interrupt Enable Registers (Read/Write) - (Base + 0BH)

The Interrupt Enable Registers provide a mask bit for the first 8 channels on any IP-EP2 model. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding input channel to generate an interrupt. Only those channels enabled for interrupts will generate interrupts. Interrupts are only available on the first eight channels.

Interrupt Enable Register							
MSB							LSB
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Ch 07	Ch 06	Ch 05	Ch 04	Ch 03	Ch 02	Ch 01	Ch 00

The Interrupt Enable register at the carrier's base address + offset 0BH is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the prior table.

Channel read operations use 8-bit, or 16-bit data transfers. The upper 8 bits of this register are "Not Used" and will always read logic "0".

All input channel interrupts are disabled (set to "0") following a power-on or software reset.

Interrupt Type Configuration Registers (Read/Write) - (Base + 0DH)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 8 possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means

the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at the carrier's base address + offset 0DH is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the table below.

Interrupt Type (COS or H/L) Configuration Register							
MSB							LSB
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch 07	Ch 06	Ch 05	Ch 04	Ch 03	Ch 02	Ch 01	Ch 00

Channel read or write operations use 8-bit, or 16-bit data transfers. The upper 8 bits of this register are "Not Used" and will always read logic "0". Note that interrupts will not occur unless they are enabled via the Interrupt Enable Register at base address + offset 0BH.

All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Interrupt Status Registers (Read/Write) - (Base + 0FH)

The Interrupt Status Register reflects the status of each of the interrupting channels. A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). This is known as the "Release On Register Access" (RORA) method, as defined in the VME system architecture specification. However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register). In addition, an interrupt will be generated if any of the channels enabled for interrupt have an interrupt pending (i.e. one that has not been cleared). Writing "0" to a bit location has no effect; that is, a pending interrupt will remain pending.

Note that interrupts are not prioritized via hardware. The system software must handle interrupt prioritization.

The Interrupt Status register at the carrier's base address + offset 0FH is used to monitor pending interrupts corresponding to channels 00 through 07. For example, channel 00 is monitored via data bit-0.

The unused upper 8 bits of this register are "Not Used" and will always read logic "0". All bits are set to "0" following a reset, meaning that all interrupts are cleared.

Interrupt Polarity Registers (Read/Write) - (Base + 11H)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the digital input channel data

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register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register at the carrier's base address + offset 11H is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the table below.

Interrupt Polarity Register							
MSB							LSB
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Ch 07	Ch 06	Ch 05	Ch 04	Ch 03	Ch 02	Ch 01	Ch 00

The upper 8 bits of this register are "Not Used" and will always read logic low. All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold (provided they are enabled for interrupt on level).

Interrupt Vector Register (Read/Write) - (Base + 13H)

The Interrupt Vector Register maintains an 8-bit interrupt pointer for all channels configured as input channels. The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL∗ cycle. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Interrupts are released on register access to the Interrupt Status register. Issue of a software or hardware reset will clear the contents of this register to 0.

Memory Data Register (Read/Write, 15H)

The Memory Data register is used to provide read or write access to SRAM memory. Reading or writing to this register is possible via 16-bit data transfers only.

In order to properly access the memory, which constitutes 64K words, an address pointer to a single word in memory must first be specified. The address is specified via the Memory Address register. The value written into the Memory Address register is used to point to one of the 64K words.

All read or write accesses to the Memory Data register will in turn implement an access to memory at the address specified by the Memory Address register.

The address specified in the Memory Address register will be automatically incremented after the read or write cycle is completed. Thus, when consecutive locations within the memory are accessed the Memory Address register need not be manually updated by software.

Read or write accesses to this register require four wait states. A software or hardware reset has no affect on this register.

Memory Address Register (Read/Write, 17H) **USER MODE**

The Memory Address register is used to point to one of 64K words in memory. The 16 bits of this register are used to specify one of 64K words that can be accessed via a read or write to the Memory Data register. Writing to this register is possible via 16-bit data transfers only.

The address specified in the Memory Address register will be automatically incremented after the read or write cycle to the Memory Data register is completed. Thus, when consecutive locations within the memory are accessed the Memory Address register need not be manually incremented by software.

A write access to this register requires one wait state. A software or hardware reset will clear this register to zero.

Clock Control Reg 1 (Read/Write) – (Base + 19H)

The Clock Control Register 1 is a 16-bit read/write register. This is used as part of the control for the Cypress CY22150 Programmable Clock. The register contains the following control bits as specified in the Cypress CY22150 spec sheet.

Bit	Data	Bit	Data
D0	DIV1N(0)	D8	Q(0)
D1	DIV1N(1)	D9	Q(1)
D2	DIV1N(2)	D10	Q(2)
D3	DIV1N(3)	D11	Q(3)
D4	DIV1N(4)	D12	Q(4)
D5	DIV1N(5)	D13	Q(5)
D6	DIV1N(6)	D14	Q(6)
D7	DIV1SRC	D15	PO

Refer to "Program procedure to set Clock Frequency" later in this manual for information on determining the value of these bits. A software or hardware reset will clear this register to zero.

Clock Control Reg 2 (Read/Write) – (Base + 1BH)

The Clock Control Register 2 is a 16-bit read/write register. This is used as part of the control for the Cypress CY22150 Programmable Clock. The register contains the following control bits as specified in the Cypress CY22150 spec sheet.

Bit	Data	Bit	Data
D0	PB(0)	D8	PB(8)
D1	PB(1)	D9	PB(9)
D2	PB(2)	D10	Pump(0)
D3	PB(3)	D11	Pump(1)
D4	PB(4)	D12	Pump(2)
D5	PB(5)	D13	CLKSRC0
D6	PB(6)	D14	CLKSRC1
D7	PB(7)	D15	CLKSRC2

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Refer to "Program procedure to set Clock Frequency" later in this manual for information on determining the value of these bits. A software or hardware reset will clear this register to zero.

Clock Control Reg 3 (Read/Write) – (Base + 1DH)

The Clock Control Register 3 is an 8-bit read/write register. This is used as part of the control for the Cypress CY22150 Programmable Clock. In this register only D0 (bit 0) and D7 (bit 7) are required. The other bits (D1-D6) are not used.

The value for D0 is zero if the carrier board provides an 8MHz clock to the FPGA. D0 is one if the carrier board provides a 32MHz signal to the FPGA. D7 is an enable/disable signal for the CY22150 IC. Writing one to D7 will disable the clock generator chip, including the programming function. Setting D7 to zero will allow for normal operation. A software or hardware reset will clear this register to zero.

Clock Trigger Register (Read/Write) – (Base + 1FH)

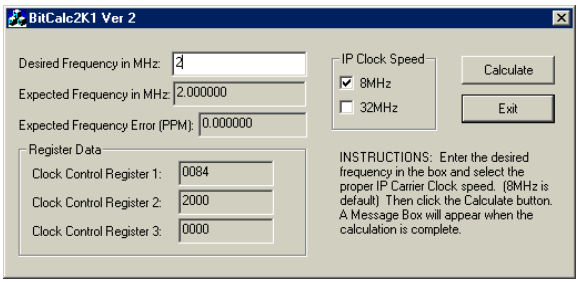
The Clock Trigger Register is an 8-bit register. To initiate programming of the Cypress CY22150 Programmable Clock with the values set in Clock Control Registers 1, 2 and 3, write a "1" to bit 0 of this register. During programming bit 0 will remain logic high. The programming process takes approximately 1.2ms to complete after the initial trigger. A software or hardware reset has no affect on this register.

Program Procedure to Set Clock Frequency

At power up the programmable clock has no valid output. The clock can be programmed for an output frequency from 250 KHz to 100 MHz. The clock can be programmed at any time during device operation. Program the clock using the following process.

The program words required for Clock Control Register 1, 2, and 3 can be calculated using a program provided by Acromag (BitCalc2K1 Version 2) supplied with the EDK. Alternately, using the Clock Control Registers Data Maps and the CY22150 specification sheet the necessary values can be calculated. Cypress® has a program CyberClocks® available to aid with calculations. Note that the user will have to combine the individual variables into the control words as outlined in the register descriptions. The CY22150 Specification Sheets and CyberClocks program are available from Cypress® at www.cypress.com.

The reference frequency input to the Cypress CY22150 is the same as the carrier clock, either 8MHz or 32MHz.



1. Start the BitCalc2K1 Version 2 program, enter the desired frequency, and select the IP clock speed.
2. Hit the Calculate Button.
3. Write to the Clock Control Register 1 at base address plus an offset of 19H using the data provided by the program.
4. Write to the Clock Control Register 2 at base address plus an offset of 1BH using the data provided by the program.
5. Write to the Clock Control Register 3 at base address plus an offset of 1DH using the data provided by the program.
6. Write 1H to the Clock Trigger Register at base address plus an offset of 1FH.

After approximately 1.2ms, programming is complete and the clock is available for use by the FPGA. A software or hardware reset during programming will cause errors. If a reset occurs, repeat the above procedure.

Programming Interrupts

Digital input channels can be programmed to generate interrupts for the following conditions:

- Change-of-State (COS) at selected input channels.
- Input level (polarity) match at selected input channels.

Interrupts generated by the IP-EP2 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism employed is the Release On Register Access (RORA) type. This means that the interrupter will release the Industrial I/O Pack interrupt request line (INTREQ0) after all pending interrupts have been cleared by writing a "1" to the appropriate bit positions in the input channel Interrupt Status Register.

In VMEbus systems, the Interrupt Vector Register contains a pointer vector to an interrupt handling routine. One interrupt handling routine must be used to service all possible channel interrupts.

When using interrupts, input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a given input channel, this could happen if multiple changes occur before the channel's interrupt is serviced. The response time of the input channels should also be considered when calculating this bandwidth. The total response time is the sum of the input buffer response time, plus the interrupt logic circuit response time, and this time must pass before another interrupt condition will be recognized. The Interrupt Input Response Time is specified in section 6.

The following programming examples assume that the IP-EP2 Series module is installed onto an Acromag AVME9630/9660/9668 carrier board (consult your carrier board documentation for compatibility details).

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Programming Example for AVME9630/9660 Carrier Boards:

1. Clear the global interrupt enable bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Perform Specific IP Module Programming - see the Change-of-State or Level Match programming examples that follow, as required for your application.
3. Write to the carrier board Interrupt Level Register to program the desired interrupt level per bits 2, 1, & 0.
4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the IP interrupt request(s) being configured.
5. Write "1" to the carrier board IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the Carrier Board Status Register.

Programming Example for Change-of-State Interrupts:

1. Program the Interrupt Vector Register with the user specified interrupt vector. This vector forms a pointer to a location in memory that contains the address of the interrupt handling routine.
2. Select channel Change-of-State interrupts by writing a "1" to each channel's respective bit in the Interrupt Type Register. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register.
4. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Change-of-State Interrupts may now be generated by the input channels programmed above for any Change-Of-State transition.

Programming Example for Level (Polarity) Match Interrupts:

1. Program the Interrupt Vector Register with the user specified interrupt vector. This vector forms a pointer to a location in memory that contains the address of the interrupt handling routine.
2. Select channel polarity match interrupts by writing a "0" to each channel's respective bit in the Interrupt Type Registers. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Select the desired polarity (High/Low) level for interrupts by writing a "0" (Low), or "1" (High) level to each channel's respective bit in the Interrupt Polarity Registers.
4. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Registers.
5. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Interrupts can now be generated by matching the input level with the selected polarity for programmed interrupt channels.

General Sequence of Events for Processing an Interrupt **USER MODE**

1. The IP-EP2 Series module asserts the Interrupt Request 0 Line (INTREQ0∗) in response to an interrupt condition at one or more inputs.
2. The AVME9630/9660 carrier board acts as an interrupter in making the VMEbus interrupt request (asserts IRQx∗) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK∗ and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN∗ signal (daisy-chained) is passed to the AVME9630/9660, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL∗ line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0∗; A1 high corresponds to INTREQ1∗.
5. The IP-EP2 Series module puts the appropriate interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK∗ to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK∗.
6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
   B. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the IP-EP2 Interrupt Enable Register.
   C. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the IP-EP2 Interrupt Status Register.
   D. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the IP-EP2 Interrupt Enable Register.
   E. Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Clear Register.
   F. Enable the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
8. If the IP-EP2 interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is complete (i.e. the carrier board negates its interrupt request, IRQ∗).
   A. If the IP-EP2 interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, the IP-EP2 should be disabled or reconfigured.
   B. If other IP modules have interrupts pending, then the interrupt request (IRQx∗) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section contains information regarding the design of the board. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the IP-EP2 Series Block Diagram drawing at the end of this manual as you review this material.

IP BUS INTERFACE LOGIC

The logic interface to the carrier board is made through connector P1 (refer to Table 2.4). P1 also provides +5V power the module (±12V is not used). Note that the ERROR∗ signal (pin 40) and two Reserved signals (pin 36 and 49) have been reserved for factory programming. These signals will not interfere in the operation of the IP interface.

The IP Specification defines all IP control signals with 5V signaling levels. Since the Altera Cyclone II Field Programmable Gate Array (FPGA) is not 5V tolerant, all signals are buffered using a Complex Programmable Logic Device (CPLD). The worst case buffer propagation delay is 10nS. This delay is significant if running the IP-EP2 Series module at 32MHz. Therefore it is recommended that 1 wait state be implemented for all IP read/write cycles. Furthermore, the direction control signals are required to control the IP Data bus. These signals are controlled from the FPGA. For more information on implementation of this requirement, refer to the documentation provided in the EDK. The Altera FPGA installed on the IP Module controls the interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The supplied FPGA logic example includes: address decoding, I/O and ID read/write control circuitry, interrupt handling, and ID storage implementation.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobes BS0∗ and BS1∗ are decoded to identify low byte, high byte, or double byte data transfers.

The carrier to IP module interface allows access to both ID and I/O space via 16 or 8-bit data transfers. Read only access to ID space provides the identification for the individual module (as given in Table 3.2) per the IP specification. Read and write accesses to the I/O space provide a means to control the IP-EP2.

The IP-EP2 has 64K words of SRAM available. Read and write accesses to the SRAM are implemented through the IP module I/O space. A start address is specified in the Memory Address register. This start address will automatically be incremented by hardware for each access to the Memory Data register.

The IP-EP2 also has a Clock Generator chip. A clock frequency from 250KHz to 100MHz is programmable via the IP module I/O space. The generated clock frequency is input to the FPGA on pin 183. This clock can be used to synchronize I/O operations with other IP modules.

Interrupt Operation

For the supplied FPGA configuration, digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions at enabled inputs. An 8-bit interrupt service routine vector is provided during interrupt acknowledge cycles on data lines D0...D7. The interrupt release mechanism employed is RORA (Release On Register Access).

FIELD INPUT/OUTPUT

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). ***Field I/O points are NON-ISOLATED***. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operational errors, and with extreme abuse, possible circuit damage.

The IP-EP2 series allows interface with a mix of up to 48 TTL I/O channels or up to 24 differential I/O signals. The signals DIO(0) to DIO(47) are utilized for digital input/output control to the field signals. The six signals DIFF_DIR(0-5) control data direction of the 24 differential I/O signals. The six signals TTL_DIR_BANK(1-6) control data direction of the 48 TTL I/O channels. Digital Field inputs are 5V tolerant. An additional External Clock input is available on all models. This input is not buffered and requires LVTTL signaling levels.

Digital Input/Output Logic

Digital TTL field I/O are provided on the IP-EP201 and IP-EP202 models through the Field I/O Connector (refer to Table 2.2). Digital input/output signals to the FPGA are buffered using an octal bus transceiver. Signals received are converted from 5V TTL to LVTTL as required by the FPGA. The digital receivers output TTL signals. The direction control of the digital channels is controlled in groups of eight.

Each field line has a 10K pull-down resistor to GND. Output operation is considered 'Fail-safe'. That is, the Digital Input/Output signals are always configured as inputs following a power-up or software reset. This is done for safety reasons to ensure reliable control under all conditions.

EIA-RS485/RS422 Input/Output Logic

Differential I/O are provided on the IP-EP202 and IP-EP203 models through the Field I/O Connector (refer to Table 2.1 and 2.2). Differential channels to the FPGA are buffered using EIA RS485/RS422 line transceivers. The transceivers are considered failsafe as a open or short circuit on the I/O will not damage the board. Field input lines are not terminated. **External 120 Ohm resistors are recommended on all receivers.** Signals received are converted from the required EIA RS485/RS422 voltages to the LVTTL levels required by the FPGA. Likewise, LVTTL signals are converted to the EIA RS485/RS422 voltages for data output transmission. The direction control of the differential channels is controlled in groups of four.

LVDS Input/Output Logic

LVDS I/O on the IP-EP204 are provided through the Field I/O Connector (refer to Table 2.3). LVDS channels (0-31) to the FPGA are buffered using multidrop LVDS line drivers and receivers. The drivers and receivers are standard LVDS signaling characteristics (TIA/EIA-644) with double the current for multipoint applications. Field inputs to these receivers include a 100 ohm termination resistor. Signals received are converted from the LVDS voltages to the LVTTL levels required by the FPGA. Likewise, LVTTL signals are converted to the TIA/EIA-644 LVDS voltages for data output transmission. The direction control of the LVDS channels is controlled in groups of four.

Fail-Safe Operation

The IP-EP2 Series operation is considered 'Fail-safe'. That is, the input/output channels are always configured as input upon power-up reset, and a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions.

JTAG INTERFACE

All IP-EP2 models have a standard Altera JTAG header. It readily connects to any compatible Altera programming cable such as the ByteBlaster 2 ® or MasterBlaster®. The JTAG interface pins connect only to the Altera FPGA. This connection can be used to program the FPGA or use the Altera debugging tool SignalTap 2®. The JTAG interface is powered by 3.3V. Refer to the EDK documentation for further information of the JTAG interface and programming procedures.

EXAMPLE DESIGN

Memory Interface

The IP-EP2 Series interfaces to a 64K word SRAM device. This memory interface utilizes the address signals RAMa1 to RAMa16, data signals RAMd0 to RAMd15, and the read/write control signals nWE_RAM, nBLE_RAM, nBHE_RAM, and nOE_RAM. The RAM device is the Integrated Device Technology IDT71V016SA, GSI Technology part GS71116A, or equivalent. A complete listing of the SRAM interface pin and their assignments on the Cyclone II FPGA is available in the IP-EP2-EDK.

IP Bus Interface

The IP-EP2 Series interfaces to the carrier board per IP Module specification ANSI/VITA 4 1995. The FPGA signals utilized are: 16 data lines (DATA0 to DATA15), and six address lines A(1 to 6). The many control lines that comprise the IP bus include: IP Reset, nIOsel, nIDsel, nMEMsel, nINTsel, R_nW, nAck, nIntReq0, nIntReq1, nDMAReq0, nDMAReq1, nDMAAck, nDMAend, nStrobe, nBS0, and nBS1. A complete listing of the IP interface pins and their assignment on the Cyclone II FPGA is available in the IP-EP2 EDK. The IP bus 8MHz or 32MHz clock signal is present on pin CLK8MZ. The function and timing requirements of all IP bus signals are specified in the ANSI/VITA 4 1995 specification. Copies of the ANSI/VITA 4 1995 specification are available from VITA (www.vita.com).

Clock Generator Interface

A clock generator chip (Cypress CY22150) is available to provide a user programmable clock frequency between 250KHz and 100MHz. A total of four signals are utilized: Ref Clock, SCLK, SDATA, and Gen Clock as seen in the tale below.

Signal	Description
Ref Clock	The Ref Clock or reference clock is a 8MHz clock generated by the FPGA from the IP carrier clock signal.
SCLK	This is the serial clock to the CY22150. It is used for clock frequency programming.
SDATA	The serial data is sent from the FPGA to the CY22150 on this pin for clock frequency programming.
Gen Clock	The clock frequency generated by the CY22150 is input to the FPGA on this pin.

FPGA Pin Definitions

The FPGA pin definitions are in the FPGA Programming Guide provided in the IP-EP2 Series Engineering Design Kit.

FPGA INITIALIZATION

The Altera Cyclone II FPGA can be initialized using several methods. First, the FPGA can be programmed over the IP Bus using the Passive Serial technique. This technique requires the programming bus jumper to be set to the "IP" position. The initialization interface utilizes six signals. nConfig, Conf_Done, Init_Done, nStatus, DCLK, and Data0.

The second and third method involve programming via the JTAG interface. This interface can be used to either direct program the FPGA or indirectly program the FLASH device. When programming the FLASH device, the FPGA acts as a bridge between the FLASH device and the JTAG interface. Once programming the FLASH is completed, the FPGA will load the program file from FLASH at power-up if the programming jumper is set to the "FLASH" position.

Refer to the Configuring Chapter of the Cyclone II Device Handbook from Altera for further information.

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

SERVICE AND REPAIR ASSISTANCE

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board. Use the unmodified example we provided.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

WHERE TO GET HELP www.acromag.com

Acromag's application engineers can also be contacted directly for technical assistance via telephone, FAX, or email through the information provided at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Single Industry Pack Board

Max Component Height	0.290 in. (7.37 mm)
Length	3.880 in. (98.5 mm)
Width	1.780 in. (45.2 mm)
Board Thickness	0.062 in. (1.59 mm)

Unit Weight

IP-EP201(E): 0.844oz (0.02626Kg)
IP-EP202(E): 0.819oz (0.02548Kg)
IP-EP203(E): 0.841oz (0.02617Kg)
IP-EP204(E): 0.824oz (0.02562Kg)

Connectors

- IP Logic Interface/Field I/O Connectors: 50-pin female receptacle header (Comm Con 8066-50G2 or equivalent)

Table 6.1: Power Requirements for Example Design

Power Requirements		IP-EP201/ IP-EP201E	IP-EP202/ IP-EP202E	IP-EP203/ IP-EP203E	IP-EP204/ IP-EP204E
5V (±5%)[1]	Typical[2]	325mA	580mA	470mA	380mA
	Max.	580mA	1100mA	850mA	680mA
+/-12V (±5%)	Typical	Not Used			
	Max.	Not Used			

1. Monotonic ramp-up required with 100ms maximum rise time.
2. Typical operating amperage assumes ½ of I/O is driving a standard load.

ENVIRONMENTAL

Operating Temperature: Standard Unit 0°C to +70°C.
E Version -40°C to +85°C

Relative Humidity: 5-95% Non-Condensing.

Storage Temperature: -55°C to 125°C.

Non-Isolated: Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI): Complies with EN61000-4-3 (3V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no register upsets.

Conducted R F Immunity (CRFI): Complies with EN61000-4-6 (3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.

Electromagnetic Interference Immunity (EMI): No register upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity: Not required for signal I/O per European Norm EN50082-1.

SPECIFICATIONS

Radiated Emissions: Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure is required to meet compliance.

Reliability Prediction

Mean Time Between Failure per MIL-HDBK-217F, Notice 2:

IP-EP201: 1,240,750 hours	IP-EP201E: 1,235,038 hours
IP-EP202: 1,580,071 hours	IP-EP202E: 1,580,413 hours
IP-EP203: 1,580,413 hours	IP-EP203E: 1,386,411 hours
IP-EP204: 1,904,795 hours	IP-EP204E: 1,904,795 hours

FPGA

Altera EP2C20F256C8 (I8 for Extended Temperature)

- 18,752 Logic Elements
- 239,303 Distributed RAM Bits
- 52 4Kbit Block RAMs
- 26 18x18 Embedded Multipliers
- 4 Digital PLL Clock Managers

SRAM

64K x 16-bit Integrated Devices Technology IDT71V016SA12PHGI (or equivalent)

CLOCK GENERATOR

Clock Generator Chip: Cypress CY22150 (or equivalent)

- Generate Frequencies from 250kHz to 100MHz

INDUSTRIAL I/O PACK INTERFACE

IP Compliance: Conforms to Industrial I/O Pack Specification per ANSI/VITA 4 1995 for 8MHz or 32MHz operation.

Module Type: IP-EP201, IP-EP202, IP-EP203 are Type I Modules. IP-EP204 is a Type II Module, since it has passive components on the back side of the board.

I/O Space: 16-bit and 8-bit read and write operations are supported.

ID Space: 16-bit and 8-bit read operations are supported. Supports Type I ID ROM data, 32 bytes per IP (data on lower byte only). IPAH is used to indicated 32MHz operation (8MHz is also supported).

Memory Space: Supported by hardware but not implemented in example design.

Interrupts: Generates INTREQ0* interrupt request as configured in the example program. An INT select cycle will return the Interrupt Vector Register. INTREQ1* is available but not implemented in the example design.

SPECIFICATIONS

DMA: Two IP requests are available but not implemented in the example design.

Wait States: Each IP bus cycle in the example design consists of three states. First is the "Select" state, where the module is given its request. Second is a wait or "processing" state implemented by the IP-EP2 module. Third is an acknowledge state. The number of wait states in both Configuration and User mode is defined in the subsequent table.

Due to the design of the IP-EP2, a minimum of 1 wait state is required for any IP bus operation when in User mode. Failure to provide the wait state may result in read or write failure.

	Configuration Mode	User Mode
ID Space	1 wait state	1 wait state
I/O Space	Write Configuration Data Register: 8 wait states All other Read/Write: 1 wait state	1 wait state
INT Space	N/A	1 wait state
MEM Space	N/A	N/A

Unless otherwise defined wait state definitions are for all read and write operations.

Channel Configuration: 24 (IP-EP202) or 12 (IP-EP203) Bi-directional EIA 485/422 differential signals are direction controlled in groups of four.

DIFFERENTIAL I/O

EIA 485/422 Differential I/O Electrical Characteristics

- 1.5 V Min., 3.3V Max.: Differential Driver Output Voltage with 54Ω load
- 3 V Max.: Common Mode Output Voltage.

- -0.2 Min to -0.05 Max: Differential Input Threshold Voltage $-7V \leq V_{CM} \leq 12V$
- 15mV Typical: Input Hysteresis
- 96KΩ Minimum Input Resistance

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating) or shorted.

Differential Propagation Delay

- Driver Input to Output Delay = 27ns Typical, 40ns Maximum
- Receiver Input to Output Delay = 33ns Typical, 60ns Maximum

Termination Resistors

Termination Resistors: Termination resistors are not provided. *External 120 Ohm termination resistors for EIA RS485/422 differential receivers are recommended.*

DIGITAL TTL I/O

TTL Channel Configuration: 48 Channels (IP-EP201) or 24 Channels (IP-EP203) of bi-directional TTL Transceivers Direction controlled in groups of eight.

Reset/Power Up Condition: All Digital Channels Default to Input.

Digital I/O DC Electrical Characteristics

Digital I/O DC Electrical Characteristics:

- $V_{OH:}$ 3.1V Minimum
- V_{OL}: 0.55V Maximum
- I_{OH}: -24.0mA
- I_{OL}: 24.0mA
- V_{IH}: 2.0V Minimum
- V_{IL}: 0.8V Maximum
- V_{MAX}: 5.5V Maximum

Digital Propagation Delay

- Driver/Receiver Input to Output Delay = 6.3ns Maximum

Pull-down Resistors: 10K pull-down resistors to GND are installed on each Digital I/O line.

LVDS I/O

Channel Configuration: 24 Channels (IP-EP204) Bi-directional LVDS signals are direction controlled in groups of 4.

LVDS I/O Electrical Characteristics

- 247mV Min., 454mV Max.: LVDS Driver Output Voltage with 50Ω load.
- 1.37 V Max.: Common Mode Output Voltage.
- -50 mV Min to +50mV Max: LVDS Input Threshold Voltage
- Compatible with either LVDS TIA/EIA-644 or M-LVDS TIA/EIA-899 for Multipoint Data Interchange

LVDS Propagation Delay

- Driver Propagation Delay Time = 2.7ns Maximum
- Driver Output Signal Transition Time = 1.0ns Maximum
- Receiver Propagation Delay Time = 4.5ns Maximum
- Receiver Output Signal Transition Time = 1.5ns Maximum

Maximum Data Rate

- Maximum Data Rate: 100MHz @ 1m

Termination Resistors

Termination Resistors: Non-removable 100Ω termination resistors are in place for each of the LVDS channels.

EXTERNAL CLOCK INPUT

Channel Configuration: 1 External LVTTL Clock input.

DC Electrical Characteristics:

- V_{IN}: 3.3V Maximum
- V_{IL}: 0.8V Maximum
- V_{IH}: 1.7V Minimum

POWER-ON RESET

Power-On Delay: The IP-EP2 has a power-up time of 0.3 seconds. During this time the IP module will not respond to any request. After this initial power-on reset another 0.4 seconds maximum is required if loading the FPGA from FLASH. During this time the board will act as if it is not configured until the download to the FPGA is complete. It is good practice to reset the board (using either an IP bus or software reset) subsequent to power-up.

APPENDIX

CABLE: MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded cable according to model number. The shielded cable is highly recommended for optimum performance with analog input or output modules.

Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660, APC8610, or APC8620/1 non-intelligent carrier board connectors (both have 50-pin connectors).

Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50-wire flat ribbon cable, 28 gage. Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).

Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).

Keying: Headers at both ends have polarizing key to prevent improper installation.

Schematic and Physical Attributes: See Drawing 4501-463.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660, APC8610, or APC8620 Boards

Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U, APC8610, or APC8620/1 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to AVME9630/9660, APC8610, or APC8620/1: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

Mounting: Termination panel is snapped on the DIN mounting rail.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: 0 to +70°C.

Storage Temperature: -25°C to +85°C.

Shipping Weight : 1.25 pounds (0.6kg) packaged.

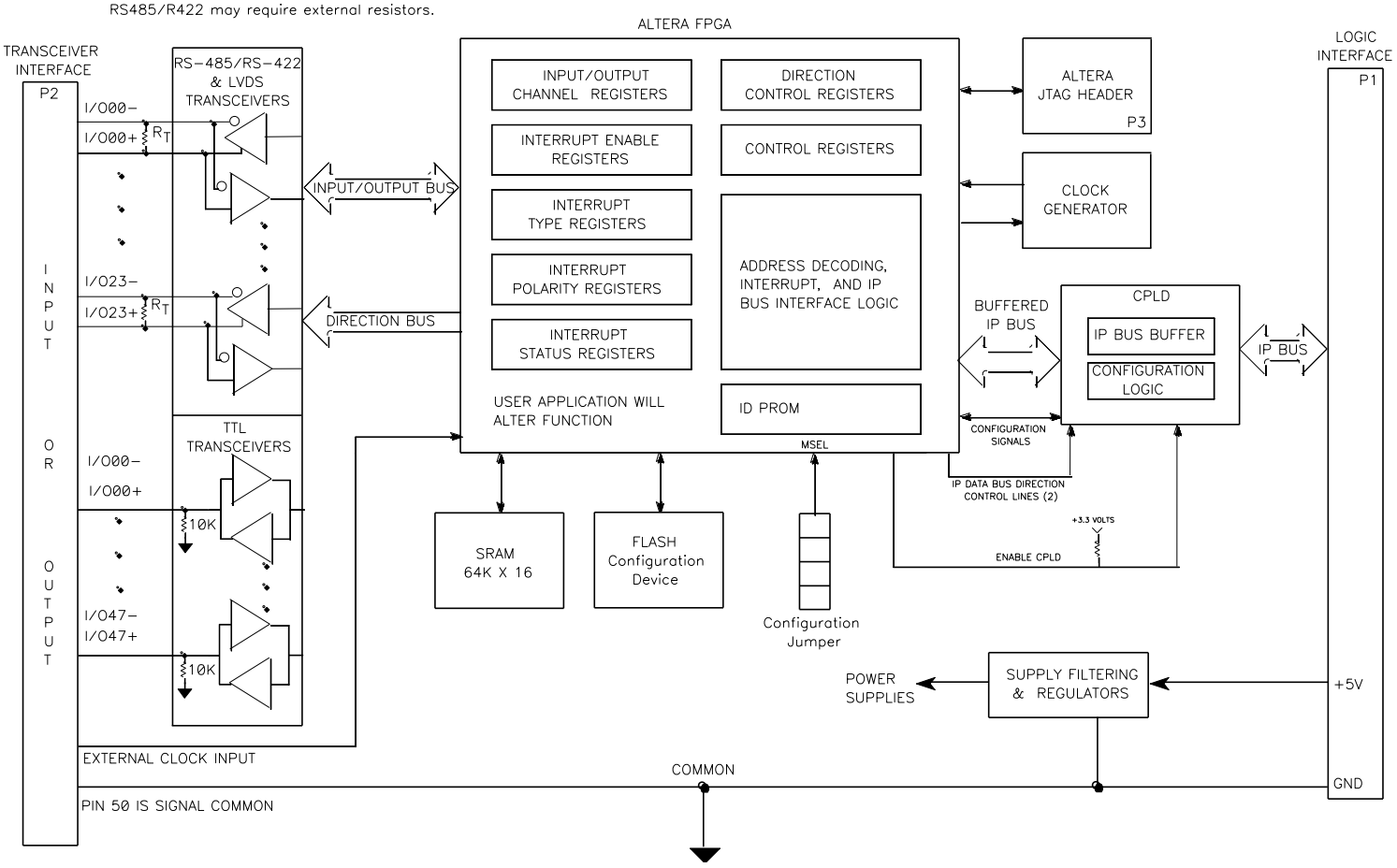
APPENDIX

TRANSITION MODULE: MODEL TRANS-GP

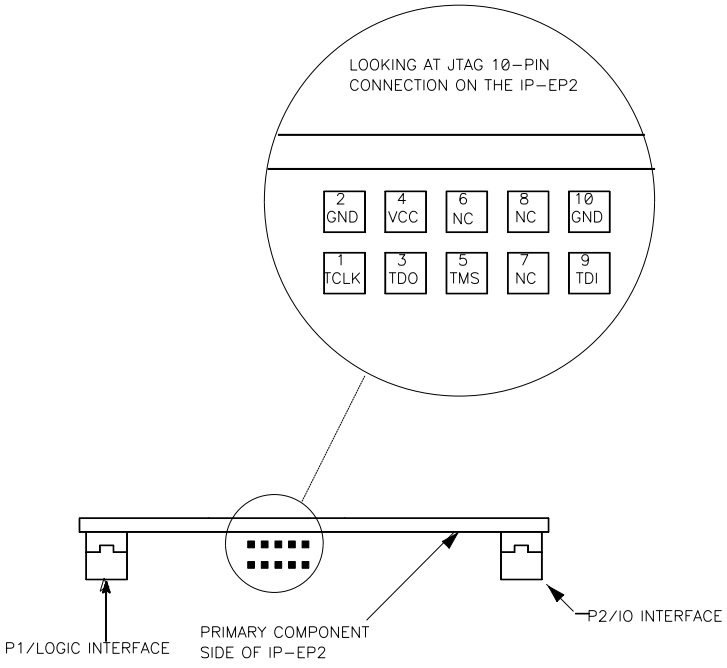
Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: 0 to +70°C.
Storage Temperature: -25°C to +85°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.

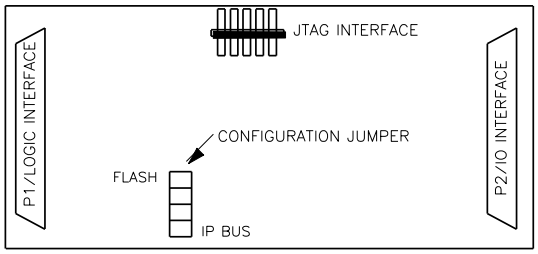
IP–EP2 SERIES BLOCK DIAGRAM

NOTE: TERMINATION RESISTOR (R_T)
100 Ohms provided for LVDS I/O.
NOT provided for RS485/R422 I/O.
RS485/R422 may require external resistors.



IP–EP2 JTAG INTERFACE/JUMPER LOCATION

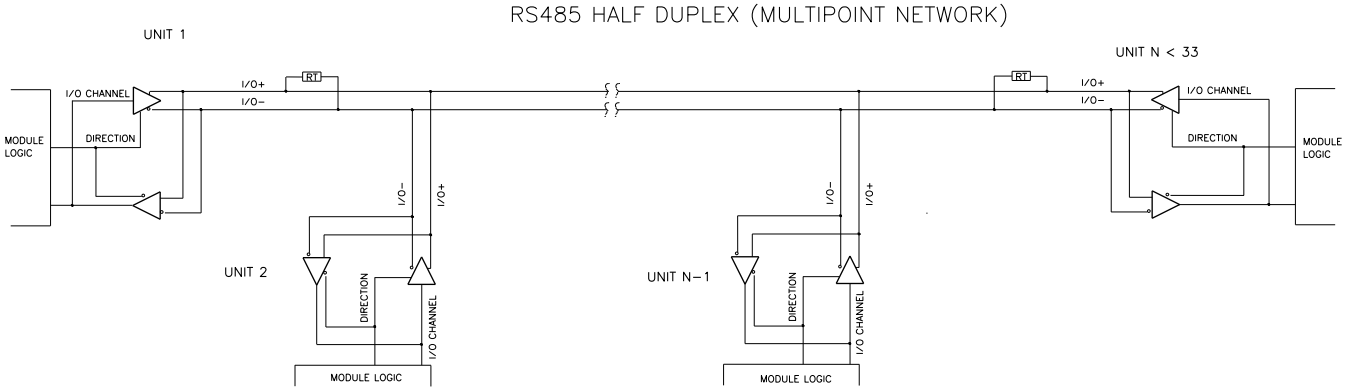




CONFIGURATION JUMPER SETTINGS	
CONFIGURE FPGA OVER IP BUS	IP BUS
LOAD CONFIGURATION FROM FLASH OR PROGRAM FLASH VIA JTAG	FLASH
PROGRAM FPGA DIRECT VIA JTAG/ SIGNALTAP II	EITHER SETTING

NOTE: JTAG PROGRAMMING WILL OVERRIDE THE CURRENT CONFIGURATION SETTING. HOWEVER TO LOAD THE FPGA FROM EITHER THE FLASH OR THE IP BUS, THE JUMPER MUST BE SET CORRECTLY.

RS485 HALF DUPLEX (MULTIPOINT NETWORK)



NOTES:

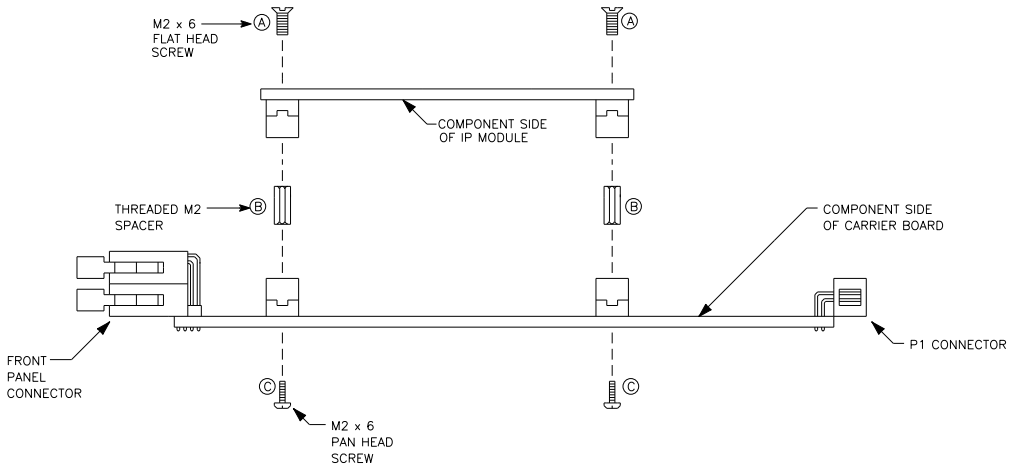
THE RS−485 STANDARD ALLOWS UP TO 32 DRIVER/RECEIVERS TO BE CONNECTED TO A SINGLE BUS. THE BUS IS A HALF DUPLEX BI−DIRECTIONAL BUS, BUT ONLY ONE DRIVER SHOULD BE ACTIVE AT A TIME.

TERMINATION SHOULD BE USED AND ONLY LOCATED AT THE TWO EXTREME ENDS OF THE BUS (NOT AT EACH NODE). THE PURPOSE OF THE TERMINATION IS TO PREVENT ADVERSE TRANSMISSION−LINE REFLECTIONS. TO MINIMIZE POWER DISSIPATION THE TERMINATION RESISTORS CAN BE LEFT OFF. THIS IS POSSIBLE IF THE CABLE IS SHORT AND THE DATA RATE IS LOW. IT IS ALSO POSSIBLE TO MINIMIZE POWER DISSIPATION BY USING AN RC TERMINATION IN PLACE OF THE RESISTOR TERMINATION.

TO MINIMIZE TRANSMISSION−LINE PROBLEMS, ALL NODES CONNECTED TO THE CABLE MUST USE MINIMUM STUB LENGHT CONNECTIONS. IDEALLY ALL NODES SHOULD BE CONNECTED IN A DAISY CHAIN FASHION.

TO MINIMIZE HIGH LEVEL OF EMI THE GROUND WIRE (ON PIN 50) MUST BE USED TO PROVIDE A PATH FOR INDUCED COMMON−MODE NOISE AND CURRENTS. THE GROUND PROVIDES A LOW−IMPEDANCE PATH TO REDUCE EMMISSIONS.

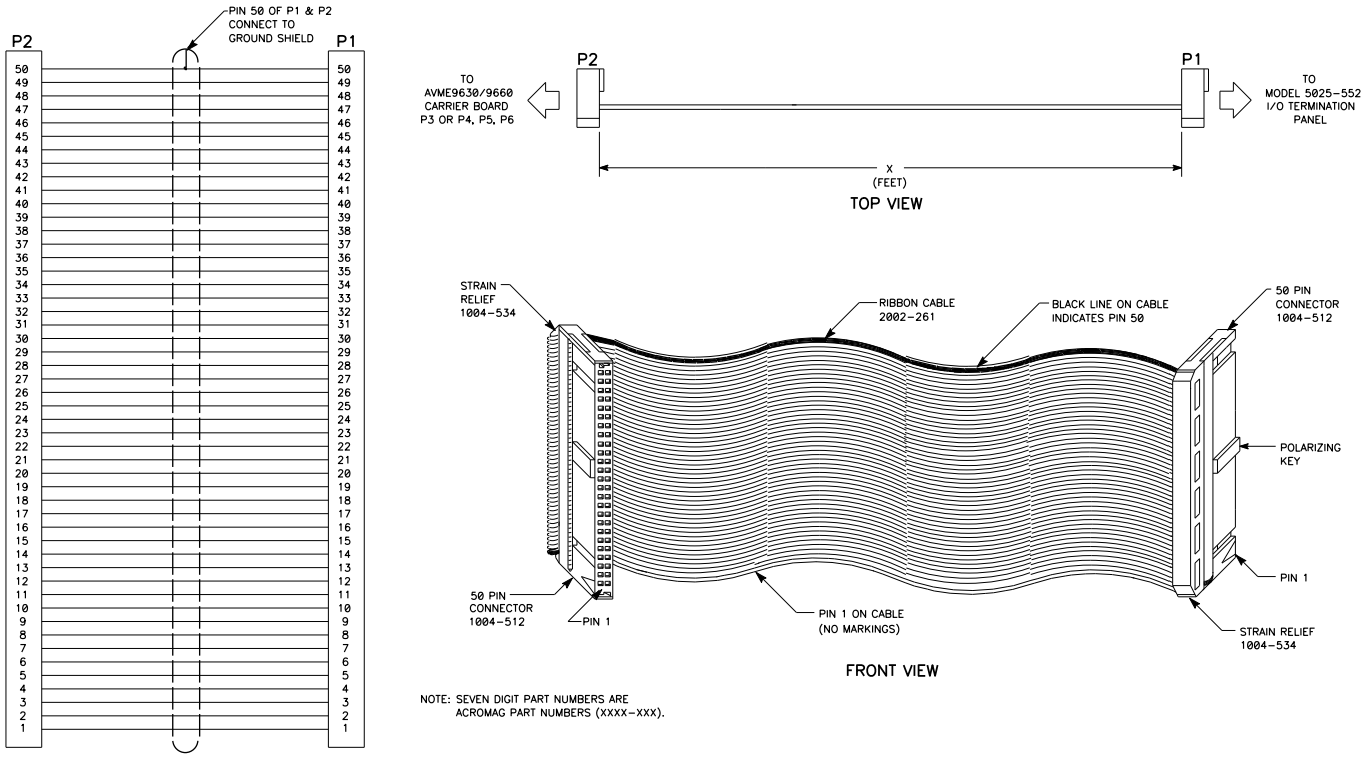
4501−702A



ASSEMBLY PROCEDURE:

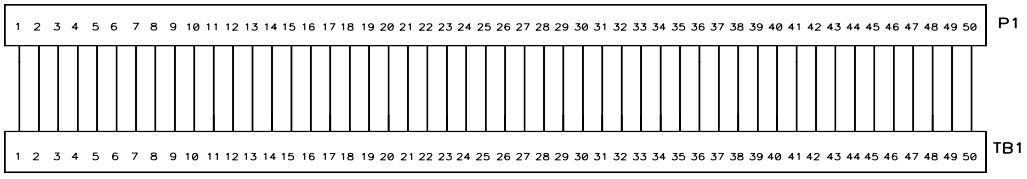
1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501−434C

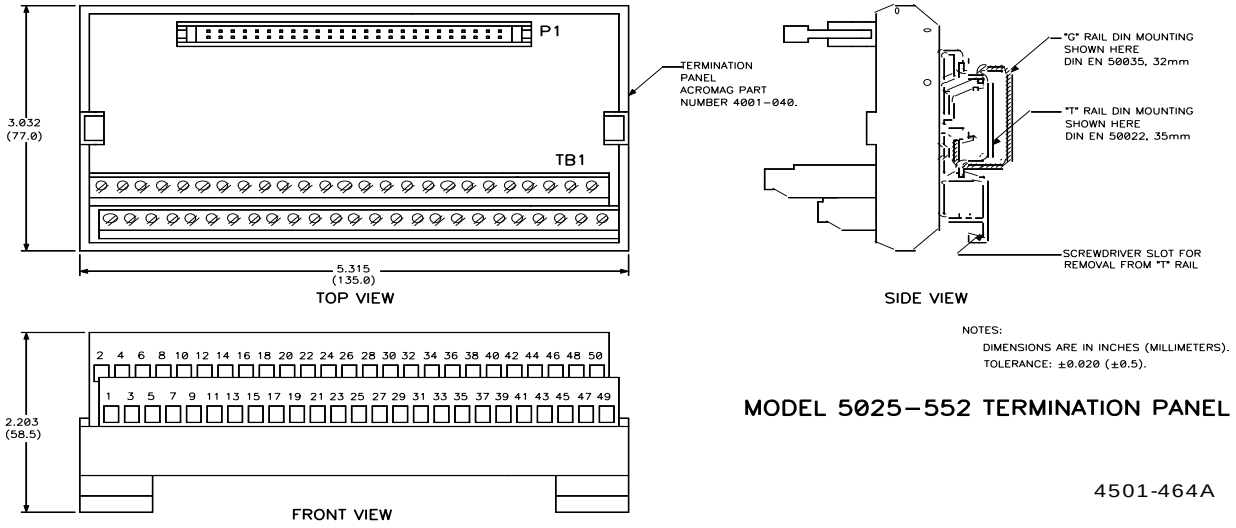


MODEL 5025-551-x SCHEMATIC

MODEL 5025-551-x SIGNAL CABLE, SHIELDED 4501-463

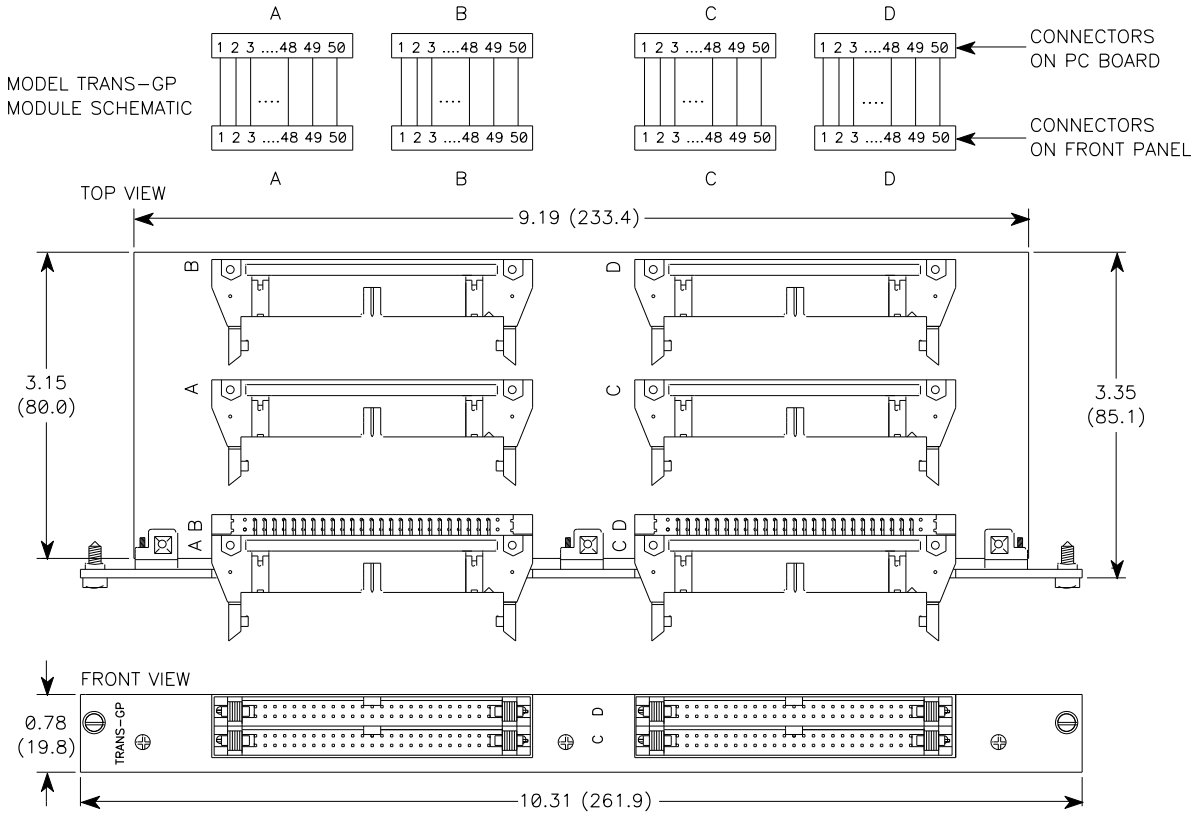


MODEL 5025-552 TERMINATION PANEL SCHEMATIC



MODEL 5025-552 TERMINATION PANEL

4501-464A



TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

4501-465

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