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Series PMC230 PCI Mezzanine Card
16-Bit High Density Analog Output Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The PCI Mezzanine Card (PMC) Series PMC230 is a precision 16-bit, high density, single-width PMC module, with eight analog voltage output channels. Each of the output channels on the PMC230 has a dedicated register from which digital values are read and simultaneously transferred to its corresponding Digital-to-Analog-Converter (DAC).

The PMC230 is available with eight cost effective 16-bit analog output channels. The PMC230 is available in standard and extended temperaterue range cards as follows.

Model	Analog Output Channels	Temperature Range
PMC230-8	8	0 to +70°C
PMC230-8E	8	-40 to +85°C

The PMC230 utilizes state of the art Surface Mounted Technology (SMT) to achieve its high channel density. The PMC230 offers a variety of features which makes it an ideal choice for many industrial and scientific applications as described below.

KEY PMC230 FEATURES

- **DAC 16-Bit Resolution** - 16-bit monolithic DAC with bipolar voltage output ranges of ±10V, ±5V, and an unipolar output range of 0 to 10V.
- **10µsec Conversion Time** - A maximum recommended conversion rate of 100KHz, for specified accuracy, is supported. The absolute maximum conversion rate of 150KHz is also supported.
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration for both gain and offset correction for each of the channels of the module.
- **Reset is Failsafe For Bipolar Output Ranges -** When the module is jumpered for bipolar operation, the analog outputs are reset to 0 volts upon power up or issue of a software or hardware reset. This eliminates the problem of applying random output voltages to actuators during power on sequences.

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- **Individual Output Control -** Output channels can be individually updated. Other channels not updated maintain their previous analog output values.
- **Simultaneous Output Control -** All output channels are simultaneously updated upon issue of a software or external trigger.
- **Hardware Jumper Setting For Selection of DAC Ranges** - Both bipolar (±5V, ±10V) and unipolar (0 to 10V) ranges are available. These ranges can be selected on a per channel basis.
- **External Trigger Scan Mode** - All channels simultaneously implement a new conversion with each external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Output** - The external trigger is assigned to a field I/O line. The external trigger may be configured as an output signal to provide a means to synchronize other PMC230 devices to a master PMC230 module.

PCI MEZZANINE CARD INTERFACE FEATURES

- **High density -** Single-width PMC Target module.
- **Field Connections –** All analog output, and external power connections are made through a single 50-pin SCSI-2 front panel I/O connector.
- **16-bit I/O** - Control register writes, DAC writes, and calibration coefficient reads are performed through 16-bit data transfer cycles in the PCI memory space.
- **Compatibility** – IEEE P1386.1 PMC module which complies to PCI Local Bus Specification Revision 2.2. Provides one multifunction interrupt. 5V signaling compliant and 3.3V signaling tolerant.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This PMC Module will mate directly to any standard PMC carrier/CPU board that supports one single width PMC mezzanine module. Once connected, the module is accessed via a 50 pin front panel connector.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the 16-bit PMC230 analog output module, use of the shortest possible length of shielded cable is recommended.

Cables:

Model 5025-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting the PMC230 module to Model 5025-552 termination panels.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag PMC230, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

PMC MODULE ActiveX CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of PMC module ActiveX (Object Linking and Embedding) controls for Windows 98, 95®, ME, 2000 and Windows NT® compatible application programs (Model PMCSW- ATX, MSDOS format). This software provides individual controls that allow Acromag PMC modules to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® 97 applications and others. The ActiveX controls provide a high-level interface to PMC modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC module.

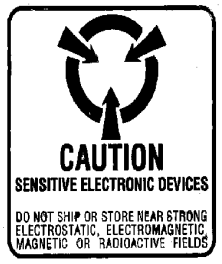
PMC MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of PMC module VxWorks® libraries. This software (Model PMCSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC modules.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.



For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier/CPU board, plus the installed PMC modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

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The dense packing of the PMC modules to the carrier/CPU board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. Jumper settings are discussed in the following sections. The jumper locations are shown in Drawing 4501-863.

Remove power from the board when configuring hardware jumpers, installing PMC modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-859 and the following paragraphs for configuration and assembly instructions.

Default Hardware Jumper Configuration

The board is shipped from the factory, configured as follows:

- Each analog output range is configured for a bipolar output with a 20 volt span (i.e. a DAC output range of -10 to +10 Volts).
- The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired mode before starting DAC analog output conversions.

Analog Output Ranges and Corresponding Digital Codes

The PMC230 is designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. Table 2.1 indicates the relationship between the data format and the ideal analog output voltage for each of the analog output ranges. Selection of an analog output range is implemented via the jumper settings given in Table 2.2.

Table 2.1: Full-Scale Ranges and Ideal Analog Output

DESCRIPTION	Digital Output Code	ANALOG OUTPUT		
Output Range		±10V	0 to 10V	±5V
LSB (Least Significant Bit) Weight		305µV	153µV	153µV
+ Full Scale Minus One LSB	$7FFF_H$	9.999695 Volts	9.999847 Volts	4.999847 Volts
Midscale	0000_H	0V[1]	5V[1]	0V[1]
One LSB Below Midscale	$FFFF_H$	-305µV	4.999847 Volts	-153µV
- Full Scale	8000_H	-10V	0V	-5V

Notes (Table2.1):

1. Upon power-up or software reset the bipolar ranges will output 0 volts while the unipolar range will output 5 volts.

Analog Output Range Hardware Jumper Configuration

The output range of the DACs are individually programmed via hardware jumpers J3 to J10. Jumpers J3 to J10 are used to control channels 0 to 7, respectively. The jumpers control the output voltage span and the selection of unipolar or bipolar output ranges. J3 to J10 pins 1 and 2 control the selection of unipolar or bipolar output ranges. J3 to J10 pins 3 and 4 control the selection of output voltage span. The configuration of the jumpers for the different ranges is shown in Table 2.2. "ON" means that the pins are shorted together with a shorting clip. "OFF" means that the clip has been removed. The individual jumper locations are shown in Drawing 4501-863.

Table 2.2: Analog Output Range Selections/Jumper Settings

Desired ADC Output Range (VDC)	Output Span (Volts)	Required Output Type	J3 to J10 Pins (1&2)	J3 to J10 Pins (3&4)
-5 to +5	10	Bipolar	ON	ON
-10 to +10**	20	Bipolar	ON	OFF
0 to +10	10	Unipolar	OFF	ON

****** The board is shipped with the default jumper setting for the ±10 volt DAC output range.

Software Configuration

Software configurable control registers are provided for control of external trigger mode and conversion mode selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as desired before starting DAC analog output conversions. Refer to section 3 for programming details.

CONNECTORS

Front Panel Field I/O Connector P1

The front panel connector P1 provides the field I/O interface connections. P1 is a SCSI-2 50-pin female connector (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the front panel via round shielded cable (Model 5028-187).

Front panel connector P1 pin assignments are shown in Table 2.3. When reading Table 2.3 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively. Further, note the output signals all have the same ground reference ("-CH00" and the minus leads of all other channels are connected to analog common on the module).

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Table 2.3: PMC230 Field I/O Pin Connections for P1

Pin Description	Number	Pin Description	Number
+CH00	1	COMMON[1]	26
-CH00[1]	2	COMMON[1]	27
COMMON[1]	3	COMMON[1]	28
+CH01	4	COMMON[1]	29
-CH01[1]	5	COMMON[1]	30
COMMON[1]	6	COMMON[1]	31
+CH02	7	COMMON[1]	32
-CH02[1]	8	COMMON[1]	33
COMMON[1]	9	COMMON[1]	34
+CH03	10	COMMON[1]	35
-CH03[1]	11	COMMON[1]	36
COMMON[1]	12	COMMON[1]	37
+CH04	13	COMMON[1]	38
-CH04[1]	14	COMMON[1]	39
COMMON[1]	15	COMMON[1]	40
+CH05	16	COMMON[1]	41
-CH05[1]	17	COMMON[1]	42
COMMON[1]	18	COMMON[1]	43
+CH06	19	COMMON[1]	44
-CH06[1]	20	COMMON[1]	45
COMMON[1]	21	COMMON[1]	46
+CH07	22	COMMON[1]	47
-CH07[1]	23	COMMON[1]	48
COMMON[1]	24	EXT TRIGGER*	49
COMMON[1]	25	SHIELD	50

Notes:

1. The minus leads of all channels are connected to analog common on the module.

Analog Outputs: Noise and Grounding Considerations

All output channels are referenced to analog common on the module (See Drawing 4501-864 for analog output connections), but each channel has a separate return (minus lead) to maintain accuracy and reduce noise. Still, the accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads > 100KΩ) provide the best accuracy. For low impedance loads, the PMC230 can source up to 5mA, but the effects of source and cabling resistance should be considered.

Output common is electrically connected to the PMC module analog ground which connects to logic ground of the module at the DAC's. As such, the PMC230 is non-isolated between the logic and field I/O grounds. Consequently, the field I/O connections are not isolated from the carrier/CPU board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog outputs when a high level of accuracy/resolution is needed. Refer to Drawing 4501-864 for example output and grounding connections.

External Trigger Input/Output

The external trigger signal on pin 49 of the P1 connector can be programmed to accept a TTL compatible external trigger input signal, or output hardware timer generated triggers to allow synchronization of multiple PMC230 modules.

As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The trigger pulse must be low for a minimum of 125n seconds to guarantee acquisition. It must not stay low for more than 6μ seconds, or additional, unwanted conversions may be triggered. The actual conversion is triggered within 6.25μ seconds of the falling edge of the external trigger signal. This type of conversion triggering can be used to synchronize generation of analog output signals to external events.

As an output an active-low TTL signal can be driven to additional PMC230s, thus providing a means to synchronize the conversions of multiple PMC230s. The additional PMC230s must program their external trigger for signal input and convert on external trigger only mode. The trigger pulse generated is low for typically 125n seconds. See section 3.0 for programming details to make use of this signal.

PCI Local Bus Connector

The PMC230 module provides a 32-bit PCI interface to the carrier/CPU via two 64 pin connectors. These connectors are 64-pin female receptacle header (AMP 120527-1 or equivalent) which mates to the male connector of the carrier/CPU board (AMP 120521-1 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric screws and spacers are supplied with the PMC module to provide additional stability for harsh environments (see Drawing 4501-859 for assembly details). The pin assignments of the PCI local bus connector are standard for all PMC modules according to the PCI Mezzanine Card Specification (see Tables 2.4 and 2.5).

Table 2.4: PMC Connector Pin Assignments for J1 (32-bit PCI)

Signal Name	Pin #	Signal Name	Pin #
TCK	1	-12V	2
GND	3	INTA#	4
INTB#	5	***INTC#***	6
BUSMODE1#	7	+5V	8
INTD#	9	***PCI-RSVD****	10
GND	11	***PCI-RSVD****	12
CLK	13	GND	14
GND	15	***GNT#***	16
REQ#	17	+5V	18
V(I/O)	19	AD[31]	20
AD[28]	21	AD[27]	22
AD[25]	23	GND	24
GND	25	C/BE[3]#	26
AD[22]	27	AD[21]	28
AD[19]	29	+5V	30
V(I/O)	31	AD[17]	32
FRAME#	33	GND	34
GND	35	IRDY#	36
DEVSEL#	37	+5V	38
GND	39	***LOCK#***	40
SDONE#	41	***SBO#***	42
PAR	43	GND	44
V(I/O)	45	AD[15]	46
AD[12]	47	AD[11]	48
AD[09]	49	+5V	50
GND	51	C/BE[0]#	52
AD[06]	53	AD[05]	54
AD[04]	55	GND	56
V(I/O)	57	AD[03]	58
AD[02]	59	AD[01]	60
AD[00]	61	+5V	62
GND	63	***REQ64#***	64

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# Indicates that the signal is active low.
BOLD ITALIC Signals are NOT USED by this PMC Model.

Table 2.5: PMC Connector Pin Assignments for J2 (32-bit PCI)

Signal Name	Pin #	Signal Name	Pin #
+12V	1	***TRST#***	2
TMS	3	***TDO***	4
TDI	5	GND	6
GND	7	***PCI-RSVD****	8
PCI-RSVD*	9	***PCI-RSVD****	10
BUSMODE2#	11	+3.3V	12
RST#	13	BUSMODE3#	14
+3.3V	15	BUSMODE4#	16
PCI-RSVD*	17	GND	18
AD[30]	19	AD[29]	20
GND	21	AD[26]	22
AD[24]	23	+3.3V	24
IDSEL	25	AD[23]	26
+3.3V	27	AD[20]	28
AD[18]	29	+GND	30
AD[16]	31	C/BE[2]#	32
GND	33	***PCI-RSVD***	34
TRDY#	35	+3.3V	36
GND	37	STOP#	38
PERR#	39	GND	40
+3.3V	41	SERR#	42
C/BE[1]#	43	GND	44
AD[14]	45	AD[13]	46
GND	47	AD[10]	48
AD[08]	49	+3.3V	50
AD[07]	51	***PCI-RSVD***	52
+3.3V	53	***PCI-RSVD***	54
PCI-RSVD	55	GND	56
PCI-RSVD	57	***PCI-RSVD***	58
GND	59	***PCI-RSVD***	60
ACK64#	61	+3.3V	62
GND	63	***PCI-RSVD***	64

# Indicates that the signal is active low.
BOLD ITALIC Signals are NOT USED by this PMC Model.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the PMC230 module.

This Acromag PMC230 is a PCI Local Bus Specification version 2.2 compliant PCI bus target only PMC module. The carrier/CPU connects a PCI host bus to the PMC module.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The PMC module can be accessed via the PCI bus memory space and configuration spaces, only.

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PMC230 module is a Plug-and-Play PCI card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to access a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the PMC module requires. It then programs the PMC module's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PMC module requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PMC module.

Since this PMC module is relocatable and not fixed in address space, this module's device driver must use the mapping information stored in the module's Configuration Space registers to determine where the module is mapped in memory space.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This PMC module provides 256 bytes of configuration registers for this purpose. The PMC230 contains the configuration registers, shown in Table 3.1, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers which must be read to determine the base address assigned to the PMC230.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=4A56		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for PMC230 4K-Byte Block			
5 : 10	Not Used			
11	Subsystem ID=0000		Subsystem Vendor ID=0000	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Not Used	

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCI bus memory space to control the programming of analog outputs to the field. As such, three types of information are stored in the memory space: control, status, and data.

The memory space address map for the PMC230 is shown in Table 3.2. Note that the base address for the PMC230 in memory space must be added to the addresses shown to properly access the PMC230 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the PMC230 are accessed via data lines D0 to D15. The most significant word of a

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32-bit access is not used by the PMC230. A 32-bit read will return logic "0" for the most significant word.

Table 3.2: PMC230 Memory Map

Hex Base Adr+	MSB D15 D08	LSB D07 D00	Hex Base Adr+
201	Control Register		200
205	Not Used[1]	Not Used[1]	204
209	Not Used[1]		208
20D	Not Used[1]		20C
211	Not Used[1]		210
215	Rd Wr~ / Calibration Coefficient Address	Calibration Coefficient Write Data	214
219	Calibration Coefficient Read Data	Wr Busy / Rd Comp	218
21D	Not Used Bits15 to Bit 01	Start Convert Bit-0	21C
221	DAC Channel 0		220
225	DAC Channel 1		224
229	DAC Channel 2		228
22D	DAC Channel 3		22C
231	DAC Channel 4		230
235	DAC Channel 5		234
239	DAC Channel 6		238
23D	DAC Channel 7		23C
241	Not Used[1]	Not Used[1]	240
245	Reserved[2]	Not Used[1]	244
249 ↓ 2FD	NOT USED[1]		248 ↓ 2FC

Notes (Table 3.2):

1. The PMC will respond to addresses that are "Not Used".
2. This byte is reserved for use at the factory to enable writing of the calibration coefficients.
3. All writes are 8 clock cycles (except when a previous write is in progress. In this case the write cycle will disconnect with retry).
4. All initial reads will disconnect without data and a retry will be issued.

This memory map reflects byte accesses using the "Little Endian" byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses "Little Endian" byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Control Register, (Read/Write) - (Base + 200H)

This read/write register is used to: control the external trigger, select one of the digital-to-analog conversion modes, and issue a software reset.

The function of each of the control register bits are described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.3: Control Register

BIT	FUNCTION
2,1,0	Not Used[1]
3	Not Used[1]
4	Not Used[1]
6, 5	External Trigger Control 00 = External Trigger Input: External and Software triggers are all enabled 01 = External Trigger Input: External triggers are only enabled. Software triggers are disabled. 10 = External Trigger Output: Software triggers are output on the External trigger pin of the field I/O connector. It is possible to synchronize the conversion of multiple PMC230 modules. A single master PMC230 must be selected to output the external trigger signal (bit 6 and 5 set to "10") while all other modules are selected to input the external trigger signal (bit 6 and 5 set to "01"). The external trigger signals (pin 49 of the field I/O connector) of all modules to be synchronized must be wired together.
7	Not Used[1]
10, 9, 8	DAC Conversion Mode 000 = Disabled 001 = Single Conversion from DAC registers 010 = Not Defined 011 = Not Defined 100 = Not Defined 101 = Not Defined 110, 111 = Not Defined All modes require either the software start convert or an external trigger to initiate DAC conversions.
11 to 14	Not Used[2]
15	Perform Software Reset when Set[2]

Notes (Table 3.3):

1. All bits labeled "Not Used" will return the last value written on a read access.
2. Bits 11 to 15 will return random values when read.

Calibration Coefficient Access Register (Write, 215H)

This register configures access to the calibration coefficient memory. Calibration data is provided so that software can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in this memory. These coefficients can be retrieved using this register.

The Calibration Coefficient Access Register is a write-only register and is used to configure and initiate a read cycle to the calibration coefficient memory. Setting bit-15 of this register high, to a "1", initiates a read cycle.

The address of the calibration coefficient to be read must be specified on bits 14 to 8 of Calibration Coefficient Access register. The address location of each of the gain and offset coefficients is given in table 3.4.

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Most Significant Byte of Calibration Coefficient Access Reg	
Read or Write~	Calibration Coefficient Address
15	14, 13, 12, 11, 10, 9, 8

Write accesses to the Calibration Coefficient Access register require one wait state and are possible via 16-bit data transfers only. A software or hardware reset has no affect on this register.

The address location of each of the gain and offset coefficients is given in table 3.4. The address corresponding to each of the offset and gain coefficients for each of the channels and ranges is given in hex. The coefficients are 16-bit values with the most significant byte at the even addresses and the least significant bytes at the odd addresses. The calibration coefficients are stored as 1/4 LSB's. For additional details on the use of the calibration coefficients, refer to the "Use of Calibration Data" section.

Table 3.4: Offset and Gain Address Memory Map

Channel		Offset Coefficient Address (Hex)		Gain Coefficient Address (Hex)	
		MSB	LSB	MSB	LSB
±10 Volt Range	0	00	01	02	03
	1	04	05	06	07
	2	08	09	0A	0B
	3	0C	0D	0E	0F
	4	10	11	12	13
	5	14	15	16	17
	6	18	19	1A	1B
	7	1C	1D	1E	1F
±5 Volt Range	0	20	21	22	23
	1	24	25	26	27
	2	28	29	2A	2B
	3	2C	2D	2E	2F
	4	30	31	32	33
	5	34	35	36	37
	6	38	39	3A	3B
	7	3C	3D	3E	3F
0 to 10 Volt Range	0	40	41	42	43
	1	44	45	46	47
	2	48	49	4A	4B
	3	4C	4D	4E	4F
	4	50	51	52	53
	5	54	55	56	57
	6	58	59	5A	5B
	7	5C	5D	5E	5F

Calibration Coefficient Status Register (Read, 219H)

The Calibration Coefficient Status register is a read-only register and is used to access the calibration coefficient read data and determine the status of a read cycle initiated by the Calibration Coefficient Access register. In addition, this register is used to determine the status of a write cycle to the coefficient memory. Bit-1 of this register when set indicates the coefficient memory is busy completing a write cycle.

All read accesses to the Calibration Coefficient Status register initiate an approximately 1m second access to the coefficient memory. **Thus, you must wait 1m second after reading this status register before a new read or write cycle to the coefficient memory can be initiated. If not you will get invalid data.**

A read request of the coefficient memory, initiated through the Calibration Coefficient Access register, will provide the addressed byte of the calibration coefficient on data bits 15 to 8 of the Calibration Coefficient Status register. Although the read request via the Calibration Coefficient Access register is accomplished in less then 800n seconds, typically, the calibration coefficient will not be available in the Calibration Coefficient Status register for approximately 2.5m seconds.

Bit-0 of the Calibration Coefficient Status register is the read complete status bit. This bit will be set high to indicate that the requested calibration coefficient is available on data bits 15 to 8 of this status register. This bit is cleared upon initiation of a new read access of the coefficient memory or upon issue of a software or hardware reset.

Writes to calibration coefficient memory require a special enable code. Writes to coefficient memory are normally only performed at the factory. The module should be returned to Acromag if recalibration is needed.

A write operation to the calibration coefficient memory, initiated via the Calibration Coefficient Access register, will take approximately 5m seconds. Bit-1 of the Calibration Coefficient Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation, and bit-1 will remain high until the requested write operation has completed. New read or write accesses to the coefficient memory, via the Calibration Coefficient Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A software or hardware reset of the PMC module will also clear this bit to 0.

Read accesses to Calibration Coefficient Status register require one wait state and are possible via 16-bit data transfers only. A software or hardware reset will clear all bits to 0.

Start Convert Register (Write Only, 21CH)

The Start Convert register is a write-only register and is used to trigger conversions by setting data bit-0 to a logic one. The desired mode of conversion must first be configured by setting the Control register.

This register can be written with either a 16-bit or 8-bit data value. Data bit-0 must be a logic one to initiate data conversions.

When External Trigger Only mode is selected via bits 6 and 5 of the control register (set to "01"), the Software Start Convert bit is disabled from starting data conversions.

Start Convert Register							
Not Used							Start Convert
07	06	05	04	03	02	01	00

The actual conversion will be initiated 6.625µ seconds after setting the Start Convert Bit. Thus in single conversion mode, you cannot reload the DAC registers with new data until at least 6.625µ seconds after a start convert.

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DAC Channel Registers (Write Only, 220H to 23CH)

The DAC Channel registers are write only registers and are used to hold the 16-bit digital values that are to be output to the Digital-to-Analog-Converter's (DAC's). The contents of the DAC registers are simultaneously transferred to their corresponding converter upon issue of a software or external trigger.

Table 3.2 lists each of the DAC Channel registers with their corresponding hex address in memory space.

Writing these registers is possible via 16 or 8 bit data transfers. Software or hardware resets will clear the contents of the DAC Channel registers to 0.

DAC MODES OF CONVERSION

The PMC230 provides two methods of trigggering analog output updates. The following sections describe the features of each and how to best use them.

Single Conversion from DAC Register-Mode

This mode of operation can be used on the PMC230 module. It can be used to update from a single DAC channel to all DAC channels with a new analog output voltage. With each conversion, initiated by a software or external trigger, the digital values in each of the DAC Channel registers are simultaneously moved to their corresponding converter for update of their analog output signal. It is possible to keep a given channel's analog voltage unchanged by simply keeping the digital value in the channel's DAC register unchanged. Only those channels with updated digital values in their corresponding DAC Channel registers will result in different analog output voltages.

Each of the DAC Channel register's digital values is moved to its corresponding converter for simultaneous conversion upon issue of a software or external trigger.

Convert On External Trigger Only

When bit-6 and 5 of the control register are set to digital code "01", each conversion is initiated by an external trigger only (logic low pulse) input to the EXT TRIGGER* signal of the P1 connector. Conversions are performed for each channel simultaneously with each external trigger pulse. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation.

The external trigger signal is configured as an input for this mode of operation.

External Trigger Only mode of operation can be used to synchronize multiple PMC230 modules to a single module running in a continuous cycle mode. The external trigger, of the PMC230 "master", must be programmed as an output. The external trigger signal of that PMC230 must then be connected to the external trigger signal of all other PMC230 modules, programmed for external trigger input, that are to be synchronized. These other PMC230 modules must be programmed for External Trigger Input only mode. Data conversion can then be started by writing high to the Start Convert bit of the master PMC230 configured for continuous cycle mode.

PROGRAMMING CONSIDERATIONS FOR GENERATION OF ANALOG OUTPUTS

The PMC230 provides different methods of analog output generation to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion from DAC Register Example

1. Execute Write of 0100H to Control Register at Base Address + 200H.
   a) External, Software, and Hardware timer genterated triggers are all enabled.
   b) Single Conversion from DAC registers is enabled.

2. Execute Write of 7FFFH to each DAC Channel Register starting at Base Address + 220H. This will drive each analog output to plus full scale minus one least significant bit.

3. Execute Write 0001H to the Start Convert Bit at Base Address + 21CH. This starts the simultaneous transfer of the digital data in each DAC Channel register to its corresponding converter for analog conversion.

USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in memory. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs.

Software calibration uses some fairly complex equations. Acromag recommends purchase of our ActiveX® or VxWorks® software to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). See the specification chapter for details regarding maximum uncalibrated error.

Calibrated Performance

Accurate calibration of the PMC230 can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in memory as (1/4 LSB's) for each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage. See the specification chapter for details regarding maximum calibrated error.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (Ideal_count)

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written to the 16-bit DAC to achieve a specified voltage within the selected output range.

Equation (1):

$$\text{Ideal_ Count} = \left[\frac{\text{Count_ Span} * \text{Desired_ Voltage}}{\text{Ideal_ Volt_ Span}} \right]$$

where,

Count_Span = 65,536 (a 16-bit converter has 2^{16} possible levels)
Ideal_Volt_Span = 20 Volts (for the bipolar -10 to +10 Volt range)
= 10 Volts (for the bipolar ±5 or unipolar 0 to 10 volt ranges).

Using equation (1), one can determine the ideal count for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts for the bipolar ±10 volt range, the Ideal_Count of 16,384 results. If this value is used to program the DAC output, the output value will approach +5 Volts to within the uncalibrated error. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal_Count into the Corrected_Count required to accurately produce the output voltage. This is illustrated in the next equation.

Equation (2):

$$\text{Corrected_ Count} = \text{Ideal_ Count} * \left[1 + \text{Gain_ Correction}\right] + \text{Offset_ Correction} + \text{Ideal_ Zero_ Count}$$

where,

Gain_Correction = Stored_Gain_Error / (4*65,536)
Offset_Correction = Stored_Offset_Error / 4
Ideal_Zero_Count = 0 for bipolar ±5 and ±10 volt ranges
-32,768 for unipolar 0 to 10 volt range

Ideal_Count is determined from equation (1) given above. Stored_Gain_Error and Stored_Offset_Error are written at the factory and are obtained from memory on the PMC230 on a per channel basis. The Stored_Gain_Error and Stored_Offset_Error are stored in memory as two's complement numbers. Refer to the "Calibration Coefficient Access Register" section for details on how to read the coefficients from memory.

Using equation (2), you can determine the corrected count from the ideal count. For the previous example, equation (1) returned a result 16,384 for the Ideal_Count to produce an output of +5 Volts. Assuming that a gain error of -185 and an offset error of -43 are read from memory on the PMC230 for the desired channel, substitution into equation (2) yields:

$$\text{Corrected_ Count} = 16{,}384 * \left[1 + \frac{-185}{4*65536}\right] - \frac{43}{4} = 16{,}361.6875$$

If this value (rounded to 16,362) is used to program the DAC output, the output value will approach +5 Volts to within the calibrated error (see the specification chapter for details regarding maximum calibrated error).

Calibration Programming Example

Assume it is necessary to program channel 0 with an output of -2.5 Volts. Also assume the bipolar range centered around 0 Volts is -10 to +10 Volts.

The Single Conversion from DAC Register mode of operation, which is available on the PMC230 module, is used in this example.

1. Execute Write of 0100H to Control Register at Base Address + 200H.
   a) External, Software, and Internal Hardware timer generated triggers are all enabled.
   b) Single Conversion from DAC registers is enabled.

2. Read the calibration memory to retrieve channel 0's unique offset coefficient. To obtain the 16-bit offset coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8000H at Base Address + 214H. The offset coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contain the most significant byte of the offset coefficient.

   To initiate a read of channel 0's least significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8100H at Base Address + 214H. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the offset coefficient.

3. Read the calibration memory to retrieve channel 0's unique 16-bit gain coefficient. To obtain the 16-bit gain coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8200H at Base Address + 214H. The gain coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contains the most significant byte of the gain coefficient.

   To initiate a read of channel 0's least significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8300H at Base Address + 214H. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the gain coefficient.

4. Calculate the Ideal_Count required to provide an uncorrected output of the desired value (-2.5 Volts) by using equation (1).
   Ideal_Count = [65,536×(-2.5)]/20 = -8,192.0

5. Calculate the Corrected_Count required to provide an accurate output of the desired value (-2.5 Volts) by using equation (2). Assume the offset and gain coefficients are -43 and -185 respectively.
   Corrected_Count = -8,192.0×[1 + -185/(4×65,536)] - 43/4 = -8,196.9687. This value is rounded to -8,197 and is equivalent to DFFB hex as a 2's complement value.

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6. Execute Write of DFFB hex to the DAC Channel 0 Register at Base Address + 220H.

7. Execute Write 0001H to the Start Convert Bit at Base Address + 21CH. This starts the simultaneous transfer of the digital data in each DAC Channel register to its corresponding converter for analog conversions. This will drive channel 0's analog output to -2.5 volts.

8. (OPTIONAL) Observe or monitor that the specific DAC channel (0) reflects the results of the digital data converted to an analog output voltage at the field connector.

Error checking should be performed on the calculated count values to insure that calculated values below 0 or above 65535 decimal are restricted to those end points. Note that the software calibration cannot generate outputs near the endpoints of the range which are clipped off due to hardware limitations(i.e. the DAC).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the PMC230. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-865 as you review this material.

FIELD ANALOG OUTPUTS

The field I/O interface to the PMC230 is provided through the front panel connector P1 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-864 for example wiring and grounding connections.

Jumpers on the board control the range selection for the DACs (-5 to +5, -10 to +10, and 0 to 10 Volts) as detailed in chapter 2. Jumper selection should be made prior to powering the unit. Channels may use different ranges.

PMC230 CONTROL LOGIC

All logic to control data conversions is imbedded in the PMC module's FPGA. The control logic of the PMC230 is responsible for controlling the operation of a user specified mode of data conversions. Once the PMC module has been configured, the control logic performs the following:

- Controls serial transfer of data from the FPGA to the individual DAC registers based on the selected mode of operation.
- Provides external or internal trigger control.
- Controls read and write access to calibration memory.

DATA TRANSFER FROM FPGA To INDIVIDUAL DACs

A 16-bit serial shift register is implemented in the PMC230 module's FPGA for each of the supported channels. These serial shift registers are referred to as the individual DAC registers in the memory map. To control transfer of digital data to the individual converters, internal FPGA counters are used to synchronize the simultaneous transfer of serial shift register data to the corresponding converter.

The DACs can be updated with new digital values or left unchanged. The DACs are updated by first writing the individual DAC registers, resident in the FPGA. Then, upon issue of a trigger (software or external), the contents of the DAC registers are simultaneously transferred to the DACs.

EXTERNAL TRIGGER

The external trigger connection is made via pin 49 of the P1 Field I/O Connector. For all modes of operation, when external trigger input is enabled via bits 6 and 5 of the control register, the falling edge of the external trigger will start the simultaneous conversion of all channels. For External Trigger Only mode (bits 6 and 5 set to "01"), each falling edge of the external trigger causes a conversion at the DAC. Once the external trigger signal has been driven low, it should remain low for a minimum of 125n seconds and a maximum of 6μ seconds, or additional unwanted conversions may be triggered.

CALIBRATION MEMORY CONTROL LOGIC

The FPGAs of the PMC230 modules contain control logic that implements read and write access to calibration memory. The calibration memory (EEPROM) contains offset and gain coefficients for each of the ranges and channels. Calibration of the individual DACs is implemented via software to avoid the mechanical drawbacks of hardware potentiometers.

PCI INTERFACE LOGIC

The PCI bus interface logic is imbedded within an FPGA. This logic includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCI target interface performs parity error detection, uses a single 4K base address register, and implements target abort, retry, and disconnect. J1 and J2 connectors also provide ±12V and +5V to power the module.

A PCI bus read of the PMC module will initially terminate with a retry. While the read data is moved to the read register (typically 1000ns), continued retries will result in retry terminations. The retry termination allows the PCI bus to be free for other system operations while the data is moved to the read register.

A PCI bus write to the PMC module will result in 1) immmediately accepting the write data and normal cycle termination or 2) issue of a retry termination. A retry termination will be issued if the previous write cycle has not completed on the PMC module. It will typically take the PMC module 1000ns to write the data to the required internal register. Thus if another write cycle is initiated on the PCI bus before the typical 1000ns has lapsed, the write cycle will be terminated with a retry.

A programmable logic device provides the control signals required to operate the board. It decodes the selected addresses and produces the chip selects, control signals, timing required by the DAC's, and software registers. It also controls the mode selection and triggering to start DAC conversions for the Transparent and Simultaneous Modes.

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The Calibration PROM contains channel specific calibration coefficients to correct both offset and gain errors. The coefficients must be used to trim the outputs to within their accuracy specification. The PROM, software registers, and DAC's are all accessed through the PCI bus interface.

PMC Module Software

Acromag also provides a software diskette (sold separately) consisting of PMC module ActiveX® controls for Windows 98, 95®, ME, 2000 and Windows NT® compatible application programs (Model PMCSW-ATX, MSDOS format). This software provides individual controls that allow all PMC modules to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® 97 applications and others. The ActiveX® controls provide a high-level interface to PMC modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX® controls. These functions consist of an ActiveX® control for each Acromag PMC module.

In addition, Acromag provides a software product (sold separately) consisting of PMC module VxWorks® libraries. This software (Model PMCSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC modules.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Annual return of the PMC230 to Acromag for re-determination of the calibration coefficients is highly recommended. Corrected data accuracies depend heavily on the calibration coefficients being within specification. Field determination of calibration coefficients requires precision test equipment. Contact Acromag for technical assistance if field recalibration is needed.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration..... Single PMC Module.
Height..... 15.11 mm (0.595 in). (See Drawing 4501-859)
Stacking Height..... 10.0 mm (0.394 in).
Length..... 149.0 mm (5.866 in).
Width..... 74.0 mm (2.913 in).
Board Thickness..... 1.59 mm (0.062 in).

Connectors:
PCI Local Bus Interface..... Two 64-pin female receptacle header (AMP 120527-1 or equivalent).
Field I/O..... 50-pin, SCSI-2, female receptacle header (AMP 787082-5 or equivalent).

Power Requirements		PMC230-8
5V[1]	Typical	70 mA
(±5%)	Max.	100 mA
+12V	Typical	100 mA
(±5%)	Max.	140 mA
-12V	Typical	185 mA
(±5%)	Max.	225 mA

1. Maximum rise time of 100mS.

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ENVIRONMENTAL

Operating Temperature..... 0°C to +70°C
-40°C to +85°C (E Versions).

Note:
The extended temperature grade version of the DAC714 is no longer available from the manufacturer. Acromag has performed operational tests of sampled commercial grade components over the extended temperature range without failure. All DAC714s' used on the -E version of the PMC230 have been functionally tested by an independent third party laboratory for use in extended temperature applications, except for verification of analog output specifications.

Relative Humidity..... 5-95% Non-Condensing.
Storage Temperature..... -55°C to 105°C.
Non-Isolated..... Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI).. Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.25% of FSR.

Electromagnetic Interference Immunity (EMI)..... Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity..... Not required for signal I/O per European Norm EN50082-1.

ESD Protection..... Complies with IEC1000-2 Level 1 (2KV direct contact discharge at input/output terminals) and European Standard EN50082-1.

Electric Fast Transient Immunity (EFT)..... Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions ..... Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

Reliability Prediction

Mean Time Between Failure..... MTBF = TBD hours (not available at time of printing) @ 25°C, Using MIL-HDBK-217F, Notice 2.

ANALOG OUTPUTS

Output Channels (Field Access).. 8 Single Ended PMC230-8
Output Signal Type..... Voltage (Non-isolated).
Output Ranges[1] ..... Bipolar -5 to +5 Volts
(Jumper selected): Bipolar -10 to +10 Volts
Unipolar 0 to +10 Volts

Note (Analog Outputs):
1. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.

Output Current..... -5mA to +5mA (Maximum); this corresponds to a minimum load resistance of 2KΩ with a 10V output.
DAC Data Format..... Positive-true binary two's complement (BTC) input codes.
DAC Programming..... Simultaneous; Input registers of multiple DAC's are directly loaded with new data before simultaneously updating DAC outputs.
Resolution..... 16-bits.
Monotonicity over Temperature... 16-bits (PMC230)
15-bits (PMC230E).
Linearity Error..... ± 2 LSB (Maximum).
Differential Linearity Error..... ± 1 LSB (Maximum).

Maximum Overall Calibrated Error[2,3]

Max. Linearity Error LSB	Max. Offset Error LSB	Max. Gain Error LSB	Max. Total Error LSB (%)
± 2	± 1	± 1	± 4 (0.0061)

Notes (Calibrated Error):
2. Offset and gain calibration coefficients stored in the coefficient memory must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error and are with outputs unloaded. Follow the output connection recommendations of Chapter 2, to keep a non-ideal grounds from degrading overall system accuracy.
3. The maximum uncalibrated error combining the linearity, offset and gain errors is ± 0.453%.
DAC714HL @ 25°C:
Linearity Error is ± 0.003% maximum (i.e. ± 2 LSB).
Bipolar Offset Error is ± 0.2% FSR (i.e. 20V SPAN) max.
Gain Error is ± 0.25% maximum.

Settling Time..... 10uS to within 0.003% of FSR for a 20V step change (load of 5KΩ in parallel with 500pF).
Conversion Rate (per channel).... 150KHz Maximum, 100KHz recommended for specified accuracy.
Maximum Throughput..... 8 X conversion rate (PMC230-8)
8 X 150KHz=1.2MHz. maximum
8 X 100KHz=0.8MHz spec accur.
Output Noise..... 120 nV/√Hz typical
Output at Reset..... Bipolar Zero Volts.
Unipolar 5 Volts (See Note 4)
Board Warm-up Time..... 8 minutes minimum

Note (Analog Output):
4. The reset function resets the DAC analog output and the FPGA's internal DAC registers. Therefore, the DAC output will remain in their reset state after simultaneous DAC output updates until the DAC registers are overwritten with new data.

Output Impedence..... 0.1Ω Typical at 25°C
Short Circuit Protection ..... Indefinite at 25°C.

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External Trigger Input/Output

As An Input:.....Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered within 6.4μ seconds of the falling edge. Minimum pulse width 125n sec. Maximum pulse width 6μ seconds, otherwise, an additional trigger is produced.

As An Output:.....Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for 125n seconds, typical. A maximum of 4 loads are allowed.

PCI Local Bus Interface

Compatibility..... Conforms to PCI Local Bus Specification, Revision 2.2 and PMC Specification, P1386.1/Draft 2.4. (See Note 6)

Electrical/Mechanical Interface... Single-Width PMC Module.

PCI Target ..... Implemented by Altera FPGA.

4K Memory Space Required..... One Base Address Register.

PCI commands Supported..... Configuration Read/Write, Memory Read/Write, 32,16, and 8-bit data transfer types supported.

Signaling..... 5V Compliant, 3.3V Tolerant.

PCI bus Write Cycle Time[5]..... 150 nS Typical measured from falling edge of FRAME# to the falling edge of TRDY#.

PCI bus Read Cycle Time[5]..... 150 nS Typical.

Notes (PCI Local Bus Interface):

5. Although the typical read or write PCI bus cycle time is only 150 nS the actual read or write implemented on the PMC Module will be typically 1000 nS. Thus, the PMC Module will issue a RETRY when a new read or write cycle is implemented before the PMC module's 1000 nS read or write has completed. When the PMC Module issues a RETRY this frees the PCI bus while the previous read or write operation is completed.
6. Due to the unique modular nature of the PMC230 assembly, it is impossible to comply with the solder side component height per the PMC Mechanical Standand. Refer to Mechanical Assembly Drawing 4501-859 for details. You must determine whether there will be adequate clearance for your application.

APPENDIX

CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).

Application: Used to connect Model 5025-552 termination panel to the PMC230 Module.

Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other lenghts. It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.

Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.

Keying: The SCSI-2 connector has a "D Shell" and the IDC connector has a polarizing key to prevent improper installation.

Schematic and Physical Attributes: See Drawing 4501-758.

Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.'s).

Operating Temperature: -20°C to +80°C.

Storage Temperature: -40°C to +85°C.

Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For PMC Module Boards

Application: To connect field I/O signals to the PMC Module. *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the PMC Module via a flat ribbon cable (Model 5025-551-x). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to field I/O (pins 1-50) on the PMC module. Each PMC module has its own unique pin assignments. Refer to the PMC module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Mounting: Termination panel is snapped on the DIN mounting rail.

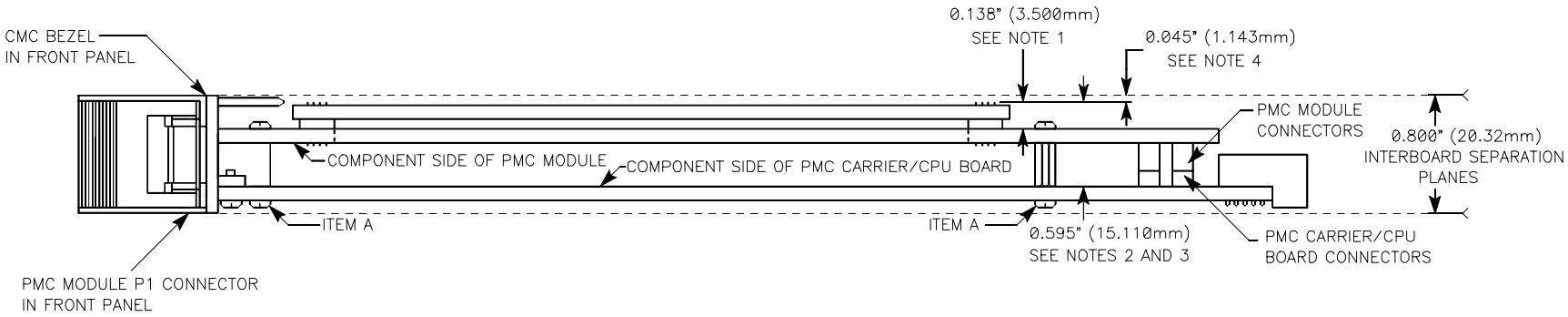
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

Storage Temperature: -40°C to +100°C.

Shipping Weight: 1.25 pounds (0.6kg) packaged.

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ASSEMBLY PROCEDURE:

1. INSERT PMC MODULE (P1 CONNECTOR SIDE) INTO THE CMC BEZEL IN THE FRONT PANEL OF THE PMC CARRIER/CPU BOARD. THEN, ALIGN THE CONNECTORS ON THE PMC MODULE AND PMC CARRIER/CPU BOARD. ONCE ALIGNED THEN PUSH TOGETHER. STACKING HEIGHT BETWEEN PMC MODULE AND PMC CARRIER/CPU BOARD IS 0.394" (10.000mm).

2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF PMC CARRIER/CPU BOARD AND INTO PMC MODULE AS SHOWN (4 PLACES). THEN TIGHTEN SCREWS.

NOTE:

1. THE USEABLE SPACE ON THE SOLDER SIDE OF THE PMC MODULE IS 0.075"(1.900mm) PER PMC MECHANICAL STANDARD P1386.1. THIS PMC MODULE EXCEEDS THIS BY 0.063" (1.600mm).

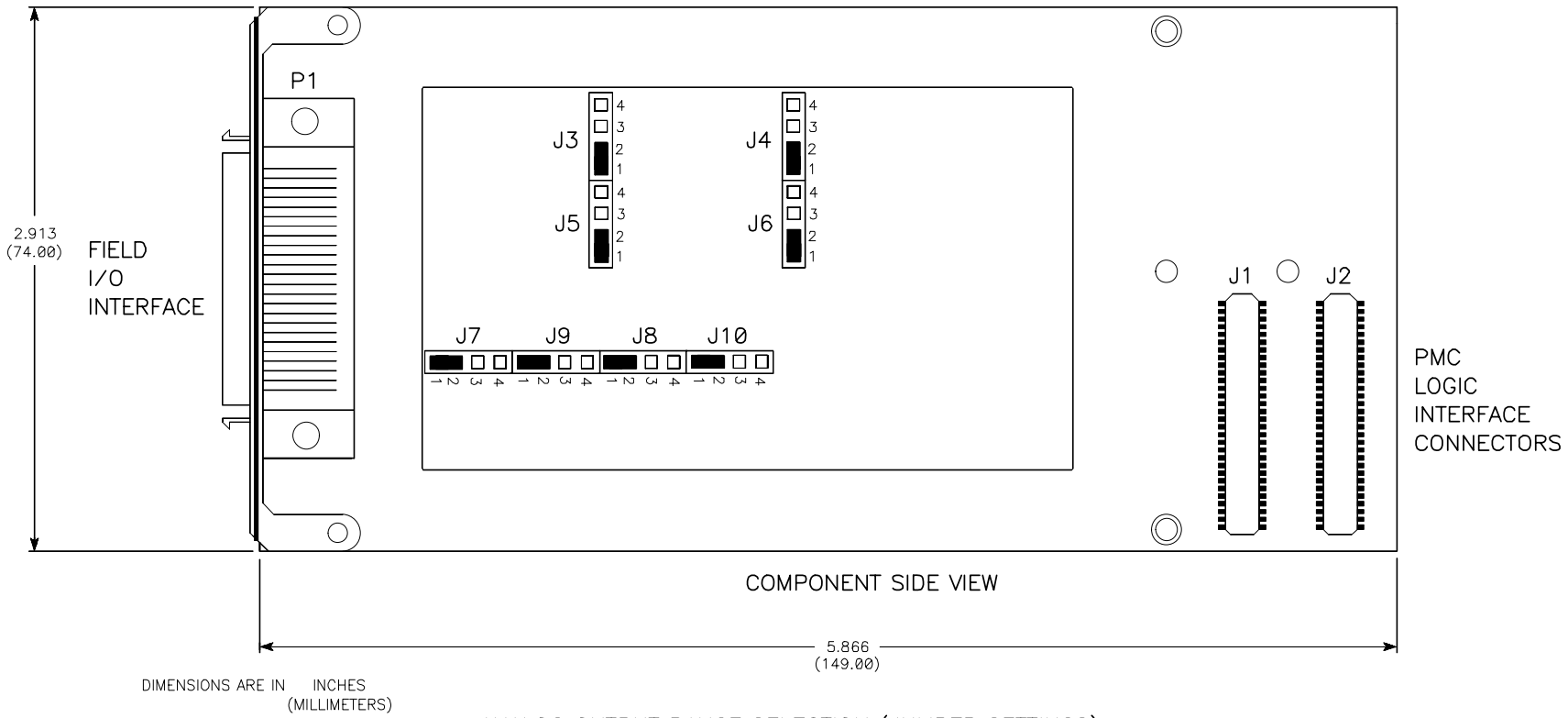
2. THE TOTAL HEIGHT OFF THE PMC CARRIER/CPU BOARD IS 0.532" (13.500mm) PER PMC MECHANICAL STANDARD P1386.1. THIS PMC MODULE EXCEEDS THIS BY 0.063" (1.600mm).

3. THE MAXIMUM COMPONENT HEIGHT FOR VME AND CompactPCI IS 0.540"(13.720mm). THIS PMC MODULE EXCEEDS THIS BY 0.055" (1.400mm).

4. DISTANCE TO INTERBOARD SEPARATION PLANE IS 0.045" (1.143mm). THE DESIRED SPACING IS 0.100" (2.540mm) FOR VME AND CompactPCI .

PMC MODULE TO PMC CARRIER/CPU BOARD MECHANICAL ASSEMBLY 4501-859A

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ANALOG OUTPUT RANGE SELECTION (JUMPER SETTINGS)

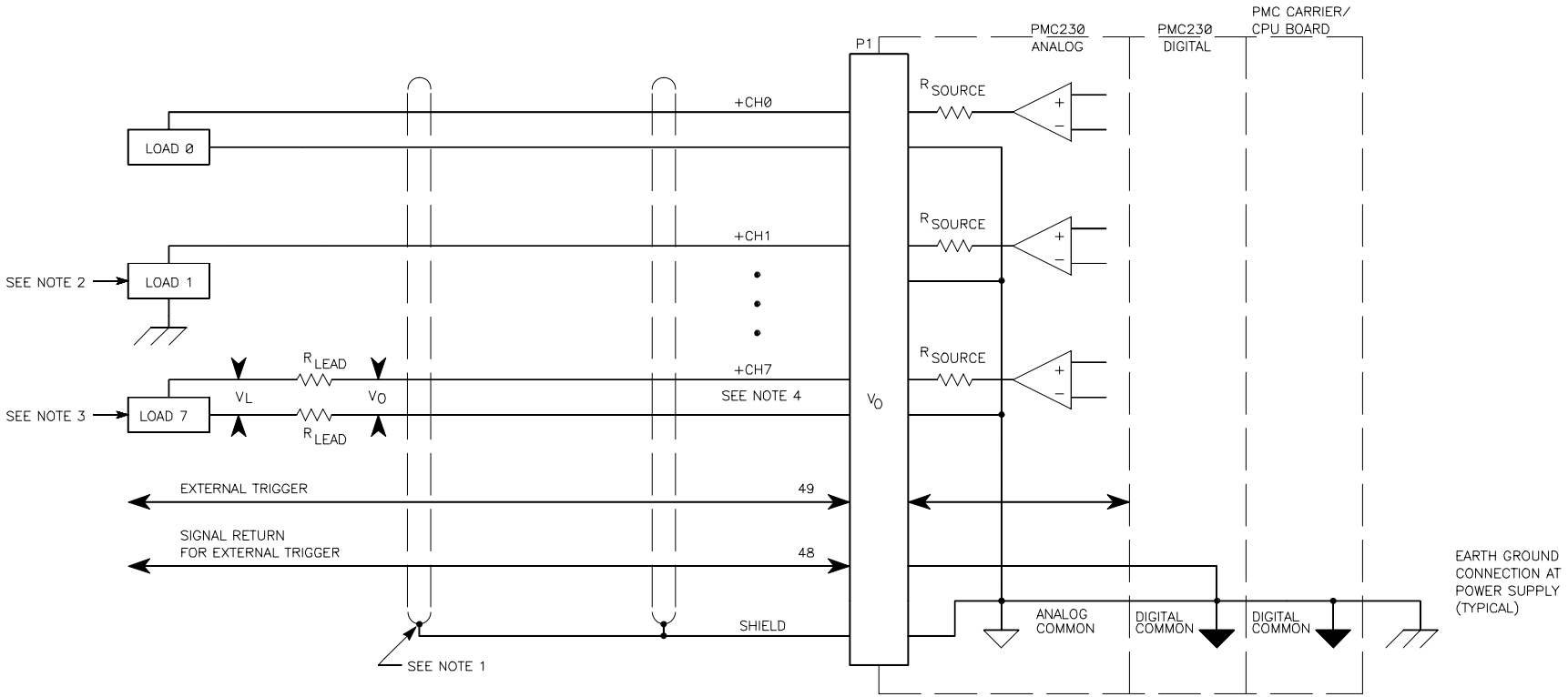
DESIRED ADC OUTPUT RANGE (VDC)	OUTPUT SPAN (VOLTS)	OUTPUT TYPE	J3 TO J10 PINS (1&2)	J3 TO J10 PINS (3&4)
−5 TO +5	10	BIPOLAR	ON	ON
−10 TO +10**	20	BIPOLAR	ON	OFF
0 TO +10	10	UNIPOLAR	OFF	ON

** THE BOARD IS SHIPPED WITH THE DEFAULT JUMPER SETTING FOR THE −10 TO +10 VOLT DAC OUTPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

PMC230 JUMPER LOCATIONS

4501−863B

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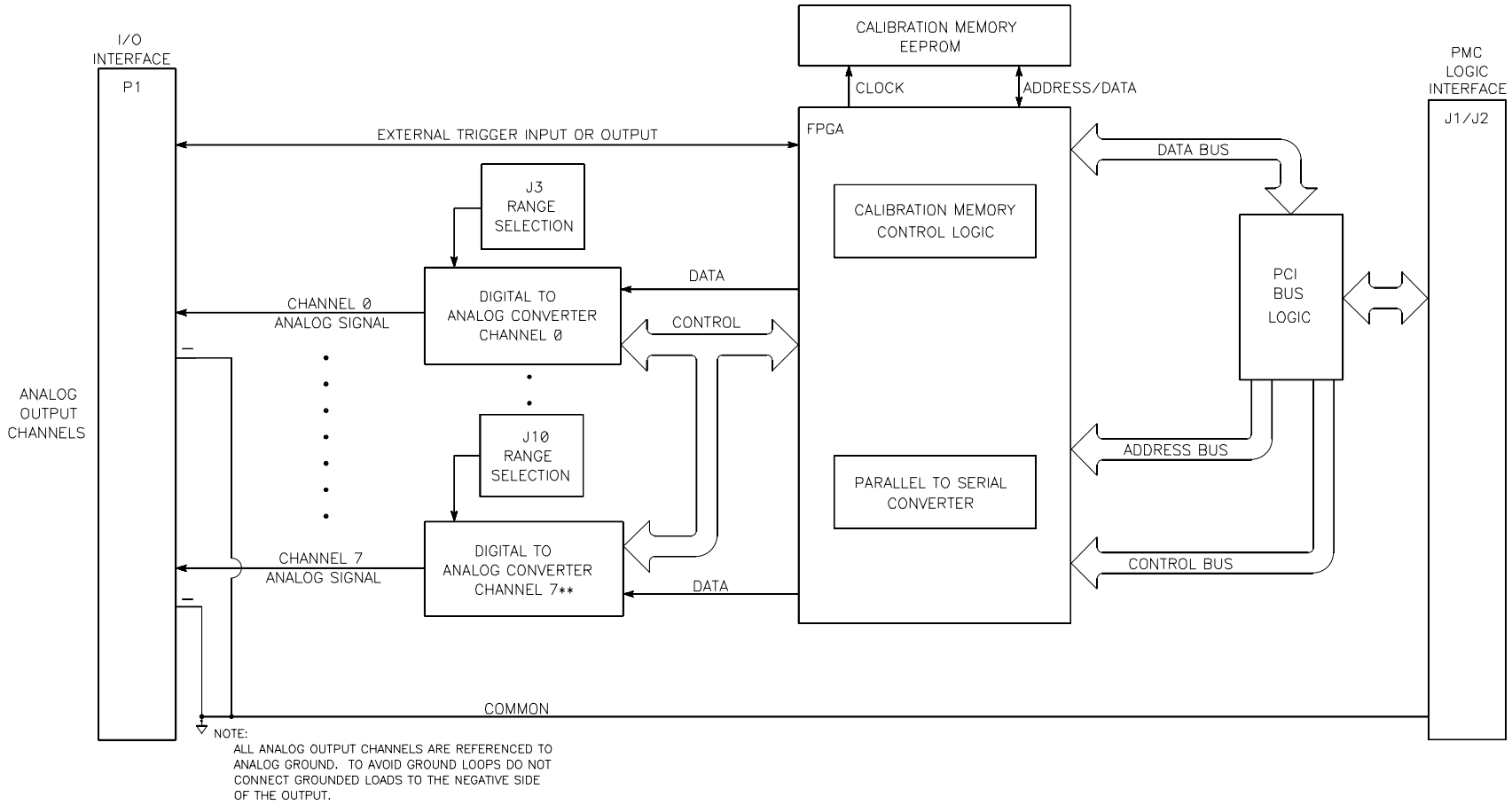
NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONLY ONE END TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. ALL 8 CHANNELS ARE REFERENCED TO ANALOG COMMON AT THE PMC230. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED CHANNELS TO THE NEGATIVE SIDE OF THE OUTPUT.
3. VL < VO DUE TO VOLTAGE DROPS ACROSS THE LEAD RESISTANCE OF THE WIRE. IT IS RECOMMENDED THAT A HIGH RESISTANCE LOAD WITH A SHORT WIRE RUN BE CONNECTED AT THE OUTPUT TO REDUCE THE EFFECTS OF LEAD AND SOURCE RESISTANCE VOLTAGE DROPS IN THE WIRE.

PMC230 ANALOG OUTPUT CONNECTION DIAGRAM

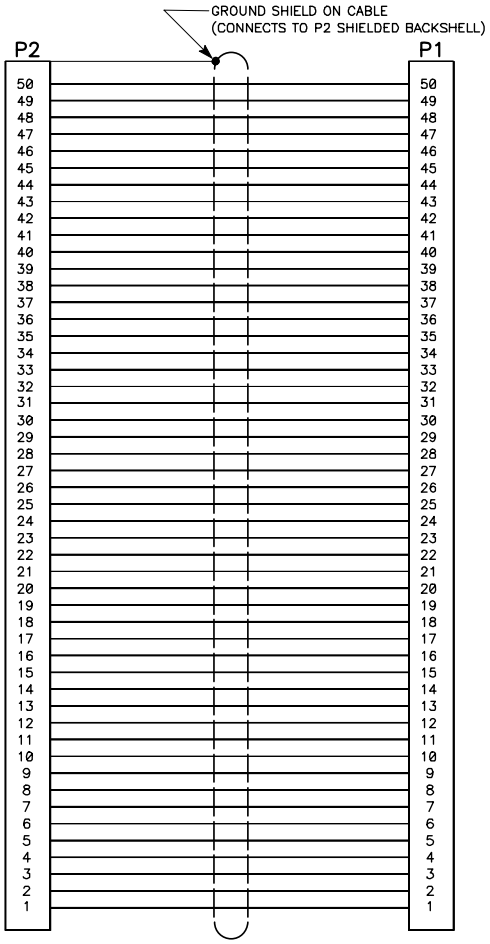
4501–864A

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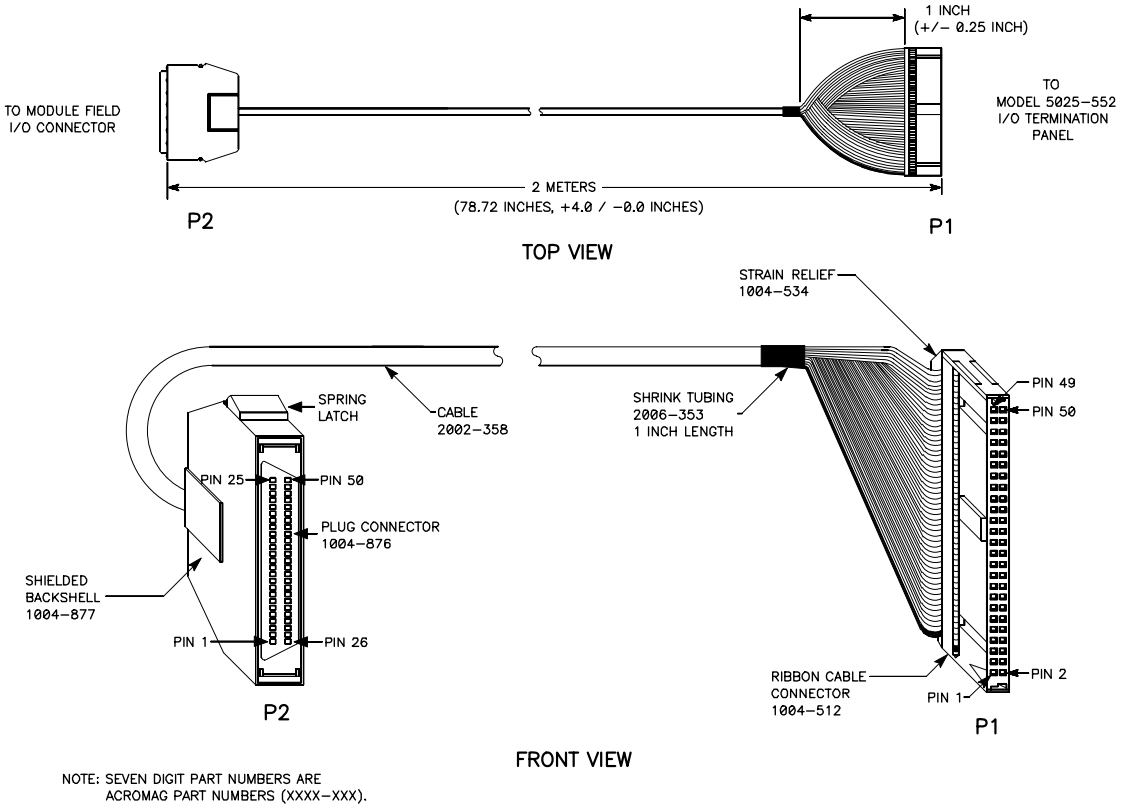


PMC230 BLOCK DIAGRAM 4501–865A

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SCHEMATIC

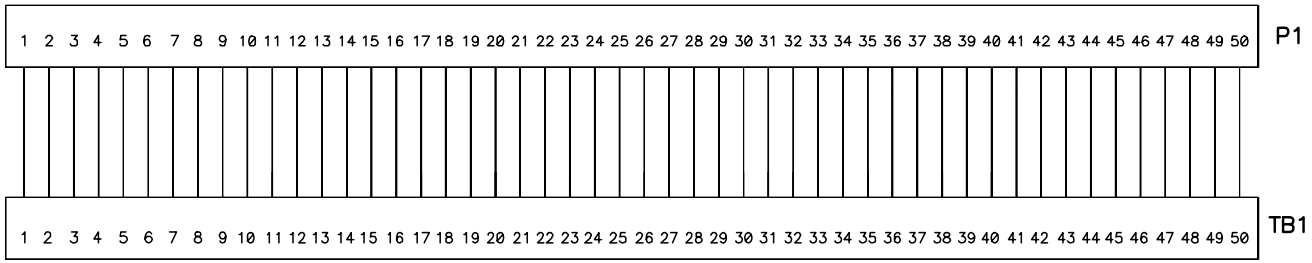


NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX–XXX).

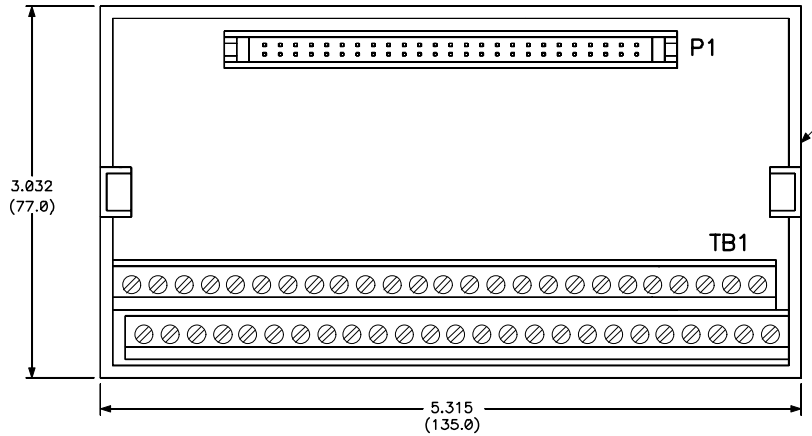
MODEL 5028–187, SCSI–2 TO FLAT RIBBON CABLE, SHIELDED

4501–758B

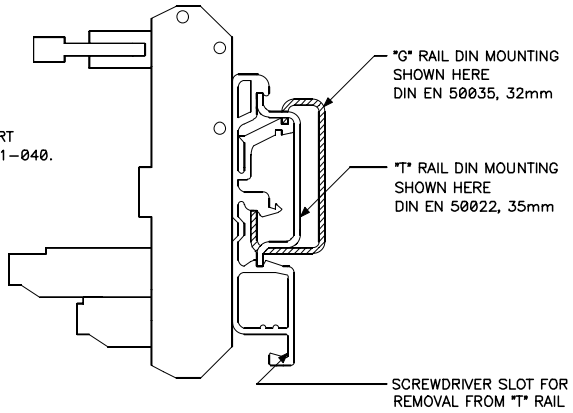
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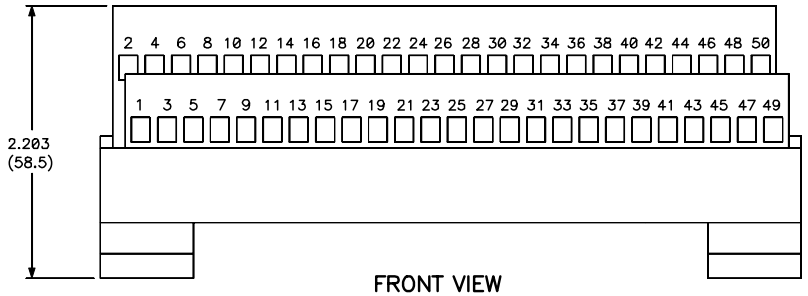
MODEL 5025-552 TERMINATION PANEL SCHEMATIC



TOP VIEW



SIDE VIEW



FRONT VIEW

NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

4501-464A

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