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VPX6860

Intel® 6th Generation Core

6U VPX CPU Module

USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the VPX6860 CPU. It is not intended for a general, non-technical audience that is unfamiliar with computer-on-module (COM) devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

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1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 Product Summary

The VPX6860 is a CPU module that uses an Intel 6th Generation Core Processor (Skylake) with a 6U VPX form factor. It is available in both air and conduction-cooled varieties.

The module can support either one or two DDR4 ECC SODIMMs, for a total of up to 32GB. The SODIMMs are firmly attached to the module with screws and surrounded by heat sink material to provide a mechanically and thermally robust mechanism. Extended temperature models are available for operating in a -40°C to +85°C range.

A large amount of I/O is available, as summarized in Section 6.2 below.

The data plane consists of 2x 40-Gigabit Ethernet ports.

The expansion plane can be configured as 2x8 (default), 1x16, or 4x4 Gen3 PCIe ports.

The VPX6860 contains two M.2 expansion card slots to provide on-board storage capabilities. The M.2 slots support the use of SATA III and PCIe Gen. 3 storage drives.

The VPX6860 supports an XMC mezzanine module, with up to a x8 Gen3 PCIe interface. It also supports one AcroPack or mini-PCIe module.

A two digit LED display is available for Power ON Self-Test (POST) codes, should a problem arise during the boot operation. This display is available for application software user codes after POST to aid in software debugging.

The optional VPX6860-RTM Rear-Transition Module is available to provide easy access to all of the P2 connector's I/O signals.

1.4 Related Material

The following manuals and part specifications provide the necessary information for in-depth understanding of the VPX6860 module.

- The APTIO Skylake Core BIOS Manual For Acromag Products using the Skylake Processor - Referred to hereafter as *Aptio Skylake Core BIOS Manual.*
- Intel® "6th Generation Intel® Processor Datasheet for H-Platforms – Volume 1 of 2", August 2018. http://www.intel.com/content/www/us/en/processors/core/6th-gen-core-family-mobile-h-processor-lines-datasheet-vol-1.html

1.5 Ordering Information

The VPX6860 ordering options are given in the following table.

Model Number	***Description***	***Temp Range***
VPX6860-42-20	*Air-cooled 6U VPX CPU Module with VITA 42 XMC Site*	*0°C to 70°C*
VPX6861-42-20	*Air-cooled 6U VPX CPU Module with VITA 42 XMC Site (No Battery)*	*0°C to 70°C*
VPX6860-61-20	*Air-cooled 6U VPX CPU Module with VITA 61 XMC Site*	*0°C to 70°C*
VPX6861-61-20	*Air-cooled 6U VPX CPU Module with VITA 61 XMC Site (No Battery)*	*0°C to 70°C*
VPX6860-42-50	*Conduction-cooled 6U VPX CPU Module with VITA 42 XMC Site*	*-40°C to 85°C*
VPX6861-42-50	*Conduction-cooled 6U VPX CPU Module with VITA 42 XMC Site (No Battery)*	*-40°C to 85°C*
VPX6860-61-50	*Conduction-cooled 6U VPX CPU Module with VITA 61 XMC Site*	*-40°C to 85°C*
VPX6861-61-50	*Conduction-cooled 6U VPX CPU Module with VITA 61 XMC Site (No Battery)*	*-40°C to 85°C*
VPX6860-RTM-LF	*VPX6860 Rear Transition Module*	*-40°C to 85°C*

Note: All VPX6860 CPU modules contain 32GB of DDR4 SDRAM memory.

VITA 61 XMC connectors are required for Gen3 PCIe XMC operation.

1.6 Key Components and Features

The VPX6860 block diagram shown in Fig. 1.6.1 illustrates the key components and features that are summarized on the following pages.

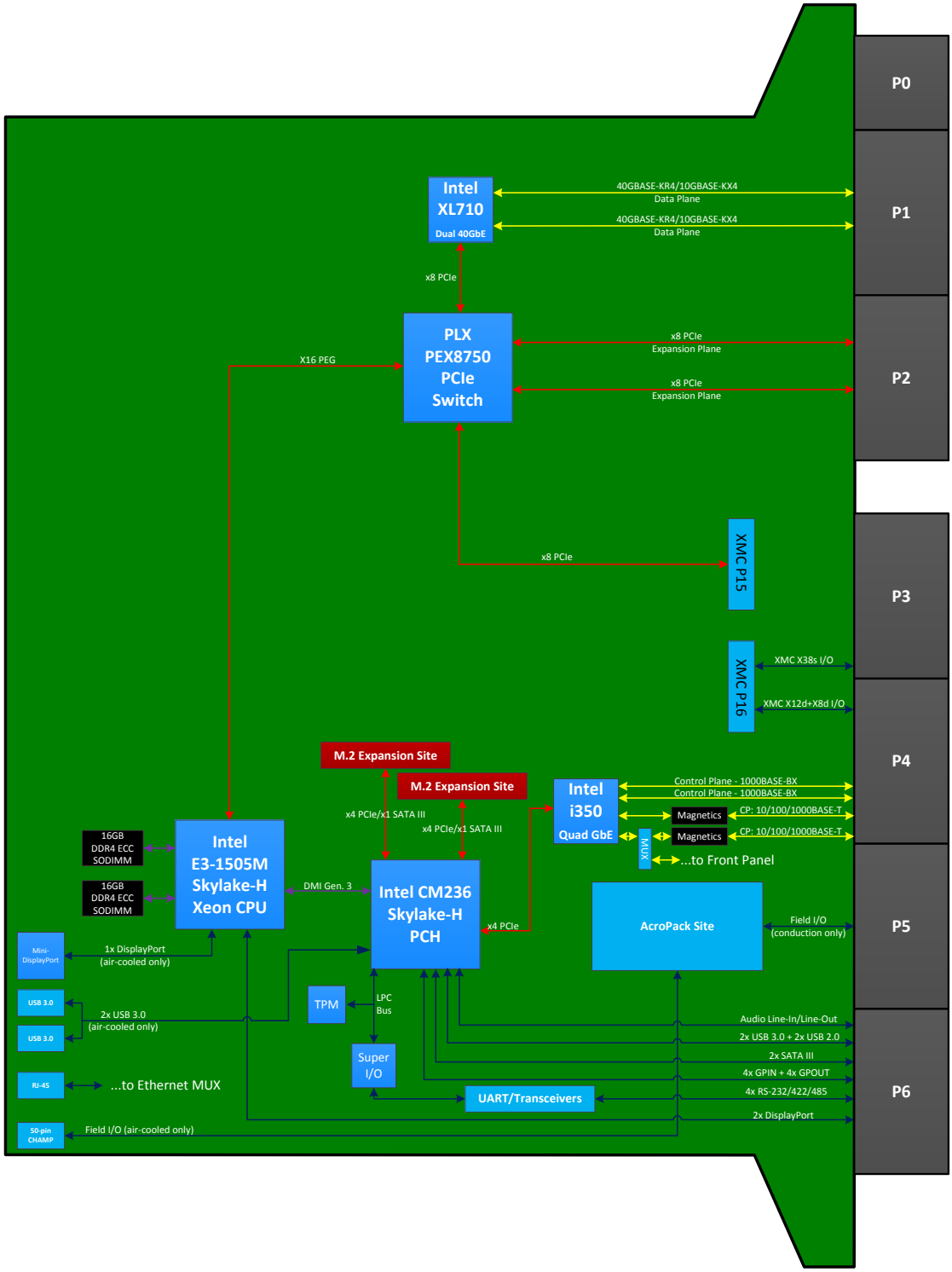


Figure 1.6.1: VPX6860 Block Diagram

1.6.1 Intel® 6th Gen (Skylake) Xeon CPU

The VPX6860 uses the 2.8GHz (3.7GHz max Turbo) quad-core Intel 6th Gen Xeon E3-1505Mv5 CPU. This is a 64-bit CPU using a 14-nanometer process with integrated GT2 graphics and contains direct interfaces for DDR4, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the CM236 Platform Control Hub (PCH).

- **DDR4 SDRAM –** Two SODIMM sockets support up to 32GB of DDR4 ECC at 2133MHz. Dual-channel mode is used with the two SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe Gen3 x16 (1) –** Traditionally used for external graphics, but supports any PCIe device(s). On the VPX6860, this x16 PCIe interface is connected to the PEX8750 Gen3 PCIe switch. This switch then connects to the XL710 40GbE controller, the XMC site, and the two Double-Fat Pipes on the Expansion Plane.
- **DDI (3) –** These Digital Display Interfaces can be configured to be DisplayPort 1.2, DVI, or HDMI. On the VPX6860, two display interfaces are routed to the P6 connector with the third available on a front I/O Mini-DisplayPort connector (Air-cooled only).
- **Programmable CPU power limits –** By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

1.6.2 Intel CM236 PCH

The Intel C230 Series CM236 PCH provides extensive I/O support, as listed below:

- **PCIe Gen3 x4 (4)** – There are four PCIe Gen3 ports of x4 width. The first is connected to the AcroPack module site (x1 only). The second is connected to the Intel I350 Quad Gigabit Ethernet Controller. The third and fourth are connected to the M.2 expansion slots.
- **SATA Gen3 (4)** – There are four SATA III ports on the VPX6860. Two are connected to the P6 backplane connector. Two are connected to the M.2 expansion sites (these can also be PCIe if a PCIe x4 M.2 module is used).
- **USB 3.0 (4)** – There are four USB 3.0 ports on the VPX6860. Two ports are connected to the P6 backplane connector. The other two are available on front I/O USB connectors (Air-cooled only)
- **USB 2.0 (2)** – There are two additional ports that function at USB 2.0 or USB 1.1 speeds that are connected to the P6 backplane connector.

- **GPIO (8) –** There are four 3.3V general purpose inputs and four 3.3V general purpose outputs available on the P4 and P6 backplane connectors.
- **LPC** – The Low Pin Count bus is connected to the NCT6106 Super I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **Line-Level Audio In/Out** – Stereo audio input and output from onboard HDA audio codec are available on the P6 backplane connector.
- **SMBUS** – This I2C-compatible System Management Bus has connections to the memory DIMMs, the VPX backplane, the Ethernet controller, the XMC site, and an on-board EEPROM that can be used for module identification.

1.6.3 Intel I350 Quad Gigabit Ethernet Controller

The Intel I350 Ethernet Controller contains four ports that can be individually configured to be either a fully-integrated gigabit Ethernet media access control (MAC), physical layer (PHY) port or a SGMII/SerDes port.

Two ports are configured to be 1000BASE-BX connections for a board-to-board control plane interface across the VPX backplane.

Two ports are configured to be 1000BASE-T Gigabit Ethernet connections available also on the control plane interface or thru the VPX P4 connector.

1.6.4 Nuvoton NCT6106 Super-I/O

The Nuvoton NCT6106D is an LPC device that provides temperature and voltage monitoring, Port 80 debug via 2 digit 7-segment display, and four RS-232/RS-422/RS-485 (software selectable) serial ports.

1.6.5 Atmel AT97SC3204 TPM

The Atmel AT97SC3204 is a fully integrated security module that implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

1.6.6 Broadcom PEX8750 PCIe Switch

The Broadcom PEX8750 is a 48-lane, 12-port PCI Express Gen 3 switch. The VPX6860 switch connects the following ports:

- Port 0: x16 PEG interface of the Intel Gen6 CPU
- Port 4: x8 Expansion Plane Double Fat Pipe A Port*
- Port 5: x8 Expansion Plane Double Fat Pipe B Port*
- Port 8: x8 Intel XL710 Dual 40 Gigabit Ethernet Controller
- Port 9: x8 XMC site

The switch can also be used in NT mode which allows it to be used in multi-processor systems that do not contain a dedicated PCIe switch card.

*Other Expansion plane port configurations are available. See Section 3.1.4.

1.6.7 M.2 Expansion Site

The VPX6860 contains two M.2 expansion sites that can be used as high-speed, high-bandwidth storage interfaces. The M.2 sites use M-keyed connectors which, according to the M.2 PCI-SIG specification, supports storage devices that use either a SATA III interface or a PCIe x4 interface. M.2 storage modules that use the PCIe x4 interface can achieve throughput speeds over 4x faster than traditional SATA III. Module lengths of 42, 60, and 80mm can be utilized on the VPX6860.

1.6.8 XL710 Dual 40-Gigabit Ethernet Controller

The Intel XL710 Ethernet Controller contains two ports that support 10GBASE-KX4 or 40GBASE-KR4 protocols. These ports are connected to Fat Pipes A and B of the data plane on the VPX backplane.

1.6.9 XMC Expansion Site

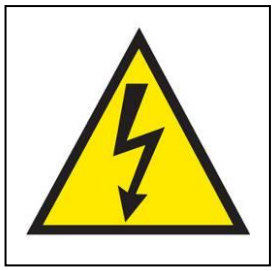
The VPX6860 contains one XMC expansion site. It is connected to the PEX8750 PCIe switch with a link width of x8. The I/O is available on the P3 and P4 connectors following the P3w3-X38s+P4w1-X12d+X8d pattern called out in VITA 46.9.

1.6.10 AcroPack Expansion Site

The VPX6860 contains one AcroPack expansion site. The site can also take advantage of an isolated DC-DC module plugged into the J9 socket. AcroPack Field I/O connections can be made through the 50-pin CHAMP connector on the front panel (air cooled only) or through the VPX P5 backplane connector (conduction cooled only).

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installing into a VPX Backplane

The VPX6860 is a 6U, single-slot VPX module. For proper cooling, the air-cooled model must only be installed into an air-cooled VPX chassis and the conduction-cooled model must only be plugged into a conduction-cooled VPX chassis.

The VPX6860 module is designed to comply with all physical and electrical specifications of the VITA 46 VPX Base Specification and the VITA 65 OpenVPX Specification.

***WARNING:* Never install or remove any boards before turning off power to the bus and all related external power supplies.**

1. Disconnect all power supplies to the backplane and the VPX chassis. Disconnect the power cable.
2. Verify that all DIP switch settings are correct.
3. Verify that the card cage slot is clear and accessible.
4. Install the VPX6860 in the card cage by centering the unit on the guides in the slots (P0 connector facing up). Push the board slowly toward the rear of the chassis until the VPX connectors engage. The board should slide freely in the guides.

***WARNING:* Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for damage or obstructions.**

1. Secure the module to the chassis by tightening the machine screws at the top and bottom of the board.

Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the VPX6860 board (air-cooled only), or on the VPX6860-RTM Rear Transition Module.

3.0 HARDWARE INFORMATION AND CONFIGURATION

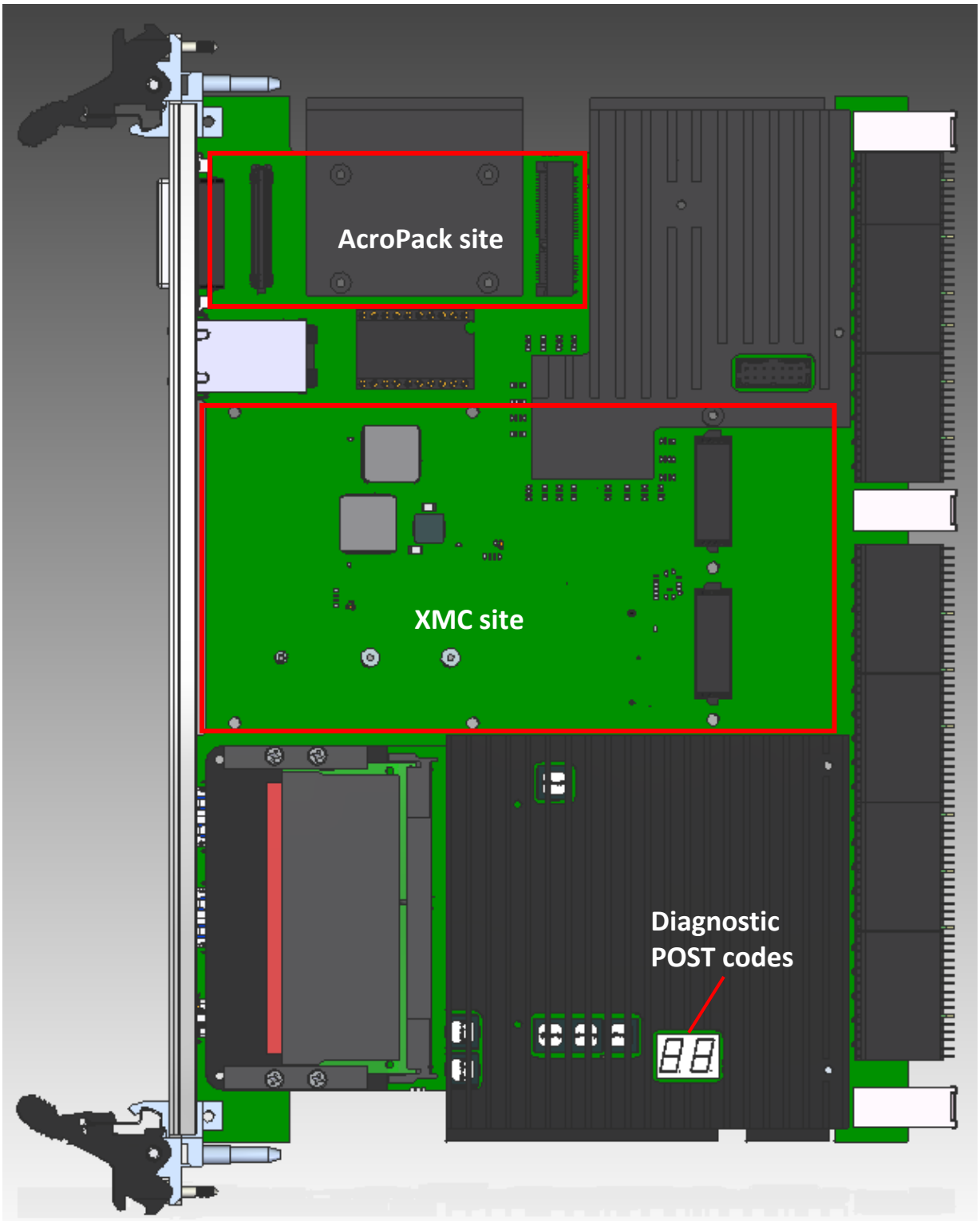


Figure 3.0.1: VPX6860 (Air Cooled) Top View

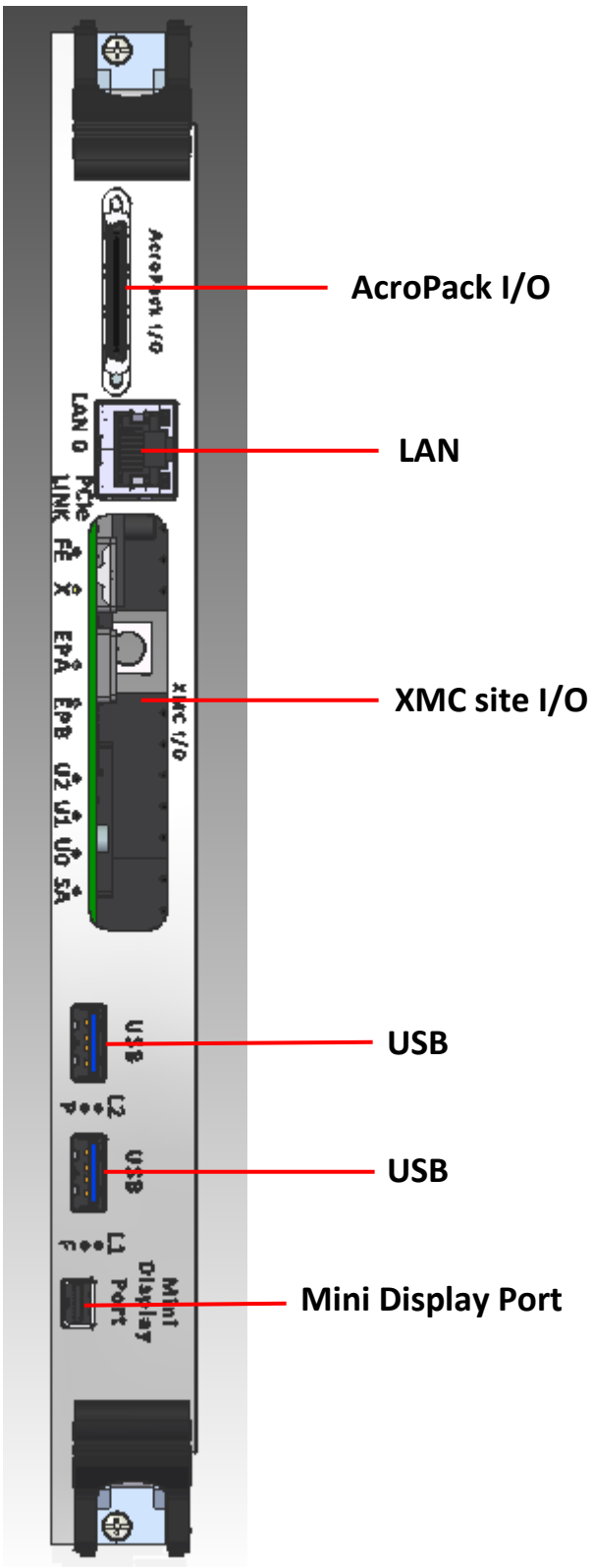
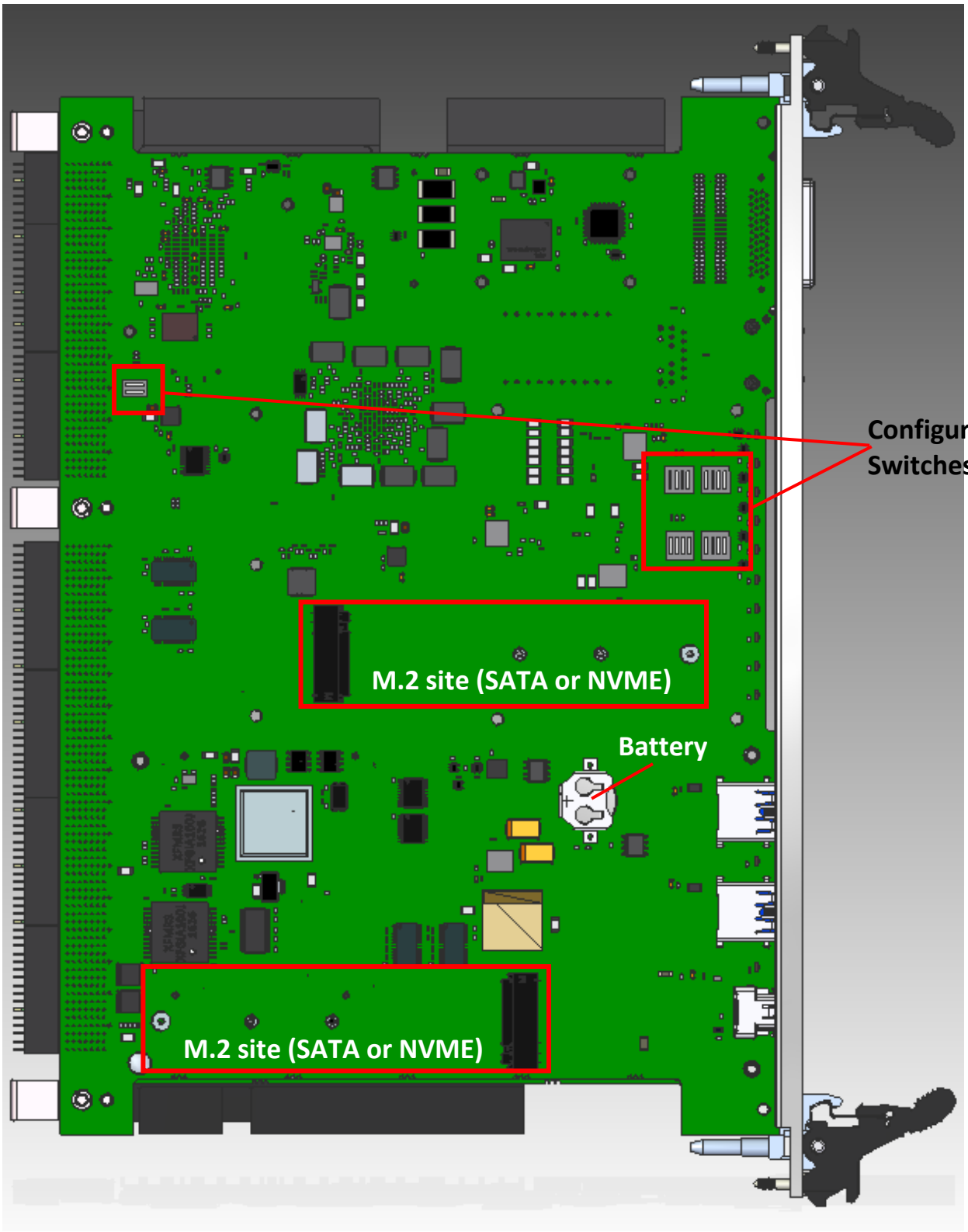


Figure 3.0.2: VPX6860 Front View


Configuration Switches
M.2 site (SATA or NVME)
Battery
M.2 site (SATA or NVME)

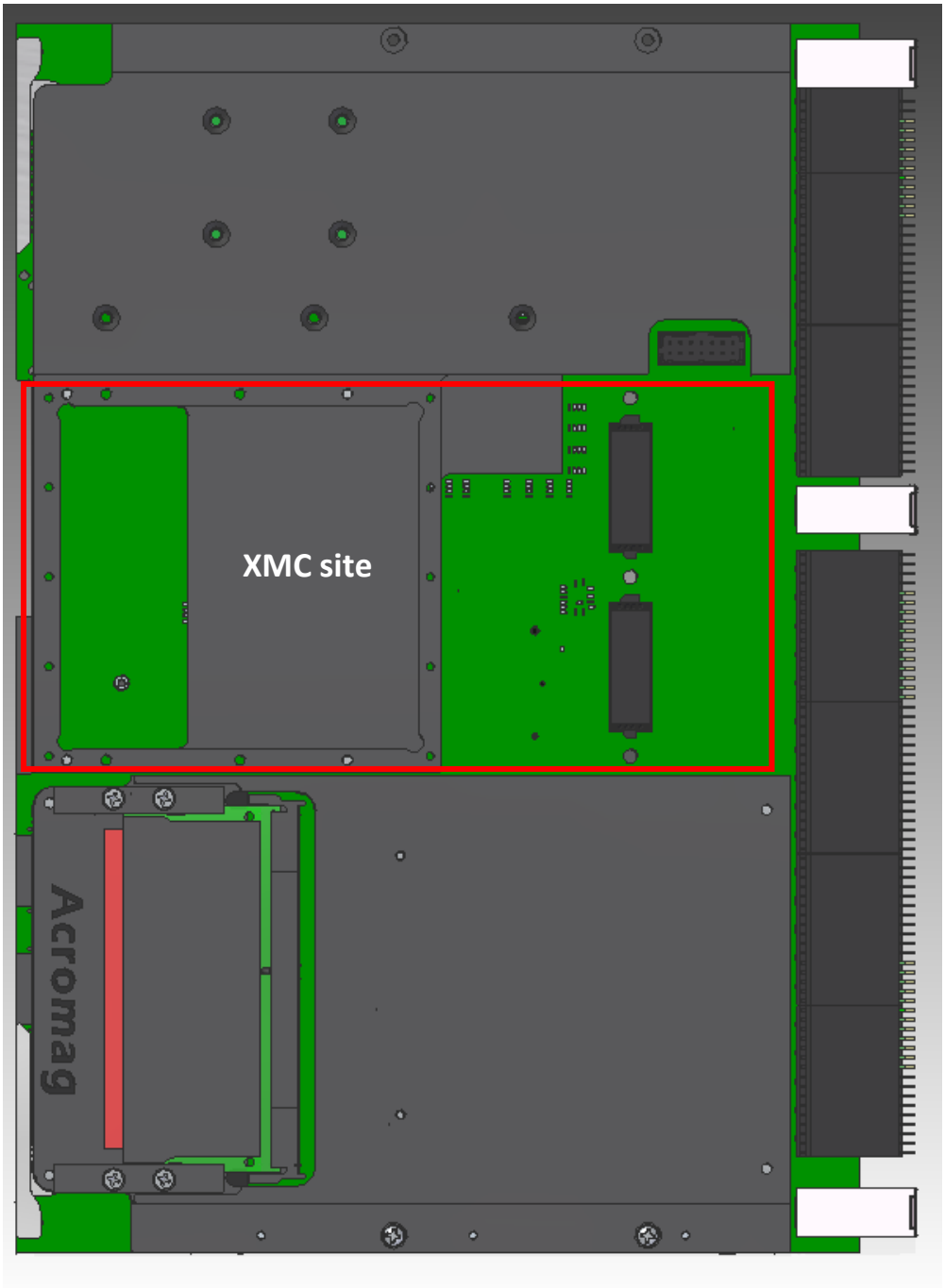


Figure 3.0.4: VPX6860 (Conduction Cooled) Top View

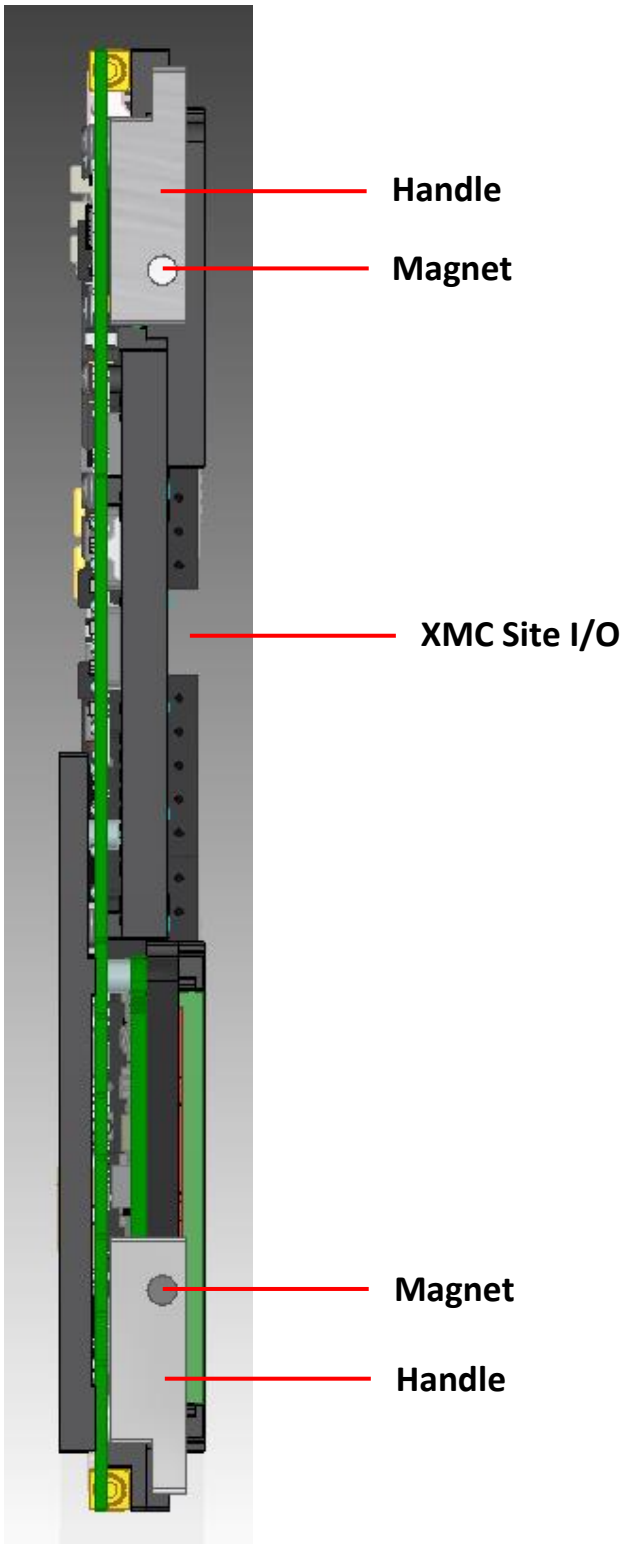


Figure 3.0.5: VPX6860 (Conduction Cooled) Front View

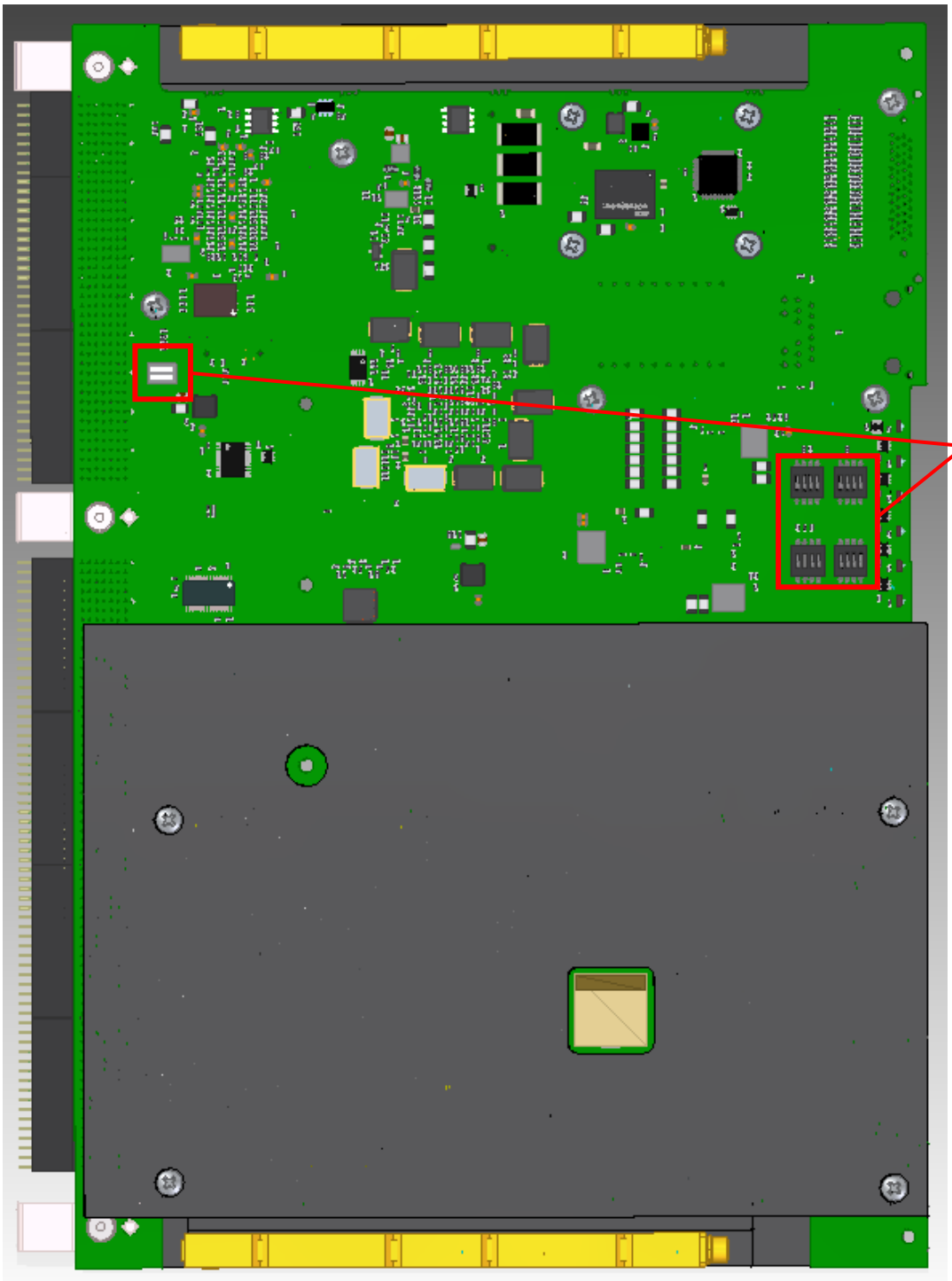


Figure 3.0.6: VPX6860 (Conduction Cooled) Bottom View

3.1 Module Hardware Switch Configuration

3.1.1 Configuration Switch SW1

Table 3.1.a summarizes the functions, settings, and descriptions for DIP switches SW1-1 thru SW1-4.

Table 3.1.a: Configuration witch SW1

SW1 Configuration Switches				
Position	**Function**	**Switch Setting**		**Description**
1 2	PCIe Switch Max Gen Speed	**OFF**	**ON**	**Gen 3**
		X	OFF	Gen 2
		ON	ON	Gen 1
3	ETHERNET0 Port Config	OFF		ENET0 OUT FRONT RJ45
		ON		ENET0 OUT REAR P4
4	RTC Voltage	**OFF**		**VPX VBAT not connected to coin cell or VRTC**
		ON		VPX VBAT connected to coin cell & VRTC

Note: Default settings are in **BOLD**.

SW1-1 and SW1-2 are used to select the maximum speed for the PEX8750 PCIe switch.

SW1-3 sets whether Gigabit Ethernet Port 0 is connected to the front panel RJ-45 connector (SW1-3 OFF; default for air-cooled modules) or to the rear P4 backplane connector (SW1-3 ON; default for conduction cooled modules)

SW1-4 is used to configure the source of the CPU's RTC voltage. When SW1-4 is ON the VPX VBAT pin will be connected to both the RTC voltage and the onboard coin cell battery. When SW1-4 is open the VPX VBAT pin is not connected to the onboard coin battery or RTC voltage.

***WARNING:** If SW1-4 is closed with a coin-cell battery installed, it will connect the coin-cell to any voltage present on the VPX Battery pin on the VPX connector P1-G3. The coin-cell battery must be removed before closing switch SW1-4 if a voltage is supplied by the VPX backplane!*

3.1.2 Configuration Switch SW2

Table 3.1.b summarizes the functions, settings, and descriptions for DIP switch SW2.

Table 3.1.b: Configuration Switch SW2

SW2 Configuration Switches		
Function	**Switch Setting**	**Description**
FRU EEPROM & Temp Sensor Voltage Select	**1-2**	**FRU/Temp Sensor uses +3.3V**
	2-3	FRU/Temp Sensor uses +3.3V_AUX
XMC JTAG Reference Voltage	**4-5**	**XMC JTAG uses +3.3V for VREF**
	5-6	XMC JTAG uses +2.5V for VREF

Note: Default settings are in **BOLD**.

SW2(1-3) is a single-pole, dual-throw switch used to select the voltage source for the following devices:

FRU EEPROM, FRU Temperature Sensor

When configured to use the auxiliary +3.3V_AUX supply, these devices can still be operated while the rest of the system is unpowered.

SW2(4-6) is a single-pole, dual-throw switch used to select the reference voltage source for the XMC JTAG interface (+3.3V or +2.5V).

3.1.3 Configuration Switch SW3

Table 3.1.c summarizes the functions, settings, and descriptions for DIP switches SW3-1 thru SW3-3.

Table 3.1.c: Configuration Switch SW3

SW3 Configuration Switches			
Position	**Function**	**Switch Setting**	**Description**
1	RTC CMOS Reset	**OFF**	Normal Operation
		ON	Clear RTC CMOS
2	Reserved	**OFF**	Normal Operation
		ON	Reserved
3	Reserved	**OFF**	NORMAL
		ON	Reserved

Note: Default settings are in **BOLD**.

SW3-1 is used to clear the Battery-backed RTC CMOS Battery-backed SRAM. To clear the CMOS SRAM, close SW3-1 momentarily and then open it again. The switch must be in the open position for normal operation.

SW3-2 is reserved and should be left in the OFF position for normal operation.

SW3-3 is reserved and should be left in the OFF position for normal operation.

3.1.4 Configuration Switch SW4

Table 3.1.d summarizes the functions, settings, and descriptions for DIP switches SW4-1 thru SW4-4.

Table 3.1.d: Configuration Switch SW4

SW4 Configuration Switches					
Function	**1**	**2**	**3**	**4**	**Description**
Expansion Plane PCIe Port Configuration	X	OFF	X	OFF	x4, x4, x4, x4
	X	OFF	OFF	ON	RESERVED
	X	OFF	ON	ON	x8, x4, x4
	OFF	ON	X	OFF	RESERVED
	ON	ON	X	OFF	x16
	OFF	ON	OFF	ON	RESERVED
	ON	**ON**	**OFF**	**ON**	**x8, x8**
	OFF	ON	ON	ON	RESERVED
	ON	ON	ON	ON	RESERVED

Note: Default settings are in **BOLD**.

SW4-1 thru SW4-4 are used to select the Expansion Plane PCIe port configuration. The default configuration is two x8 double fat pipes.

3.1.5 Configuration Switch SW5

Table 3.1.e summarizes the functions, settings, and descriptions for DIP switches SW5-1 thru SW5-3.

Table 3.1.e: Configuration Switch SW5

SW5 Configuration Switches				
Function	**1**	**2**	**3**	**Description**
NT MODE CONFIGURATION	**ON**	**ON**	**ON**	**NT MODE DISABLED**
	OFF	OFF	OFF	NT UPSTREAM PORT 4
	OFF	OFF	ON	NT UPSTREAM PORT 5

Note: Default settings are in **BOLD**.

SW5-1 thru SW5-3 are used to enable/disable non-transparent mode on the PEX8750 PCIe switch. Non-transparent mode provides the ability to use multiple processors in the same system. NT Mode can be enabled for either of the two Expansion Plane ports on the P2 connector.

3.2 Power Supply and Management

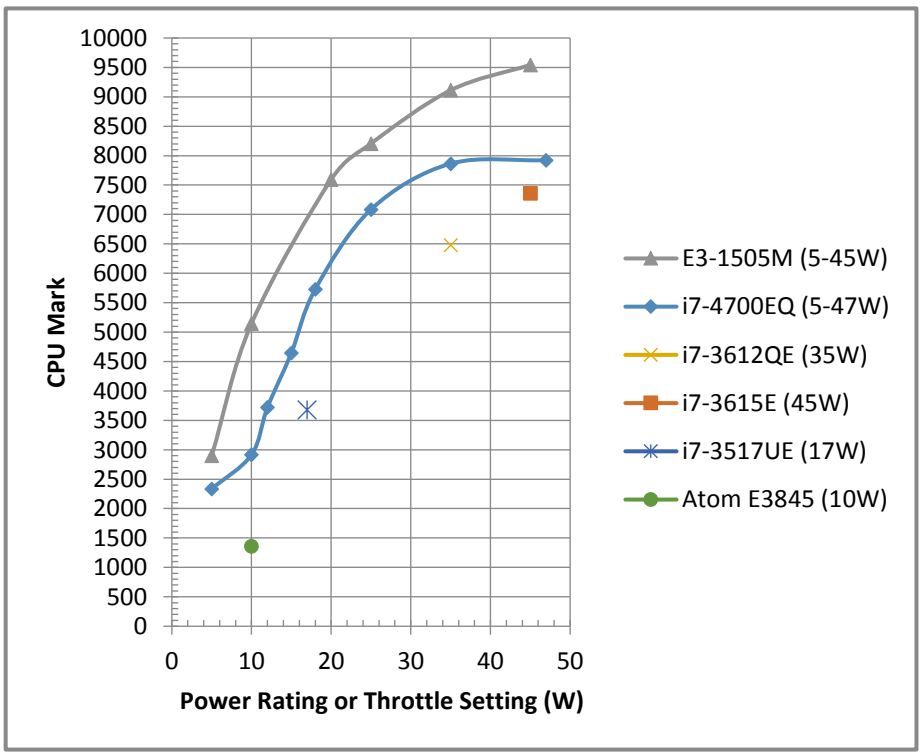
3.2.1 Power Supply Requirements

The VPX6860 must be supplied with +12V (VS1) from the VPX backplane. VS2 and VS3 voltage rails are not used.

For allowed voltage ranges and expected power draw, see the specifications listed in Section 6.3.

3.2.2 Programmable CPU Power Limits

The VPX6860 features programmable power limits, allowing the user to 'dial-down' the maximum power consumption of the CPU in systems where power is a concern. The graph below shows that the E3-1505M CPU outperforms other available embedded Intel CPU's at every power point from 5W - 47W.



By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

Note: Once the minimum frequency of 800MHz is reached the programmed limit could be exceeded. Extremely large workloads have a realistic minimum power of around 20W. However, light to medium workloads can effectively maintain a power limit as low as 5-10W.

There are two programmable CPU limits. These are the long-term average Power Limit 1 (PL1) and the short-term Power Limit 2 (PL2). Depending on a windowed

Power Limit 1 Time 'constant', the CPU can spend a short time above power level PL1 up to a maximum of PL2, allowing a significant performance boost for short workloads. If the CPU power remains above PL1 at the end of this time the power is then limited back to PL1. The power must drop below the PL1 limit before it allowed to increase back to PL2 again. For time spent above PL1 an equivalent amount of time must be spent below PL1 in order for it to rise again to PL2. The maximum time could be as much 2.5x the value of the PL1 Time.

The default values for the CPU are as follows:

PL1: 45W
PL2: 56W
Tau: 28 seconds

PL1 and PL2 can be programmed in watts to any value below the default. Entering a value above the default will result in the default value being used. Entering 0 also results in the default value being used.

PL1 Time can be programmed to any number of seconds up to 256, however it is recommended by Intel to always use the default value of 28. This value maximizes the effectiveness of the short-term performance boost while ensuring that the life of the part is not jeopardized by spending too much time above PL1.

More details about programming these power limits using the BIOS setup utility are provided in *Aptio Skylake Core BIOS Manual*.

3.2.3 Power Management

The VPX6860 module uses the Advanced Configuration and Power Interface (ACPI) 3.0 standard to provide user-managed power via the operating system, contingent upon the carrier board selected.

The Advanced Configuration and Power Interface (ACPI) provides an open standard for device configuration and power management by the operating system. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.3 CPU

The VPX6860 uses the 2.8GHz (3.7GHz max Turbo) quad-core Intel 6th Gen (Skylake) Xeon E3-1505Mv5 CPU. This is a 64-bit CPU using a 14-nanometer process with integrated GT2 graphics and contains direct interfaces for DDR4, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the CM236 Platform Control Hub (PCH).

- **DDR4 ECC SDRAM –** 2 SODIMM sockets support up to 32GB of DDR4 ECC at 2133MHz. Dual-channel mode is used with 2 SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.

- **PCIe Gen3 x16 (1) –** Traditionally used for external graphics, but supports any PCIe device(s). On the VPX6860, this x16 PCIe interface is connected to the PEX8750 Gen3 PCIe switch. This switch then connects to the XL710 40GbE controller, the XMC site, and the two Double-Fat Pipes on the Expansion Plane.
- **DDI (3) –** These Digital Display Interfaces can be configured to be DisplayPort 1.2, DVI, or HDMI. On the VPX6860, two display interfaces are routed to the P2 connector with the third available on a front I/O Mini-DisplayPort connector (Air-cooled only).
- **Programmable CPU power limits –** By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

3.3.1 Active Processor Core Selection

All of the CPU cores should be kept active in high-performance systems requiring all available computing power. Conversely, applications having reduced power requirements can save power by disabling one or more of the CPU cores. The number of active CPU cores can be specified in the CPU configuration menu. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.3.2 Turbo Boost Configuration

By default, Turbo Mode is enabled in the BIOS setup screen. Turbo Mode allows the CPU to go beyond the rated nominal clock frequency when there is headroom from the maximum Thermal Design Power of the CPU. This results in the highest available performance, but with a larger, more dynamic power draw during peak operations. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.4 Platform Controller Hub (PCH)

The Intel C230 Series CM236 PCH provides extensive I/O support, as listed below:

- **PCIe Gen3 x4 (4)** – There are four PCIe Gen3 ports of x4 width. The first is connected to the AcroPack module site (x1 only). The second is connected to the Intel I350 Quad Gigabit Ethernet Controller. The third and fourth are connected to the M.2 expansion slots.
- **SATA Gen3 (4)** – There are four SATA III ports on the VPX6860. Two are connected to the P6 backplane connector. Two are connected to the M.2 expansion sites (these can also be PCIe if a PCIe x4 M.2 module is used).
- **USB 3.0 (4)** – There are four USB 3.0 ports on the VPX6860. Two ports are connected to the P6 backplane connector. The other two are available on front I/O USB connectors (Air-cooled only)
- **USB 2.0 (2)** – There are two additional ports that function at USB 2.0 or USB 1.1 speeds that are connected to the P6 backplane connector.
- **GPIO (8) –** There are four 3.3V general purpose inputs and four 3.3V general purpose outputs available on the P4 and P6 backplane connectors.

- **LPC** – The Low Pin Count bus is connected to the NCT6106 Super I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **Line-Level Audio In/Out** – Stereo audio input and output from onboard HDA audio codec are available on the P6 backplane connector.
- **SMBUS** – This I2C-compatible System Management Bus has connections to the memory DIMMs, the VPX backplane, the Ethernet controller, the XMC site, and an on-board EEPROM that can be used for module identification.

3.5 System Memory

The VPX6860 CPU module has two 260-pin, right-angle SODIMM sockets to accept DDR4 ECC SDRAM modules. At least one SDRAM module is required to make the system operational.

Note: ECC (x72) SODIMM modules are required. Non-ECC SODIMM modules (x64) are not supported.

Support for the following features is provided by the system memory interface:

- DDR4 SDRAM with transfer rates of 2133 MT/s
- Up to 16GB capacity DIMMs using 4Gb or 8Gb DDR4 SDRAM densities
- 72-bit wide channels (64-bits plus 8 bits of ECC)

3.6 Video

Up to 3 displays are supported, all of which can be active at the same time. Each display type supports the following maximum resolution:

DP:	4096x2304 @ 60Hz
HDMI:	4096x2160 @ 24Hz
DVI:	1920x1200 @ 60Hz

3.6.1 Digital Display Interfaces

The Intel® Gen6 (Skylake) CPU used on the VPX6860 CPU module integrates three digital display ports (B, C, and D) that support DisplayPort, HDMI, or DVI interfaces.

DisplayPort can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and the link data rate of the RBR (1.62 GT/s), HBR (2.7 GT/s), and HBR2 (5.4 GT/s).

All three ports support DP++, which transmits DVI/HDMI signals as well as DisplayPort. A simple passive adapter can be used to connect DVI/HDMI display devices to any of these ports. The BIOS will detect and automatically configure any of these attached devices.

When configured as HDMI, the DDIx4 port can support 2.97 GT/s link rate.

The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.

The processor also integrates a dedicated Mini HD audio controller to drive audio on integrated digital display interfaces, such as HDMI and DisplayPort.

The HD audio controller on the PCH would continue to support down CODECs, and so on. The processor Mini HD audio controller supports two High-Definition Audio streams simultaneously on any of the three digital ports.

The processor supports streaming any 3 independent and simultaneous display combination of DisplayPort/HDMI/DVI. In the case of three simultaneous displays, two High Definition Audio streams over the digital display interfaces are supported.

3.6.1.1 DisplayPort

DisplayPort is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The Intel 6th Gen Skylake Core CPU is designed in accordance to VESA DisplayPort Standard 1.2, VESA DisplayPort PHY Compliance Test Specification 1.2, and VESA DisplayPort Link Layer Compliance Test Specification 1.2.

3.6.1.2 HDMI

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audio-visual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. The HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The Intel 6th Gen Skylake Core CPU is designed in accordance with the High-Definition Multimedia Interface Specification Version 1.4.

3.6.1.3 Integrated Audio

- HDMI and DisplayPort interfaces carry audio along with video.
- The processor supports three High Definition audio streams on three digital ports simultaneously.
- The integrated audio processing (DSP) is performed by the PCH and delivered to the processor.
- The processor supports only the internal HDMI and DP CODECs.

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

3.6.2 Configuring the Primary Display

To select a specific primary display, refer to *Aptio Skylake Core BIOS Manual.*

3.6.3 Configuring the Video Memory

To configure the video memory, refer to *Aptio Skylake Core BIOS Manual.*

3.6.4 Video Display Options

The VPX6860 supports three simultaneous, independent displays.

Display mode choices when using multiple monitors include:

- Single display, in which one port is activated to display the output on one device.
- Clone mode, in which the same content, resolution, and color depth are sent to up to three display devices. Different refresh rates may be used on each display.
- Extended desktop, in which a larger Windows desktop spans up to three display devices. The displays can support different refresh rates, resolutions, and color depth.

3.6.5 Multi-Stream Transport

The VPX6860 module supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector. The max MST DP supported resolution is:

One panel display:	4096x2304 @ 60Hz
Two panel displays concurrently:	2880x1800 @ 60Hz
Three panel displays concurrently:	2304x1440 @ 60Hz

3.7 Intel® High Definition Audio

The VPX6860 uses Intel High Definition Audio through an ALC892 Audio CODEC to provide both a stereo line-level audio input and a stereo line-level audio output.

The module can also generate a separate PC speaker signal, although most CODECs intercept this signal and pipe it out through the speakers attached to the CODEC. Enabling and configuring the HDA is discussed in *Aptio Skylake Core BIOS Manual.*

3.8 Storage I/O

3.8.1 SATA

SATA (Serial Advance Technology Attachment) is the interface that connects the PCH to the supported mass storage devices (see below). Note that the PCH SATA controller no longer supports IDE legacy mode. Therefore, AHCI software is required.

The SATA features support:

- The SATA hard disk drives, solid state drives (SSD), and CD-ROM/DVD-ROM drives
- AHCI and RAID (0, 1, 5, and 10) modes
- Data transfer rates of up to 6.0Gbps

SATA0 and SATA4 are available on the M.2 Expansion sites, while SATA2 and SATA3 are available on the P6 backplane connector.

To configure SATA operation, refer to *Aptio Skylake Core BIOS Manual.*

3.8.2 PCIe

In addition to SATA, the two M.2 expansion sites can use the NVMe protocol to connect to x4 PCIe Storage Devices with transfer rates of up to 32Gbps

3.9 Flexible I/O

The lanes going to the M.2 connector are configured automatically by the storage module that is installed to be either SATA or PCIe.

3.10 General I/O

3.10.1 General Purpose I/O (GPIO)

The VPX6860 supports 4 GPIN pins and 4 GPOUT pins. The GPIO pins are available on the P4 and P6 VPX backplane connectors. They are 3.3V level signals and the outputs can source/sink 12mA.

3.10.2 SMBus

The SMBus is connected directly to the PCH, as well as to other devices on the module. The SMBus is also connected to the VPX backplane as specified in VITA 46.0 VPX Base Specification.

Refer below to Table 3.10.2.a, SMBus/I2C Address Table, below for additional information.

Table 3.10.2.a: SMBus/I2C Address Table

SMBus ADDR	Function
0x32	DIMMA TEMP
0x34	DIMMA TEMP
0x5A	NCT6016 Super-I/O
0xA0	Acro-Express ID EEPROM
0xA2	DIMMA SPD
0xA4	DIMMB SPD
0x49	I350 Ethernet Controller
0x4*	PCA9500 I/O Expander
0xA*	PCA9500 EEPROM
0x9*	TMP75 Temp Sensor

Note: Slave addresses of FRU devices (PCA9500, TMP75) are slot dependent based on VPX Geographical Addressing Bits per VITA 46.

3.10.3 Low Pin Count (LPC)

The LPC interface contains the onboard NTC6106 Super I/O device, which supplies the two serial ports and also outputs the Port80 Power On Self Test (POST) codes to the dual 7-segment display.

The onboard Atmel AT97SC3204 TPM device fully integrated security module, implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

For further information regarding the system BIOS and LPC interfaces, refer to *Aptio Skylake Core BIOS Manual.*

3.10.4 Serial Ports

Four 16550-compatible serial ports are supplied by the NCT6106 Super I/O device. All ports are software selectable between RS-232/RS-422/RS-485 and are available on the P3 and P6 VPX backplane connectors.

For further information regarding BIOS serial port configuration, refer to *Aptio Skylake Core BIOS Manual.*

3.10.5 USB

The Intel® CM236 PCH has one eXensible Host Controller Interface (xHCI) controller to support the four USB 3.0 ports and the two USB 2.0 ports.

USB 3.0 ports support up to 5Gbps and USB 2.0 supports up to 480Mbps.

Note that EHCI mode is no longer supported, which may affect the installation of some operating systems.

These USB features support:

- USB hard disk drives, flash drives, floppy disk drives, and CD-ROM/DVD-ROM drives
- Super-speed, high-speed, full-speed, and low-speed USB
- USB debug capability on any USB 3.0-capable port

Two of the USB 3.0 ports are available via the front panel of the VPX6860 for air-cooled models only. The remaining 2 USB 3.0 ports and the two USB 2.0 ports are routed to the P6 VPX backplane connector.

For information on configuring specific USB ports see *Aptio Skylake Core BIOS Manual.*

3.11 Gigabit Ethernet

The VPX6860 uses the Intel i350 Quad Gigabit Ethernet Controller, which contains both the media access control (MAC) and the physical layer (PHY) for each port.

The VPX6860 provides four Gigabit Ethernet ports configured as follows:

- Two 1000BASE-BX ports connected to the P4 VPX backplane connector to be used on the board-to-board Control Plane interface as specified in VITA 65 OpenVPX specification.
- Two 1000BASE-T fully-integrated ports available on the P4 VPX backplane connector to be used either as standard Ethernet connections or on the Control Plane interface. Note that one of these ports can instead be directed out the front panel RJ-45 on the air-cooled model.

3.11.1 Configuring PXE Boot

For information regarding how to boot from the network, refer to *Aptio Skylake Core BIOS Manual.*

3.12 Real Time Clock (RTC)

A Motorola® MS146818B-compatible real-time clock (RTC) is included in the Intel® CM236 PCH. The RTC has 256 bytes of battery-backed RAM and runs on a 32.768 KHz crystal with a 3V battery. The RTC performs two key functions:

- It keeps track of the time of day, and
- It stores system data, even after powering down the system.

Note: After the RTC battery is removed from the board with it otherwise unpowered, the last BIOS settings will be retained for approximately 80 minutes by an onboard supercap. After that, the settings will be lost unless the module is reconnected to the RTC battery or connected to VCC_3.3VSBY.

Note: If the supercap has drained and the RTC voltage drops below 2.5V, or when a BIOS update has been done, the first time the system is powered on it may partially boot and then restart up to two times. This behavior is normal.

3.13 Security

3.13.1 Trusted Platform Support

The VPX6860 uses the Atmel AT97SC3204 fully integrated security module, which implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

3.13.2 Password Control

You are able to specify:

- An Administrator password with full control, and
- A User password with limited access to the BIOS settings.

For further information on setting the password, refer to *Aptio Skylake Core BIOS Manual.*

3.14 System Management

3.14.1 Intel® Hyper-Threading Technology

(Note: The following information is from Intel® "6th Generation Intel® Processor Datasheet for H-Platforms– Volume 1 of 2", August 2018.)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

The Intel® HT Technology is enabled by default; no action by the operator is required.

For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.2 Enhanced Intel® SpeedStep Technology (EIST)

The Enhanced Intel® SpeedStep Technology (EIST) used by this processor enables very high performance while also meeting power-conservation needs. When EIST is enabled, the clock frequency of the CPU is dynamically changed in response to the CPU load.

The Intel® SpeedStep feature is enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.3 Intel® Virtualization Technology (Intel VT-x and VT-d)

Intel® Virtualization Technology (Intel VT) makes a single system appear as multiple independent systems to software. This allows for multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. The first revision of this technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel VT-d) adds chipset hardware implementation to improve I/O performance and robustness.

The Intel® VT-x and VT-d features are enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.4 Intel® Trusted Execution Technology (TXT)

The featured Intel® Trusted Execution Technology attests to the authenticity of a platform and its operating system and assures that an authentic OS starts in a trusted environment and can be considered a trusted OS.

Intel® TXT works in conjunction with the TPM so that the system software may make trust decisions.

The Intel TXT feature is enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.5 Intel® Turbo Boost Technology

The number of active cores determines the maximum processor core operating frequency. See Section 3.3.1, "Active Processor Core Selection" for information and instructions.

(Note: The following information is from Intel® "6th Generation Intel® Processor Datasheet for H-Platforms– Volume 1 of 2", August 2018.)

The Intel® Turbo Boost Technology allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads.

The processor supports a Turbo mode in which the processor can use the thermal capacity associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, surging usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Refer to *Aptio Skylake Core BIOS Manual* and the appropriate processor Turbo Implementation Guide for more information.

3.14.6 Intel® Active Management Technology

Intel® Active Management Technology (Intel® AMT) is a set of advanced manageability features developed to extend the manageability capability for IT through Out Of Band (OOB). This allows asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low power, or "off" state, or in situations when the operating system is hung.

For further information on configuring this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.7 Intel® Matrix Storage Technology

Intel® Matrix Storage Technology is supported by Intel's CM236 PCH, which provides:

- AHCI functionality,
- RAID 0/1/5/10 Support, and
- Intel® Rapid Storage Technology.

3.14.8 Intel® Configurable TDP Technology

Intel® Configurable TDP Technology (cTDP) allows users to reconfigure the 45W thermal design power (TDP) level of the E3-1505M CPU down to 35W in systems where a lower amount of power is available or a smaller thermal solution is required.

For further information on configuring the TDP levels, refer to Aptio Skylake Core BIOS Manual.

3.15 Thermal Management

The Intel® Skylake processor contains a digital thermal sensor for each execution core and a thermal monitor to measure the processor's temperature. A thermal sensor connected to the NCT6106 Super-I/O is used to measure the module's temperature.

The integrated graphics and memory controller (GMC) monitors its temperature and initiates thermal management with an internal digital thermal sensor. Memory loading or high GMC temperatures will result in bandwidth throttling. THERMTRIP# and Render Thermal Throttling are also supported by the internal digital thermal sensor.

The temperature of the Intel® CM236 PCH is monitored by two thermal sensors located on the PCH. The system will be shut down by the PCH when its thermal limit is reached.

3.15.1 Thermal Monitoring

The system setup utility displays the processor and board temperatures. For further information on how to check these temperatures, refer to *Aptio Skylake Core BIOS Manual.*

3.15.2 Thermal Throttling

3.15.2.1 CPU Throttling (Hardware Controlled)

The processor must not exceed the 100°C maximum junction temperature (Tj).

When the integrated thermal monitor on the processor determines that the maximum processor temperature has been reached, the CPU clock speed will be throttled back in 100MHz increments to keep Tj from exceeding the maximum junction temperature of 100° C.

If throttling is not enough to keep the processor's Tj below the catastrophic temperature limit of 105° C:

- The THERMTRIP# signal will be sent, and
- The voltage supply to the processor will be turned off within 500ms to prevent permanent silicon damage.

3.15.2.2 Thermal Management (OSPM Controlled)

The active and passive trip points are configured using the system Bios. For information on how to configure these trip points, refer to *Aptio Skylake Core BIOS Manual.*

3.15.3 Memory Throttling

The memory bandwidth can be throttled back automatically if a thermal sensor is on the DIMM. The NCT6106 will alert the memory controller via PECI when the system memory exceeds its normal operating temperature.

For further information on configuring the memory bandwidth throttling based on temperature readings from the DIMM's thermal sensor, refer to *Aptio Skylake Core BIOS Manual*.

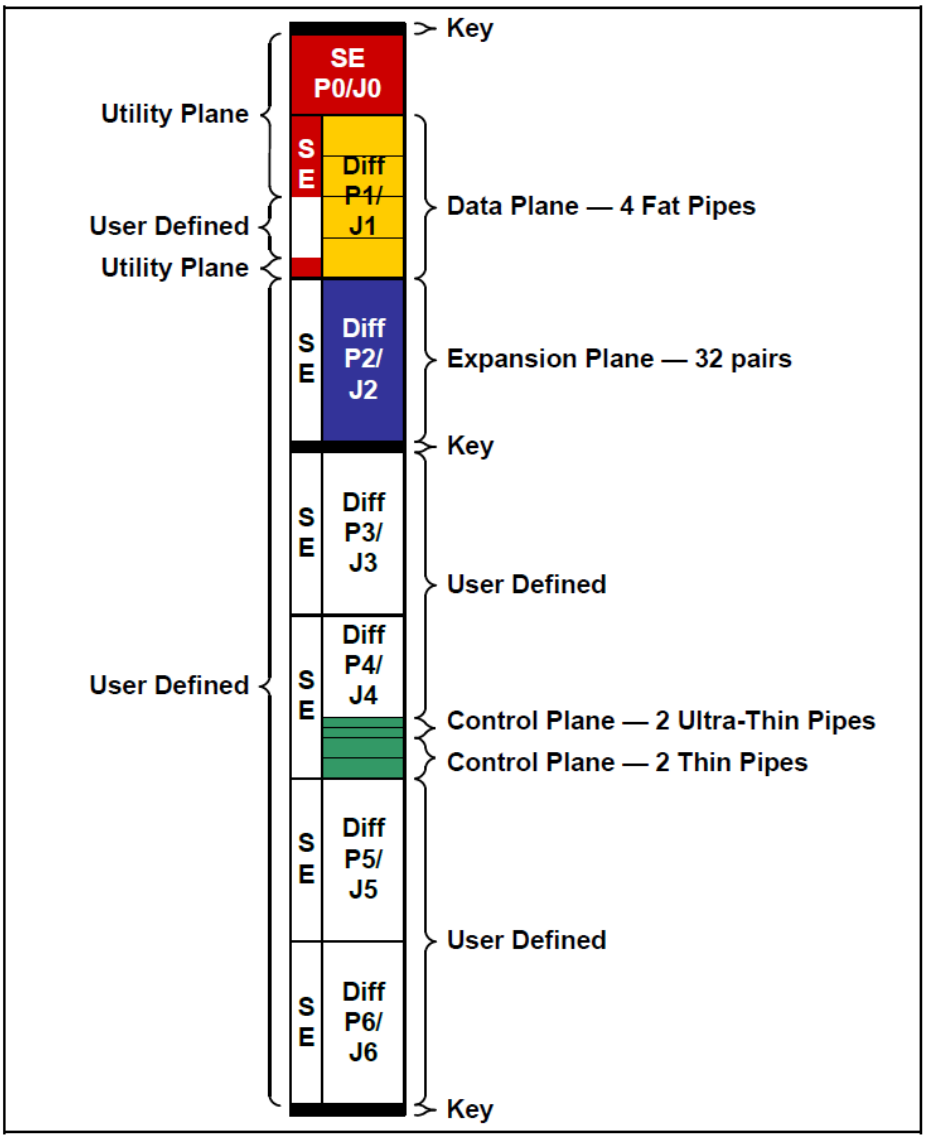
3.16 VPX Profile

The VPX6860 is designed to be used in OpenVPX module profile MOD6-PAY-4F1Q2U2T-12.2.1-15. This module profile complies with OpenVPX slot profile SLT6-PAY-4F1Q2U2T-10.2.1 shown in Figure 3.16.a below.

This module profile defines four 40GBASE-KR4 Ethernet ports to be used as a Data Plane, however the VPX6860 only supports two ports.

This module profile also defines 2 PCIe Gen 2 Double Fat Pipes to be used as Expansion Planes, as well as two 1000BASE-BX and two 1000BASE-T Gigabit Ethernet connections to be used as Control Planes.

Fig. 3.16.a OpenVPX Slot Profile SLT6-PAY-4F1Q2U2T-10.2.1



3.16.1 Data Plane

The VPX6860 uses two 40GBASE-KR4 ports from the Intel XL710 Dual 40Gigabit Ethernet Controller for its Data Plane connection. The 10GBASE-KX4 protocol is also supported for 10Gigabit connections.

Note: a 40Gbps maximum throughput is available from both ports concurrently, even if both ports are linked at 40Gbps. This is a limitation of the XL710 IC.

3.16.2 Expansion Plane

The VPX6860 uses the Broadcom PEX8750 PCIe switch for its Expansion Plane connection. The PCIe switch supports non-transparent bridging which allows the VPX6860 to be used in multi-processor VPX systems that do not contain a dedicated switch card. For port width configuration see section 3.1.4.

3.16.3 Control Plane

The VPX6860 uses the Intel i350 Quad Gigabit Ethernet Controller for the Control Plane interface. The i350 is configured to generate two 1000BASE-BX and two 1000BASE-T Gigabit Ethernet ports for the Control Plane or for external Internet connections.

3.17 Expansion Sites

The VPX6860 contains two expansion sites for mezzanine cards that can greatly expand its I/O capabilities. These modules can be used on both the air and conduction versions of the VPX6860.

3.17.1 XMC Expansion Site

The VPX6860 contains one XMC expansion site. It is connected to the PEX8750 PCIe switch with a link width of x8. The I/O is available on the P3 and P4 connectors following the P3w3-X38s+P4w1-X12d+X8d pattern called out in VITA 46.9.

3.17.2 AcroPack Expansion Site

The VPX6860 contains one AcroPack expansion site. The site can also take advantage of an isolated DC-DC module plugged into the J9 socket (air cooled only). AcroPack Field I/O connections can be made through the 50-pin CHAMP connector on the front panel (air cooled only) or through the VPX P5 backplane connector (conduction cooled only).

4.0 BIOS INFORMATION AND CONFIGURATION

4.1 VPX6860 Special BIOS Features

This section contains information on configuring features specific to the VPX6860. For other, more generic BIOS setup information, refer to *Aptio Skylake Core BIOS Manual.*

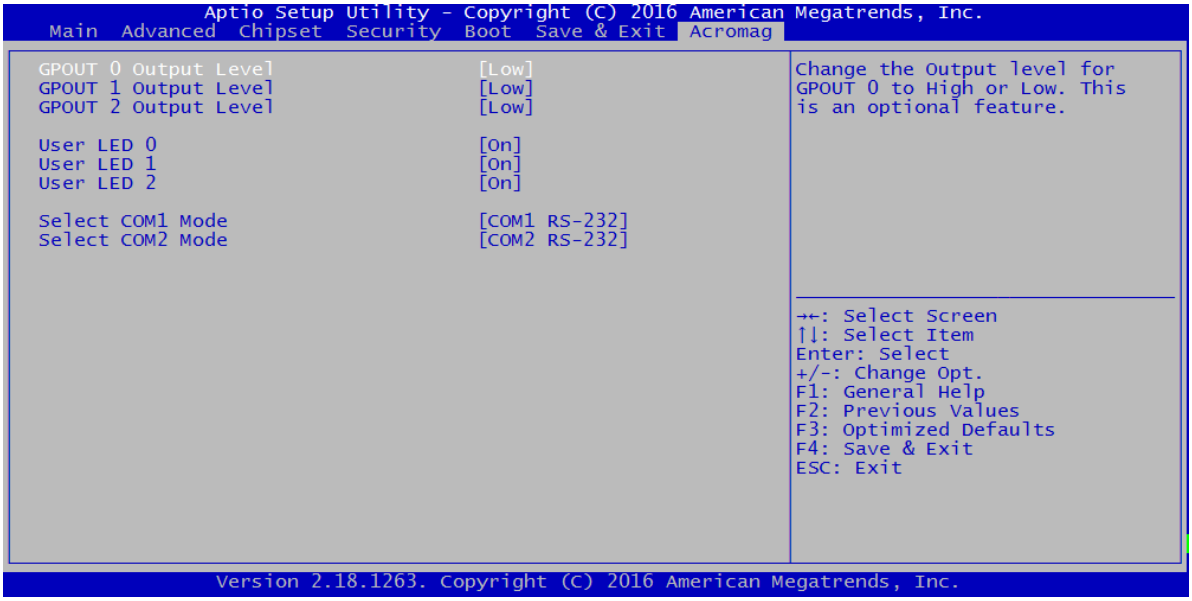


Fig. 4.1.a Acromag BIOS Setup Menu

The following hardware configuration options are available in the Acromag menu of the BIOS setup Utility:

- **GPOUT x Output Level -** Sets the corresponding General Purpose Output level to Low or High. The default is Low.
- **User LED x Output Level -** Sets the corresponding User LED output level to Low or High. The LED is on when the level is set to High. The default is High.
- **Select COMx Mode -** Sets the corresponding COM port protocol to RS-232 or RS-422/485. The default is RS-232.

4.2 Drivers and Utilities

Drivers and Utilities for the VPX6860 can be downloaded from Acromag's website at https://www.acromag.com/.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Single Board Computer (SBC) products like the VPX6860 VPX CPU module are generally difficult to repair. The module can be easily damaged unless special SBC repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. For these and other reasons, it is strongly recommended that a non-functioning SBC be returned to Acromag for repair.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation for the module to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

5.3 Where to Get Help

If the problem persists, the next step should be to visit the Acromag worldwide web site at https://www.acromag.com/. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6.0 SPECIFICATIONS

6.1 Physical

The VPX6860 is a 6U VPX module that conforms to the 1" backplane spacing set forth by the VITA 48 specification (both air and conduction models).

Height	233.35 mm (9.187 in)
Depth	160.0 mm (6.299 in)
PCB Thickness	1.68 mm (0.066 in)
Unit Weight (Air-Cooled):	24.75 oz (0.7015 kg)
Unit Weight (Conduction-Cooled):	32.61 oz (0.9245 kg)
Unit Weight (RTM):	9.46 oz (0.2683 kg)

6.2 Connector Information

6.2.1 VPX Backplane Connectors

6.2.1.1 P0 VPX Connector

P0 Wafer	A	B	C	D	E	F	G
1	N/C	N/C	N/C	N/C	+12 V	+12 V	+12 V
2	N/C	N/C	N/C	N/C	+12 V	+12 V	+12 V
3	+5 V	+5 V	+5 V	N/C	+5 V	+5 V	+5 V
4	NVMRO	SYSRESET#	GND	N/C	GND	N/C	N/C
5	SMB_DATA	SMB_CLK	GND	+3.3V AUX	GND	GA4#	N/C
6	GA0#	GA1#	GND	N/C	GND	GA2#	GA3#
7	N/C	N/C	GND	N/C	N/C	GND	N/C
8	GND	N/C	N/C	GND	N/C	N/C	GND

6.2.1.2 P1 VPX Connector

P1 Wafer	A	B	C	D	E	F	G
1	40GBE_DP1_RX0_P	40GBE_DP1_RX0_N	GND	40GBE_DP1_TX0_P	40GBE_DP1_TX0_N	GND	N/C
2	GND	40GBE_DP1_RX1_P	40GBE_DP1_RX1_N	GND	40GBE_DP1_TX1_P	40GBE_DP1_TX1_N	GND
3	40GBE_DP1_RX2_P	40GBE_DP1_RX2_N	GND	40GBE_DP1_TX2_P	40GBE_DP1_TX2_N	GND	VPX_VBAT
4	GND	40GBE_DP1_RX3_P	40GBE_DP1_RX3_N	GND	40GBE_DP1_TX3_P	40GBE_DP1_TX3_N	GND
5	40GBE_DP2_RX0_P	40GBE_DP2_RX0_N	GND	40GBE_DP2_TX0_P	40GBE_DP2_TX0_N	GND	SYS_CON#
6	GND	40GBE_DP2_RX1_P	40GBE_DP2_RX1_N	GND	40GBE_DP2_TX1_P	40GBE_DP2_TX1_N	GND
7	40GBE_DP2_RX2_P	40GBE_DP2_RX2_N	GND	40GBE_DP2_TX2_P	40GBE_DP2_TX2_N	GND	N/C
8	GND	40GBE_DP2_RX3_P	40GBE_DP2_RX3_N	GND	40GBE_DP2_TX3_P	40GBE_DP2_TX3_N	GND
9	N/C	N/C	GND	N/C	N/C	GND	N/C
10	GND	N/C	N/C	GND	N/C	N/C	GND
11	N/C	N/C	GND	N/C	N/C	GND	N/C
12	GND	N/C	N/C	GND	N/C	N/C	GND
13	N/C	N/C	GND	N/C	N/C	GND	RESERVED
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	N/C
16	GND	N/C	N/C	GND	N/C	N/C	GND

6.2.1.3 P2 VPX Connector

P2 Wafer	A	B	C	D	E	F	G
1	PCIE_EP1_RX0_P	PCIE_EP1_RX0_N	GND	PCIE_EP1_TX0_P	PCIE_EP1_TX0_N	GND	N/C
2	GND	PCIE_EP1_RX1_P	PCIE_EP1_RX1_N	GND	PCIE_EP1_TX1_P	PCIE_EP1_TX1_N	GND
3	PCIE_EP1_RX2_P	PCIE_EP1_RX2_N	GND	PCIE_EP1_TX2_P	PCIE_EP1_TX2_N	GND	N/C
4	GND	PCIE_EP1_RX3_P	PCIE_EP1_RX3_N	GND	PCIE_EP1_TX3_P	PCIE_EP1_TX3_N	GND
5	PCIE_EP1_RX4_P	PCIE_EP1_RX4_N	GND	PCIE_EP1_TX4_P	PCIE_EP1_TX4_N	GND	N/C
6	GND	PCIE_EP1_RX5_P	PCIE_EP1_RX5_N	GND	PCIE_EP1_TX5_P	PCIE_EP1_TX5_N	GND
7	PCIE_EP1_RX6_P	PCIE_EP1_RX6_N	GND	PCIE_EP1_TX6_P	PCIE_EP1_TX6_N	GND	N/C
8	GND	PCIE_EP1_RX7_P	PCIE_EP1_RX7_N	GND	PCIE_EP1_TX7_P	PCIE_EP1_TX7_N	GND
9	PCIE_EP2_RX0_P	PCIE_EP2_RX0_N	GND	PCIE_EP2_TX0_P	PCIE_EP2_TX0_N	GND	N/C
10	GND	PCIE_EP2_RX1_P	PCIE_EP2_RX1_N	GND	PCIE_EP2_TX1_P	PCIE_EP2_TX1_N	GND
11	PCIE_EP2_RX2_P	PCIE_EP2_RX2_N	GND	PCIE_EP2_TX2_P	PCIE_EP2_TX2_N	GND	N/C
12	GND	PCIE_EP2_RX3_P	PCIE_EP2_RX3_N	GND	PCIE_EP2_TX3_P	PCIE_EP2_TX3_N	GND
13	PCIE_EP2_RX4_P	PCIE_EP2_RX4_N	GND	PCIE_EP2_TX4_P	PCIE_EP2_TX4_N	GND	N/C
14	GND	PCIE_EP2_RX5_P	PCIE_EP2_RX5_N	GND	PCIE_EP2_TX5_P	PCIE_EP2_TX5_N	GND
15	PCIE_EP2_RX6_P	PCIE_EP2_RX6_N	GND	PCIE_EP2_TX6_P	PCIE_EP2_TX6_N	GND	N/C
16	GND	PCIE_EP2_RX7_P	PCIE_EP2_RX7_N	GND	PCIE_EP2_TX7_P	PCIE_EP2_TX7_N	GND

6.2.1.4 P3 VPX Connector

P3 Wafer	A	B	C	D	E	F	G
1	N/C	N/C	GND	N/C	N/C	GND	COM4_TX
2	GND	N/C	N/C	GND	N/C	N/C	GND
3	J16_SIO18_P	J16_SIO18_N	GND	N/C	N/C	GND	COM4_RTS#_485_TX-
4	GND	J16_SIO17_P	J16_SIO17_N	GND	J16_SIO16_P	J16_SIO16_N	GND
5	J16_SIO15_P	J16_SIO15_N	GND	J16_SIO14_P	J16_SIO14_N	GND	COM4_RX
6	GND	J16_SIO13_P	J16_SIO13_N	GND	J16_SIO12_P	J16_SIO12_N	GND
7	J16_SIO11_P	J16_SIO11_N	GND	J16_SIO10_P	J16_SIO10_N	GND	COM4_CTS#_485_RX-
8	GND	J16_SIO9_P	J16_SIO9_N	GND	J16_SIO8_P	J16_SIO8_N	GND
9	J16_SIO7_P	J16_SIO7_N	GND	J16_SIO6_P	J16_SIO6_N	GND	COM3_TX
10	GND	J16_SIO5_P	J16_SIO5_N	GND	J16_SIO4_P	J16_SIO4_N	GND
11	J16_SIO3_P	J16_SIO3_N	GND	J16_SIO2_P	J16_SIO2_N	GND	COM3_RTS#_485_TX-
12	GND	J16_SIO1_P	J16_SIO1_N	GND	J16_SIO0_P	J16_SIO0_N	GND
13	N/C	N/C	GND	N/C	N/C	GND	COM3_RX
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	COM3_CTS#_485_RX-
16	GND	N/C	N/C	GND	N/C	N/C	GND

6.2.1.5 P4 VPX Connector

P4 Wafer	A	B	C	D	E	F	G
1	J16_DP05_N	J16_DP05_P	GND	J16_DP04_N	J16_DP04_P	GND	ENET_TP1_LINK#
2	GND	J16_DP07_N	J16_DP07_P	GND	J16_DP06_N	J16_DP06_P	GND
3	J16_DP09_N	J16_DP09_P	GND	J16_DP08_N	J16_DP08_P	GND	ENET_TP2_LINK#
4	GND	J16_DP15_N	J16_DP15_P	GND	J16_DP14_N	J16_DP14_P	GND
5	J16_DP17_N	J16_DP17_P	GND	J16_DP16_N	J16_DP16_P	GND	ENET_UTP2_LINK#
6	GND	J16_DP19_N	J16_DP19_P	GND	J16_DP18_N	J16_DP18_P	GND
7	J16_DP01_N	J16_DP01_P	GND	J16_DP00_N	J16_DP00_P	GND	ENET_UTP1_LINK#
8	GND	J16_DP03_N	J16_DP03_P	GND	J16_DP02_N	J16_DP02_P	GND
9	J16_DP11_N	J16_DP11_P	GND	J16_DP10_N	J16_DP10_P	GND	N/C
10	GND	J16_DP13_N	J16_DP13_P	GND	J16_DP12_N	J16_DP12_P	GND
11	UTP_CP2_RX_P	UTP_CP2_RX_N	GND	UTP_CP2_TX_P	UTP_CP2_TX_N	GND	N/C
12	GND	UTP_CP1_RX_P	UTP_CP1_RX_N	GND	UTP_CP1_TX_P	UTP_CP1_TX_N	GND
13	TP_CP2_P0_P	TP_CP2_P0_N	GND	TP_CP2_P1_P	TP_CP2_P1_N	GND	GPIN3
14	GND	TP_CP2_P2_P	TP_CP2_P2_N	GND	TP_CP2_P3_P	TP_CP2_P3_N	GND
15	TP_CP1_P0_P	TP_CP1_P0_N	GND	TP_CP1_P1_P	TP_CP1_P1_N	GND	GPOUT3
16	GND	TP_CP1_P2_P	TP_CP1_P2_N	GND	TP_CP1_P3_P	TP_CP1_P3_N	GND

6.2.1.6 P5 VPX Connector

P5 Wafer	A	B	C	D	E	F	G
1	AP FIELD I/O 49	AP FIELD I/O 50	GND	AP FIELD I/O 47	AP FIELD I/O 48	GND	N/C
2	GND	AP FIELD I/O 45	AP FIELD I/O 46	GND	AP FIELD I/O 43	AP FIELD I/O 44	GND
3	AP FIELD I/O 41	AP FIELD I/O 42	GND	AP FIELD I/O 39	AP FIELD I/O 40	GND	N/C
4	GND	AP FIELD I/O 37	AP FIELD I/O 38	GND	AP FIELD I/O 35	AP FIELD I/O 36	GND
5	AP FIELD I/O 33	AP FIELD I/O 34	GND	AP FIELD I/O 31	AP FIELD I/O 32	GND	N/C
6	GND	AP FIELD I/O 29	AP FIELD I/O 30	GND	AP FIELD I/O 27	AP FIELD I/O 28	GND
7	AP FIELD I/O 25	AP FIELD I/O 26	GND	AP FIELD I/O 23	AP FIELD I/O 24	GND	N/C
8	GND	AP FIELD I/O 21	AP FIELD I/O 22	GND	AP FIELD I/O 19	AP FIELD I/O 20	GND
9	AP FIELD I/O 17	AP FIELD I/O 18	GND	AP FIELD I/O 15	AP FIELD I/O 16	GND	N/C
10	GND	AP FIELD I/O 13	AP FIELD I/O 14	GND	AP FIELD I/O 11	AP FIELD I/O 12	GND
11	AP FIELD I/O 9	AP FIELD I/O 10	GND	AP FIELD I/O 7	AP FIELD I/O 8	GND	N/C
12	GND	AP FIELD I/O 5	AP FIELD I/O 6	GND	AP FIELD I/O 3	AP FIELD I/O 4	GND
13	AP FIELD I/O 1	AP FIELD I/O 2	GND	N/C	N/C	GND	N/C
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	N/C
16	GND	N/C	N/C	GND	N/C	N/C	GND

6.2.1.7 P6 VPX Connector

P6 Wafer	A	B	C	D	E	F	G
1	USB6_P	USB6_N	GND	USB5_P	USB5_N	GND	GPIN0
2	GND	DPC_AUX_SEL	USB_5_6_OC#	GND	DPB_AUX_SEL	USB_1_2_OC#	GND
3	USB1_SSRX_P	USB1_SSRX_N	GND	USB1_P	USB1_N	GND	GPIN1
4	GND	USB2_P	USB2_N	GND	USB1_SSTX_P	USB1_SSTX_N	GND
5	USB2_SSTX_P	USB2_SSTX_N	GND	USB2_SSRX_P	USB2_SSRX_N	GND	GPIN2
6	GND	AGND_AUDIO	LINEOUT_L	GND	AGND_AUDIO	LINEIN_L	GND
7	LINEOUT_R	AGND_AUDIO	GND	LINEIN_R	AGND_AUDIO	GND	GPOUT0
8	GND	SATA2_RX_P	SATA2_RX_N	GND	SATA2_TX_P	SATA2_TX_N	GND
9	SATA3_RX_P	SATA3_RX_N	GND	SATA3_TX_P	SATA3_TX_N	GND	GPOUT1
10	GND	DPB_TX1_P	DPB_TX1_N	GND	DPB_TX0_P	DPB_TX0_N	GND
11	DPB_TX3_P	DPB_TX3_N	GND	DPB_TX2_P	DPB_TX2_N	GND	GPOUT2
12	GND	COM1_RTS#_485_TX-	COM1_TX	GND	DPB_CTRL_AUX_P	DPB_CTRL_AUX_N	GND
13	COM1_CTS#_485_RX-	COM1_RX	GND	COM2_RTS#_485_TX-	COM2_TX	GND	DPB_HPD
14	GND	DPC_TX1_P	DPC_TX1_N	GND	DPC_TX0_P	DPC_TX0_N	GND
15	DPC_TX3_P	DPC_TX3_N	GND	DPC_TX2_P	DPC_TX2_N	GND	DPC_HPD
16	GND	COM2_CTS#_485_RX-	COM2_RX	GND	DPC_CTRL_AUX_P	DPC_CTRL_AUX_N	GND

6.2.2 I/O Connectors

There are two USB 3.0 connectors and one Mini-DisplayPort connector located on the front panel of the air cooled VPX6860 model. Using these connectors, along with an on-board bootable M.2 storage device, the VPX6860 can be operated without the need for a Rear Transition Module.

There are also an RJ-45 Ethernet connector and a 50-pin AcroPack Field I/O connector available on the air-cooled model's front panel. See Section 3.1.4 for configuration information regarding this.

6.2.2.1 J6 USB 3.0 Connector (air-cooled only)

This standard 9-pin USB3.0 connector (Molex – 48394-003) brings USB Port 3 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB3_N
3	USB3_P
4	GND
5	USB3_SSRX_N
6	USB3_SSRX_P
7	GND
8	USB3_SSTX_N
9	USB3_SSTX_P

6.2.2.2 J7 USB 3.0 Connector (air-cooled only)

This standard 9-pin USB3.0 connector (Molex – 48394-003) brings USB Port 4 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB4_N
3	USB4_P
4	GND
5	USB4_SSRX_N
6	USB4_SSRX_P
7	GND
8	USB4_SSTX_N
9	USB4_SSTX_P

6.2.2.3 J8 Mini-DisplayPort Connector (air-cooled only)

This standard 20-pin Mini-DisplayPort connector (TE Connectivity – 2129320) brings DisplayPort D out to the front panel.

PIN	SIGNAL
1	GND
2	DPC_HPD
3	DPC_TX0_P
4	DPC_AUX_SEL
5	DPC_TX0_N
6	GND
7	GND
8	GND
9	DPC_TX1_P
10	DPC_TX3_P
11	DPC_TX1_N
12	DPC_TX3_N
13	GND
14	GND
15	DPC_TX2_P
16	DPC_CTRL_AUX_P
17	DPC_TX2_N
18	DPC_CTRL_AUX_N
19	GND
20	+3.3V

6.2.2.4 J10 RJ-45 1000BASE-T Ethernet Connector (air-cooled only)

This standard 8-pin 1000BASE-T connector (Bel Fuse – 0826-1K1T-23-F) brings Ethernet Port 0 out to the front panel. Note this port is only available when SW3-3 is OFF.

PIN	SIGNAL
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6.2.2.5 J9 Isolated DC-DC Socket for AcroPack Modules (air-cooled only)

This standard 20-pin DIP socket accepts an Isolated DC-DC power module for use with isolated AcroPack modules.

PIN	SIGNAL	FIELD I/O PIN
1	GND	
2	GND	
8	Isolated COM	FIELD I/O 48
10	Isolated -VOUT	FIELD I/O 49
11	Isolated +VOUT	FIELD I/O 50
13	Isolated COM	FIELD I/O 48
19	+12V Input	
20	+12V Input	

6.2.2.6 J4 AcroPack Field I/O Connector (air-cooled only)

This 50-pin 0.8mm CHAMP connector (TE – 6658751-1) brings the AcroPack Field I/O connections to the front panel.

PIN	SIGNAL	PIN	SIGNAL
1	FIELD I/O 1	**26**	FIELD I/O 2
2	FIELD I/O 3	**27**	FIELD I/O 4
3	FIELD I/O 5	**28**	FIELD I/O 6
4	FIELD I/O 7	**29**	FIELD I/O 8
5	FIELD I/O 9	**30**	FIELD I/O 10
6	FIELD I/O 11	**31**	FIELD I/O 12
7	FIELD I/O 13	**32**	FIELD I/O 14
8	FIELD I/O 15	**33**	FIELD I/O 16
9	FIELD I/O 17	**34**	FIELD I/O 18
10	FIELD I/O 19	**35**	FIELD I/O 20
11	FIELD I/O 21	**36**	FIELD I/O 22
12	FIELD I/O 23	**37**	FIELD I/O 24
13	FIELD I/O 25	**38**	FIELD I/O 26
14	FIELD I/O 27	**39**	FIELD I/O 28
15	FIELD I/O 29	**40**	FIELD I/O 30
16	FIELD I/O 31	**41**	FIELD I/O 32
17	FIELD I/O 33	**42**	FIELD I/O 34
18	FIELD I/O 35	**43**	FIELD I/O 36
19	FIELD I/O 37	**44**	FIELD I/O 38
20	FIELD I/O 39	**45**	FIELD I/O 40
21	FIELD I/O 41	**46**	FIELD I/O 42
22	FIELD I/O 43	**47**	FIELD I/O 44
23	FIELD I/O 45	**48**	FIELD I/O 46
24	FIELD I/O 47	**49**	FIELD I/O 48
25	FIELD I/O 49	**50**	FIELD I/O 50

6.3 Power Requirements

The VPX6860 requires +12V(VS1) and +5V from the VPX backplane.

Additionally, the switch SW2 can be used to configure certain devices to use the auxiliary +3.3V_AUX supply instead of the onboard-generated +3.3V supply.

The amount of power required to properly operate the VPX6860 module will vary depending on many variables, including the operating system, application software, and the components that the module is integrated with. See notes below for defined variables used to measure the following power values:

12V:

S0 Idle[1]:	3.5A (42W)	S0 Max[2]:	8A (96W)
S0 Typ[3]:	6.5A (78W)		

[1] S0 Idle was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System, idle at desktop with no active applications running. 32GB RAM. One connected SATA device, one USB keyboard, one USB mouse, DisplayPort monitor.

[2] S0 Max was measured with module operating at 23°C ambient with 600LFM airflow, using Windows 8.1 Operating System. Prime95 Large FFT torture test stressing all CPU cores at max. 32GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, DisplayPort monitor.

Power is shown as PL1/PL2, where PL1 is the long-term power used, and PL2 is a short-term (typically <30 sec) power draw during turbo bursts. If Turbo is not used the board should not exceed the PL1 power, but performance may be impacted.

[3] S0 Typ was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System. Passmark Burn-In test running the following tests: CPU, Memory, 2D Graphics, 3D Graphics, Disk, and Network. 16GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, DisplayPort monitor.

6.4 Environmental Considerations

6.4.1 Operating Temperature

0°C to 70°C (Air Cooled models) [1]
-40°C to 85°C (Conduction Cooled models) [2]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification. Tested under Windows 8.1 with Passmark BurnInTest V7.1, running CPU, Memory, and 3D Graphics tests simultaneously. During application testing CPU temp should be closely monitored for max junction temp of 100°C using a program such as Argus Monitor or Open Hardware Monitor.

[2] Measured as Ambient Air Temperature inside conduction VPX enclosure. Every board sold tested to ensure this temperature specification. Tested under Windows 8.1 with Passmark BurnInTest V7.1 running CPU, Memory, Disk, and 3D Graphics tests simultaneously. During application testing CPU temp should be closely monitored for max junction temp of 100°C using a program such as Argus Monitor or Open Hardware Monitor.

Note: CPU frequency throttling will occur if the CPU Tj temperature reaches 100°C. This is an effective mechanism to keep the unit from overheating. A small amount of intermittent throttling at high ambient temperatures is to be expected and does not greatly affect system performance. However, an inadequate final thermal solution as the result of inadequate air flow or improper conduction mounting could result in continual CPU throttling which will greatly affect system performance.

6.4.2 Relative Humidity

5% to 95% Non-condensing

6.4.3 Vibration and Shock Standards

Vibration, Random Operating: Designed to comply with VITA 47 Class V1. Shall withstand vibration from 5 to 100Hz. with Power Spectral Density (PSD) = 0.04g2/Hz, for 1 hour per axis. Testing shall be in accordance with MIL-STD-810, Method 514, Procedure 1

Shock, Operating: Designed to comply with VITA 47 Class OS1, 20g, 11ms half sine and terminal sawtooth shock pulses. 3 shock pulses in each direction along 3 axes (36 shocks, total). Testing shall be in accordance with MIL-STD-810, Method 516, Procedure 1.

6.4.4 EMC Directives

The VPX6860 is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.

Note: This is a Class A product

- **RoHS Directive 2011/65/EU – All Models**
  In compliance per EN 50581

6.5 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Table 6.5.a
VPX6860-xx-20 MTBF

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	168,771	19.3	5,925.2
40°C	115,715	13.2	8,641.9

[1] FIT is Failures in 10^9 hours.

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Table 6.5.b
VPX6860-xx-50 MTBF

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	168,779	19.3	5,924.9
40°C	115,719	13.2	8,641.7

[1] FIT is Failures in 10^9 hours.

6.6 Installation of M.2 Expansion Cards and Battery Replacement

6.6.1 VPX6860-LF (Air-Cooled) M.2 Expansion Card Installation

The M.2 sites can support module sizes up to 2280. There are two different methods for securing the M.2 module to the VPX6860 depending on the size of the module.

For the 2280 sized module there is a non-removable spacer fixed to the bottom side of the VPX6860. A single M2 x 4mm screw is required to secure the module to the VPX6860.

For 2260 and 2242 sized modules there is a threaded non-removable spacer fixed to the Top side of the board. A washer and a shoulder screw are required to secure the module to the VPX6860.

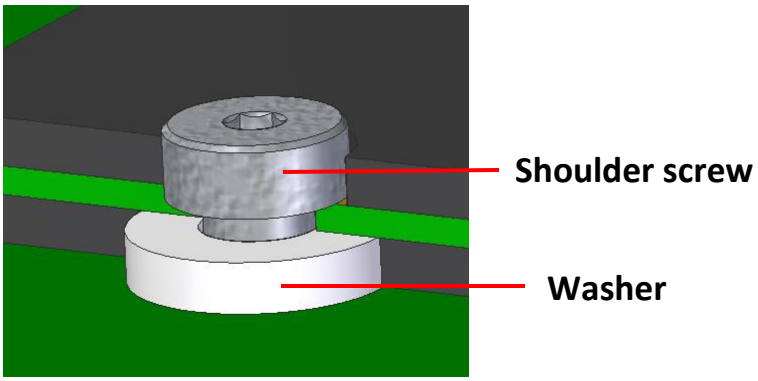
The following M.2 mounting hardware is supplied with each VPX6860:

Qty. 2 – Screw M2 x 4mm Philips Pan Head

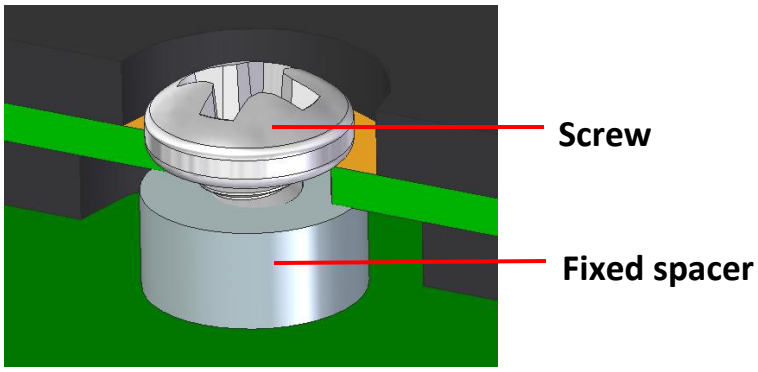
Qty. 2 - Shoulder Screw 3mm Dia. x 2mm long, M2 Thread, 1.5mm Hex

Qty. 2 – Washer Plastic Flat, ID .130in, OD .285in, Thickness 0.55 - 0.70in

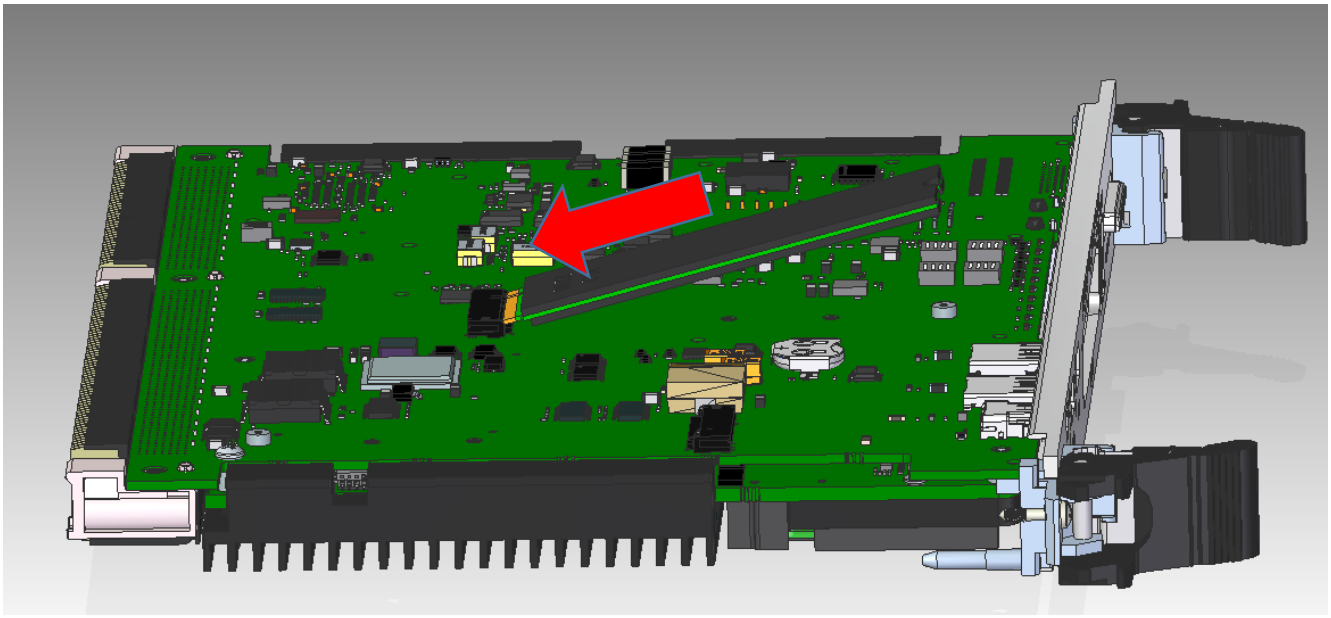
NOTE: When installing a 2260 or 2242 sized module the washer is under the M.2 module on the VPX660 and the shoulder screw is on top of the M.2 module as shown.



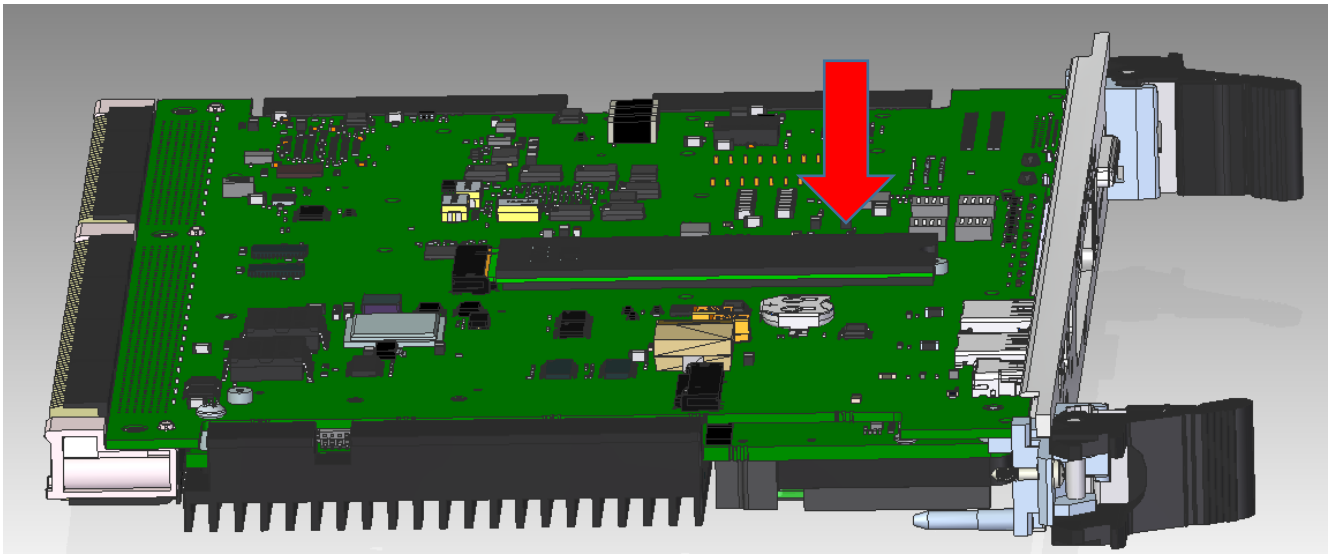
When installing a 2280 sized module use only the screw as shown.



1. Install the M.2 into the socket at approximately a 15° angle.



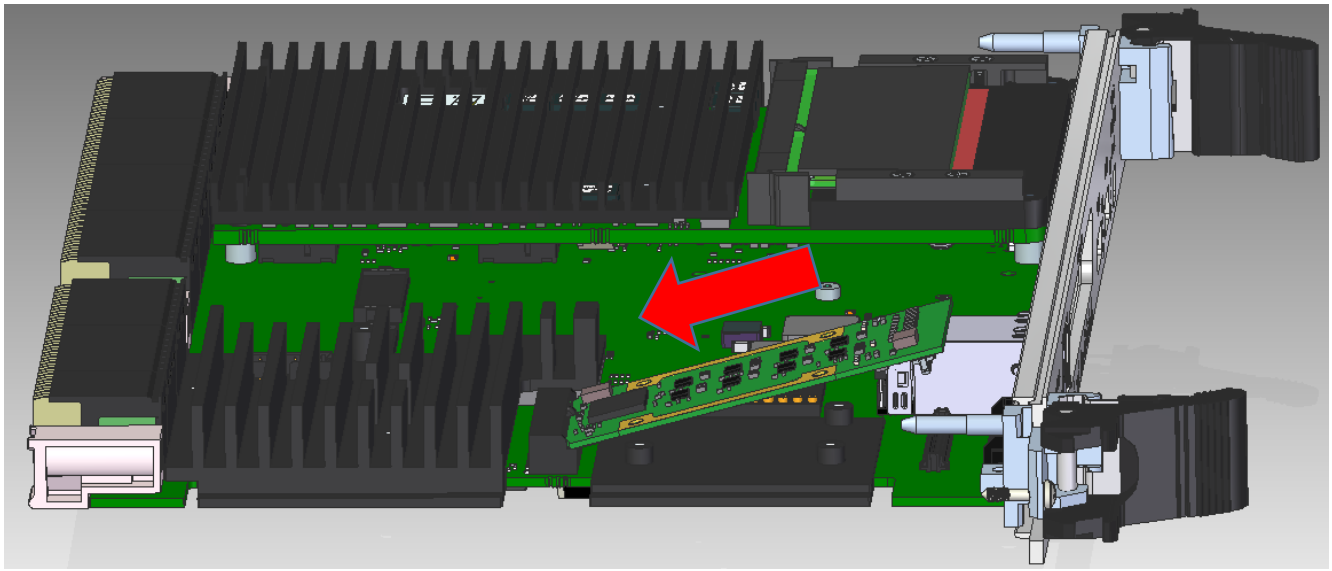
2. Press down and secure into place using one of the methods mentioned above.



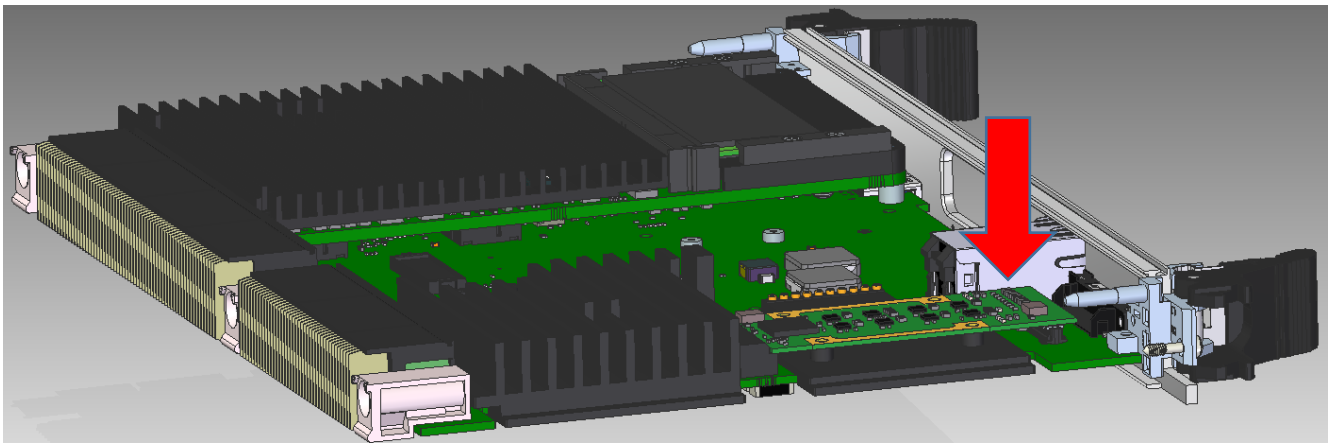
M.2 installation is complete.

6.6.2 VPX6860-LF (Air-Cooled) AcroPack Module Installation

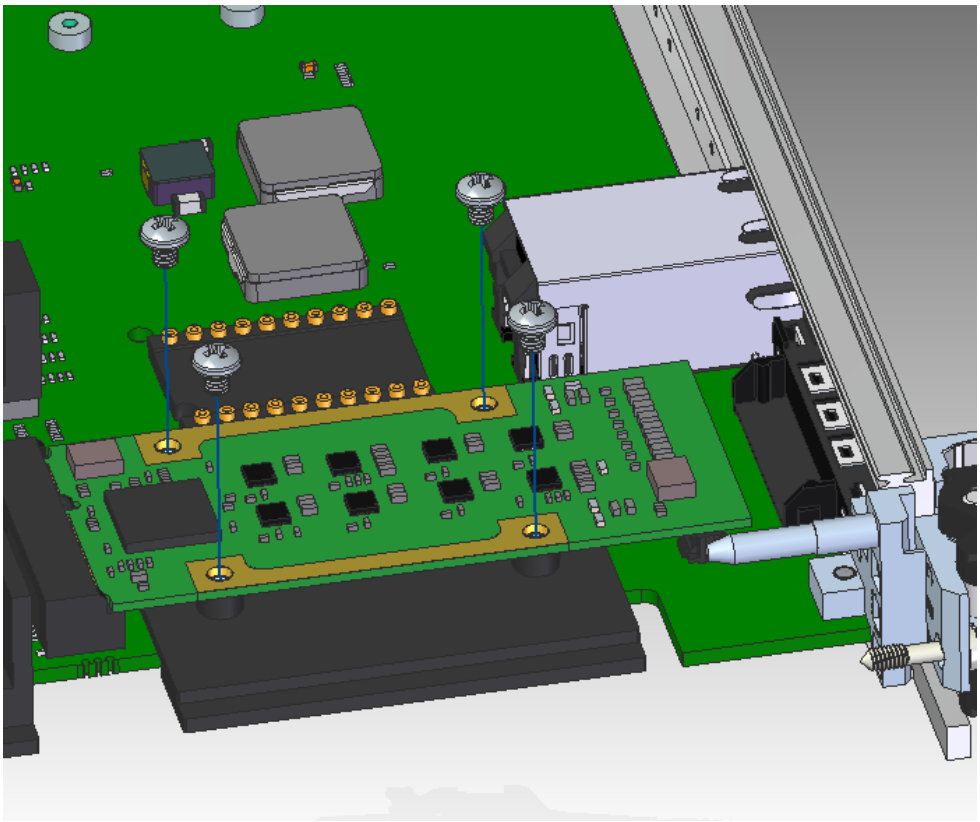
1. Install the AcroPack module into the socket at approximately a 15° angle.



2. Carefully align the AcroPack module while pressing down until the connector on the module is fully seated into the mating connector on the VPX6860.



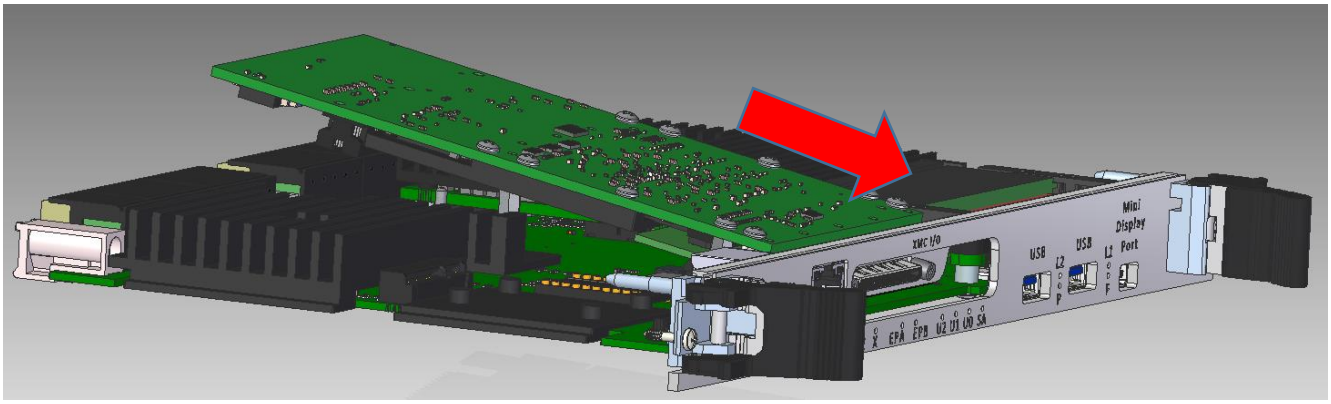
3. Secure with Qty. 4 screws (M2.5 x 3mm).



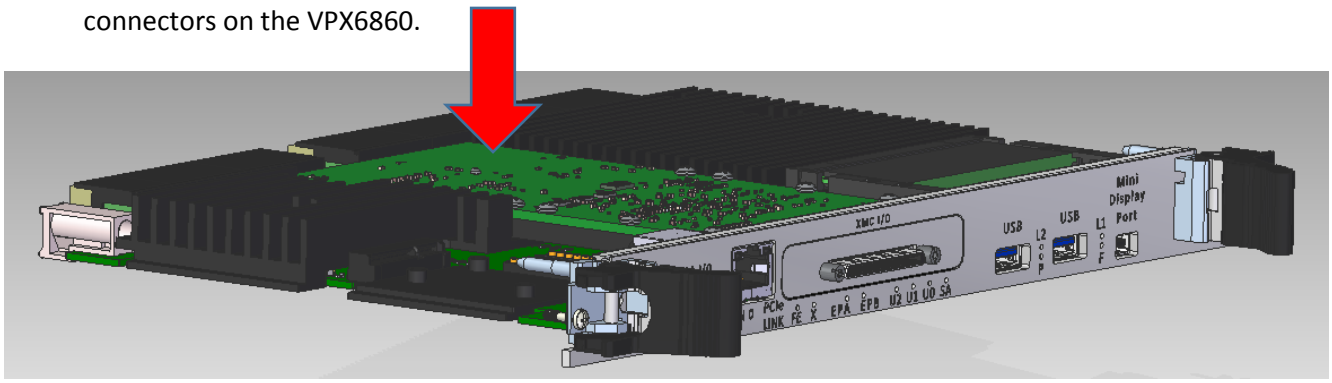
AcroPack installation is complete.

6.6.3 VPX6860-LF (Air-Cooled) XMC Module Installation

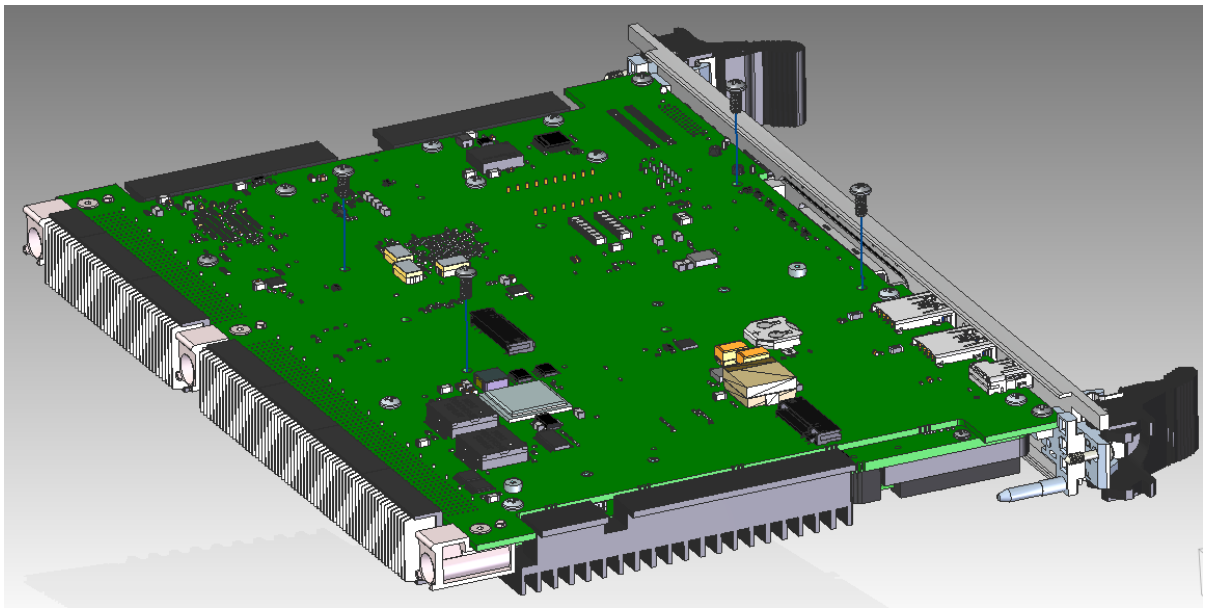
1. Insert the front of the XMC module into the XMC I/O opening located on the VPX6860 front panel first.



2. Push down on the back of the XMC module aligning the XMC interface connectors with the mating connectors on the VPX6860.



3. Secure with 4 screws (M2.5 x 6mm) on the bottom side of the VPX6860



XMC Module installation is complete

6.6.4 VPX6860-CC-LF (Conduction-Cooled) M.2 Expansion Card Installation

The M.2 sites can support module sizes up to 2280. There are two different methods for securing the M.2 module to the VPX6860 depending on the size of the module.

For the 2280 sized module there is a non-removable spacer fixed to the bottom side of the VPX6860. A single M2 x 4mm screw is required to secure the module to the VPX6860.

For 2260 and 2242 sized modules there is a threaded non-removable spacer fixed to the Top side of the board. A washer and a shoulder screw are required to secure the module to the VPX6860.

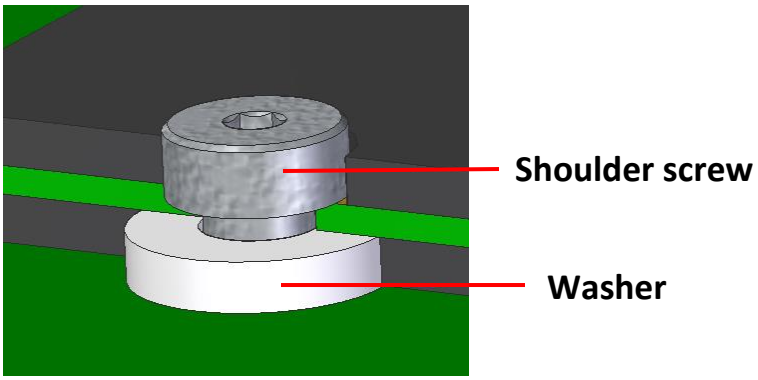
The following M.2 mounting hardware is supplied with each VPX6860:

Qty. 2 – Screw M2 x 4mm Philips Pan Head

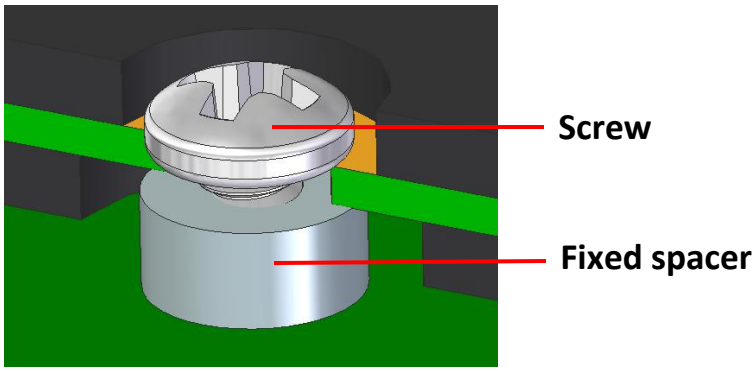
Qty. 2 - Shoulder Screw 3mm Dia. x 2mm long, M2 Thread, 1.5mm Hex

Qty. 2 – Washer Plastic Flat, ID .130in, OD .285in, Thickness 0.55 - 0.70in

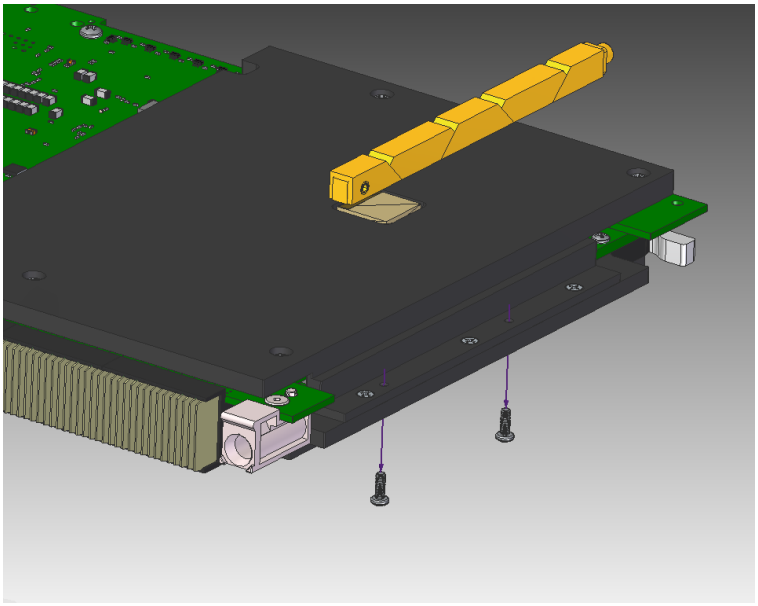
NOTE: When installing a 2260 or 2242 sized module the washer is under the M.2 module on the VPX660 and the shoulder screw is on top of the M.2 module as shown.



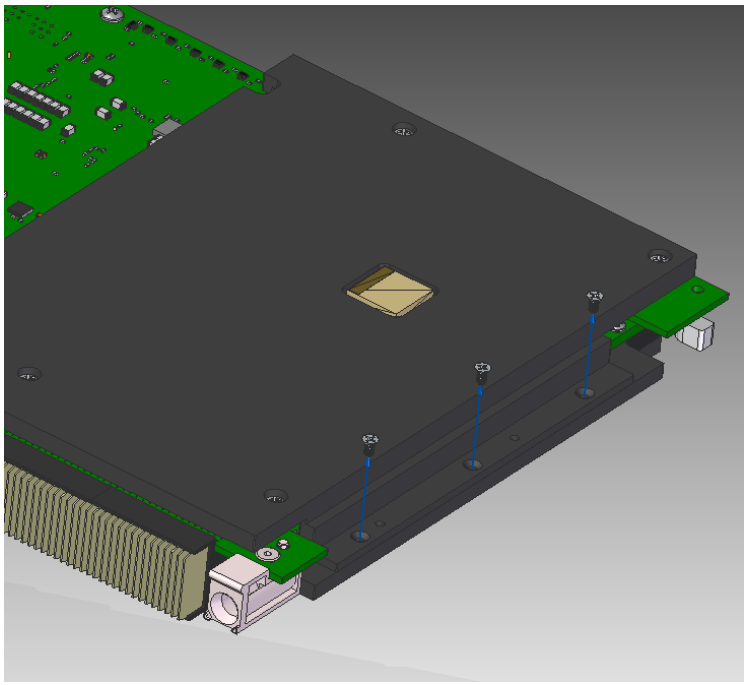
When installing a 2280 sized module use only the screw as shown.



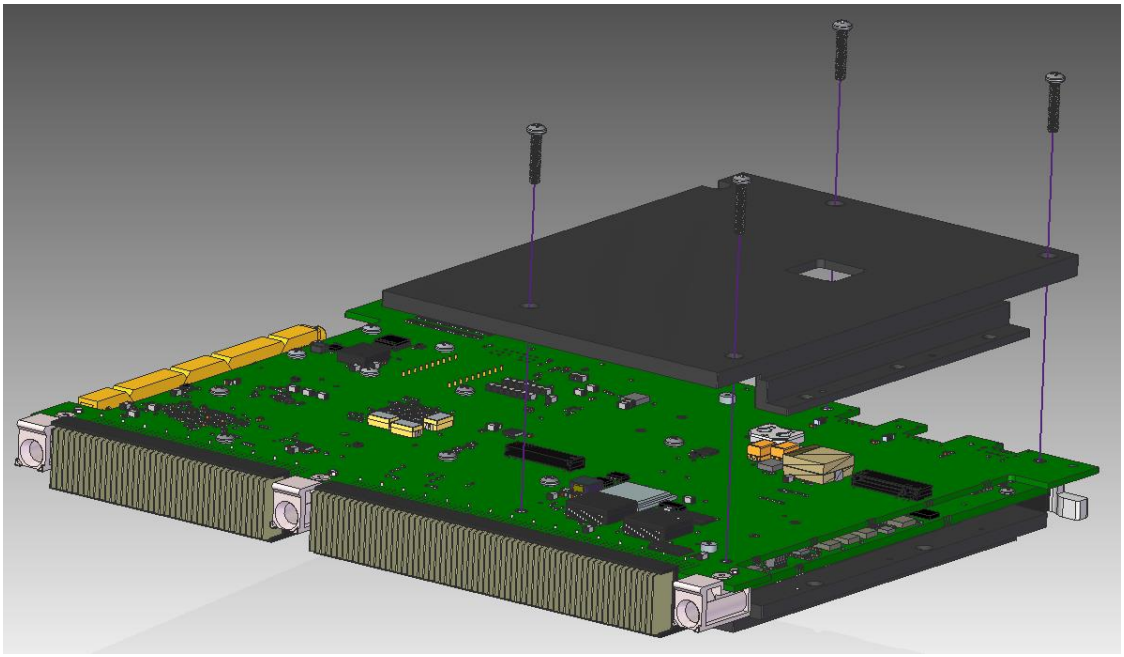
1. Remove the 2 screws (M2.5 x 6mm) that secure the wedge lock to the VPX6860. Remove the wedge lock to expose the 3 flat head screws (M2 x 4mm)



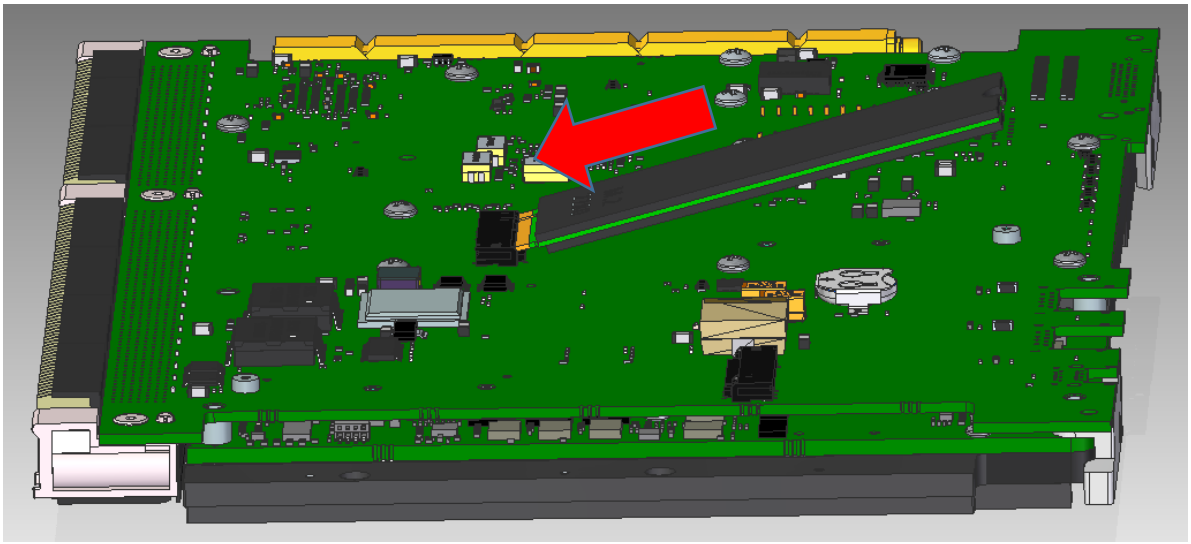
2. Remove the 3 flat head screws.



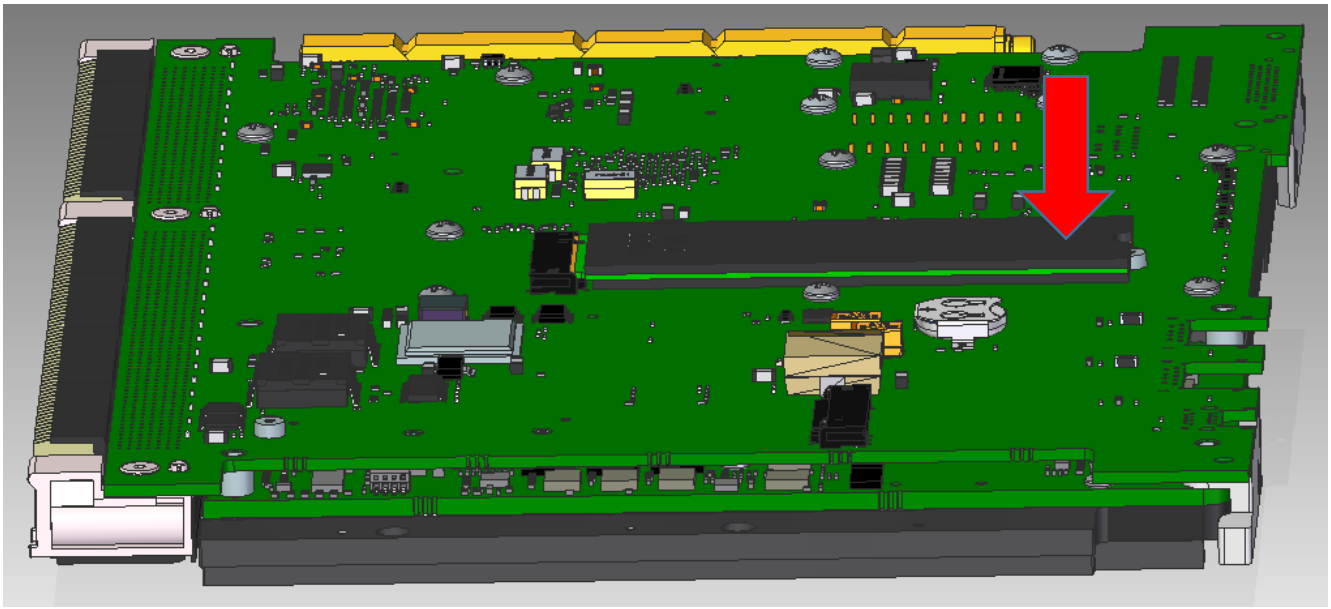
3. Remove the 4 remaining screws (M2.5 x 14mm) that secure the bottom conduction heatsink to the VPX6860. Remove the bottom conduction heatsink.



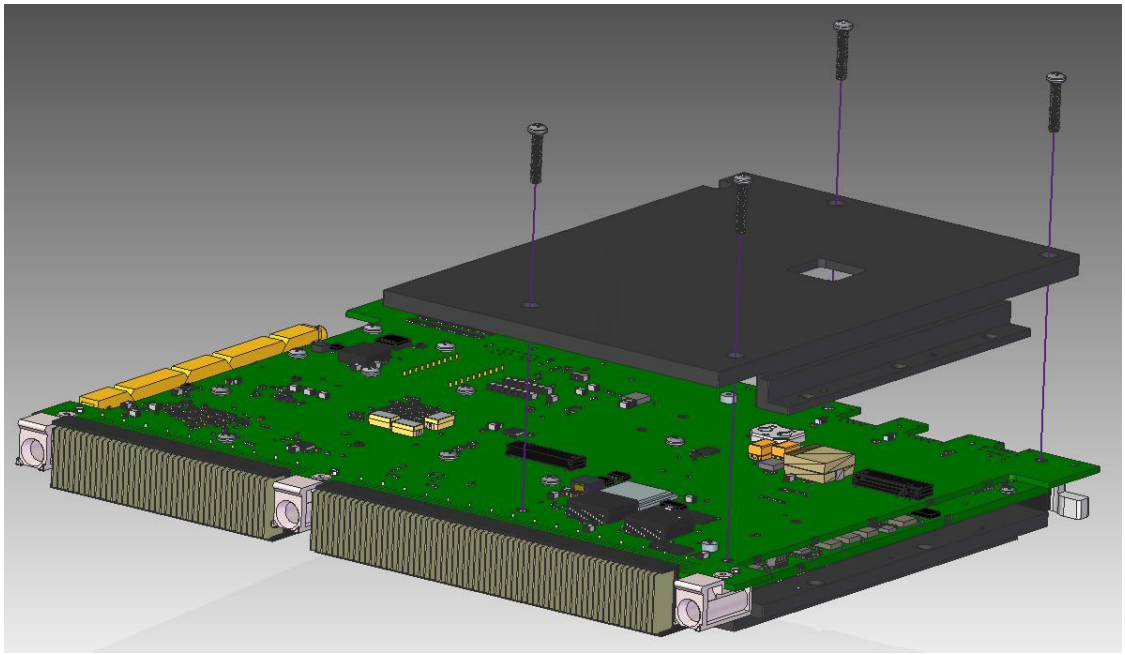
4. install the M.2 into the socket at approximately a 15° angle.



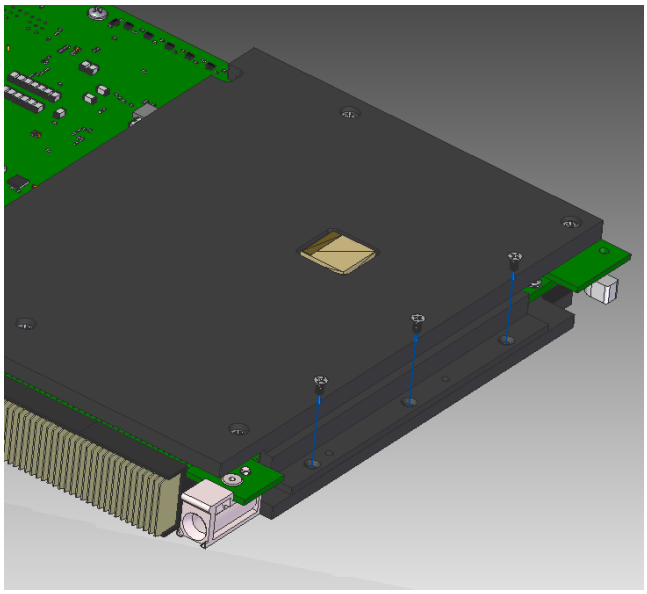
5. Press down and secure into place using one of the methods mentioned above.



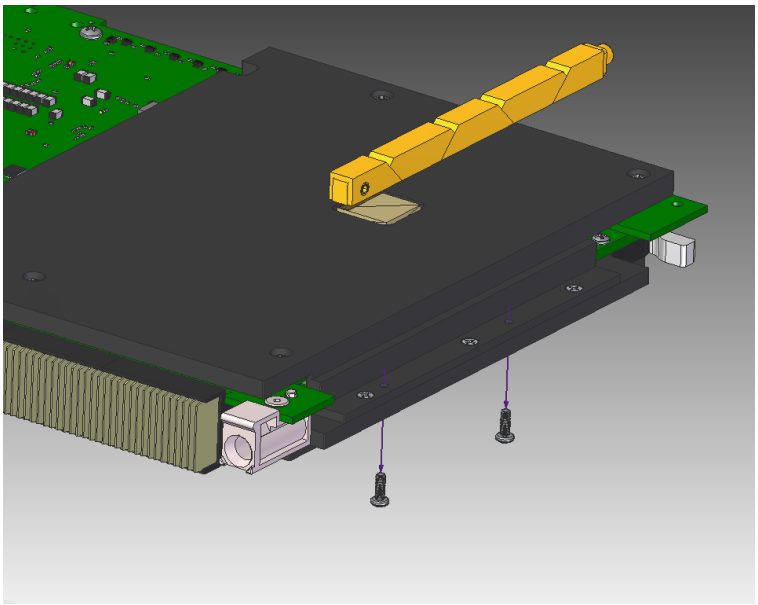
6. Install the bottom conduction heatsink and secure with 4 screws (M2.5 x 14mm).



7. Install the 3 flat head screws (M2 x 4mm) that secure the bottom conduction heatsink to the AE2200 heatsink.



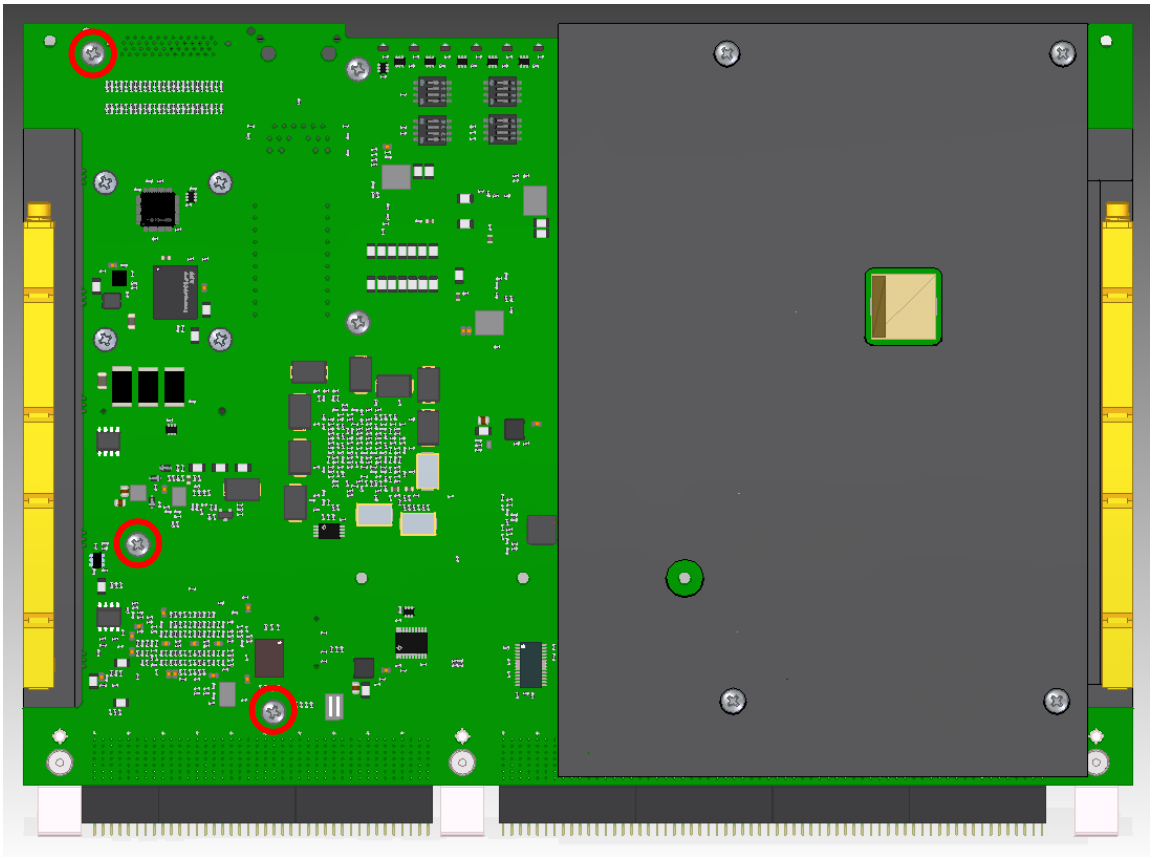
8. Install the wedge lock and secure with 2 screws (M2.5 x 6mm)



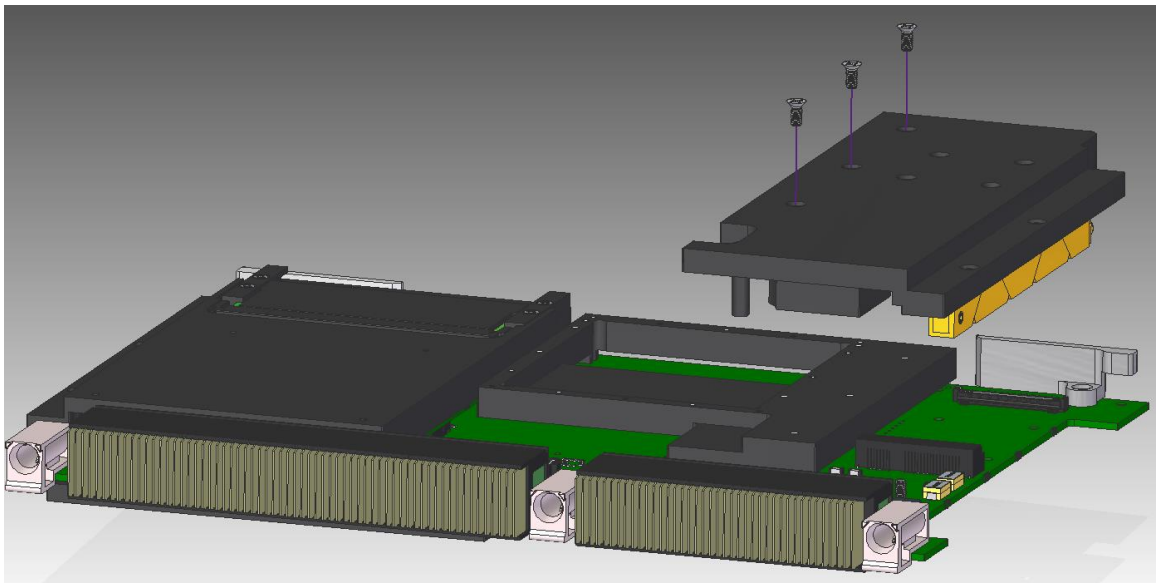
M.2 Installation is complete.

6.6.5 VPX6860-CC-LF (Conduction-Cooled) AcroPack Module Installation

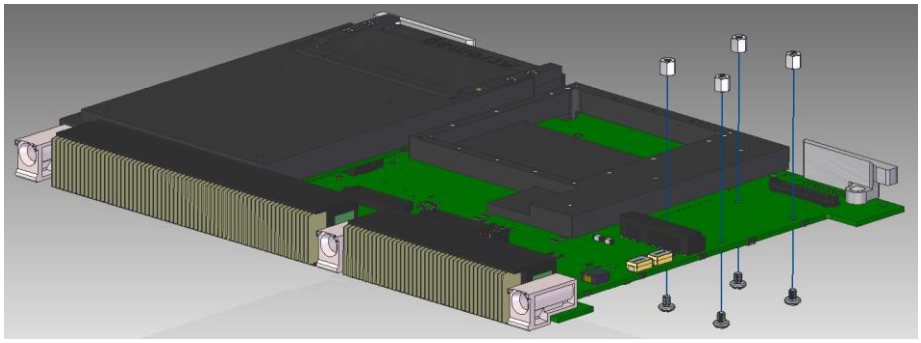
1. Remove 3 screws (M2.5 x 6mm) located on the bottom side of the VPX6860.



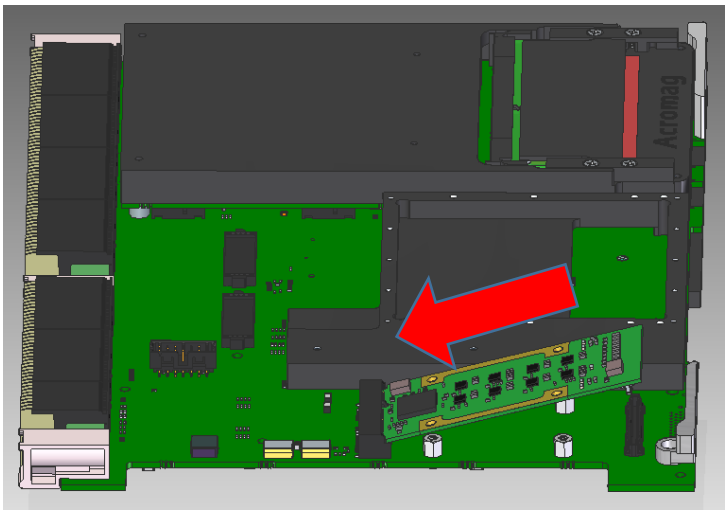
2. Remove the 3 screws (M2.5 x 6, Flat head) that secure the VPX6860 Conduction heatsink to the VPX6860, located on the top side of the board. Remove the heatsink.



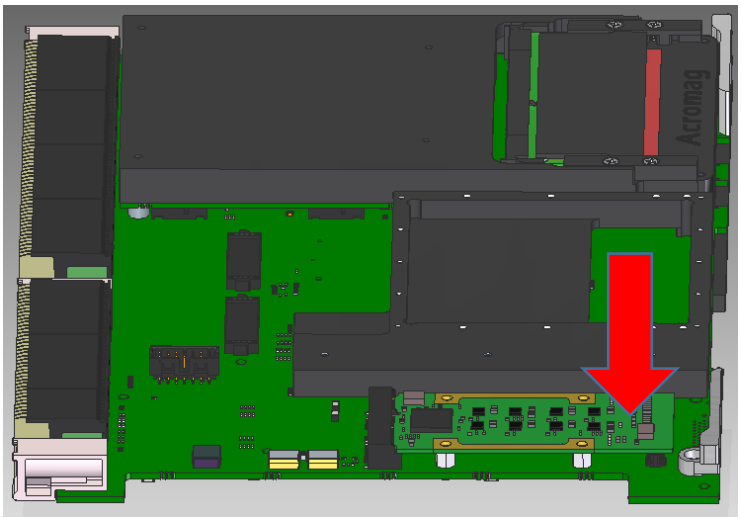
3. Attach the 4 standoffs (M2.5 x 4.5mm, Hex) that are supplied with AP-CC-01 (AcroPack Conduction Heatsink kit) and secure with 4 screws (M2.5 x 3mm).



4. Install the AcroPack module into the socket at approximately a 15° angle.

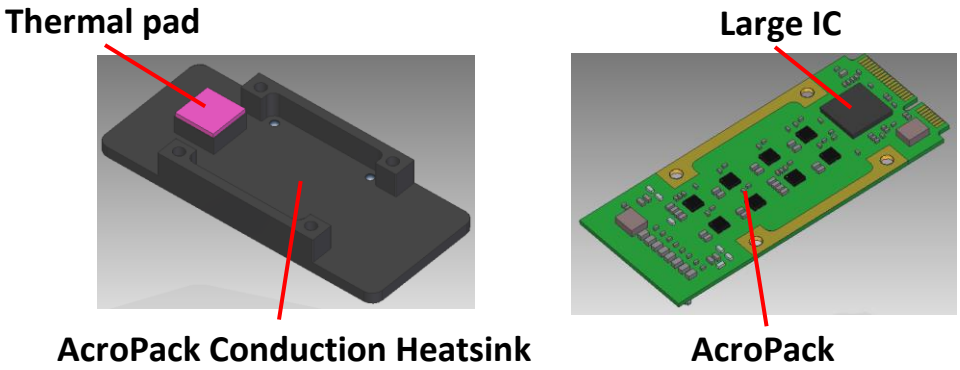


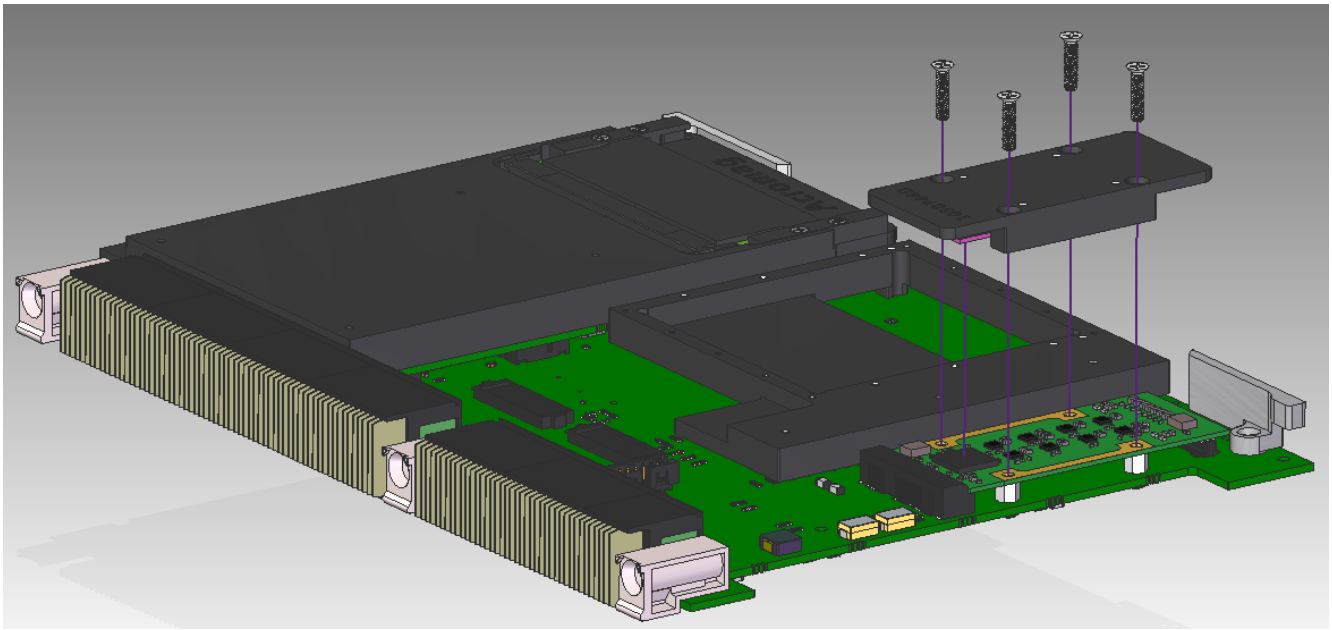
5. Carefully align the AcroPack module while pressing down until the connector on the module is fully seated into the mating connector on the VPX6860.



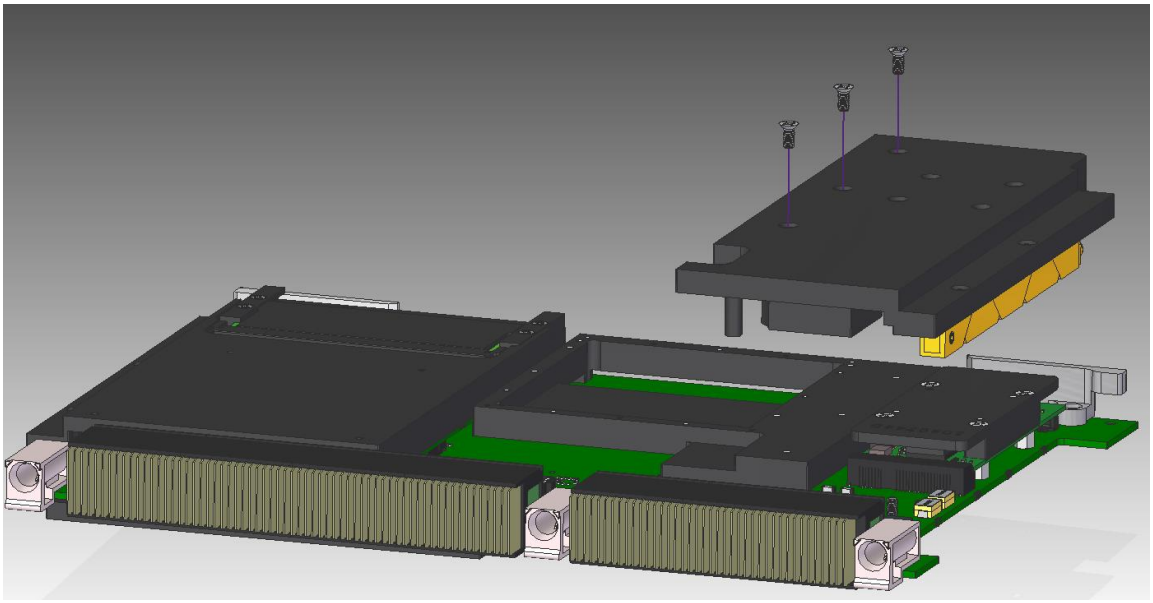
6. Install the AcroPack conduction heatsink (AP-CC-01) and secure with 4 screws (M2.5 x 12, Flat head)

Note: Ensure the thermal pad on the AcroPack conduction heatsink is positioned on the AcroPack module so that the thermal pad contacts the large IC on the AcroPack Module.

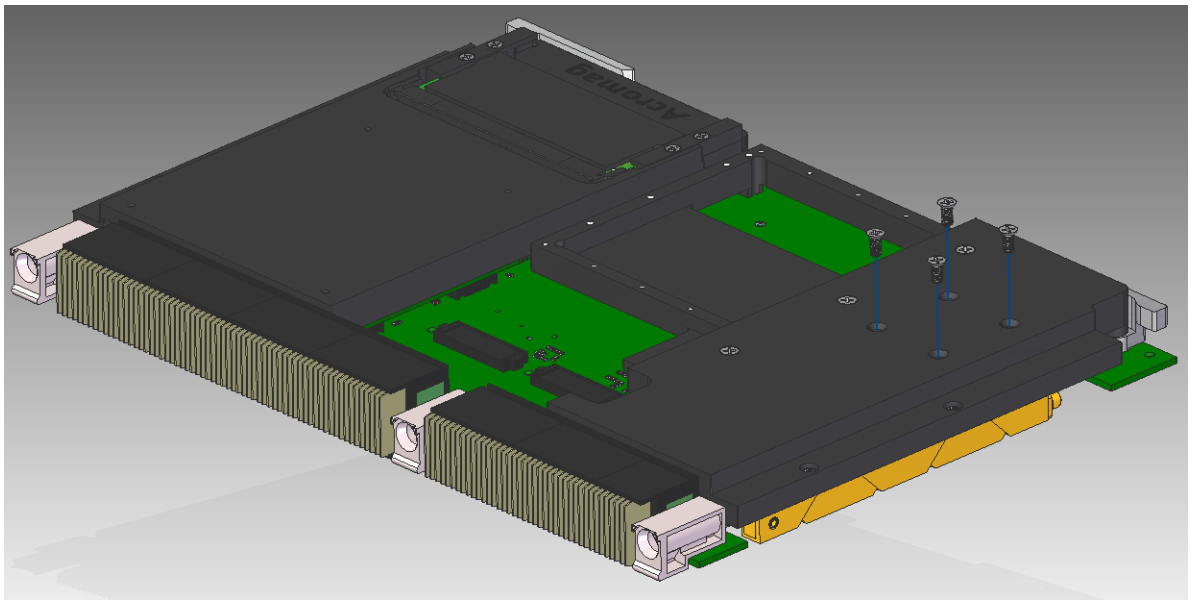




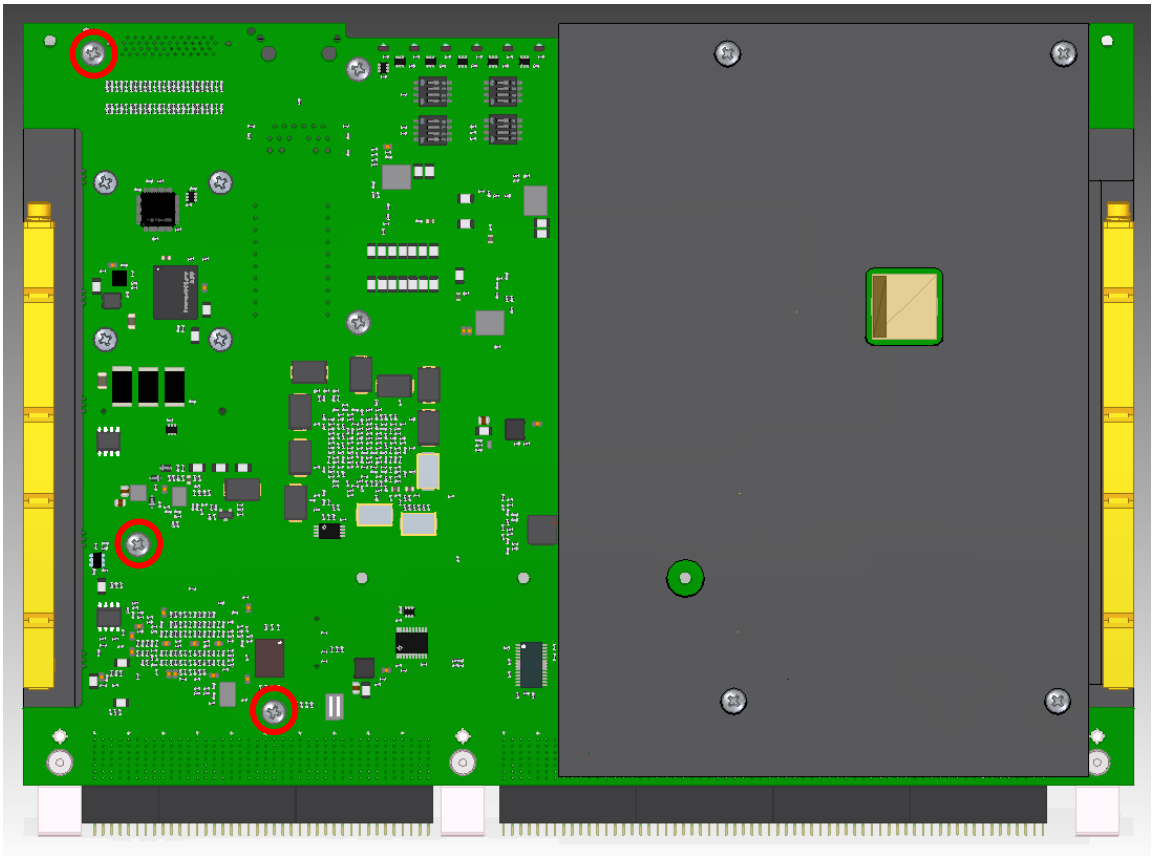
7. Install the VPX6860 top Conduction heatsink, secure with 3 screws (M2.5 x 6, Flat head).



8. Install the 4 screws (M2.5 x 6mm, flat head) that secure the AP-CC-01 heatsink to the VPX6860 heatsink.



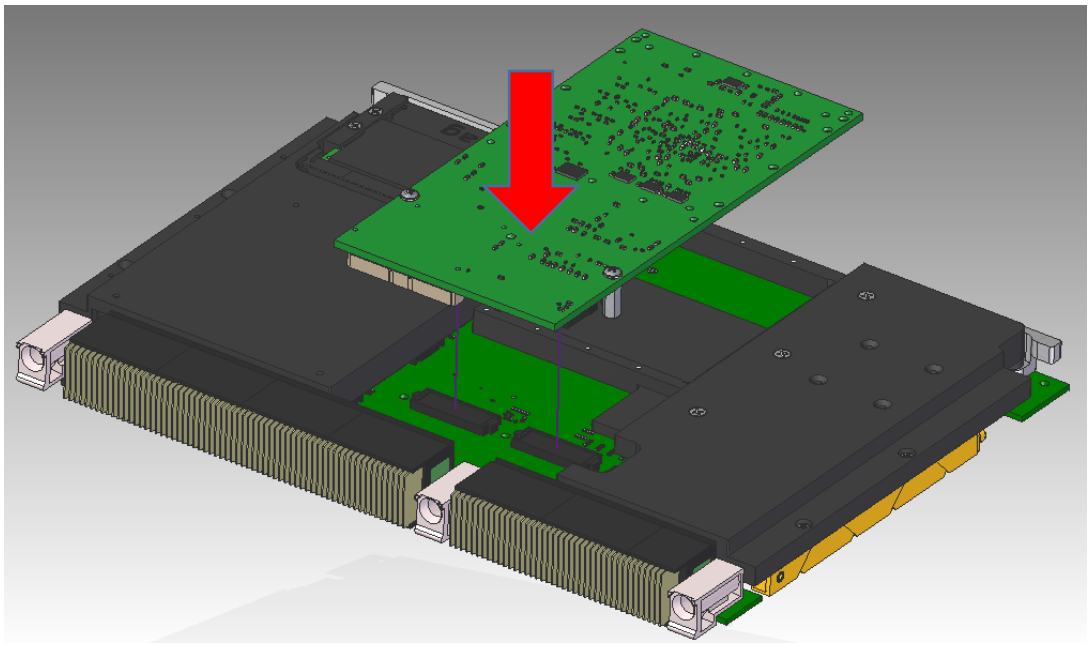
9. Install 3 screws (M2.5 x 6mm) located on the bottom side of the VPX6860.



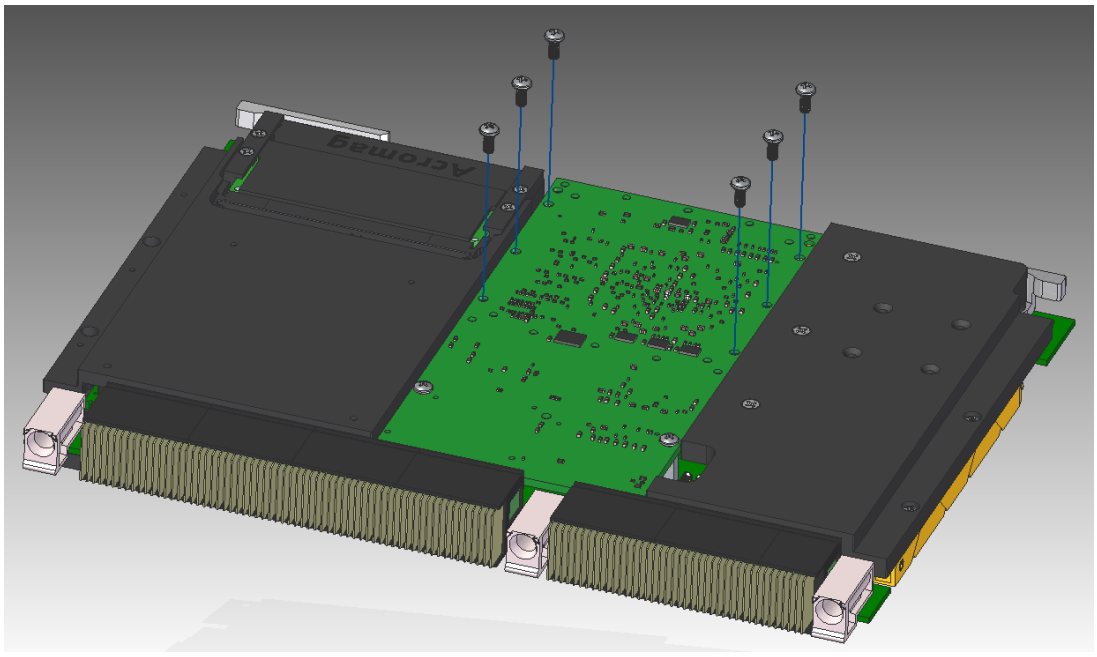
AcroPack module installation is complete.

6.6.6 VPX6860-CC-LF (Conduction-Cooled) XMC Module Installation

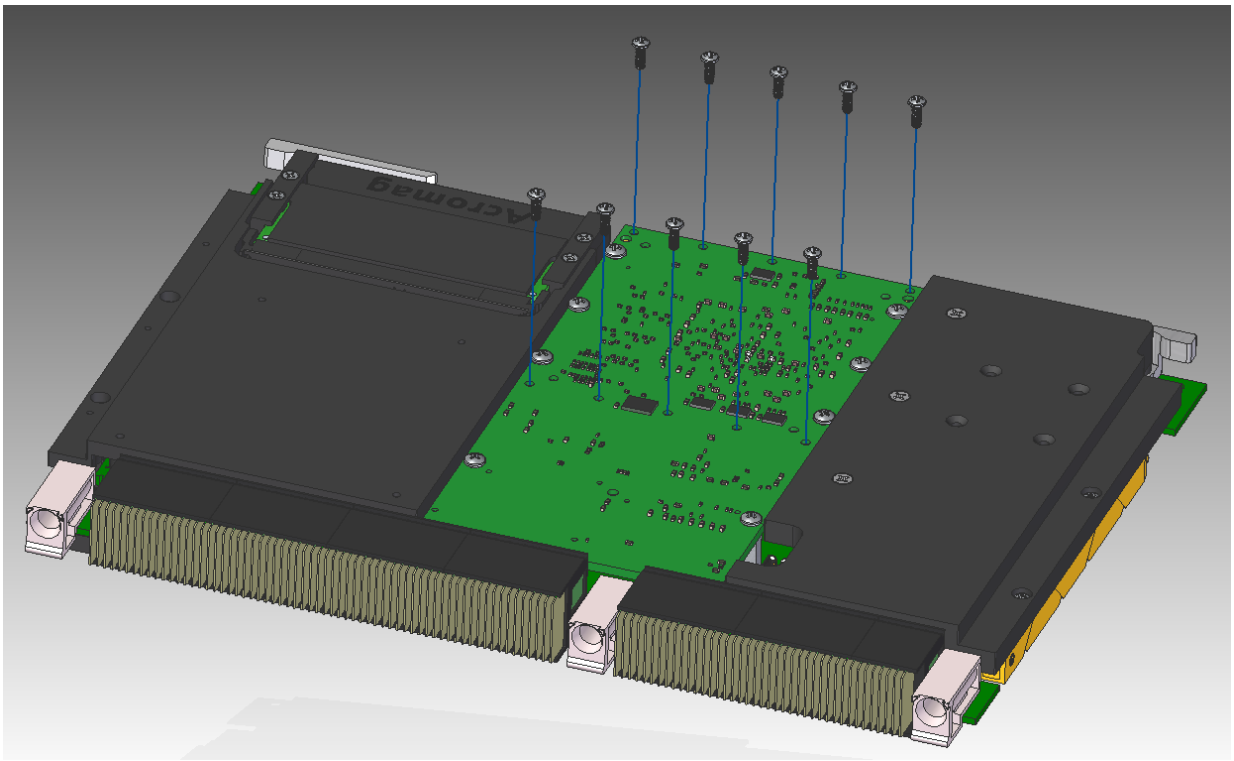
1. Align the XMC interface connectors with the mating connectors on the VPX6860 and carefully push downward until fully seated.



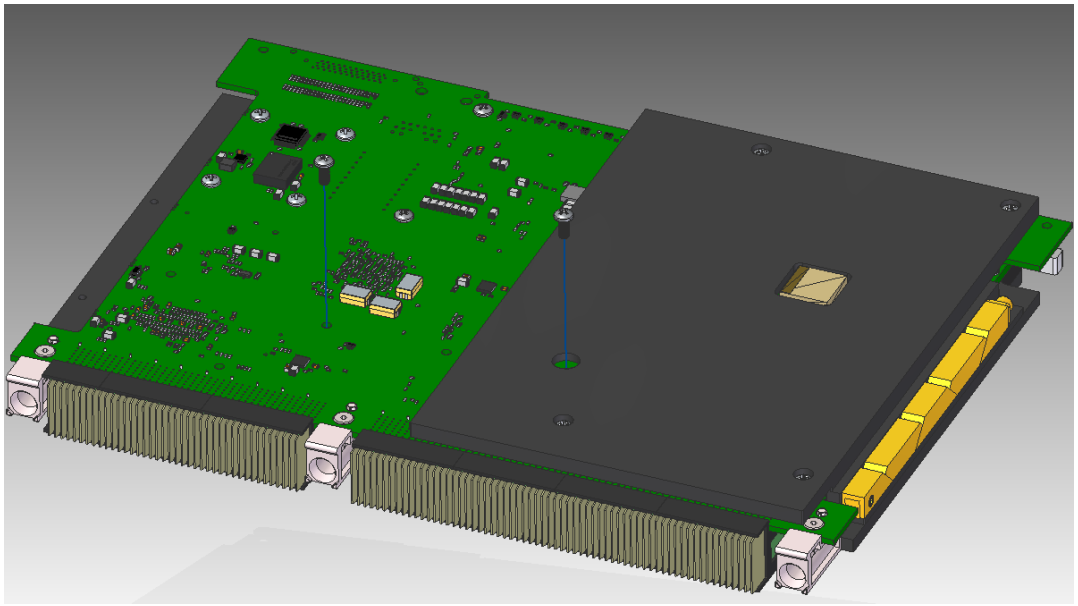
2. Install 6 screws (M2.5 x 6mm) to secure the XMC module to the XMC heatsink on the VPX6860.



3. Install 10 screws (M2 x 6mm) that secure the XMC module to the heatsink on the VPX6860.



4. Install the 2 screws (M2.5 x 6mm) on the bottom side of the VPX6860.



XMC module installation is complete.

6.7 Certificate of Volatility

Certificate of Volatility				
Acromag Model VPX6860-42-20 VPX6860-61-20 VPX6860-42-50 VPX6860-61-50	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) SDRAM	Size: 32GB	User Modifiable ■ Yes □ No	Function: Storage of code/data for CPU	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.) PCH internal CMOS SRAM	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Data storage for system/BIOS	Process to Sanitize: Set SW1-1 into the ON position momentarily.
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 16 Mbytes	User Modifiable ■ Yes □ No	Function: Storage of Code and Data for system/BIOS	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash
Type(EEPROM, Flash, etc.) EEPROM (CPU ID EERPROM)	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Storage of CPU model and serial	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type(EEPROM, Flash, etc.) EEPROM (VPX ID EERPROM)	Size: 2 kbytes	User Modifiable ■ Yes □ No	Function: Storage of VPX model and serial	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type(EEPROM, Flash, etc.) EEPROM (i350 EERPROM)	Size: 16 kbytes	User Modifiable ■ Yes □ No	Function: Storage of i350 firmware	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type(EEPROM, Flash, etc.) Flash (XL710 Flash)	Size: 16 Mbytes	User Modifiable ■ Yes □ No	Function: Storage of XL710 firmware	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash.
Type(EEPROM, Flash, etc.) EEPROM (PEX8750 EERPROM)	Size: 8 kbytes	User Modifiable ■ Yes □ No	Function: Storage of PEX8750 firmware	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Acromag Representative				
Name: Russ Nieves	Title: Director of Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

7.0 VPX6860-RTM Rear-Transition Accessory Module

The optional VPX6860-RTM module may be installed into the rear slot directly behind the VPX6860 to easily access all of the available I/O on P2 connector.

The following I/O is available on the front panel of the VPX6860-RTM:

- Two USB 2.0 ports via standard USB 2.0 connector.
- Two USB 3.0 ports via standard USB 3.0 connector.
- Two DisplayPort ports via standard Mini-DisplayPort connector.
- Two Gigabit Ethernet ports via standard RJ45 connectors (one of these is shared with the port on the front panel of the air-cooled VPX6860.

The following I/O is available via internal connectors on the VPX6860-RTM:

- Two SATA III ports via standard 7-pin SATA data connectors.
- Four software-selectable RS-232/RS-422/RS-485 Serial Ports are available via 10-pin headers.
- Stereo Audio Line-In & Line-Out via a 5-pin connector.
- Six General Purpose I/O pins via an 8-pin header.

7.1 Ordering Information

The VPX6860-RTM ordering options are given in the following table.

Model Number	***Description***	***Temp Range***
VPX6860-RTM-LF	*VPX6860 Rear Transition Module*	*-40°C to 85°C*

7.2 Connector Information

7.2.1 VPX Backplane Connectors

7.2.1.1 RP0 VPX Connector

RP0 Wafer	A	B	C	D	E	F	G
1	NC	NC	NC	NC	NC	NC	NC
2	NC	NC	NC	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	NC	NC	GND	NC	GND	NC	NC
5	NC	NC	GND	+3.3V AUX (REQUIRED)	GND	NC	NC
6	NC	NC	GND	NC	GND	NC	NC
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	NC	GND	NC	NC	GND	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	NC	GND	NC	NC	GND	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC	NC	GND	NC	NC	GND	NC
14	GND	NC	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	NC
16	GND	NC	NC	GND	NC	NC	GND

7.2.1.2 RP3 VPX Connector

RP3 Wafer	A	B	C	D	E	F	G
1	N/C	N/C	GND	N/C	N/C	GND	COM4_TX
2	GND	N/C	N/C	GND	N/C	N/C	GND
3	J16_SIO18_P	J16_SIO18_N	GND	N/C	N/C	GND	COM4_RTS#_485_TX-
4	GND	J16_SIO17_P	J16_SIO17_N	GND	J16_SIO16_P	J16_SIO16_N	GND
5	J16_SIO15_P	J16_SIO15_N	GND	J16_SIO14_P	J16_SIO14_N	GND	COM4_RX
6	GND	J16_SIO13_P	J16_SIO13_N	GND	J16_SIO12_P	J16_SIO12_N	GND
7	J16_SIO11_P	J16_SIO11_N	GND	J16_SIO10_P	J16_SIO10_N	GND	COM4_CTS#_485_RX-
8	GND	J16_SIO9_P	J16_SIO9_N	GND	J16_SIO8_P	J16_SIO8_N	GND
9	J16_SIO7_P	J16_SIO7_N	GND	J16_SIO6_P	J16_SIO6_N	GND	COM3_TX
10	GND	J16_SIO5_P	J16_SIO5_N	GND	J16_SIO4_P	J16_SIO4_N	GND
11	J16_SIO3_P	J16_SIO3_N	GND	J16_SIO2_P	J16_SIO2_N	GND	COM3_RTS#_485_TX-
12	GND	J16_SIO1_P	J16_SIO1_N	GND	J16_SIO0_P	J16_SIO0_N	GND
13	N/C	N/C	GND	N/C	N/C	GND	COM3_RX
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	COM3_CTS#_485_RX-
16	GND	N/C	N/C	GND	N/C	N/C	GND

7.2.1.3 RP4 VPX Connector

RP4 Wafer	A	B	C	D	E	F	G
1	J16_DP05_N	J16_DP05_P	GND	J16_DP04_N	J16_DP04_P	GND	ENET_TP1_LINK#
2	GND	J16_DP07_N	J16_DP07_P	GND	J16_DP06_N	J16_DP06_P	GND
3	J16_DP09_N	J16_DP09_P	GND	J16_DP08_N	J16_DP08_P	GND	ENET_TP2_LINK#
4	GND	J16_DP15_N	J16_DP15_P	GND	J16_DP14_N	J16_DP14_P	GND
5	J16_DP17_N	J16_DP17_P	GND	J16_DP16_N	J16_DP16_P	GND	ENET_UTP2_LINK#
6	GND	J16_DP19_N	J16_DP19_P	GND	J16_DP18_N	J16_DP18_P	GND
7	J16_DP01_N	J16_DP01_P	GND	J16_DP00_N	J16_DP00_P	GND	ENET_UTP1_LINK#
8	GND	J16_DP03_N	J16_DP03_P	GND	J16_DP02_N	J16_DP02_P	GND
9	J16_DP11_N	J16_DP11_P	GND	J16_DP10_N	J16_DP10_P	GND	N/C
10	GND	J16_DP13_N	J16_DP13_P	GND	J16_DP12_N	J16_DP12_P	GND
11	UTP_CP2_RX_P	UTP_CP2_RX_N	GND	UTP_CP2_TX_P	UTP_CP2_TX_N	GND	N/C
12	GND	UTP_CP1_RX_P	UTP_CP1_RX_N	GND	UTP_CP1_TX_P	UTP_CP1_TX_N	GND
13	TP_CP2_P0_P	TP_CP2_P0_N	GND	TP_CP2_P1_P	TP_CP2_P1_N	GND	GPIN3
14	GND	TP_CP2_P2_P	TP_CP2_P2_N	GND	TP_CP2_P3_P	TP_CP2_P3_N	GND
15	TP_CP1_P0_P	TP_CP1_P0_N	GND	TP_CP1_P1_P	TP_CP1_P1_N	GND	GPOUT3
16	GND	TP_CP1_P2_P	TP_CP1_P2_N	GND	TP_CP1_P3_P	TP_CP1_P3_N	GND

7.2.1.4 RP5 VPX Connector

RP4 Wafer	A	B	C	D	E	F	G
1	AP FIELD I/O 49	AP FIELD I/O 50	GND	AP FIELD I/O 47	AP FIELD I/O 48	GND	N/C
2	GND	AP FIELD I/O 45	AP FIELD I/O 46	GND	AP FIELD I/O 43	AP FIELD I/O 44	GND
3	AP FIELD I/O 41	AP FIELD I/O 42	GND	AP FIELD I/O 39	AP FIELD I/O 40	GND	N/C
4	GND	AP FIELD I/O 37	AP FIELD I/O 38	GND	AP FIELD I/O 35	AP FIELD I/O 36	GND
5	AP FIELD I/O 33	AP FIELD I/O 34	GND	AP FIELD I/O 31	AP FIELD I/O 32	GND	N/C
6	GND	AP FIELD I/O 29	AP FIELD I/O 30	GND	AP FIELD I/O 27	AP FIELD I/O 28	GND
7	AP FIELD I/O 25	AP FIELD I/O 26	GND	AP FIELD I/O 23	AP FIELD I/O 24	GND	N/C
8	GND	AP FIELD I/O 21	AP FIELD I/O 22	GND	AP FIELD I/O 19	AP FIELD I/O 20	GND
9	AP FIELD I/O 17	AP FIELD I/O 18	GND	AP FIELD I/O 15	AP FIELD I/O 16	GND	N/C
10	GND	AP FIELD I/O 13	AP FIELD I/O 14	GND	AP FIELD I/O 11	AP FIELD I/O 12	GND
11	AP FIELD I/O 9	AP FIELD I/O 10	GND	AP FIELD I/O 7	AP FIELD I/O 8	GND	N/C
12	GND	AP FIELD I/O 5	AP FIELD I/O 6	GND	AP FIELD I/O 3	AP FIELD I/O 4	GND
13	AP FIELD I/O 1	AP FIELD I/O 2	GND	N/C	N/C	GND	N/C
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	N/C
16	GND	N/C	N/C	GND	N/C	N/C	GND

7.2.1.5 RP6 VPX Connector

RP4 Wafer	A	B	C	D	E	F	G
1	USB6_P	USB6_N	GND	USB5_P	USB5_N	GND	GPIN0
2	GND	DPC_AUX_SEL	USB_5_6_OC#	GND	DPB_AUX_SEL	USB_1_2_OC#	GND
3	USB1_SSRX_P	USB1_SSRX_N	GND	USB1_P	USB1_N	GND	GPIN1
4	GND	USB2_P	USB2_N	GND	USB1_SSTX_P	USB1_SSTX_N	GND
5	USB2_SSTX_P	USB2_SSTX_N	GND	USB2_SSRX_P	USB2_SSRX_N	GND	GPIN2
6	GND	AGND_AUDIO	LINEOUT_L	GND	AGND_AUDIO	LINEIN_L	GND
7	LINEOUT_R	AGND_AUDIO	GND	LINEIN_R	AGND_AUDIO	GND	GPOUT0
8	GND	SATA2_RX_P	SATA2_RX_N	GND	SATA2_TX_P	SATA2_TX_N	GND
9	SATA3_RX_P	SATA3_RX_N	GND	SATA3_TX_P	SATA3_TX_N	GND	GPOUT1
10	GND	DPB_TX1_P	DPB_TX1_N	GND	DPB_TX0_P	DPB_TX0_N	GND
11	DPB_TX3_P	DPB_TX3_N	GND	DPB_TX2_P	DPB_TX2_N	GND	GPOUT2
12	GND	COM1_RTS#_485_TX-	COM1_TX	GND	DPB_CTRL_AUX_P	DPB_CTRL_AUX_N	GND
13	COM1_CTS#_485_RX-	COM1_RX	GND	COM2_RTS#_485_TX-	COM2_TX	GND	DPB_HPD
14	GND	DPC_TX1_P	DPC_TX1_N	GND	DPC_TX0_P	DPC_TX0_N	GND
15	DPC_TX3_P	DPC_TX3_N	GND	DPC_TX2_P	DPC_TX2_N	GND	DPC_HPD
16	GND	COM2_CTS#_485_RX-	COM2_RX	GND	DPC_CTRL_AUX_P	DPC_CTRL_AUX_N	GND

7.2.2 I/O Connectors

7.2.2.1 J14 Mini-DisplayPort Connector

This standard 20-pin Mini-DisplayPort connector (JAE Electronics – DP3R020SU32JQR400) brings DisplayPort B out to the front panel.

PIN	SIGNAL
1	GND
2	DPB_HPD
3	DPB_TX0_P
4	DPB_AUX_SEL
5	DPB_TX0_N
6	GND
7	GND
8	GND
9	DPB_TX1_P
10	DPB_TX3_P
11	DPB_TX1_N
12	DPB_TX3_N
13	GND
14	GND
15	DPB_TX2_P
16	DPB_CTRL_AUX_P
17	DPB_TX2_N
18	DPB_CTRL_AUX_N
19	GND
20	+3.3V

7.2.2.2 J4 Mini-DisplayPort Connector

This standard 20-pin Mini-DisplayPort connector (JAE Electronics – DP3R020SU32JQR400) brings DisplayPort C out to the front panel.

PIN	SIGNAL
1	GND
2	DPC_HPD
3	DPC_TX0_P
4	DPC_AUX_SEL
5	DPC_TX0_N
6	GND
7	GND
8	GND
9	DPC_TX1_P
10	DPC_TX3_P
11	DPC_TX1_N
12	DPC_TX3_N
13	GND
14	GND
15	DPC_TX2_P
16	DPC_CTRL_AUX_P
17	DPC_TX2_N
18	DPC_CTRL_AUX_N
19	GND
20	+3.3V

7.2.2.3 J5 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48404-003) brings USB Port 1 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB1_N
3	USB1_P
4	GND
5	USB1_SSRX_N
6	USB1_SSRX_P
7	GND
8	USB1_SSTX_N
9	USB1_SSTX_P

7.2.2.4 J6 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48404-003) brings USB Port 2 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB2_N
3	USB2_P
4	GND
5	USB2_SSRX_N
6	USB2_SSRX_P
7	GND
8	USB2_SSTX_N
9	USB2_SSTX_P

7.2.2.5 J9 SATA Connector

This standard 7-pin SATA connector (Molex – 67800-8005) brings SATA Port 2 out to an internal connector.

PIN	SIGNAL
1	GND
2	SATA2_TXP
3	SATA2_TX_N
4	GND
5	SATA2_RX_N
6	SATA2_RX_P
7	GND

7.2.2.6 J10 SATA Connector

This standard 7-pin SATA connector (Molex – 67800-8005) brings SATA Port 3 out to an internal connector.

PIN	SIGNAL
1	GND
2	SATA3_TXP
3	SATA3_TX_N
4	GND
5	SATA3_RX_N
6	SATA3_RX_P
7	GND

7.2.2.7 J11 USB 2.0 Connector

This standard 4-pin USB2.0 connector (Molex – 67329-8001) brings USB Port 3 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB3_N
3	USB3_P
4	GND

7.2.2.8 J12 USB 2.0 Connector

This standard 4-pin USB2.0 connector (Molex – 67329-8001) brings USB Port 4 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB4_N
3	USB4_P
4	GND

7.2.2.9 J7 Ethernet Connector

This standard 8-pin Ethernet connector (TE Connectivity – 2-406549-1) brings Ethernet Port 0 out to the front panel.

PIN	SIGNAL
1	ENET1_P0_P
2	ENET1_P0_N
3	ENET1_P1_P
4	ENET1_P2_P
5	ENET1_P2_N
6	ENET1_P1_N
7	ENET1_P3_P
8	ENET1_P3_N

7.2.2.10 J13 Ethernet Connector

This standard 8-pin Ethernet connector (TE Connectivity – 2-406549-1) brings Ethernet Port 0 out to the front panel.

PIN	SIGNAL
1	ENET0_P0_P
2	ENET0_P0_N
3	ENET0_P1_P
4	ENET0_P2_P
5	ENET0_P2_N
6	ENET0_P1_N
7	ENET0_P3_P
8	ENET0_P3_N

7.2.2.11 P1 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM1 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM1_RX-[1] COM1_CTS#[2]	2
3	COM1_RX	NC	4
5	COM1_TX	NC	6
7	COM1_TX-[1] COM1_RTS#[2]	NC	8
9	GND	GND	10

[1] RS-422/RS-485 mode
[2] RS-232 mode

7.2.2.12 P2 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM2 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM1_RX-[1] COM1_CTS#[2]	2
3	COM1_RX	NC	4
5	COM1_TX	NC	6
7	COM1_TX-[1] COM1_RTS#[2]	NC	8
9	GND	GND	10

[1] RS-422/RS-485 mode
[2] RS-232 mode

7.2.2.13 P5 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM3 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM3_RX-[1] COM3_CTS#[2]	2
3	COM3_RX	NC	4
5	COM3_TX	NC	6
7	COM3_TX-[1] COM3_RTS#[2]	NC	8
9	GND	GND	10

[1] RS-422/RS-485 mode

[2] RS-232 mode

7.2.2.14 P6 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM4 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM4_RX-[1] COM4_CTS#[2]	2
3	COM4_RX	NC	4
5	COM4_TX	NC	6
7	COM4_TX-[1] COM4_RTS#[2]	NC	8
9	GND	GND	10

[1] RS-422/RS-485 mode

[2] RS-232 mode

7.2.2.15 P3 GPIO Connector

This 8-pin 0.1" header (Samtec – TSM-104-01-L-DV) is used to access the general purpose I/O signals.

PIN	SIGNAL	SIGNAL	PIN
1	GPIN0	GPOUT0	2
3	GPIN1	GPOUT1	4
5	GPIN2	GPOUT2	6
7	GPIN3	GPOUT3	8

7.2.2.16 P4 Audio Connector

This 5-pin connector (Molex – 533980571) is used for the stereo audio line-in and line-out connections.

PIN	SIGNAL
1	LINEOUT_R
2	LINEOUT_L
3	AGND_AUDIO
4	LINEIN_R
5	LINEIN_L

7.2.2.17 J8 AcroPack Field I/O Connector

This 50-pin 0.8mm CHAMP connector (TE – 6658751-1) brings the AcroPack Field I/O connections from the conduction cooled VPX6860 to the RTM's panel.

PIN	SIGNAL	PIN	SIGNAL
1	FIELD I/O 1	26	FIELD I/O 2
2	FIELD I/O 3	27	FIELD I/O 4
3	FIELD I/O 5	28	FIELD I/O 6
4	FIELD I/O 7	29	FIELD I/O 8
5	FIELD I/O 9	30	FIELD I/O 10
6	FIELD I/O 11	31	FIELD I/O 12
7	FIELD I/O 13	32	FIELD I/O 14
8	FIELD I/O 15	33	FIELD I/O 16
9	FIELD I/O 17	34	FIELD I/O 18
10	FIELD I/O 19	35	FIELD I/O 20
11	FIELD I/O 21	36	FIELD I/O 22
12	FIELD I/O 23	37	FIELD I/O 24
13	FIELD I/O 25	38	FIELD I/O 26
14	FIELD I/O 27	39	FIELD I/O 28
15	FIELD I/O 29	40	FIELD I/O 30
16	FIELD I/O 31	41	FIELD I/O 32
17	FIELD I/O 33	42	FIELD I/O 34
18	FIELD I/O 35	43	FIELD I/O 36
19	FIELD I/O 37	44	FIELD I/O 38
20	FIELD I/O 39	45	FIELD I/O 40
21	FIELD I/O 41	46	FIELD I/O 42
22	FIELD I/O 43	47	FIELD I/O 44
23	FIELD I/O 45	48	FIELD I/O 46
24	FIELD I/O 47	49	FIELD I/O 48
25	FIELD I/O 49	50	FIELD I/O 50

7.2.2.18 P7 XMC Rear I/O Connector 1

This 40-pin Samtec QTH connector (Samtec – QTH-020-01-F-D-DP-A-K)) contains half the Rear I/O from the XMC module's P16 connector on the VPX6860.

PIN	SIGNAL	PIN	SIGNAL
1	J16_DP00_P	**2**	J16_DP10_P
3	J16_DP00_N	**4**	J16_DP10_N
5	J16_DP01_P	**6**	J16_DP11_P
7	J16_DP01_N	**8**	J16_DP11_N
9	J16_DP02_P	**10**	J16_DP12_P
11	J16_DP02_N	**12**	J16_DP12_N
13	J16_DP03_P	**14**	J16_DP13_P
15	J16_DP03_N	**16**	J16_DP13_N
17	J16_DP08_P	**18**	J16_DP09_P
19	J16_DP08_N	**20**	J16_DP09_N
21	J16_SIO0_P	**22**	J16_SIO1_P
23	J16_SIO0_N	**24**	J16_SIO1_N
25	J16_SIO2_P	**26**	J16_SIO3_P
27	J16_SIO2_N	**28**	J16_SIO3_N
29	J16_SIO4_P	**30**	J16_SIO5_P
31	J16_SIO4_N	**32**	J16_SIO5_N
33	J16_SIO6_P	**34**	J16_SIO7_P
35	J16_SIO6_N	**36**	J16_SIO7_N
37	J16_SIO8_P	**38**	J16_SIO9_P
39	J16_SIO8_N	**40**	J16_SIO9_N

7.2.2.19 P8 XMC Rear I/O Connector 1

This 40-pin Samtec QTH connector (Samtec – QTH-020-01-F-D-DP-A-K)) contains half the Rear I/O from the XMC module's P16 connector on the VPX6860.

PIN	SIGNAL	PIN	SIGNAL
1	J16_DP04_P	2	J16_DP14_P
3	J16_DP04_N	4	J16_DP14_N
5	J16_DP05_P	6	J16_DP15_P
7	J16_DP05_N	8	J16_DP15_N
9	J16_DP06_P	10	J16_DP16_P
11	J16_DP06_N	12	J16_DP16_N
13	J16_DP07_P	14	J16_DP17_P
15	J16_DP07_N	16	J16_DP17_N
17	J16_DP18_P	18	J16_DP19_P
19	J16_DP18_N	20	J16_DP19_N
21	J16_SIO10_P	22	J16_SIO11_P
23	J16_SIO10_N	24	J16_SIO11_N
25	J16_SIO12_P	26	J16_SIO13_P
27	J16_SIO12_N	28	J16_SIO13_N
29	J16_SIO14_P	30	J16_SIO15_P
31	J16_SIO14_N	32	J16_SIO15_N
33	J16_SIO16_P	34	J16_SIO18_P
35	J16_SIO16_N	36	J16_SIO18_N
37	J16_SIO17_P	38	NC
39	J16_SIO17_N	40	NC

7.3 Power Requirements

The VPX6860-RTM board requires +5V and +3.3V_AUX from the VPX backplane. The power consumed by the board itself is negligible, however USB devices connected to the RTM will contribute to the power draw.

7.4 Environmental Considerations

7.4.1 Operating Temperature

-40°C to 85°C[1]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required.

7.4.2 Relative Humidity

5% to 95% Non-condensing

7.4.3 Vibration and Shock Standards

Vibration, Random Operating: Designed to comply with VITA 47 Class V1. Shall withstand vibration from 5 to 100Hz. with Power Spectral Density (PSD) = 0.04g2/Hz, for 1 hour per axis. Testing shall be in accordance with MIL-STD-810, Method 514, Procedure 1

Shock, Operating: Designed to comply with VITA 47 Class OS1, 20g, 11ms half sine and terminal sawtooth shock pulses. 3 shock pulses in each direction along 3 axes (36 shocks, total). Testing shall be in accordance with MIL-STD-810, Method 516, Procedure 1.

7.4.4 EMC Directives

The VPX6860 is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.

Note: This is a Class A product

- **RoHS Directive 2011/65/EU – All Models**
  In compliance per EN 50581

7.5 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Table 7.5.a MTBF

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	TBD	TBD	TBD
40°C	TBD	TBD	TBD

[1] FIT is Failures in 10^9 hours.

7.6 Certificate of Volatility

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
VPX6860-RTM-LF</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
□ Yes ■ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
□ Yes ■ No</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)</td><td>Size:</td><td>User Modifiable
□Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:
.</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Director of Sales and Marketing</td><td>Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td colspan="2">Office Fax:
248-624-9234</td></tr>
</table>

Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
----------	Prelim	MDW/ARP	Preliminary release.
25 MAR 2019	A	MDW/MJO	Rev A Release
31 MAY 2019	B	JBO/ARP	Added new Batteryless products to the Ordering Information section.

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