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Series AP418 AcroPack

16-Channels Low-Side/High-Side Switching Module

USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module. It is not intended for a general, non-technical audience that is unfamiliar with I/O devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

1.2.1 Trademark, Trade Name and Copyright Information

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All rights reserved. Acromag and Xembedded are registered trademarks of Acromag Incorporated. All other trademarks, registered trademarks, trade names, and service marks are the property of their respective owners.

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

The AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an additional 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

The AP418 is a 16-channel combination digital input/output board. This model supports both 0 to 60V DC inputs, and 60VDC low-side or high-side switch outputs, in any combination up to 16 channels. As a combination input/output module, input channels on this model can be used for "loopback" monitoring of the output channel states. Up to 16 input channels can be programmed to generate Change-Of-State (COS), Low, or High level transition interrupts. The AP418 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitor applications that require high-density, high-reliability, and high-performance at a low cost.

1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Model Number	***Description***	***Temp Range***
AP418E-LF [1]	*16-Channel Digital I/O*	*-40°C to 85°C*

Note 1: *Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 with a minimum airflow of 400LFM. For temperature below 70°C the module will require a minimum airflow of 200LFM.*

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix B for installation instructions)

1.3.2 Key Features

- **High-Side and Low-Side Switch** – A P-channel MOSFET and N-channel MOSFET are used for each of the 16 channels allowing for true high and low side switching at up to 60V.
- **High Channel Count** - Interfaces with up to 16 input/output points. Input and output channels may be intermixed in any combination.
- **TTL-Compatible Input Threshold** - Input threshold is at TTL levels and includes hysteresis.
- **Input Hysteresis** - Buffered inputs include hysteresis for increased noise immunity.
- **Programmable Change-of-State/Level Interrupts -** Interrupts are software programmable for any bit Change-Of-State or level on up to 16 channels.
- **Loopback Output Control & Fault Diagnostics** - Input and output circuitry is connected in tandem to each I/O channel, making it directly compatible for "loopback monitoring" of the output channel states. This feature can also be used to implement self-test or fault diagnosis, since inherent loopback can be used to detect open output switches or shorts.
- **High Voltage Inputs & Outputs** - Inputs and outputs are rated to 60VDC. I/O channels are non-isolated and share a common connection.
- **High Impedance Inputs** - High impedance inputs minimize loading of the input source and input current.
- **Power Up & System Reset is Failsafe** - For safety, the outputs are always OFF upon power-up and cleared after a system reset. Unlike some competitive units, output gate resistors are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the AP module.
- **Positive True Logic** - Outputs operate using Positive True-Logic (1=ON/SWITCH CLOSED, 0=OFF/SWITCH OPEN).
- **Low R_{dsON} (200 mΩ Maximum)** - Low output drain-to-source ON resistance ensures TTL logic-low compatibility at high currents and reduces power dissipation.
- **High Output Current** - individual output channels may sink up to 2A DC continuous (up to 5A total, all channels combined), or 312mA DC (with all 16 channels ON). No deration of maximum output current is required at elevated ambient temperatures.

- **Module Health Monitoring** – On-board supply voltages and FPGA junction temperature can be monitored for out-of-tolerance conditions via XADC registers.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a 50 pin front panel connector.

The cables and termination panels are also available. For optimum performance with the AP418 digital I/O module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

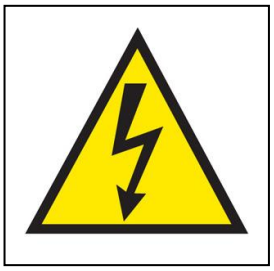
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 http://www.pcisig.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the PCIe bus and AcroPack module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Pin assignments are unique to each AP model. Table 2.1 lists signal pin assignments for the module field I/O connector. Pins are left unconnected in order to meet the minimum creepage distance required for 60 Volt isolation.

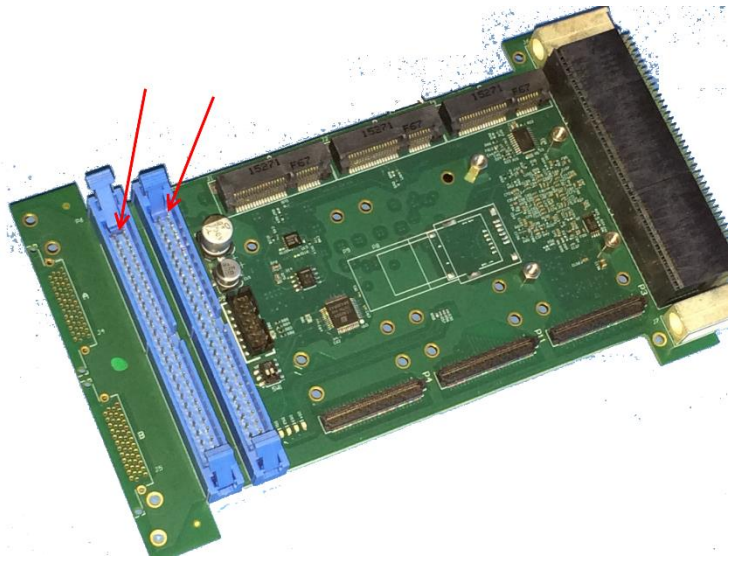
Table 2.1 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	Field I/O 0
35	26	2	1	Field I/O 0
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	Field I/O 1
36	27	4	5	Field I/O 1
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	GND
37	28	6	9	GND
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	Field I/O 2
38	29	8	13	Field I/O 2
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	Field I/O 3
39	30	10	17	Field I/O 3
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	Field I/O 4
40	31	12	21	Field I/O 4
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	Field I/O 5
41	32	14	25	Field I/O 5
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	GND
42	33	16	29	GND
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	Field I/O 6
43	34	18	33	Field I/O 6
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	Field I/O 7
44	35	20	37	Field I/O 7
			40	Reserved/isolation
			39	Reserved/isolation
11	11	21	42	Field I/O 8

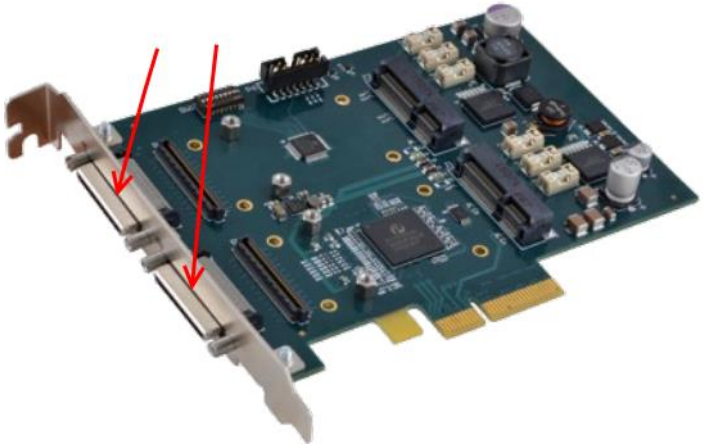
68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
45	36	22	41	Field I/O 8
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	Field I/O 9
46	37	24	45	Field I/O 9
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	GND
47	38	26	49	GND
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	Field I/O 10
48	39	28	53	Field I/O 10
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	Field I/O 11
49	40	30	57	Field I/O 11
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Field I/O 12
50	41	32	61	Field I/O 12
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	Field I/O 13
51	42	34	65	Field I/O 13
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	GND
52	43	36	69	GND
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	Field I/O 14
53	44	38	73	Field I/O 14
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Field I/O 15
54	45	40	77	Field I/O 15
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	External Excitation
55	46	42	81	External Excitation
			84	Reserved/isolation

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			83	Reserved/isolation
22	22	43	86	External Excitation
56	47	44	85	External Excitation
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	GND
57	48	46	89	External Excitation
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	External Excitation
58	49	48	93	External Excitation
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	External Excitation
59	50	50	97	GND
			100	Reserved/isolation
			99	Reserved/isolation

Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector. See image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the Champ connector. See image of carrier.



2.5 Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules, according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The 'Present' signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter controls are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.2 Logic Interface Connections

Pin #	Name	Pin #	Name
51	+5V[1,2]	52	+3.3V[3]
49	+12V[1,2]	50	GND
47	-12V[1,2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	N.C. (+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: Signals are not applicable for the AP418 implementation. Pins are either "no connects" on the module or are repurposed for JTAG.

Note 2: +5V, +12V, and -12V power supplies have been assigned to pins that are reserved in the mini-PCIe specification.

Note 3: All +3.3Vaux power pins are changed to +3.3V power.

Note 4: The 'Present' signal is tied to circuit common on the AP module.

Note 5: The SM Bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP418 module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AP418 module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access an AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request assigned to the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers which must be read to determine the base address assigned to the board and the Interrupt Register which must be read to determine the interrupt request that goes active on a board interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7027 AP418		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x7027 AP418		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

Table 3.2 BAR0 Registers

Note that any registers/bits not mentioned will remain at the default value logic low.

BAR0 Base Address	Bit(s)	Description
0x0000 0000	31:0	Interrupt Enable Status Register
0x0000 0004	31:0	Module Location in System Register
0x0000 0008	31:0	Digital Input Register
0x0000 000C	31:0	Output Configuration Register
0x0000 0010	31:0	Digital Output Register
0x0000 0014	31:0	Not Used
0x0000 0018	31:0	Interrupt Enable Register
0x0000 001C	31:0	Interrupt Type Configuration Register
0x0000 0020	31:0	Interrupt Polarity Register
0x0000 0024	31:0	Interrupt Status Register
0x0000 0028→0x00000044	31:0	Not Used
0x0000 0048	31:0	XADC Status/Control Register
0x0000 004C	31:0	XADC Address Register
0x0000 0200	31:0	Firmware Revision Register
0x0000 0204	7:0	Flash Data
0x0000 0208	Bit-0	Flash Chip Select
0x0000 0050→0x000007FF	31:0	Not Used

Interrupt Enable Status Register (Read/Write) - (BAR0 + 0x0000 0000)

This read/write register is used to: enable board interrupt, and determine the pending status of interrupts.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Bit-8 of this register when set will issue a software reset to the AP module.

Table 3.3 Interrupt Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
0	Board Interrupt Enable Bit. This bit must be set to logic "1" to enable generation of interrupts from the AP module. Setting this bit to logic "0" will disable board interrupts. (Read/Write Bit)	
	0	Disabled
	1	Enabled
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt
	1	Interrupt Pending
7 to 2	Not Used	
8	Software Reset Writing logic "1" to this bit will cause a reset of AP module. Bit-0 of this register will not be affected.	
	0	No Reset
	1	Reset
31 to 9	Not Used	

Module Location in System Register (Read Only) - (BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.4 Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or a carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

Digital Input Register (Read Only) - (BAR0 + 0x0000 0008)

When the Digital Input Data Register is read, the value read corresponds to the actual state of the input channels at the time of the read. A "0" bit means that the corresponding input signal is below the threshold value. A "1" bit means that the corresponding input signal is at or above the threshold value.

If the channel's tandem output MOSFET is being controlled and its drain is loaded, then reading the digital input channel data register will return the state of the output (it is directly connected to the drain). This is an efficient method of accomplishing "loopback" control of the output.

When a channel's output is configured for low-side switching, a read of the input channel register will be the inverse of a read of the output channel register for a loaded output channel. That is, writing a '1' to an output turns the switch ON (gate signal high). In turn, this drives the drain low (N-channel MOSFET is conducting).

When a channel's output is configured for high-side switching, a read of the input channel register will mirror a read of the output channel register for a loaded output channel. That is, writing a '1' to an output turns the switch ON (gate signal high). In turn, this drives the drain high to the excitation voltage connected to the source (P-channel MOSFET is conducting).

Sixteen possible input channels numbered 0 through 15 may be read. Channel read operations use 8-bit or 16-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below).

It is recommended that unused inputs not be left floating, but pulled low by configuring the corresponding tandem output for low-side switching and turning it ON (see Output Configuration Register and Digital Output Register).

Table 3.5 Digital Input

Note that any registers/bits not mentioned will remain at the default value logic low.

Register Bit	Channel
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16 to 31	Not Used

Output Configuration Register (Read/Write) - (BAR0 + 0x0000 000C)

Each output channel can be configured to be a high-side switch or a low-side switch. Writing a "0" bit means that the corresponding output channel is configured as a low-side switch. Writing a "1" bit means that the corresponding output channel is configured as a high-side switch. The default configuration for all channels is low-side switching.

For high-side switching, an excitation voltage source must be applied either externally or internally. The default voltage source configuration requires an externally supplied excitation source. A +12V internal excitation is available with a zero-ohm resistor change. Please consult the factory if an internal excitation voltage source is required.

Read/Write Control for 16 output channels numbered 0 through 15 is provided. Channel configuration state Read/Write operations use 8-bit or 16-bit transfers with the lowest ordered bits corresponding to the lower-numbered channels for the register of interest (see below).

Note that any registers/bits not mentioned will remain at the default value logic low.

Table 3.6 Output Configuration Register

Register Bit	Channel
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16 to 31	Not Used

Digital Output Register (Read/Write) - (BAR0 + 0x0000 0010)

When the Digital Output Channel Data Register is written to, the value written is represented at the corresponding output channels. Before writing to the Digital Output Register, the channel's Output Configuration Register bit must be properly configured. The default configuration is for low-side switching.

Writing a logic low "0" bit sets the corresponding output switch to OPEN (OFF). Writing a logic high "1" CLOSES the corresponding output switch (turns it ON). There are two ways to accomplish an output read. Reading the digital output channel register returns the state configuration of this register (which is equivalent to the output MOSFET gate signal). Since input channels operate in tandem with the output channels, reading the digital input channel register will return the actual state of the output (it returns the level of the output MOSFET drain). That is, writing a "1" to an output turns the switch ON (gate signal high). When configured for low-side switching, this drives the drain low meaning that a read of the input channel register will be the inverse of a read of the output channel register for a loaded output. When configured for high-side switching, this drives the drain high meaning that a read of the input channel register will be the same as a read of the output channel register for a loaded output.

Read/Write Control for 16 output channels numbered 0 through 15 is provided. Channel state Read/Write operations use 8-bit or 16-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below).

Note that any registers/bits not mentioned will remain at the default value logic low.

Table 3.7 Digital Output Register

Register Bit	Channel
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16 to 31	Not Used

All outputs are OFF (switch OPEN) following a power-on reset, and are immediately cleared following a system reset. It is recommended that unused outputs be turned on so that the corresponding unused inputs are pulled low, rather than floating.

Interrupt Enable Register (Read/Write) - (BAR0 + 0x0000 0018)

The digital input channel Interrupt Enable Registers provide a mask bit for each of the 16 possible interrupt channels. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding input channel to generate an interrupt.

The Interrupt Polarity register is used to control differential channels 0 through 15 as mapped in the Interrupt Enable Register. For example, channel 0 is controlled via data bit-0.

All bits are set to "0" following a reset which means that all interrupts will be disabled.

Interrupt Type (COS or H/L) Configuration Register (Read/Write) - (BAR0 + 0x0000 001C)

The Interrupt Type Configuration Register determines the type of input channel transition that will generate an interrupt for each of the sixteen possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the output channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register is used to control channels 0 through 15 as mapped in the Interrupt Enable Register. For example, channel 0 is controlled via data bit-0.

All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the Interrupt Polarity Register.

Channel interrupt type read or write operations use 8-bit, 16-bit, or 32-bit data transfers. Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register.

Interrupt Polarity Register (Read/Write) - (BAR0 + 0x0000 0020)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the input channel data register). A "1" bit means

that an interrupt will occur when the input channel is high (i.e. a "1" in the input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register is used to control monitoring of digital input channels 0 through 15 as mapped in the Interrupt Enable Register. For example, channel 0 is controlled via data bit-0.

All bits are set to "0" following a reset, which means that the input will cause interrupts when they are logic low (provided they are enabled for interrupt on level).

Interrupt Status Register (Read/Write) - (BAR0 + 0x0000 0024)

The Interrupt Status Register reflects the status of the 16 possible interrupt channels. A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register).

Note that the input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel, this could happen if multiple changes occur before the channel's interrupt is serviced.

All interrupts are cleared following a reset.

XADC Status/Control Register (Read/Write) - (BAR0 + 0x0000 0048)

This read/write register will access the XADC register at the address set in the XADC Address Register allowing the module's key supply voltages and FPGA junction temperature to be monitored.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x4CH. Next, this register at BAR0 plus 0x48H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only) - (BAR0 + 0x0000 004C)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x48H.

Table 3.8 System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 3.9 FPGA Voltage and Temperature Range

	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Recommended Operating Temperature Range	-40C	50-60C	100C[1]

Note 1: Absolute maximum junction temperature is 125°C

Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Figure 1, in Appendix A, as you review this material.

4.1 Logic/Power Interface

The PCIe bus interface logic is embedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe target interface uses a single 4K base address register.

A FPGA device provides the control signals required to operate the board. It decodes the selected addresses and control signals. It also returns the acknowledgement messages required by the carrier/CPU board per the PCIe specification. The program for the FGPA is stored in separate Flash memory and loaded upon power-up.

4.2 Output Ports

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field I/O points are NONISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connector pin assignments). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Figures 2, 3, and 4 in Appendix A for example I/O and grounding connections.

A Field Programmable Gate Array (FPGA) is used to generate all the logic necessary to operate the board. With respect to input acquisition, all 16 input channels support interrupts and drive the FPGA through buffers. The field input signals are tied to the inputs of these buffers via a 100kΩ series resistor which limits the input current (but raises the tandem output's off-state drain current). Additionally, the buffer inputs are clamped to +3.3V to provide overvoltage protection for the FPGA. The input signal threshold is TTL compatible. The typical threshold is 1.5V DC with 200mV of hysteresis.

For output control, 16 open-drain outputs are connected in tandem with the 16 input buffers to each I/O channel. The outputs can be configured for either low-side switching or high-side switching. When configured for low-side switching, the drain is connected to the output, the gate is driven by the FPGA, and the source is connected to a common ground. When configured for high-side switching, the drain is connected to the output, the gate is driven by the FPGA, and the source is connected to an excitation voltage source, either internal (+12V) or external.

Writing a '1' to the output will turn the switch ON (closed-circuit), a '0' will turn it OFF (open-circuit). Since the input buffers are connected in tandem

with the output MOSFETs, efficient loopback monitoring of the output state can be accomplished by reading the input channel registers.

With respect to output control, the 100KΩ input buffer resistors in combination with +3.3V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output MOSFET drain circuitry are connected in tandem to the same I/O pin. If this presents a problem for your application, then you should consider separating the inputs and outputs by using other boards like the Acromag AP440 32-channel input board and the AP445 32-channel output board.

Output operation is considered 'fail-safe'. That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions. Further, output gate pulldowns are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the AP module.

The output MOSFETs employed are rated for a much higher current than specified. However, the field connector and cabling used are only rated to 1A per pin (each channel has 2 pins limiting each to 2A). For compatibility with other AP models, 10 pins have been reserved for ground. The low Rds-ON of the output MOSFETs will ensure TTL level compatible logic-low output signals even at high (2A) output currents.

The output MOSFETs include an integrated zener diode between the drain and the source. This provides output voltage clamp protection to 60V. The tandem input channel is also rated to 60V. However, when driving inductive loads such as relay coils, you should always place a shunt diode across the load to shunt the reverse EMF that develops across the coil when the current through it is turned off (see Figures 2 and 3 in Appendix A for an example of this type of protection).

Since the input buffer and output MOSFET circuitry share an I/O pin, inputs and outputs may be intermixed in any combination. Further, by providing an input channel for each output, efficient loopback monitoring of the output state can be easily accomplished (see Figure 4 in Appendix A).

Digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions for all input channels.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.2624 oz (7.5 g)

6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
• 3.3 VDC +/- 5%	400 mA Typical, 600 mA maximum
• 1.5 VDC +/- 5%	Not Used
• 5.0 VDC +/- 5%	Not Used
• +12 VDC +/- 5%	20 mA Typical, 50 mA maximum
• -12 VDC +/- 5%	Not Used

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	***Description***	***Temp Range***
AP418E-LF	*16-Channel Digital I/O*	*-40°C to 85°C*[1]

Note 1: *Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 with a minimum airflow of 400LFM. For temperature below 70°C the module will require a minimum airflow of 200LFM.*

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix B for installation instructions)

6.3.2 Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

6.3.3 Isolation

The PCIe bus and field commons are non-isolated and have a direct electrical connection.

6.3.4 Vibration and Shock Standards

The AcroPack is designed to comply with the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.3.5 EMC Directives

The AcroPack is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,075,287	122.7	930.0
40°C	678,771	77.5	1,473.3

[1] FIT is Failures in 10^9 hours.

6.5 Digital Inputs

Input Channel Configuration	16 non-inverting buffered inputs with a common connection. For DC voltage applications only, observe proper polarity.
Input Signal Voltage Range	0 to +60V DC, Maximum
Input Signal Threshold	TTL compatible. 1.5V DC with 200mV of hysteresis, typical.
Input Resistance	100 kΩ, typical.
Input Hysteresis	200mV DC centered at a 1.5V DC threshold, typical.
Input Current	560 µA, typical at 60VDC

6.6 Digital Outputs – Low-Side Switching

Output Channel Configuration	16 open-drain MOSFETs with common source connection. For DC voltage applications only, observe proper polarity.
Output "OFF" Voltage Range	0 to +60V DC, Maximum
Output "OFF" Leakage Current	1 µA Maximum (MOSFET only, 25°C, 60VDC). 500 µA Maximum (MOSFET only, 150°C, 60VDC) Does not include tandem input bias current.
Output "ON" Current Range	0 to +2A DC, continuous (up to 5A total for all channels combined) 312mA DC, continuous (all channels ON) No deration required at elevated temperature.
Output R_{DS} ON Resistance	60mΩ, Maximum (25°C) 110mΩ, Maximum (150°C)

6.7 Digital Outputs – High-Side Switching

Output Channel Configuration	16 open-drain MOSFETs with source connection to excitation voltage. For DC voltage applications only, observe proper polarity.
Output "OFF" Voltage Range	0 to +60V DC, Maximum
Output "OFF" Leakage Current	1 µA Maximum (MOSFET only, 25°C, 60VDC). 500 µA Maximum (MOSFET only, 150°C, 60VDC). Does not include tandem input bias current.
Output "ON" Current Range	0 to +2A DC, continuous (up to 5A total for all channels combined) 312mA DC, continuous (all channels ON)

	No deration required at elevated temperature.
Output R_{DS} ON Resistance	105mΩ, Maximum (25°C) 200mΩ, Maximum (150°C)
Turn – ON Time	125 ns, Typical
Turn – OFF Time	25ns, Typical

6.8 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) available through PCIe connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register (BAR)

Table 6.8 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\ Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

Appendix A

AP418 Functional Block Diagram

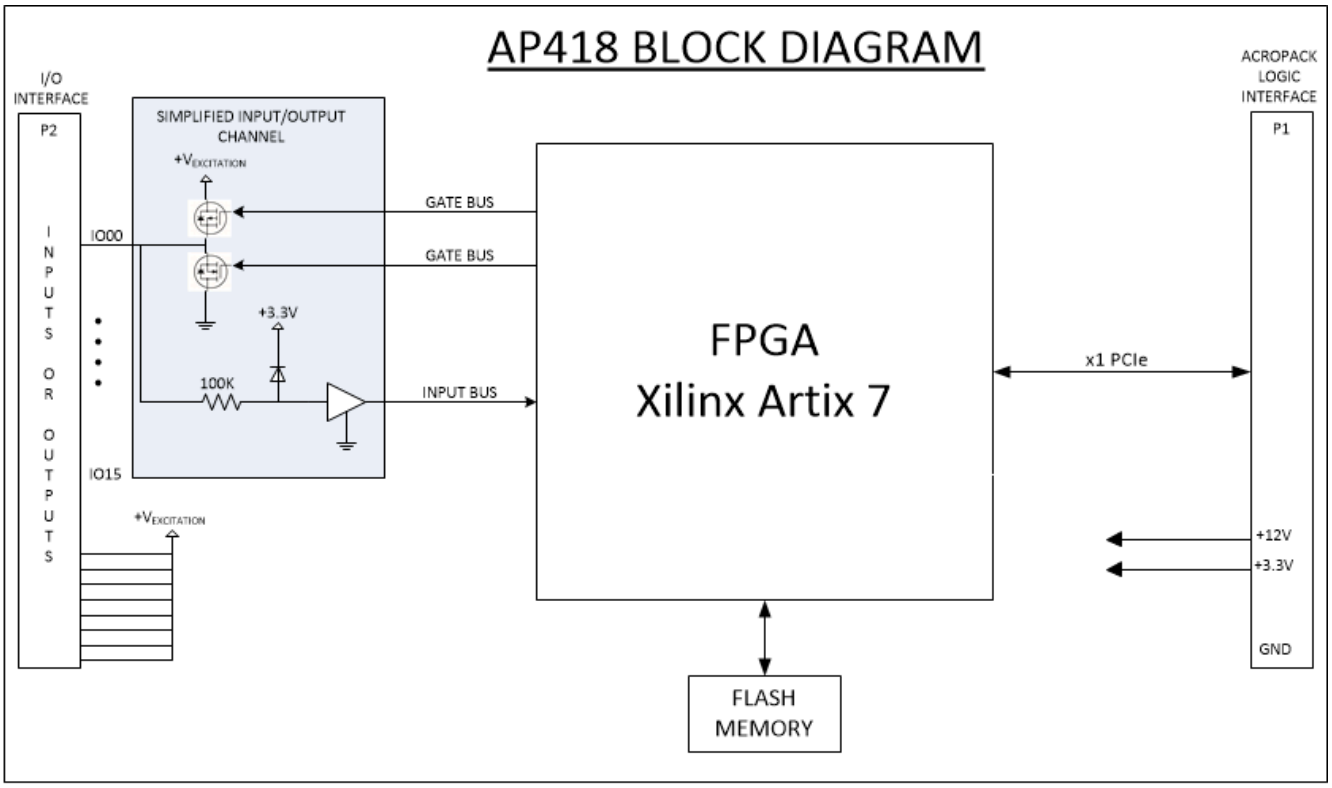


Figure 1: AP418 Block Diagram

AP418 Example Sourcing Output Connections (High-Side Switch)

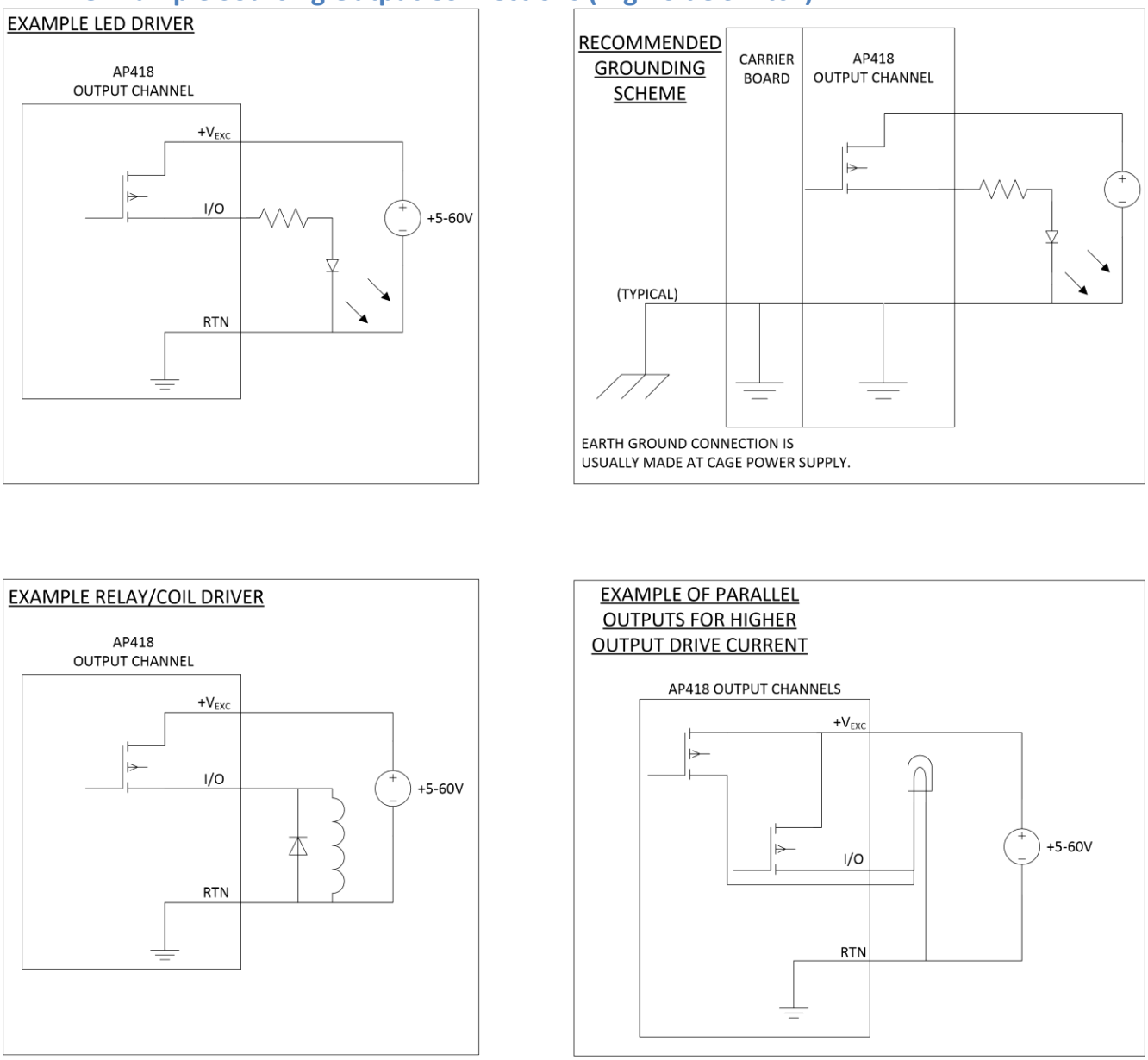


Figure 2: AP418 Example Sourcing Output Connections

AP418 Example Sinking Output Connections (Low-Side Switch)

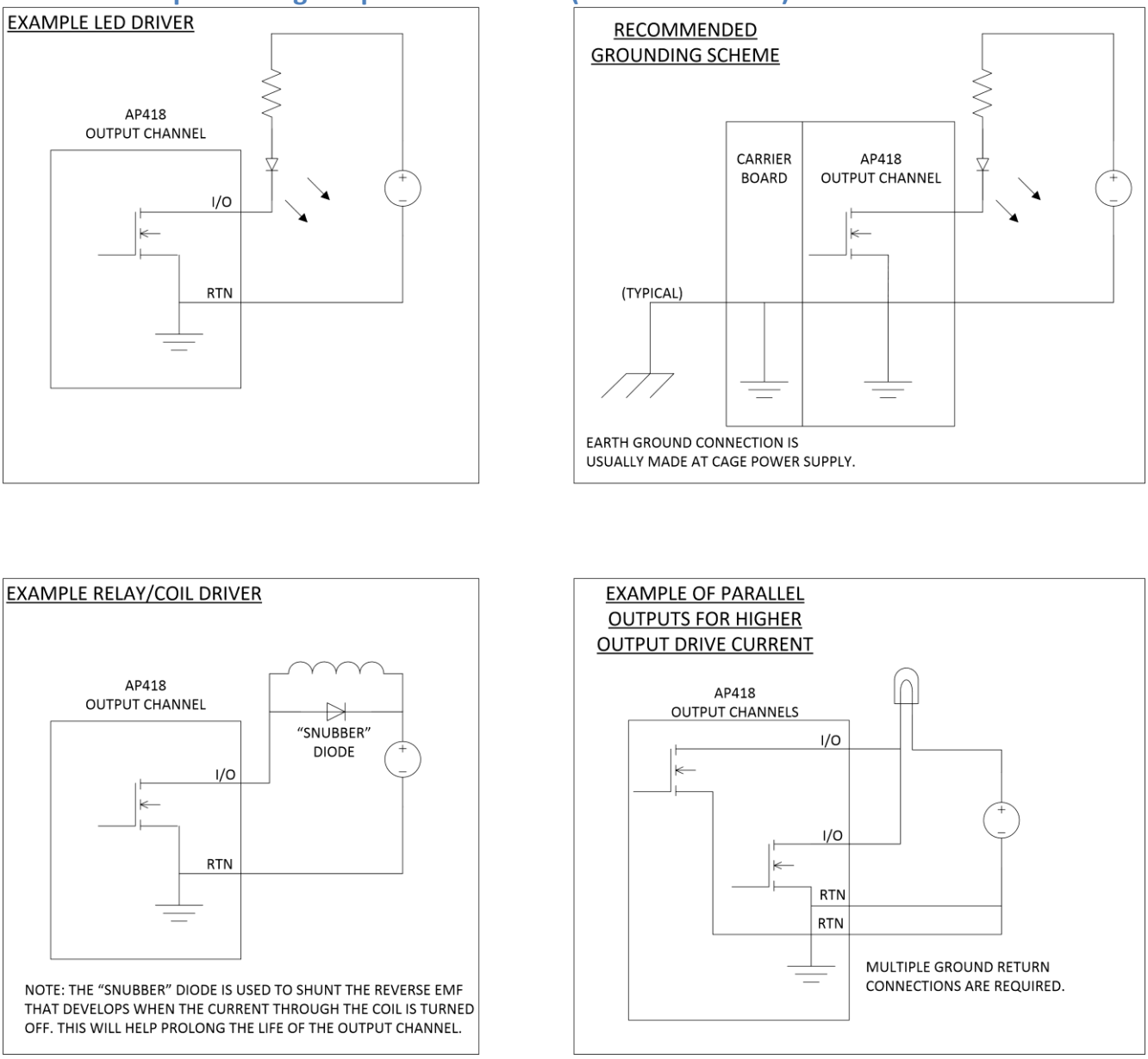


Figure 3: AP418 Example Sinking Output Connections

AP418 Example Input Connections

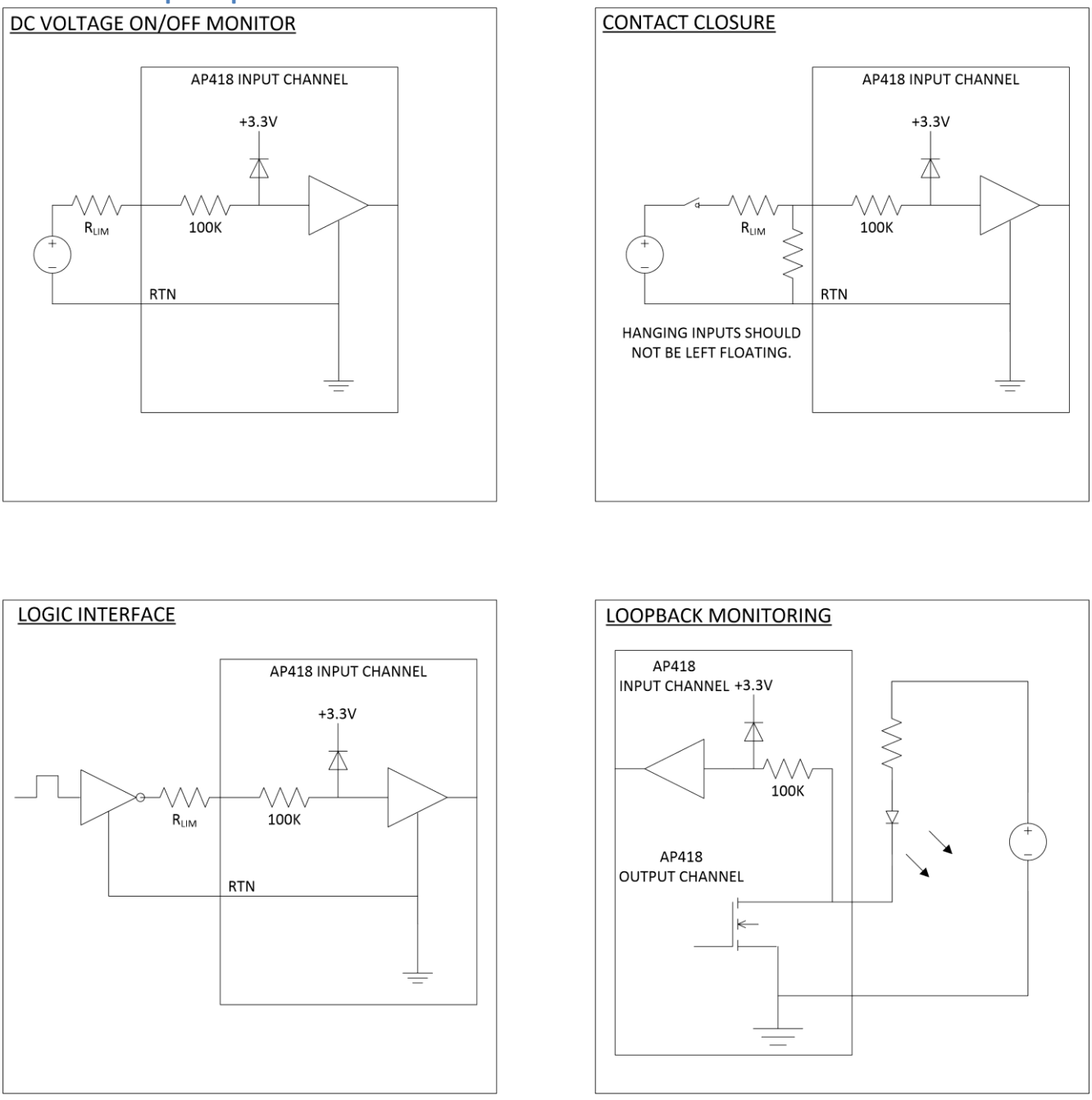
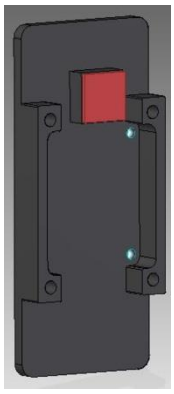


Figure 4: AP418 Example Input Connections

Appendix B

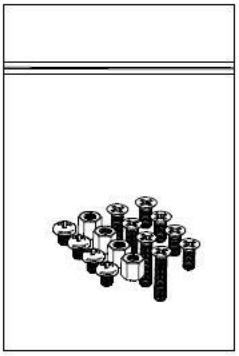
AP-CC-01 Heatsink Kit Installation



Bottom view



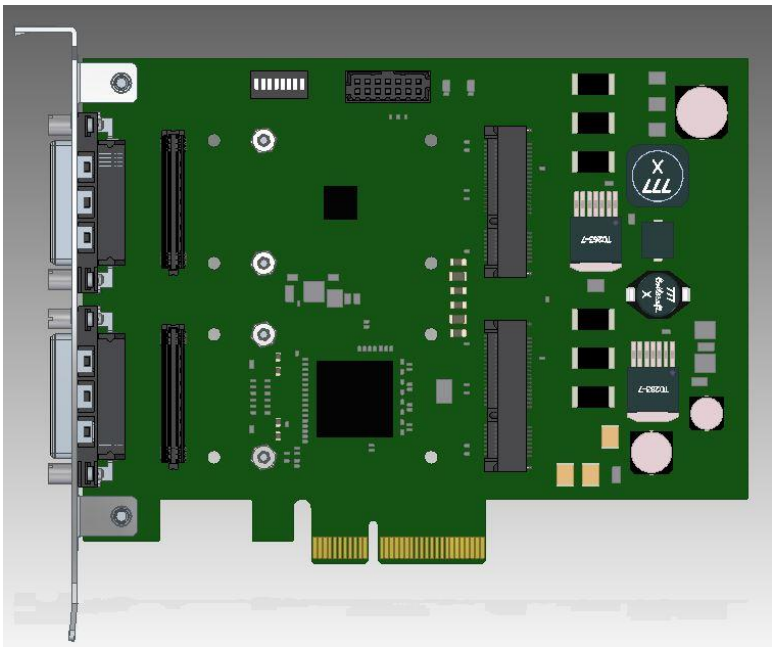
Top view



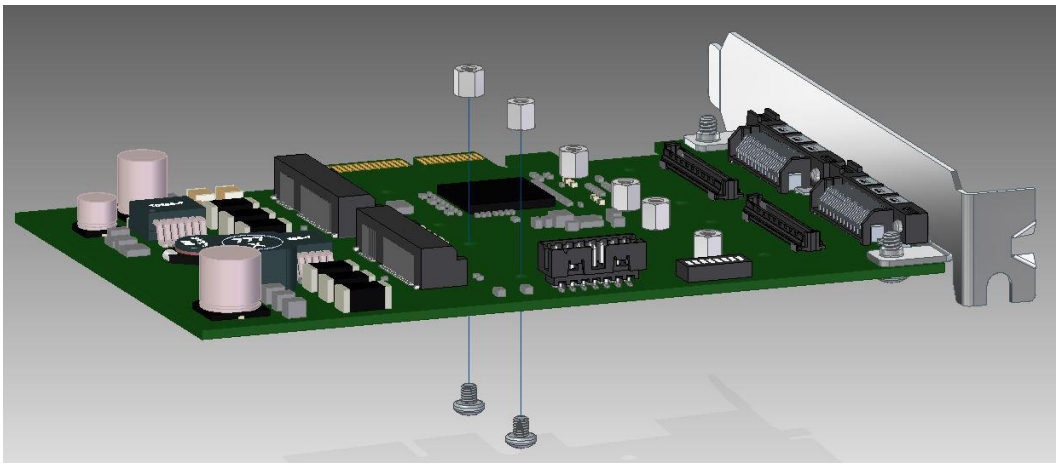
Hardware

AP-CC-01 Heat Sink Kit

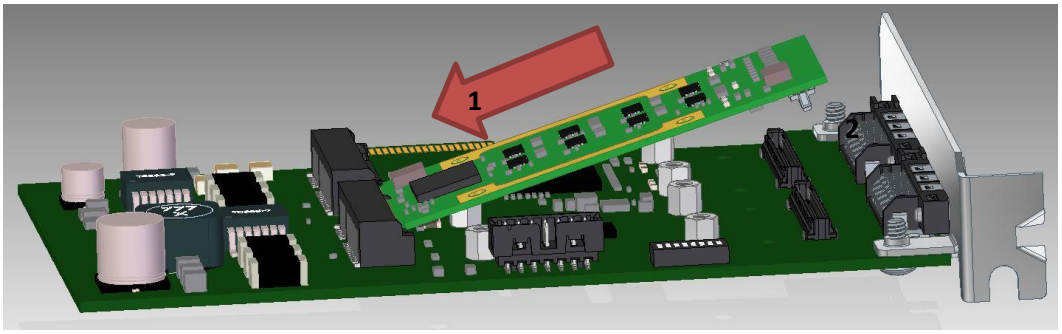
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



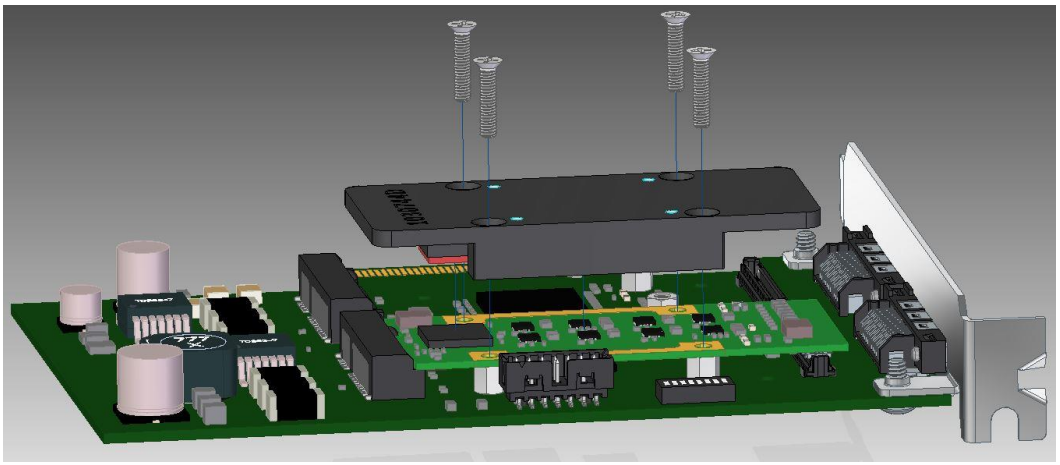
1. Install two standoffs and secure with two screws.



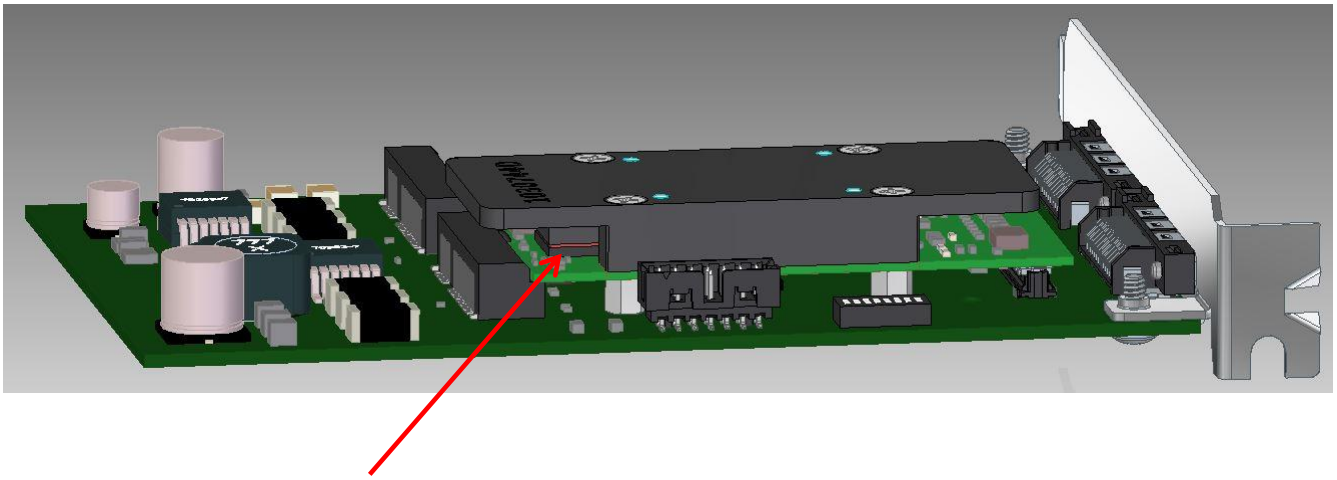
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Certificate of Volatility

Acromag Model AP418E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks and Block RAM Blocks	Size:16,640 Logic Cells and 900 Kb Block RAM	User Modifiable ■ Yes □ No	Function: FPGA logic blocks and RAM blocks.	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 32Mb	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Erase using JTAG
Type(EEPROM, Flash, etc.) One Time Programmable area in flash device	Size: 3 x 256-byte	User Modifiable □ Yes ■ No	Function: The OTP area has been disabled by writing the lock bits with logic 1.	Process to Sanitize: Not applicable

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Revision History

The revision history for this document is summarized in the table below.

Release Date	Version	EGR/DOC	Description of Revision
27 FEB 2017	Preliminary	MDW/ARP	Preliminary Document Publication
16 MAR 2017	A	MDW/ARP	Rev A Release
28 NOV 2017	B	MDW/ARP	Add turn-on/turn-off timing specifications.
16 JAN 2018	C	LMP/ARP	Add Table 6.8 PCIe Bus Data Rates.
27 JAN 2018	D	LMP/ARP	Added Reliability Prediction MTBF Table Data.

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