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Series AP445 AcroPack
32-Channel Isolated Digital Output Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road

Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310
Fax: (248) 624-9234

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This user's manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module. It is not intended for a general, non-technical audience that is unfamiliar with I/O devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

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1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

The AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an added 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

The AP445 module is a bus isolated 32-channel output module. It provides control for 32 solid state relays which are bipolar (may be used to switch positive or negative voltages). The AP445 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance interface at a low cost.

1.3.1 Ordering Information

The AP445 AcroPack module is available in one model as described in the following table.

Model Number	*Description*
AP445E-LF[1]	32 channel, isolated output module

Note 1: Operating temperature range for models:*-40*°C *to 85*°C

AP-CC-01
AcroPack Heatsink Conduction Cool Kit

See Appendix A for installation instructions.

1.3.2 Key Features

- **High Channel Count** – Individual control of up to 32 (SPST-NO) bipolar Solid State Relays (SSR's) is provided.
- **Isolated Field I/O** – Individual bipolar SSR's provide isolation. There are four groups (ports) of 8 channels, each which include separate port commons to ensure port-to-port isolation. Individual ports are isolated from each other and from the control logic.
- **Low-Side or High-Side Switch Configuration** – Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching applications.
- **TTL Compatible** – When configured as a low side switch will sink 32mA at 0.2 volts. Sourcing can be controlled by on-board surface mount or external pull-up resistors. On-board surface mount resistors are depopulated by default. Please contact factory for a custom configuration.
- **Power Up & System Reset Fail-Safe** – For safety, the outputs are turned OFF upon power-up and a system reset. Thus, the SSR's will

be disabled after a power-up or system reset.

- **Wide Range Bipolar Voltage Outputs** – Outputs are rated from 0 to ±60 volts. The bipolar solid state relays allow both AC and DC switching.
- **Output Readback Function** – A 32-bit readback buffer is provided to allow the output channel registers to be read back.
- **No Configuration Jumpers or Switches** – All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Loopback Compatible with AP440 Digital Input Module** – The P2 field I/O pin assignments of this model are directly compatible with those of the Acromag Model AP440 32-Channel Isolated Input Module for direct closed-loop monitoring of the output states. The AP445 also shares the same pinout used on the Acromag non-isolated AP408 32-Channel I/O Module, for channels 0-31.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a 50 pin front panel connector.

The cables and termination panels are also available. For optimum performance with the AP445 isolated output module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

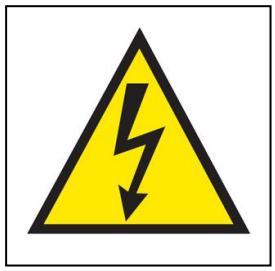
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2
  http://www.acromag.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Board Configuration

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. Model AP445 isolated output boards have no hardware jumpers or switches to configure.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-T Samtec connector on the carrier. The stack height is 4.5mm.

Pin assignments are unique to each AP model. Table 2.1 lists signal pin assignments for the module field I/O connector. Every other pin of the 100 pin connector is left unconnected in order to meet the minimum creepage distance required for 60 volt isolation.

Table 2.1: Field I/O Connector Pin Assignments

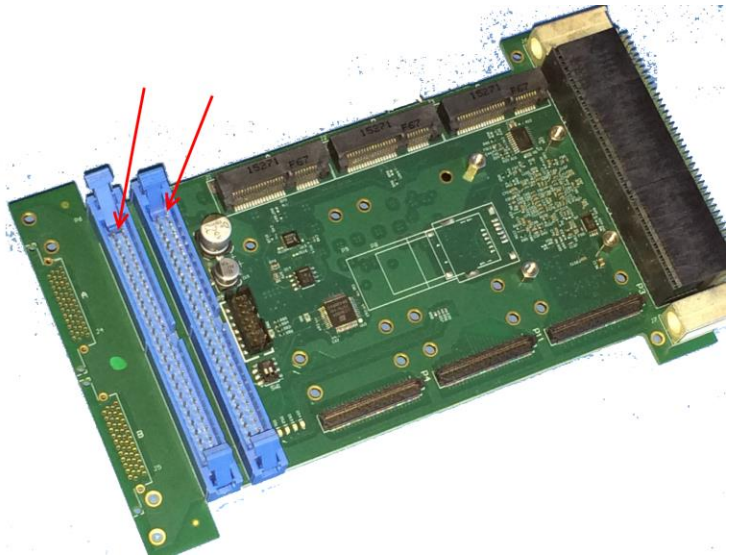
Ribbon Carrier Connector[1]	50 Pin Champ Carrier Connector[2]	68 Pin Champ Carrier Connector[3]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	Field Output 1
2	26	35	1	Field Output 2
			4	Reserved/isolation
			3	Reserved/isolation
3	2	2	6	Field Output 3

4	27	36	5	Field Output 4
			8	Reserved/isolation
			7	Reserved/isolation
5	3	3	10	ASUP
6	28	37	9	Field Output 5
			12	Reserved/isolation
			11	Reserved/isolation
7	4	4	14	Field Output 6
8	29	38	13	Field Output 7
			16	Reserved/isolation
			15	Reserved/isolation
9	5	5	18	Field Output 8
10	30	39	17	ACOM
			20	Reserved/isolation
			19	Reserved/isolation
11	6	6	22	Field Output 9
12	31	40	21	Field Output 10
			24	Reserved/isolation
			23	Reserved/isolation
13	7	7	26	Field Output 11
14	32	41	25	Field Output 12
			28	Reserved/isolation
			27	Reserved/isolation
15	8	8	30	BSUP
16	33	42	29	Field Output 13
			32	Reserved/isolation
			31	Reserved/isolation
17	9	9	34	Field Output 14
18	34	43	33	Field Output 15
			36	Reserved/isolation
			35	Reserved/isolation
19	10	10	38	Field Output 16
20	35	44	37	BCOM
			40	Reserved/isolation
			39	Reserved/isolation
21	11	11	42	Field Output 17
22	36	45	41	Field Output 18
			44	Reserved/isolation

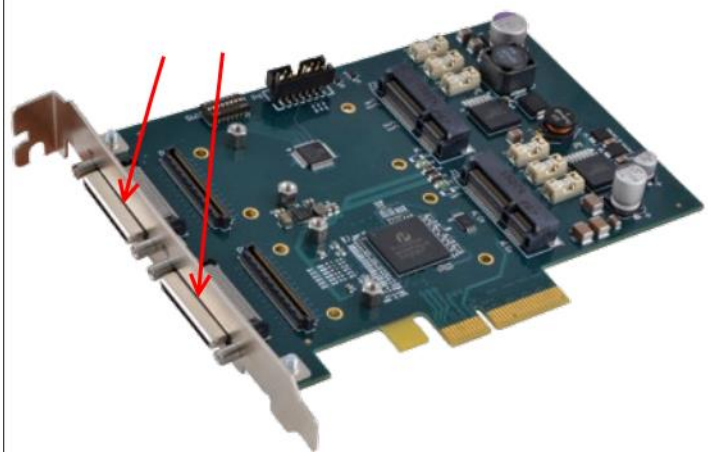
			43	Reserved/isolation
23	12	12	46	Field Output 19
24	37	46	45	Field Output 20
			48	Reserved/isolation
			47	Reserved/isolation
25	13	13	50	CSUP
26	38	47	49	Field Output 21
			52	Reserved/isolation
			51	Reserved/isolation
27	14	14	54	Field Output 22
28	39	48	53	Field Output 23
			56	Reserved/isolation
			55	Reserved/isolation
29	15	15	58	Field Output 24
30	40	49	57	CCOM
			60	Reserved/isolation
			59	Reserved/isolation
31	16	16	62	Field Output 25
32	41	50	61	Field Output 26
			64	Reserved/isolation
			63	Reserved/isolation
33	17	17	66	Field Output 27
34	42	51	65	Field Output 28
			68	Reserved/isolation
			67	Reserved/isolation
35	18	18	70	DSUP
36	43	52	69	Field Output 29
			72	Reserved/isolation
			71	Reserved/isolation
37	19	19	74	Field Output 30
38	44	53	73	Field Output 31
			76	Reserved/isolation
			75	Reserved/isolation
39	20	20	78	Field Output 32
40	45	54	77	DCOM
			80	Reserved/isolation
			79	Reserved/isolation
41	21	21	82	NC

42	46	55	81	NC
			84	Reserved/isolation
			83	Reserved/isolation
43	22	22	86	NC
44	47	56	85	NC
			88	Reserved/isolation
			87	Reserved/isolation
45	23	23	90	NC
46	48	57	89	NC
			92	Reserved/isolation
			91	Reserved/isolation
47	24	24	94	NC
48	49	58	93	NC
			96	Reserved/isolation
			95	Reserved/isolation
49	25	25	98	NC
50	50	59	97	NC
			100	Reserved/isolation
			99	Reserved/isolation

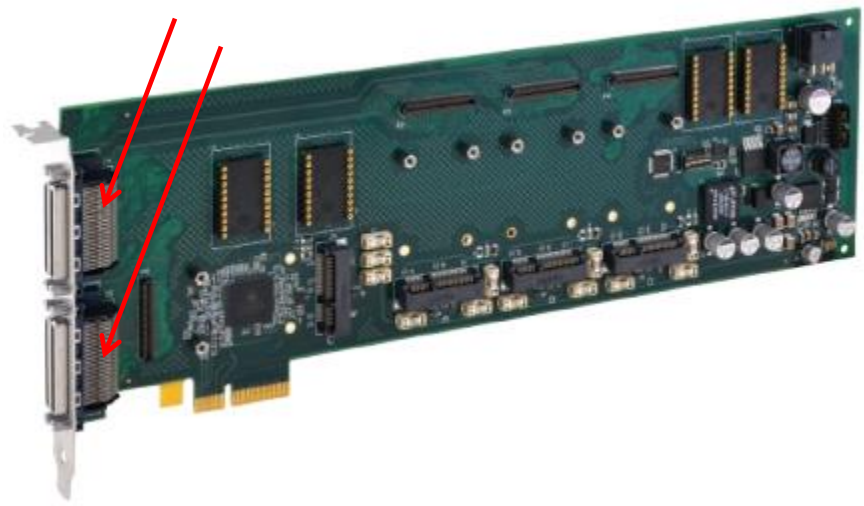
Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector see image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the Champ connector. See image of carrier.



Note 3: APCe7040E-LF is an example of a carrier that uses the 68-pin Champ connector. See image of carrier.



Output channels of this module are divided into four ports of eight channels each. Channels of a port share a common signal connection with each other (ACOM, BCOM, CCOM and DCOM). Isolation is provided between ports and between each port and the AcroPack logic circuitry.

Field I/O pinouts are arranged to be compatible with similar AcroPack models. This model is directly loopback compatible with the Acromag Model AP440 Isolated Input Module. Likewise, pin assignments are identical to those of Acromag Model AP408.

Note that the inputs of this device are bipolar, and may be connected in any polarity with respect to the port common. Further, do not confuse port commons with signal common. For the AP445, port common only infers that this lead is connected common to the 8 inputs of the port (a separate port common for each port). Likewise, the port commons of the AP445 output module and AP440 input module are normally not connected together for

loopback interconnection (see Figure 3 in Appendix A)

2.5 Noise and Earth Grounding Considerations

Output lines of the AP445 are isolated between the logic and field I/O connections. Likewise, separate port commons facilitate port-to-port isolation. Consequently, the field I/O connections are isolated from the carrier board and backplane, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations to avoid inadvertent isolation bridges, noise pickup, isolation voltage clearance violations, equipment failure, or earth ground loops.

2.6 Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Threaded metric M2.5 screws and spacers are supplied with the AP module carriers and conduction cooling kit to provide additional stability for harsh environments.

Power supplies +5V, +12V, and -12V have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.2: Logic Interface Connections

Pin #	Name	Pin #	Name
51	+5V[1,2]	52	+3.3V[3]
49	+12V[1,2]	50	GND
47	-12V[1,2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	N.C. (+1.5V)[1]

25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: Signals are not applicable for the AP445 implementation. Pins are either "no connects" on the module or are repurposed for JTAG.

Note 2: +5V, +12V, and -12V power supplies have been assigned to pins that are reserved in the mini-PCIe specification.

Note 3: All +3.3Vaux power pins are changed to +3.3V power.

Note 4: The Present signal is tied to circuit common on the AP module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP445 module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AP445 module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access an AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request. Interrupts are not supported on the AP445 module.

Table 3.1: Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7014 AP445E-LF		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x7014 AP445E-LF		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

The memory space address map for the AP445 is shown in Table 3.2. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these AP445 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted.

Memory Map

The AP445 registers provide simple control and readback of 32 digital output lines. Data is read from or written to one of four groups (ports) as designated by the address and read and write signals.

Table 3.2: AP445 Memory Map

BAR0 Base Address	Bit(s)	Description
0x0000 0000	32:0	Reset Register
0x0000 0004	32:0	Location in System Register
0x0000 0008	32:0	Port Output Register OUTPUT00-OUTPUT31
0x0000 000C→ 0x0000 0044	32:0	NOT USED[1]
0x0000 0048	32:0	XADC Status Control Register
0x0000 004C	32:0	XADC Address Register

Notes:

1. The AP will respond to addresses that are "Not Used". The board will return "0" for all address reads that are not used or reserved.

Software Reset Register (Write Only) - (BAR0 + 0x0000 0000)

This write only register is used to reset all the output ports to 0 (SSR switches OFF).

Table 3.3: Reset Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION
0	Writing a '1' to this bit will cause a software reset.
31 to 1	Not Used

Module Location In System Register (Read Only) - (BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.4: Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or a carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

Port Output Register (Read/Write) - (BAR0 + 0x0000 0008)

This register is provided to control 32 possible output points. Data can be read from or written to one of the four groups of eight output lines (Ports 0-3), as designated by the address and read/write signals.

Table 3.5: Port Output Register

Bit(s)	FUNCTION
7 to 0	Port A: Output Channels 7 to 0
15 to 8	Port B: Output Channels 15 to 8
23 to 16	Port C: Output Channels 23 to 16
31 to 24	Port D: Output Channels 31 to 24

Write a zero to each channel's position to turn the corresponding SSR OFF.
Write a one to each channel's position to turn the corresponding SSR ON.

Each output channel can be conveniently read back for verification purposes. For critical control applications, it is recommended that outputs be directly fed back to an input point and the input point be monitored (loopback I/O). Acromag Model AP440 32-channel isolated input modules can be used to implement loopback output monitoring with this module (see Figure 3 in Appendix A).

On power-up or software reset, the ports are reset to 0 forcing the outputs (SSR's) to be OFF.

XADC Status/Control Register (Read/Write) – (BAR0 + 48H)

This read/write register will access the XADC register at the address set in the XADC Address Register.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x4CH. Next, this register at BAR0 plus 0x48H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only) – (BAR0 + 4CH)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x48H.

Table 3.6: System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 3.7 FPGA Voltage and Temperature Range

Symbol	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Temperature operating range	-40C	50-60C	100C

Firmware Revision Register (Read Only) – (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A, then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Figure 1, in Appendix A, as you review this material.

4.1 Logic/Power Interface

The PCIe bus interface logic is embedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe target interface uses a single 4K base address register.

A FPGA device provides the control signals required to operate the board. It decodes the selected addresses and control signals. It also returns the acknowledgement messages required by the carrier/CPU board per the PCIe specification. The program for the FGPA is stored in separate Flash memory and loaded upon power-up.

4.2 Output Ports

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Individual Solid State Relays (SSR's) for each channel isolate the field from the control logic for the AP445. Channels are isolated from each other in groups of eight. There are eight channels to a group or port. Because the output lines of a single port share a common connection, individual outputs are not isolated from each other within the same port. However, separate port commons are provided to facilitate port-to-port isolation.

32 Single Pole Single Throw – Normally Open (SPST-NO, "1 Form A") SSR outputs are controlled by this module. Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching. 0603 size surface mount resistors can be provided for low side switching applications. These resistors are not populated on the standard model. They should not be populated for high side switching applications. For low side applications the resistor value will need to be calculated. Lower values will provide a faster pull-up while higher values will keep power dissipation from becoming a problem at higher voltages – see Specifications in Chapter 6.5 for details.

The SSR's are controlled by an output register within the FPGA. Writing a '1' to the output register will turn the switch ON (closed-circuit) while writing a '0' will turn it OFF (open-circuit). Readback of the output state is accomplished by reading the output register. However, for complete confidence in output control, loopback should be performed. This may be accomplished using the AP440 isolated digital input module. (Refer to Figure

2 and Figure 3 in Appendix A).

The SSR's employed are rated for a much higher voltage than specified for the AP445. However, the printed circuit board foil spacings limit applied voltages to ±60VDC or AC peak. Each port (group of eight channels) has a single common. Due to the printed circuit board foil width, each port is limited to 1A maximum. Thus the sum of currents conducted by the eight channels must stay below that maximum. The low on resistance of the SSR's helps to reduce their power dissipation when they conduct high currents; however, given the large number of channels on the board, adequate air circulation must be maintained. The SSR's do not contain any built in current limiting for their protection. Please refer to the Specifications in Chapter 6.5 for providing external current limiting, if necessary. The SSR's provide clean, bounce free switching and can replace electromechanical relays in many applications. SSR switching speeds are comparable to electromechanical relays (1ms typical) but are slow compared to high speed optocouplers.

Output operation is "Fail-safe." That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a software (reset register) or system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag website at www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.314ounces (8.9g)

6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
• 3.3 VDC +/- 5%	495mA typ (all outputs OFF) 675mA typ/800mA max (all outputs ON)
• 1.5 VDC +/- 5%	Not Used
• 5.0 VDC +/- 5%	Not Used
• +12 VDC +/- 5%	Not Used
• -12 VDC +/- 5%	Not Used

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	*Description*	*Temp Range*
AP445E-LF	32 channel, isolated output module	*-40*°C *to 85*°C[1]

Note 1: An air cooled application with an AcroPack module will require a minimum airflow of 200LFM.

6.3.2. Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

6.3.3 Isolation

Logic and field connections are isolated (see OUTPUT specifications). Individual ports are also isolated from each other. However, output lines of individual ports share a common connection and are not isolated from each other. Separate port commons are provided to facilitate port-to-port working voltage isolation of 100VAC or DC. Logic and field lines are isolated from each other for working voltages up to 250VAC or DC on a continuous basis (unit will withstand a 1450V AC dielectric strength test for one minute without breakdown).

6.3.4 Vibration and Shock Standards

The AcroPack passes the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Complies with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating: Complies with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Complies with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.3.5 EMC Directives

The AcroPack complies with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

Table 6.1 AP445E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	TBD	TBD	TBD
40°C	TBD	TBD	TBD

[1] FIT is Failures in 10^9 hours.

6.5 OUTPUTS

Output Channel Configuration	32 isolated Solid State Relay (SSR) output supporting AC or DC (high or low side switching) operation. SPST-NO, "1 Form A" contacts.
"OFF" Voltage Range	0 to ±60V DC or peak AC.
Output "OFF" Leakage Current	1uA maximum
Output "ON" Current Range	150mA maximum continuous (up to 1A total per port). Outputs are NOT current limited and may need external current limiting circuitry to ensure current does not exceed 150mA (R = V/I). When choosing a current limiting resistor, also be sure not to exceed to maximum power rating for that resistor (Power = V^2/R).
Ouput ON resistance	8Ω, maximum (25°C)
Turn-On Time	1ms typical, 2ms maximum
Turn-Off Time	0.2ms typical, 1ms maximum
Reset Condition	All output SSR's OFF
Output Pull-up Resistors	Pull-up resistors are depopulated on standard model for high side switching applications. The 0603 surface mount pull-ups can be installed by factory at customer request for low side switching applications. Calculate resistor power for user supplied voltage (Power = V^2/R). Limit power to 0.2W per resistor (30.6V max @ 4.7KΩ). Install a lower value (check power) to obtain faster, stronger pull-up.
TTL Compatibility	Yes, used as a low side switch can sink 32mA at 0.2V; source 500uA at 2.4V with a 4.7k ohm pull-up to 5V supply.

6.6 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) available through PCIe connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register (BAR)

Table 6.6 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\,Bytes} =$ 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

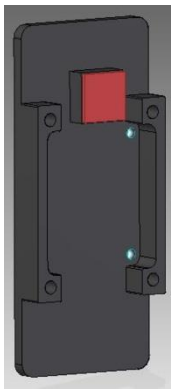
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

Appendix A

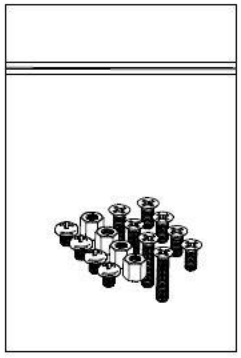
AP-CC-01 Heatsink Kit Installation



Bottom view



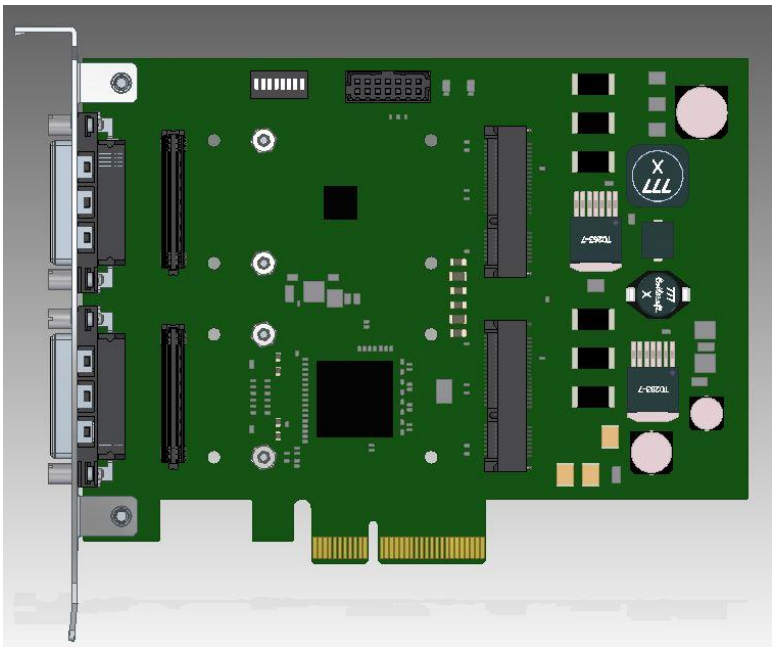
Top view



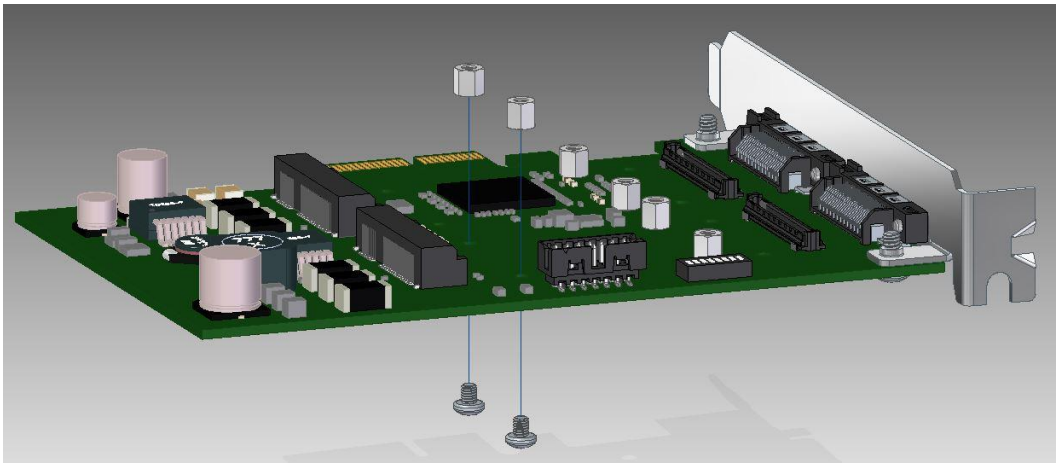
Hardware

AP-CC-01 Heat Sink Kit

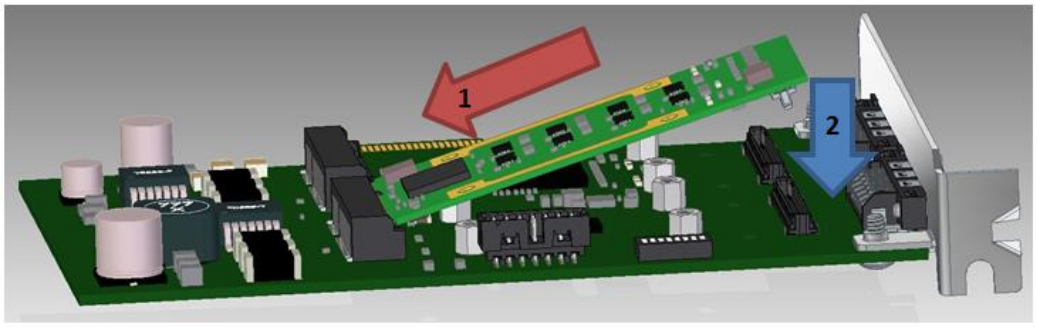
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



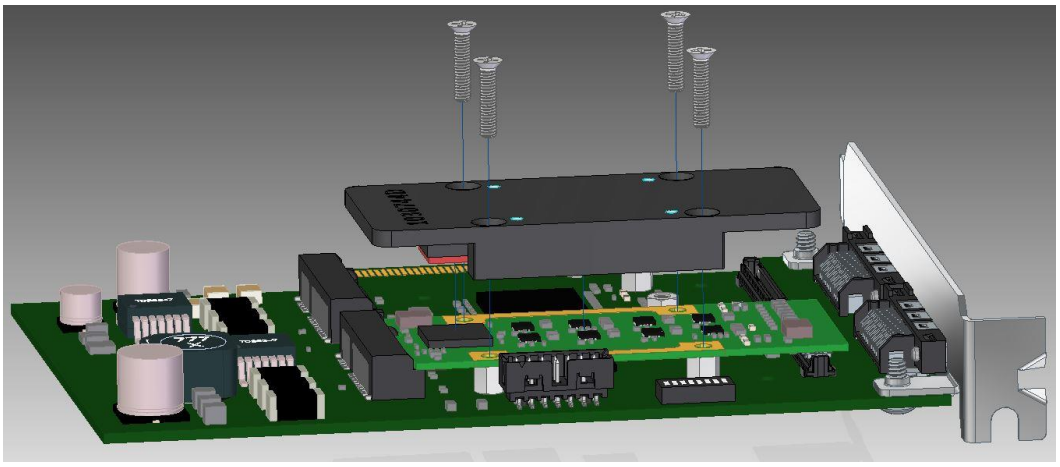
1. Install two standoffs and secure with two screws.



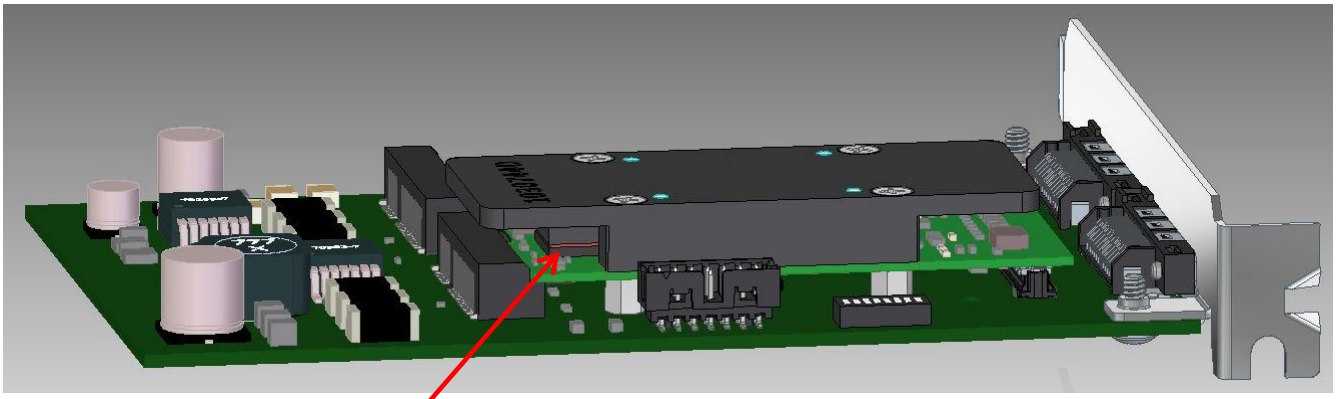
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Appendix B

Figure 1 AP445 Block Diagram

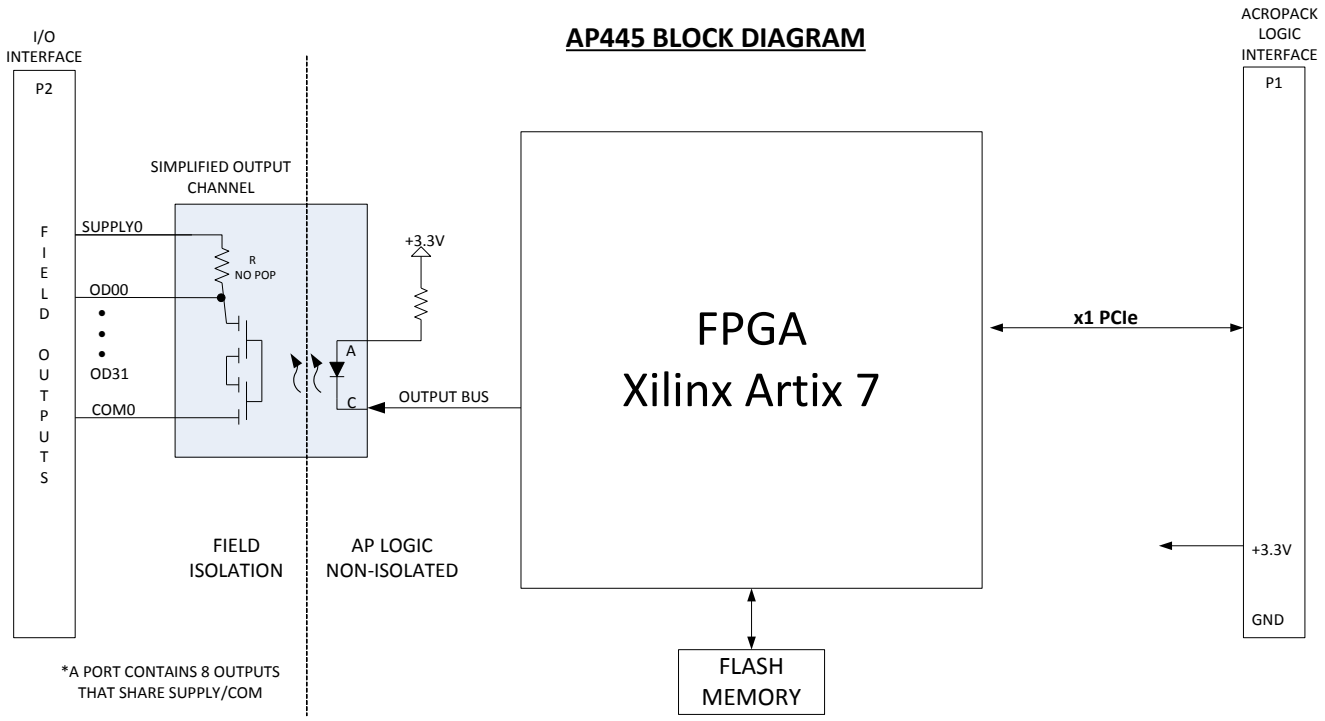
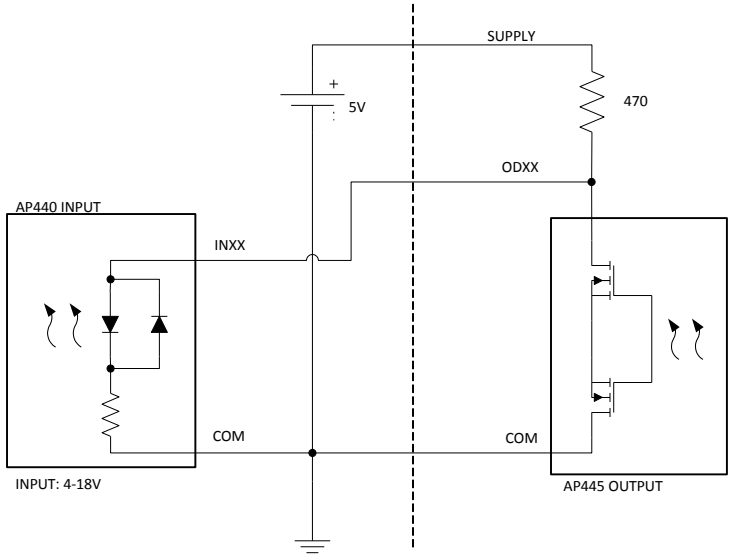


FIGURE 1: AP445 Block Diagram

Figure 2 AP445 Digital Out to AP440 Digital In



AP445 DIGITAL OUT TO AP440 DIGITAL INPUT

WHEN INTERFACING DIGITAL OUTPUT LEVELS TO THE AP440., USE THE MODEL AP440-1 (4V THRESHOLD) AND ADJUST THE EXTERNAL PULLUP VALUE ACCORDINGLY.

470 OHM PULLUPS SHOULD BE INSTALLED ON THE AP445.

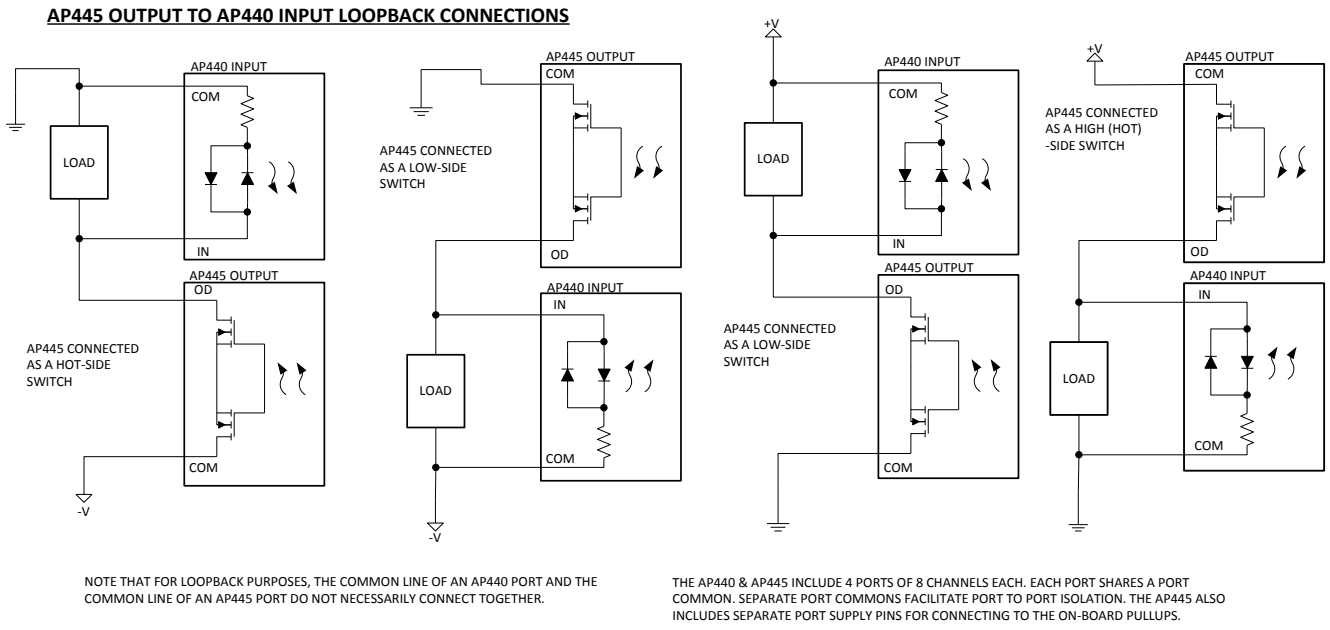
WHEN INTERFACING THE AP445 TO A TYPICAL TTL INPUT DEVICE LIKE THE 74LS541. THE 4.7K PULLUPS SHOULD BE INSTALLED AND THE CONNECTED TO THE PART SUPPLY PIN.

P2 PINOUTS OF THE AP440 AND AP445 ARE DIRECTLY COMPATABLE. HOWEVER, THE AP445INCLUDES A PULLUP SUPPLY PIN FOR EACH PORT AT PIN 5 (PORT0), PIN 15 (PORT 1), PIN 25 (PORT 2), AND PIN 35 (PORT 3). THESE PINS ARE NOT CONNECTED ON THE AP440.

AP440 INPUTS AND AP445 OUTPUTS ARE BIPOLAR AND MAY BE CONNECTED IN ANY DIRECTION WITH RESPECT TO PORT COMMON.

FIGURE 2: AP445 DIGITAL OUT TO AP440 DIGITAL IN

Figure 3 AP445 to AP440 Loopback Connections



NOTE THAT FOR LOOPBACK PURPOSES, THE COMMON LINE OF AN AP440 PORT AND THE COMMON LINE OF AN AP445 PORT DO NOT NECESSARILY CONNECT TOGETHER.

THE AP440 & AP445 INCLUDE 4 PORTS OF 8 CHANNELS EACH. EACH PORT SHARES A PORT COMMON. SEPARATE PORT COMMONS FACILITATE PORT TO PORT ISOLATION. THE AP445 ALSO INCLUDES SEPARATE PORT SUPPLY PINS FOR CONNECTING TO THE ON-BOARD PULLUPS.

FIGURE 3: AP445 TO AP440 LOOPBACK CONNECTIONS

Certificate of Volatility

Acromag Model AP445E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks and Block RAM Blocks	Size: 16,640 Logic Cells and 900 Kb Block RAM	User Modifiable ■ Yes □ No	Function: FPGA logic blocks and RAM blocks	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 32Meg x 1bit	User Modifiable ■ Yes □ No	Function: FPData storage for FPGA	Process to Sanitize: Erase using JTAG
Type(EEPROM, Flash, etc.) One Time Programmable area in Flash device	Size: 3 x 256-byte	User Modifiable □ Yes ■ No	Function: The OTP area has been disabled by writing the lock bits with logic 1.	Process to Sanitize: Not applicable
Acromag Representative				
Name: Russ Nieves	Title: Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

Revision History

The revision history for this document is summarized in the table below.

Release Date (mm/dd/yyyy)	Version	EGR/DOC	Description of Revision
1/15/2016	Preliminary	ENZ/ENZ	Preliminary Document Publication
7/19/2016	Rev A	ENZ/MJO	Rev A Release
8/02/2016	Rev B	ENZ/MJO	Minor format changes, carrier installation instructions added, isolation voltage added and Firmware Revision Register added.
10/11/2016	Rev C	ENZ/MJO	Added 68-pin Champ connector, Updated EMC Directives, Vibration and Shock Standards and Certificate of Volatility
15 NOV 2017	Rev D	ENZ/MJO	Added APCe7040E-LF carrier picture, updated Where To Get Help Section, added more info on TTL compatibility
11 JAN 2018	Rev E	LMP/MJO	Added Table 6.6 PCIe Bus Data Rates.

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