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Series AP471 AcroPack
48-Channel Digital I/O Module
USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack modules. It is not intended for a general, non-technical audience that is unfamiliar with I/O devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

1.2.1 Trademark, Trade Name and Copyright Information

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1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an additional 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Model Number	*Description*	*Temp Range*
AP471E-LF [1]	*48-Channel Digital I/O*	*-40°C to 85°C*

Note 1: *Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 with a minimum airflow of 200LFM. For temperatures below 70°C the module will require a minimum airflow of 200LFM.*

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix B for installation instructions)

1.3.2 Key Features

The AP471 module provides 48 channels of general-purpose digital inputs and outputs. Inputs and outputs of this module are CMOS and TTL compatible. Each of the I/O lines can be used as either an input, an output, or an output with read-back capability. Each I/O line has built-in event sense circuitry with programmable polarity and interrupt support. The inputs may also operate as independent event sense inputs (without interrupts). Outputs are open drain and may sink up to 15mA each. A 4.7K pull-up is provided for each drain. Inputs include hysteresis and programmable debounce. Interrupt, event, and debounce functionality applies to all 48 channels of this model. The AP471 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance interface at a low cost.

- **High Channel Count** - Provides programmable monitor and control of 48 discrete I/O points.
- **Programmable Polarity Event Interrupts (all 48 channels)** - Interrupts are software programmable for change-of-state, positive (low-to-high) or negative (high-to-low) input level transitions on all 48 channels.

- **Programmable Debounce (all 48 channels)** - The event sense input circuitry includes programmable debounce times for all 48 channels. Debounce time is the duration of time that must pass before the input transition is recognized as valid. This helps prevent false event detections and increases noise immunity.
- **CMOS (TTL Compatible)** - Input threshold is at TTL levels and includes hysteresis. I/O circuitry uses CMOS technology. As such, output levels are CMOS compatible, even while sinking high current.
- **Output Read-back Function** – Read-back buffers are provided that allow the output port registers to be read back.
- **High Output Sink Capability** - All outputs may sink up to 15mA with a voltage drop ≤ 0.5V.
- **Outputs are "Glitch-Free"** - Unlike some competitive units, the outputs of this device do not "glitch" (momentarily turn on) upon power-up or power-down for reliable and safe control.
- **Open Drain Outputs Include Pull-ups** - All outputs include 4.7K pull-up resistors to +5V.
- **Overvoltage Protection** - Individual I/O channels include over-voltage clamps for increased ESD & transient protection.
- **High Impedance Inputs** - High impedance inputs minimize input current and loading of the input source.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a front panel connector on most carrier boards.

Accessory cables and termination panels are also available. For optimum performance with the AP471 digital I/O module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

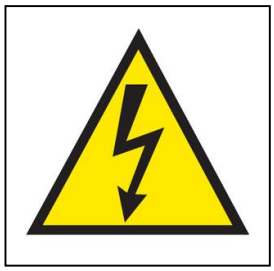
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 http://www.pcisig.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air-cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the PCIe bus and AcroPack module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Pin assignments are unique to each AP model. Table 2.1 lists signal pin assignments for the module field I/O connector. Some pins are left unconnected in order to meet the minimum creepage distance required for 60 Volt isolation.

For the most accurate pinout information, see the manual of the specific carrier board model being used.

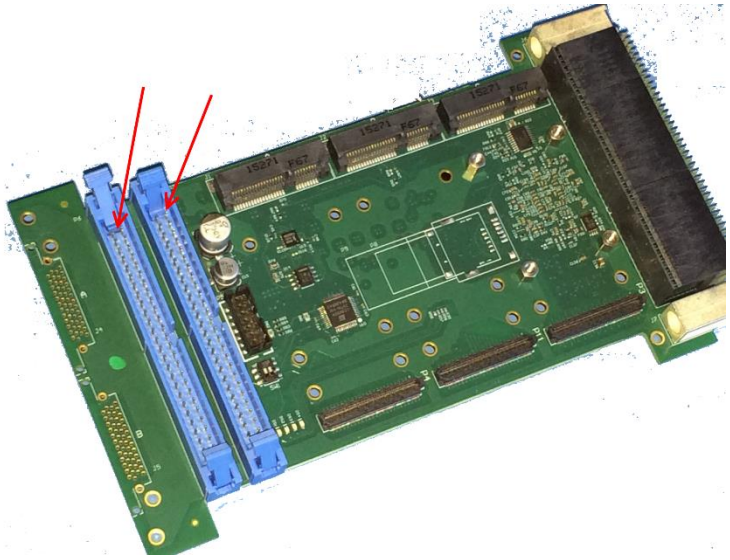
Table 2.1 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	Field I/O 1
35	26	2	1	Field I/O 2
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	Field I/O 3
36	27	4	5	Field I/O 4
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	Field I/O 5
37	28	6	9	Field I/O 6
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	Field I/O 7
38	29	8	13	Field I/O 8
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	Field I/O 9
39	30	10	17	Field I/O 10
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	Field I/O 11
40	31	12	21	Field I/O 12
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	Field I/O 13
41	32	14	25	Field I/O 14
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	Field I/O 15
42	33	16	29	Field I/O 16
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	Field I/O 17
43	34	18	33	Field I/O 18
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	Field I/O 19
44	35	20	37	Field I/O 20
			40	Reserved/isolation

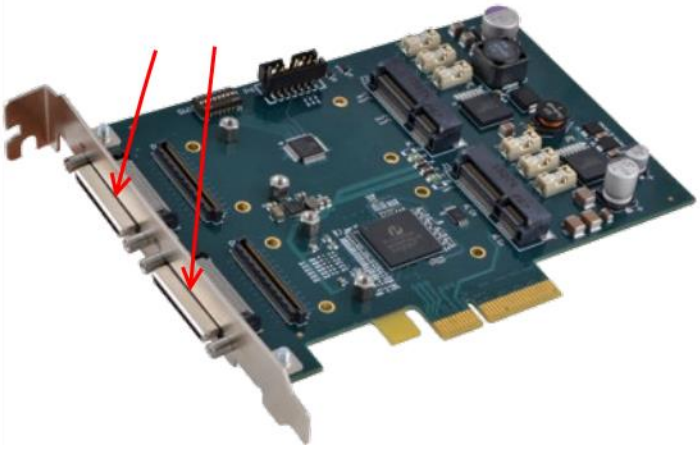
68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			39	Reserved/isolation
11	11	21	42	Field I/O 21
45	36	22	41	Field I/O 22
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	Field I/O 23
46	37	24	45	Field I/O 24
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	Field I/O 25
47	38	26	49	Field I/O 26
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	Field I/O 27
48	39	28	53	Field I/O 28
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	Field I/O 29
49	40	30	57	Field I/O 30
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Field I/O 31
50	41	32	61	Field I/O 32
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	Field I/O 33
51	42	34	65	Field I/O 34
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	Field I/O 35
52	43	36	69	Field I/O 36
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	Field I/O 37
53	44	38	73	Field I/O 38
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Field I/O 39
54	45	40	77	Field I/O 40
			80	Reserved/isolation
			79	Reserved/isolation

68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
21	21	41	82	Field I/O 41
55	46	42	81	Field I/O 42
			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	Field I/O 43
56	47	44	85	Field I/O 44
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	Field I/O 45
57	48	46	89	Field I/O 46
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	Field I/O 47
58	49	48	93	Field I/O 48
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	+5V (Fused)
59	50	50	97	GND
			100	Reserved/isolation
			99	Reserved/isolation

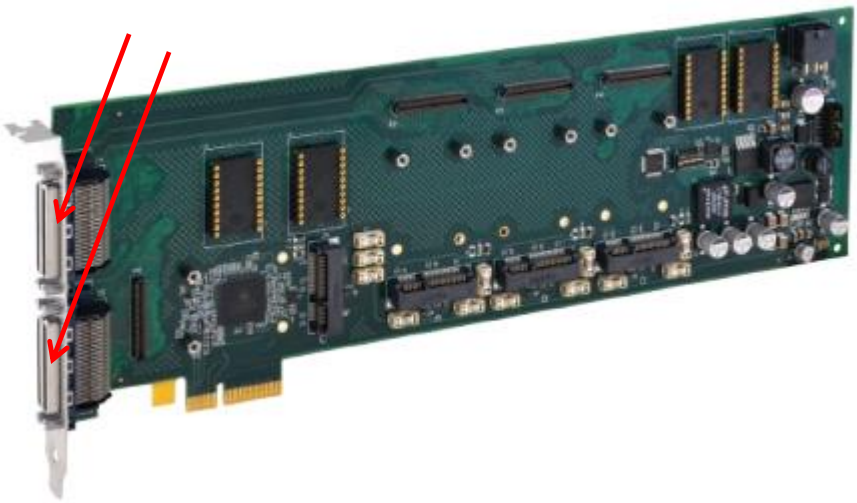
Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector. See image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the 50-pin Champ connector. See image of carrier.



Note 3: APCe7040E-LF is an example of a carrier that uses the 68-pin Champ connector. See image of carrier.



2.5 Logic Interface Connector

The AP module logic card edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The 'Present' signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.2 Logic Interface Connections

Pin #	Name	Pin #	Name
51	+5V[1,2]	52	+3.3V[3]
49	+12V[1,2]	50	GND
47	-12V[1,2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	N.C. (+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: Signals are not applicable for the AP471 implementation. Pins are either "no connects" on the module or are repurposed for JTAG.

Note 2: +5V, +12V, and -12V power supplies have been assigned to pins that are reserved in the mini-PCIe specification.

Note 3: All +3.3Vaux power pins are changed to +3.3V power.

Note 4: The 'Present' signal is tied to circuit common on the AP module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP471 module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AP471 module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access an AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request assigned to the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers which must be read to determine the base address assigned to the board and the Interrupt Register which must be read to determine the interrupt request that goes active on a board interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7015 AP471		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x7015 AP471		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

This board is addressable in the PCIe memory space to control the configuration and status monitoring of 48 digital input or output channels.

Memory Map

The memory space address map for the AP471 is shown in Table 3.2. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these AP471 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the AP471 are accessed via data lines D0 to D31.

This board provides access to the control, configuration and monitoring of the 48 digital I/O lines. Each input line is configured as either an input or output with readback capability. Data is read or written to the channels as designated by the address and read and write signals. A mask register is used to disable writes to I/O channels designated as inputs to prevent possible contention between external input signals and the open drain output circuitry. Event Sense inputs allow for event triggered flags to be set and interrupts to be generated. Selectable hardware debounce may also be applied for noise free edge-detection of incoming signals. Registers are also provided to enable interrupt generation and to generate a software reset.

Table 3.2: Memory Map

Notes:

1. The AP471 will respond to addresses that are "Not Used". The board will return "0" for all address reads that are not used or reserved.

Base BAR0 Address	Bit(s)	Name
0x0000	7:0	Interrupt Enable Status Register
0x0004	7:0	Location in System Register
0x0008	15:0	I/O Register IO00-IO15
0x000C	15:0	I/O Register IO16-IO31
0x0010	15:0	I/O Register IO32-IO47
0x0014	15:0	Write Mask Register IO00-IO15
0x0018	15:0	Write Mask Register IO16-IO31
0x001C	15:0	Write Mask Register IO32-IO47
0x0020	15:0	Event Enable Register IO00-IO15
0x0024	15:0	Event Enable Register IO16-IO31
0x0028	15:0	Event Enable Register IO32-IO47
0x002C	15:0	Event Type Register IO00-IO15
0x0030	15:0	Event Type Register IO16-IO31
0x0034	15:0	Event Type Register IO32-IO47
0x0038	15:0	Event Polarity Control Reg. IO00-IO15
0x003C	15:0	Event Polarity Control Reg. IO16-IO31
0x0040	15:0	Event Polarity Control Reg. IO32-IO47
0x0044	15:0	Event Pending/Clear Register IO00-IO15
0x0048	15:0	Event Pending/Clear Register IO16-IO31
0x004C	15:0	Event Pending/Clear Register IO32-IO47

0x0050	15:0	Debounce Control Register IO00-IO15
0x0054	15:0	Debounce Control Register IO16-IO31
0x0058	15:0	Debounce Control Register IO32-IO47
0x005C	31:0	Debounce Duration Register IO00-IO15
0x0060	31:0	Debounce Duration Register IO16-IO31
0x0064	31:0	Debounce Duration Register IO32-IO47
0x0068	0	Debounce Clock Select Register
0x006C	0	Software Reset Register
0x0070	32:0	XADC Status/Control Register
0x0074	32:0	XADC Address Register
0x0078→0x01FC	-	Not Used
0x0200	7:0	Firmware Revision Register

Interrupt Enable Status Register (Read/Write)

(BAR0 + 0x0000 0000)

This read/write register is used to: enable board interrupts and determine the pending status of interrupts.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

With both an enabled Event Sense bit and Board Interrupt Enable bit, then interrupts can be generated.

Table 3.3 Interrupt Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
0	Board Interrupt Enable Bit. This bit must be set to logic "1" to enable generation of interrupts from the AP module. Setting this bit to logic "0" will disable board interrupts. (Read/Write Bit)	
	0	Disabled
	1	Enabled
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt
	1	Interrupt Pending
31 to 2	Not Used	

Module Location In System Register (Read Only)

(BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.4 Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or an on-carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

I/O Registers (Read/Write)

(BAR0 + 0x0000 0008 – 0x0000 0010)

Three registers are provided to control/monitor 48 possible I/O points. Data is read from or written to one of three groups of sixteen I/O lines, as designated by the address and read and write signals. A read of this register returns the status (ON/OFF) of the I/O point. A write to this register controls the state of the open-drain output (low level true). Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point. The Mask Register is used to disable writes to I/O points designated as input channels. That is, when a line is used as an input channel, writes to this channel must be blocked (masked) to prevent contention between the output circuitry and any external device driving this input line.

Outputs are configured as open-drain with resistive pull-ups installed. Thus, on power-up or reset, the I/O registers are reset to 0, forcing the outputs to be set high (OFF).

Write Mask Registers (Read/Write)

(BAR0 + 0x0000 0014 – 0x0000 001C)

The Write Mask Registers are used to individually mask the ability to write data to each of the 48 channels of this model. Writing a '1' to any channel's corresponding bit of the Mask Register will mask that channel, from inadvertent writes. A read of these registers will return the status of the mask. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Bits 31 down to 16 of these registers are not used. On power-up reset, all bits are set to '0', allowing writes to the output channels.

Event Enable Registers (Read/Write)

(BAR0 + 0x0000 0020 – 0x0000 0028)

The Event Enable Registers provide a mask bit for each of the 48 possible interrupt channels. A "0" bit will prevent the corresponding input channel from detecting an event. A "1" bit will allow the corresponding input channel to detect events as configured by the Event Type and Event Polarity Control Registers. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

If both an Event Sense and the board Interrupt Enable bit is set, then interrupts can be generated.

Event Type (COS or H/L) Configuration Registers (Read/Write)

(BAR0 + 0x0000 002C – 0x0000 0034)

The Event Type Configuration Registers determine the type of input channel transition that will generate an event for each of the forty-eight possible event sensing channels. A "0" bit selects event on level transition. An event will be generated when the input channel level specified by the Event Polarity Register occurs (i.e. low or high-level transition event). A "1" bit means the event will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low). Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset which means that, if enabled, the inputs will cause events and/or interrupts for the levels specified by the Interrupt Polarity Register.

Event Polarity Control Registers (Read/Write)

(BAR0 + 0x0000 0038 – 0x0000 0040)

A write to these registers controls the polarity of the input sense event for each channel. A "1" written to a bit in these registers will cause the corresponding event sense input channel to flag positive events (low-to-high transitions). A "0" will cause negative events to be sensed (high-to-low transitions). Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset which means that negative events will be flagged by default.

Event Pending/Clear Registers (Read/Write)

(BAR0 + 0x0000 0044 – 0x0000 004C)

The Event Pending/Clear Registers reflect the status of the 48 possible interrupt channels. A "1" bit indicates that an event flag has been set for the corresponding channel. A channel that does not have events enabled will never set its event pending flag. A channel's event can be cleared by writing a "1" to its bit position in the Event Pending/Clear Register. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset.

Debounce Control Registers (Read/Write)

(BAR0 + 0x0000 0050 – 0x0000 0058)

These registers are used to control whether each individual channel is to be passed through the debounce logic before being recognized by the circuitry. A "0" disables the debounce logic for the corresponding channel, and a "1" enables the debounce logic. Debounce applies to both inputs and event sense inputs. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Furthermore, after enabling the debounce circuitry, wait at least three times the programmed debounce duration prior to reading the input ports or event signals to ensure valid data.

Debounce Duration Registers (Read/Write)

(BAR0 + 0x0000 005C – 0x0000 0064)

These registers control the duration required by each input signal before it is recognized by each individual input. Two bits control the debounce duration for each channel. If the debounce clock selected is the 31.25MHz internal system clock (see Debounce Clock Select Register), then the debounce times are selected as shown below (actual times vary to within minus 25% of nominal). Alternately, the debounce clock may be input on I/O47 and other values configured (see Debounce Clock Select Register), but this reduces the effective number of I/O channels to 47.

Table 3.5 Debounce Duration Register Channels 0 to 15 (Channels 16 to 31 and 32 to 47 similar)

Bit(s)	FUNCTION	
1 to 0	Channel 0 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
3 to 2	Channel 1 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
. . .	Channel x Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
31 to 30	Channel 15 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms

The default value is 00, setting 3-4us debounce period. This register is cleared following a reset (setting debounce to 3-4us). Note that the debounce clock must be re-selected to re-enable debounce following a reset (see below).

When using I/O47 as the debounce clock the effective debounce duration can be calculated by taking the clock period (in seconds) and multiplying it by the appropriate constant shown in Table 3.6 below. The debounce will have an error of ±2 clock periods.

Table 3.6 Debounce Duration Clock Multiplier Selection

Debounce Duration Selection	Debounce Count Constant
00	125
01	2000
10	31250
11	250000

Debounce Clock Select Register (Read/Write)

(BAR0 + 0x0000 0068)

This register selects the source clock for the event sense input debounce circuitry. If bit 0 is set to 0 (default), then the 31.25MHz internal system clock is used (recommended). If bit 0 of this register is 1, then the debounce source clock is taken from I/O47 thus reducing the effective number of I/O

points to 47. Bits 1-7 of this register are not used and will always read as zero.

WARNING: IF USING I/O47 AS THE DEBOUNCE CLOCK, DO NOT SET THE I/O AS AN ACTIVE OUTPUT VIA THE CHANNEL I/O REGISTERS. SETTING I/O47 AS AN ACTIVE OUTPUT MAY CAUSE A BUS CONFLICT.

Bit(s)	FUNCTION	
0	Debounce Clock Select	
	0	Internal clock @ 31.25 MHz (default)
	1	External clock on I/O47
7 to 1	Not Used	

Software Reset Register (Write Only)

(BAR0 + 0x0000 006C)

Writing a 1 to the bit 0 position of this register will cause a software reset to occur. This bit is not stored and merely acts as a trigger for software reset generation (this bit will always read back as 0). The Interrupt Enable Bit of the Interrupt Enable and Status register is not cleared in response to a software reset. Bits 1-7 of this register are not used and will always read as zero.

XADC Status/Control Register (Read/Write)

(BAR0 + 0x0000 0070)

This read/write register will access the XADC register at the address set in the XADC Address Register. This allows the board's temperature and supply voltages to be read.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x74H. Next, this register at BAR0 plus 0x70H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(^{\circ}C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only)

(Bar0 + 0x0000 0074)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x70H.

Table 3.7: System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 3.8: FPGA Voltage and Temperature Range

	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Temperature operating range	-40C	50-60C	100C

Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

The Effect of Reset

A power-up or bus-initiated software reset will set the outputs to the false (high) state with no event sensing, no interrupts, and no debounce enabled. Pull-up resistors on the I/O lines ensure a false (high) input signal for inputs left floating (i.e. reads as 0). A reset will also clear the channel mask register and enable writes to the I/O ports. Further, all I/O event inputs are reset, set to negative events, and are disabled following reset. However, the Interrupt Enable bit is not cleared with a software reset.

Basic I/O Operation

Note that the I/O lines of this module are split into groups of 16 for simplicity in the memory map. Each channel can be individually configured as an output, or as an input with different event polarity and debounce duration.

The input signals are inverted – when an output is ON (set to '1'), the transistor sinks current and drives the output low (this is read back as a '1'). Inputs include hysteresis. Further, each input channel is connected such that the current status of a given output channel can be read back via the corresponding input channel. Individual channels may also be masked from writes to the channel when the channel is intended for input only to help prevent contention errors.

Each channel has an associated event sense input and debounce logic circuit. The event sense inputs are used to sense high-to-low level or low-to-high level transitions on digital input lines at CMOS thresholds. Interrupts may also be triggered by events. The optional debounce logic can act as a filter to "glitches" or transients present on the received signals. Further, events may be defined as change-of-state, or positive or negative polarity for individual channels.

Each I/O line includes an integrated 4.7kΩ pull-up resistor to +5V. For inputs, the pull-ups provide a low (false=0) input indication if the input is otherwise left floating.

Each I/O line is in the form of an open-drain signal. Thus, data written to any channel used as an input must be masked or always false (zero) to avoid contention between the output circuitry and an input signal from an external device. All 48 I/O lines are placed into the false (high output) state following power-up or a system reset. The 4.7kΩ pull-up resistors installed on the board provide digital high-drive capability for the output signals. If this does not provide adequate current sourcing capability, another pullup can be added external to the module.

Event Sensing

The AP471 has event sense logic built-in for all 48 digital I/O lines, I/O00 through I/O47. Event sensing may be configured to generate an interrupt to the carrier, or merely reflect the interrupt internally. Inputs can be individually set to detect change-of-state, or positive or negative events. The event sensing is also enabled on an individual channel basis. You can

combine event sensing with the built-in debounce control circuitry to obtain "glitch-free" edge detection of incoming signals.

To program events, determine which I/O lines are to have events enabled and which polarity is to be detected, high-to-low level transitions (negative) or low-to-high level transitions (positive). Set each bit to the desired polarity, and then enable each of the event inputs to be detected. Optionally, set the interrupt enable bit in the Interrupt Register to enable board level interrupts. Note that all I/O event inputs are reset, set to negative events, and disabled after a power-up or software reset has occurred.

Note that no events will be detected until enabled via the Event Enable Registers. Further, interrupts will not be reported to the carrier board unless the interrupt enable bit of the Interrupt Register has been set.

Debounce Control

Debounce control is built into the on-board digital FPGA employed by the AP471. You can combine debounce with event sensing to obtain "glitch-free" edge detection of incoming signals for all 48 channels. That is, the debounce circuitry will automatically filter out "glitches" or transients that can occur on received signals, for error-free edge detection and increased noise immunity. With debounce, an incoming signal must be stable for the entire debounce time before it is recognized by the I/O or event sense logic. Debounce is applied to both inputs and event sense inputs.

The debounce circuitry can be configured to use the 31.25MHz internal system clock, or a clock signal present on I/O channel 47, to determine the debounce times (see the Debounce Clock Select register). If the debounce clock is taken from I/O47, then the effective number of inputs is reduced to 47. If the AP471 is configured to use the 31.25MHz internal system clock (recommended), a debounce value of 4us, 64us, 1ms, or 8ms may be selected (see the Debounce Duration Registers). As such, an incoming signal transition must be stable for the debounce time before it is recognized by the I/O pin or event sense logic. A slower clock may be used to provide even longer debounce times (this clock would have to be provided on I/O47).

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input channels or event signals to ensure that the input data is valid prior to being used by the software.

Interrupt Generation

This model provides control for generation of interrupts on change-of-state, or positive or negative events, for all 48 channels. Interrupts are only generated when events are enabled via the Event Enable registers. Writing "1" to the corresponding event sense bit in the Event Pending/Clear register will clear the event. Interrupts may be reflected internally and reported by polling the module. Control of this line is initiated via bit 0 of the Interrupt Enable Register.

The event sense status is a flag that is raised when a specific change-of-state, positive, or negative transition has occurred for a given I/O point, while the state refers to its current level.

Enabling both an Event Sense bit and the board interrupts will allow interrupts to be generated

Note that the Interrupt Enable Register is cleared following a power-up or bus initiated hardware reset, but not a software reset initiated via writing a one to bit 0 of the Software Reset Register. Keep this in mind when you wish to preserve the information in these two registers following a reset.

Programming Example

The following example outlines the steps necessary to configure the AP471 to setup event-generated interrupts, configure debounce, and read and write I/O. It is assumed that the module has been reset and no prior (non-default) configuration exists.

For this example, we will configure channels 0 thru 3 as a four-channel positive (low-to-high) transition detector. I/O00-I/O03 will be tied to input signals. Any positive transition detected on these input signals will cause an interrupt to be generated.

1. The default debounce duration is 4µs with the default 31.25MHz debounce clock. Write 0000 0055H to the Debounce Duration Register to select a 64µs debounce time for channels 0 thru 3. An incoming signal must be stable for the entire debounce time before it will be recognized as a valid input transition.
2. Enable the debounce circuitry for channels 0 thru 3 inputs by setting bits 0 thru 3 of the Debounce Control Register. Write 000FH to the Debounce Control Register. If the module had been configured earlier, you would first read this register to check the existing settings of debounce enable for the other channels of this module with the intent of preserving their configuration by adjusting the value written above.
3. For our example, I/O00-I/O03 will be used to detect positive events (low-to-high transitions). Write 000FH to the Event Polarity Control Register to set I/O00-I/O03 to positive edge detection. If the module had been configured earlier, you would first read this register to check the existing settings of event polarity for the other channels of this module with the intent of preserving their configuration by adjusting the value written above.
4. To enable event sensing for channels 0 thru 3, write 000FH to the Event Enable Register.
5. For our example, channels 0 thru 3 are to be used for inputs only and writes to this port should be masked to prevent the possibility of

data contention between the built-in output circuitry and the devices driving these inputs. Write 000FH to the Write Mask Register.

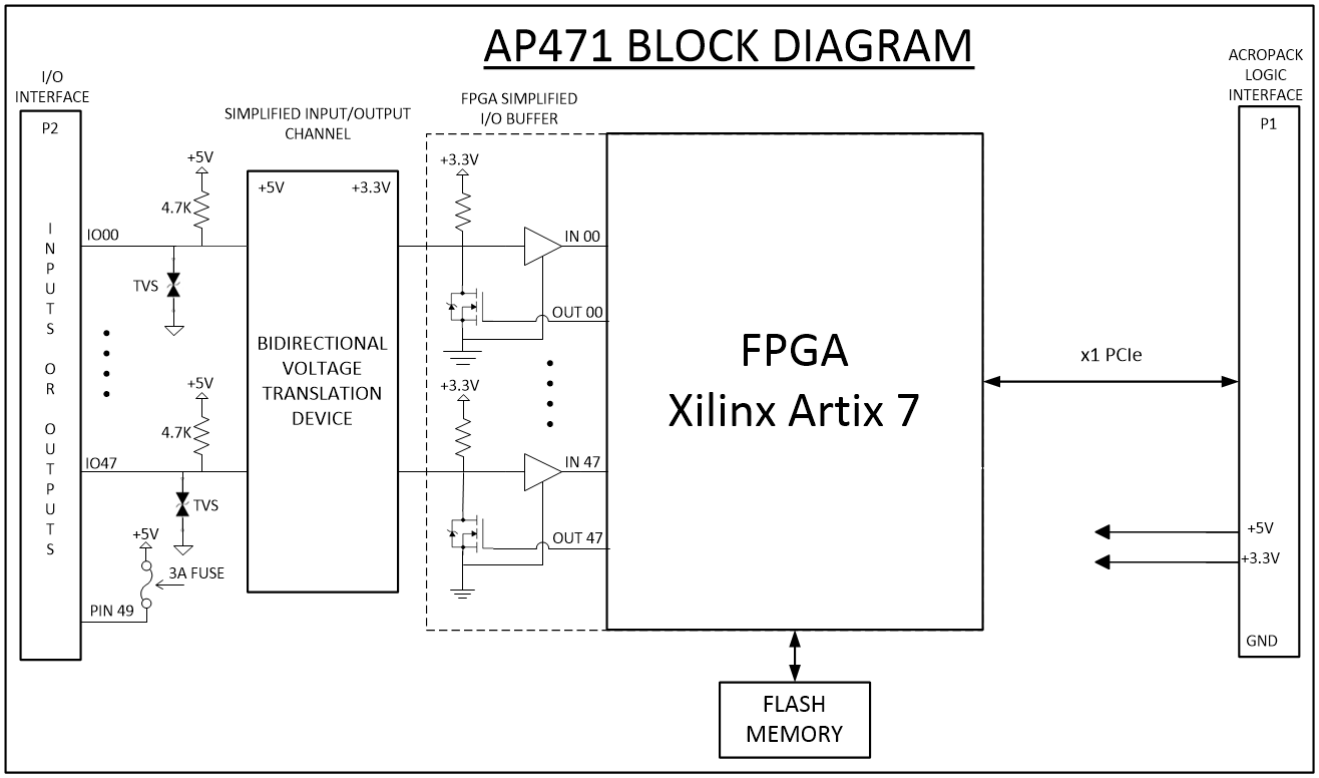
6. (OPTIONAL) Write 01H to the Interrupt Enable Register to enable interrupt request.

   When a positive transition is detected, an interrupt will be generated (if the event sense detection circuitry has been enabled and Interrupt Enable bit 0=1).

   Note that the state of the inputs (on/off) can be determined by reading the corresponding I/O Registers. The event sense status can only be determined by reading the corresponding Event Pending/Clear Register. Remember, the event sense status is a flag that is raised when a specific positive or negative transition has occurred for a given input point, while the state refers to its current level.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown below as you review this material.



4.1 Logic/Power Interface

The PCIe bus interface logic is embedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe target interface uses a single 4K base address register.

A FPGA device provides the control signals required to operate the board. It decodes the selected addresses and control signals. It also returns the acknowledgement messages required by the carrier/CPU board per the PCIe specification. The program for the FGPA is stored in separate Flash memory and loaded upon power-up.

4.2 I/O Ports

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field I/O points are NONISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

A Field Programmable Gate Array (FPGA) is used to generate all the logic necessary to operate the board. With respect to input acquisition, all 48 input channels support interrupts and drive the FPGA through buffers. The input signal threshold is TTL compatible and includes hysteresis. Further, each input channel is connected such that the current status of a given output channel can be read back via the corresponding input channel. Individual channels may also be masked from writes to the channel when the channel is intended for input only to help prevent contention errors.

Each I/O line includes an integrated 4.7kΩ pull-up resistor to +5V. For inputs, the pull-ups provide a low (false=0) input indication if the input is otherwise left floating.

Each I/O line is in the form of an open-drain signal. Thus, data written to any channel used as an input must be masked or always false (zero) to avoid contention between the output circuitry and an input signal from an external device. All 48 I/O lines are placed into the false (high output) state following power-up or a system reset. The 4.7kΩ pull-up resistors installed on the board provide digital high-drive capability for the output signals.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier and I/O boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag website at www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.2624 oz (7.5 g)

6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
3.3 VDC +/- 5%[1]	400 mA Typical 600 mA Max
1.5 VDC +/- 5%[1]	Not Used
5.0 VDC +/- 5%[1]	0.5 mA (All Outputs OFF) 60 mA (All Outputs ON w/ 4.7 kΩ pull-ups)
+12 VDC +/- 5%	Not Used
-12 VDC +/- 5%[1]	Not Used

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	***Description***	***Temp Range***
AP471E-LF	*48-Channel Digital I/O*	*-40*°C *to 85*°C[1]

Note 1: *Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 with a minimum airflow of 200LFM. For temperature below 70°C the module will require a minimum airflow of 200LFM.*

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix B for installation instructions)

6.3.2 Relative Humidity

The range of acceptable relative humidity is 5% to 95%, non-condensing.

6.3.3 Isolation

The PCIe bus and field commons are non-isolated and have a direct electrical connection.

6.3.4 Vibration and Shock Standards

The AcroPack is designed to meet the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.3.5 EMC Directives

The AcroPack complies with EMC Directive 2014/30/EU.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	TBD	TBD	TBD
40°C	TBD	TBD	TBD

[1] FIT is Failures in 10^9 hours.

6.5 Digital Inputs

Input Channel Configuration	48 buffered inputs with programmable debounce circuitry. For DC voltage applications only, observe proper polarity.
Input Signal Voltage Range	-0.25V to +5.25V DC
Input Low Voltage Range	0.8V Max to 0.25V below common ground.
Input High Voltage Range	2.2V Min to 0.25V above +5V supply Max.
Input Transition Rise or Fall Time	3ms/V Max.
Input Response Time	250ns Typical
Input Threshold	1.5V Typical
Input/Output Capacitance	20pF Max, 10pF Typical
Input Leakage Current	±10µA Typical

6.6 Digital Outputs

Output Channel Configuration	48 open-drain CMOS outputs. For DC voltage applications, only, observe proper polarity.
Output Low Voltage	0.1VDC Typical, 0.4VDC Maximum at 12mA
Output High Voltage	4.8VDC at -10µA
Output "ON" Current Range	0 to 15mA DC (for $V_{OL} \leq 0.5V$)
Output R_{DS} ON Resistance	33Ω Maximum (25°C)
Output Pullups	4.7kΩ integrated pull-ups installed on board.

Turn On Time	125ns Typical
Turn Off Time (4.7K pull-ups)	2us Typical

6.7 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) available through PCIe connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register (BAR)

6.7.1 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\,Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

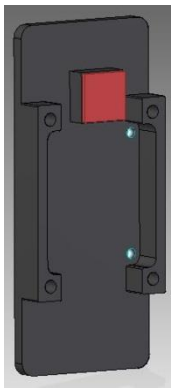
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

Appendix A

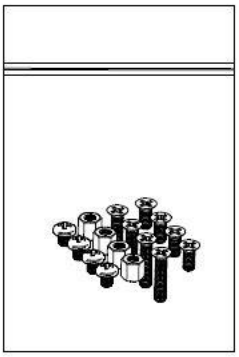
AP-CC-01 Heatsink Kit Installation



Bottom view



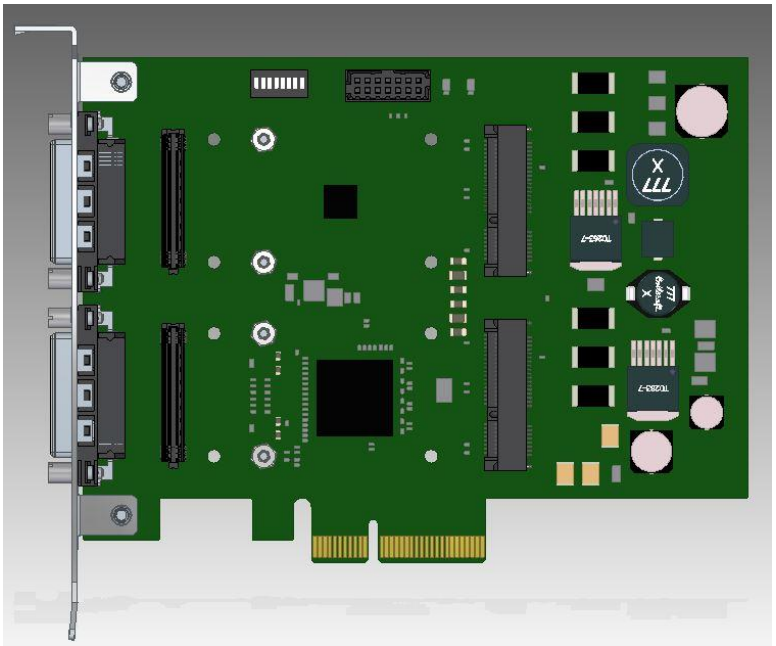
Top view



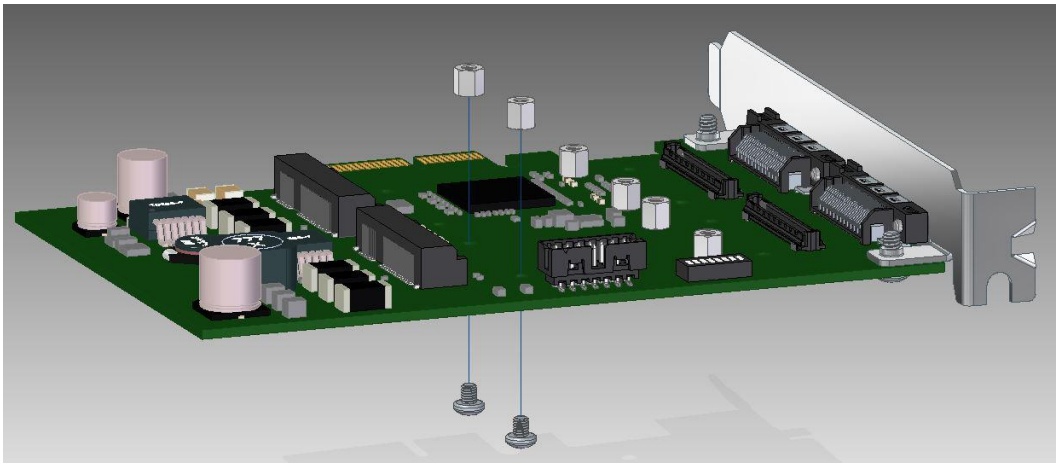
Hardware

AP-CC-01 Heat Sink Kit

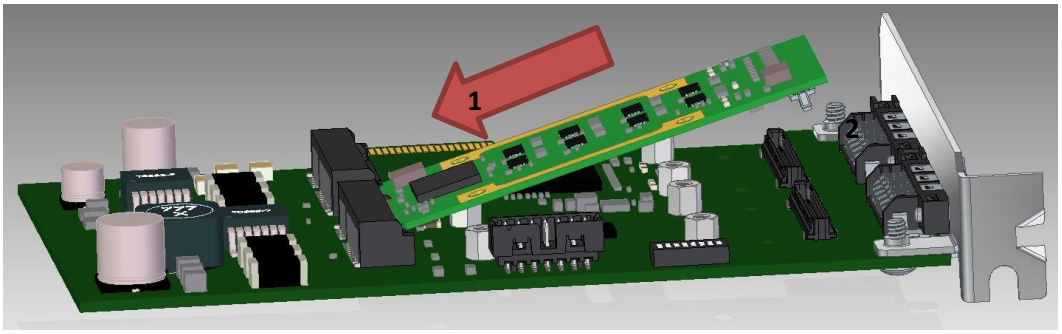
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



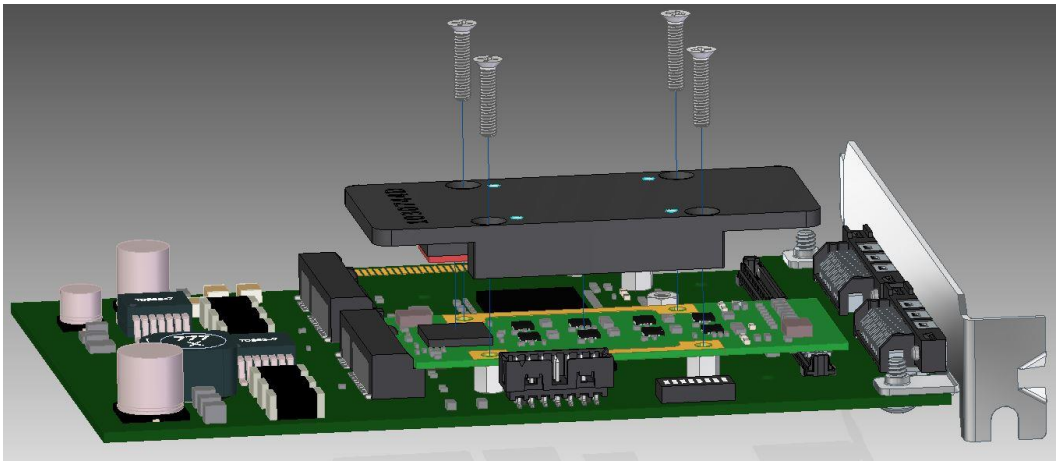
1. Install two standoffs and secure with two screws.



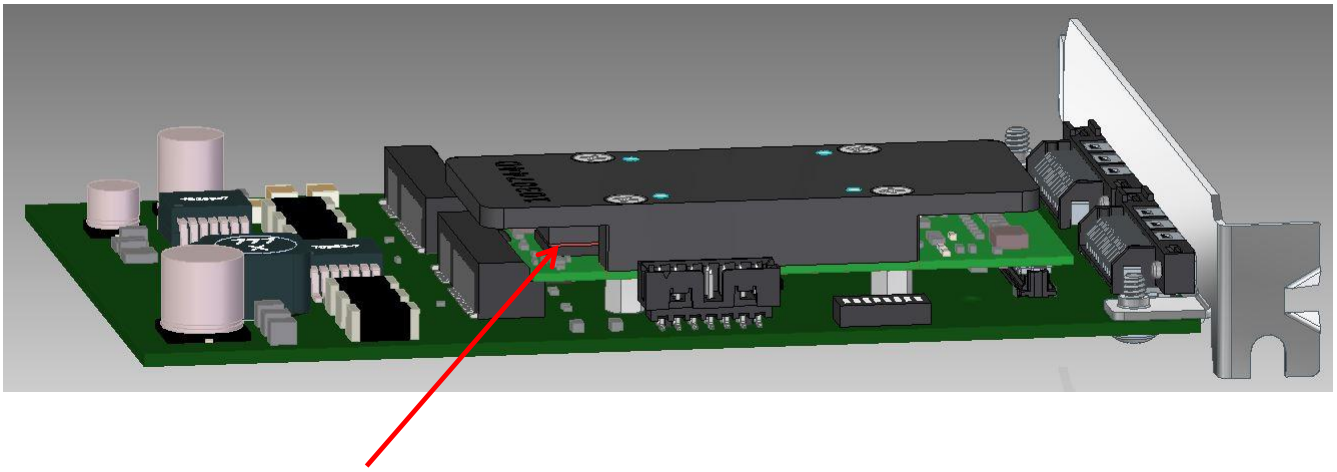
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Certificate of Volatility

<table>
<tr><td colspan="6"></td></tr>
<tr><td colspan="2">Acromag Model
AP471E-LF</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><td colspan="6">Volatile Memory</td></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
■ Yes □ No</td></tr>
<tr><td colspan="2">Type (SRAM, SDRAM, etc.)
Configurable Logic Blocks and Block RAM Blocks</td><td>Size:

16,640 Logic Cells and 900 Kb Block RAM</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
FPGA logic blocks and RAM blocks.</td><td>Process to Sanitize:
Power Down</td></tr>
<tr><td colspan="2">Type (SRAM, SDRAM, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td>Process to Sanitize:</td></tr>
<tr><td colspan="6">Non-Volatile Memory</td></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No</td></tr>
<tr><td colspan="2">Type(EEPROM, Flash, etc.)
Flash</td><td>Size:
32Mb</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Data storage for FPGA</td><td>Process to Sanitize:
Erase using JTAG</td></tr>
<tr><td colspan="2">Type(EEPROM, Flash, etc.)
One Time Programmable area in flash device</td><td>Size:
3 x 256-byte</td><td>User Modifiable
□ Yes
■ No</td><td>Function:
The OTP area has been disabled by writing the lock bits with logic 1.</td><td>Process to Sanitize:
Not applicable</td></tr>
<tr><td colspan="6">Acromag Representative</td></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Sales and Marketing</td><td colspan="2">Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td>Office Fax:
248-624-9234</td></tr>
</table>

Revision History

The revision history for this document is summarized in the table below.

Release Date	Version	EGR/DOC	Description of Revision
10 AUG 2017	Preliminary	ENZ/ENZ	Preliminary Document Publication.
23 OCT 2017	A	ENZ/MJO	Initial Release.
15 NOV 2017	B	ENZ/MJO	Added input rise/fall times and ouput turn on/turn off times.
12 JAN 2018	C	LMP/MJO	Added PCIe Bus Data Rates, Section 6.7.1.
23 JUL 2018	D	ENZ/MJO	Block diagram change.

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