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Carrier Card Series

APCe8675 PCI Express Bus XMC Carrier

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1. GENERAL INFORMATION

The APCe8675 card is a Peripheral Component Interconnect Express (PCIe) bus card carrier for an XMC module. The carrier enables the use of XMC mezzanine I/O modules in a standard desktop computer. The carrier card acts as an adapter to route PCIe bus signals between the PCIe bus of your PC and the P15 connector of an XMC module card. Access to XMC P16 and P4 rear I/O is provided through connectors P2, P3 and J1. XMC modules with front I/O can be accessed through the front mounting bracket. Cables are available to connect the P2 and P3 rear I/O signals to other carrier cards in adjacent slots. Cables are also available to connect the J1 rear I/O to a front panel bracket mounted connector located in an adjacent slot.

Model	Board Size (Length)	Operating Temperature Range
APCe8675	Long (12.283”)	0 to +70°C

KEY APCe8675 FEATURES

PCI Express Carrier: - Eight PCI Express lanes are connected to the XMC P15 connector.

Removable Fan: For applications that do not require the cooling fan, the fan can be easily removed. With the fan removed the APCe8675 will fit in the space of a single slot.

High Speed Serial Rear I/O: The APCe8675 provides the capability to connect to neighboring carrier cards using high speed serial protocols such as XAUI or Aurora. Two connectors are provided which enable connection to left and right neighbors. Each cable includes 20 high speed differential pairs. The cables are Samtec QPairs® High Speed Twinax cable assemblies.

Rear I/O: 32 differential pairs are routed from the XMC P4 connector to an MD68 (internal SCSI) male connector. With an optional cable, these signals may be connected to a panel mount connector in a PCI card bracket installed in an adjacent slot. A cutout in the board has been provided for routing cabling internal to the PC

Auxiliary Power Connection: 12 Volt power may be optionally supplied through a PCI express graphics power connector if the XMC card requires more power than what is available from the PCIe card slot.

JTAG Programming Header: The APCe8675 carrier includes a programming connector that mates with a Xilinx programmer for programming Acromag FPGA products. Acromag XMC FPGA boards can be configured to route the JTAG programming signals through the XMC P15 connector.

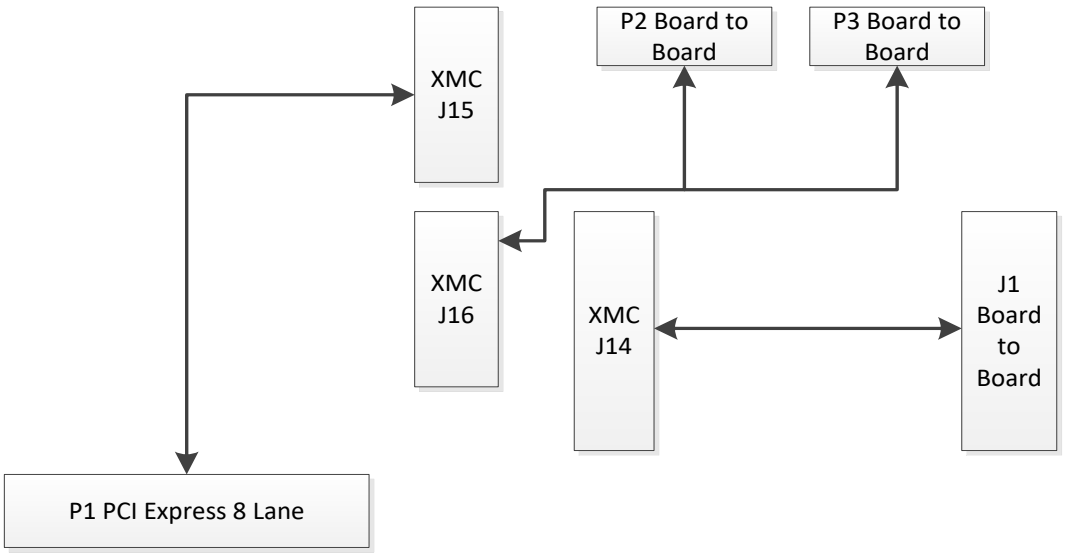


Figure 1 Block Diagram Showing Data Paths

SIGNAL INTERFACE PRODUCTS

Cables

Acromag offers a cable (Acromag part number 5025-917) that connects P2 and P3 rear I/O signals to other Acromag APCe8675 carriers in neighboring slots. This cable is a crossover cable; it routes the transmit differential pairs from one board to the receive differential pairs on another board. See Table 2-11.

Acromag also offers a cable that makes the XMC rear I/O signals routed through J14 and J1 accessible from the back panel of the PC. This cable connects J1 to a MD68 connector mounted on a PCI card bracket. The Acromag part number is 5025-913.

2. PREPARATION FOR USE

UNPACKING AND INSPECTION



Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed XMC module, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Board Configuration

Power should be removed from the board when changing jumper configurations or when installing an XMC module, cables and field wiring.

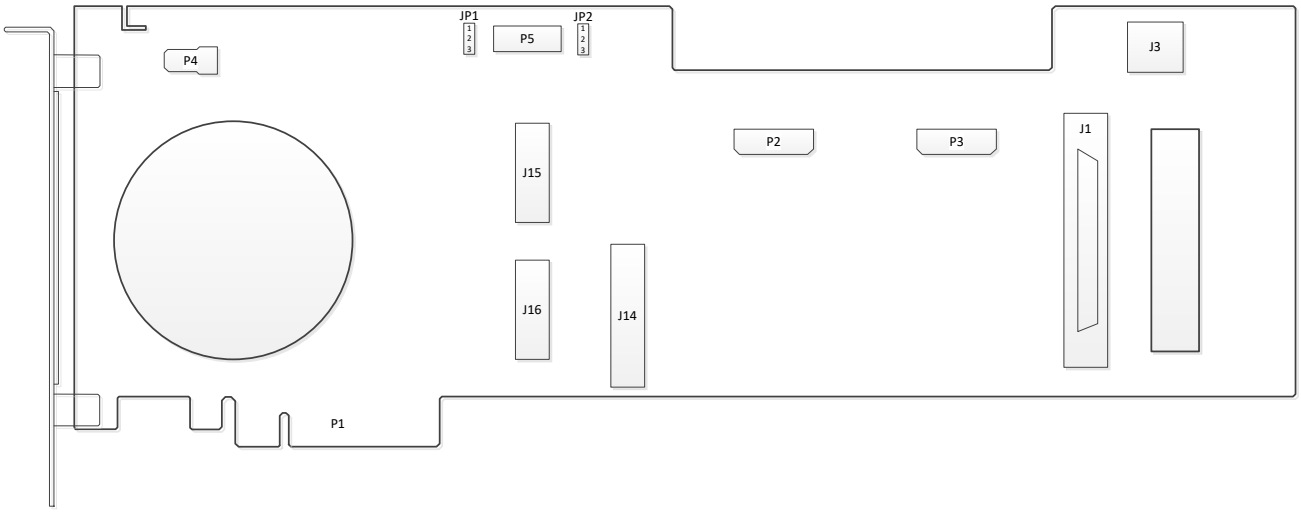


Figure 2 Jumper and Connector Locations

JUMPERS

Refer to Figure 2. Jumper JP1 selects the source of +12 Volt power. The jumper must be present in one of the two configurations for proper board operation.

Table 2-1 JP1 +12V Power Source Select Jumper

Power Source	Jumper Position
PCIe Card Edge	1 - 2
PCIe Graphics Power	2 - 3

Jumper JP2 routes either of two reference voltages to the Xilinx programmer connector. Select +2.5 Volts for Virtex 6 FPGAs.

Table 2-2 JP2 Programming Reference Voltage Select Jumper

VRef Voltage	Jumper Position
+3.3V	1 - 2
+2.5V	2 - 3

CONNECTORS

Refer Figure 2. Connectors on the APCe8675 carrier consist of two carrier IP module field I/O connectors, four IP module logic connectors, four field I/O ribbon cable connectors, a peripheral power connector, a PCIe graphics power connector and one PCI Express bus interface connector. These interface connectors are discussed in the following sections.

J1 .....board to board cable connection to J14 user signals
J3 .....auxiliary power connector (PCIe graphics)
J14 and J16 .....XMC user signals (Rear I/O)
J15 .....XMC PCIe signals
P1 .....PCI Express v1.1 x8 lanes card edge
P2 and P3 .....board to board cable connection to J16 user signals

P4 .....fan power
P5 .....JTAG (Xilinx programming adapter)

Table 2-3 J1 Board to Board Cable Connection to J14 User Signals

Pin Description	Number	Pin Description	Number
RIO0_GCLK_P	1	RIO0_GCLK_N	35
RIO1_P	2	RIO1_N	36
RIO2_P	3	RIO2_N	37
RIO3_P	4	RIO3_N	38
RIO4_P	5	RIO4_N	39
RIO5_P	6	RIO5_N	40
RIO6_P	7	RIO6_N	41
RIO7_P	8	RIO7_N	42
RIO8_P	9	RIO8_N	43
RIO9_P	10	RIO9_N	44
RIO10_P	11	RIO10_N	45
GND	12	GND	46
RIO11_P	13	RIO11_N	47
RIO12_P	14	RIO12_N	48
RIO13_P	15	RIO13_N	49
RIO14_P	16	RIO14_N	50
RIO15_P	17	RIO15_N	51
RIO16_P	18	RIO16_N	52
RIO17_P	19	RIO17_N	53
RIO18_P	20	RIO18_N	54
RIO19_P	21	RIO19_N	55
RIO20_P	22	RIO20_N	56
GND	23	GND	57
RIO21_P	24	RIO21_N	58
RIO22_P	25	RIO22_N	59
RIO23_P	26	RIO23_N	60
RIO24_P	27	RIO24_N	61
RIO25_P	28	RIO25_N	62
RIO26_P	29	RIO26_N	63
RIO27_P	30	RIO27_N	64
RIO28_P	31	RIO28_N	65
RIO29_P	32	RIO29_N	66
RIO30_P	33	RIO30_N	67
RIO31_GCLK_P	34	RIO31_GCLK_N	68

Table 2-4 J3 PCIe Graphics Power

Pin Description	Number	Pin Description	Number
+12V_AUX	1	+12V_AUX	2
+12V_AUX	3	GND	4
GND	5	GND	6
GND	7	GND	8

Table 2-5 J14 XMC User Signals (Rear I/O)

Pin Description	Number	Pin Description	Number
RIO0_GCLK_P	1	RIO1_P	2
RIO0_GCLK_N	3	RIO1_N	4
RIO2_P	5	RIO3_P	6
RIO2_N	7	RIO3_N	8
RIO4_P	9	RIO5_P	10
RIO4_N	11	RIO5_N	12
RIO6_P	13	RIO7_P	14
RIO6_N	15	RIO7_N	16
RIO8_P	17	RIO9_P	18
RIO8_N	19	RIO9_N	20
RIO10_P	21	RIO11_P	22
RIO10_N	23	RIO11_N	24
RIO12_P	25	RIO13_P	26
RIO12_N	27	RIO13_N	28
RIO14_P	29	RIO15_P	30
RIO14_N	31	RIO15_N	32
RIO16_P	33	RIO17_P	34
RIO16_N	35	RIO17_N	36
RIO18_P	37	RIO19_P	38
RIO18_N	39	RIO19_N	40
RIO20_P	41	RIO21_P	42
RIO20_N	43	RIO21_N	44
RIO22_P	45	RIO23_P	46
RIO22_N	47	RIO23_N	48
RIO24_P	49	RIO25_P	50
RIO24_N	51	RIO25_N	52
RIO26_P	53	RIO27_P	54
RIO26_N	55	RIO27_N	56
RIO28_P	57	RIO29_P	58
RIO28_N	59	RIO29_N	60
RIO30_P	61	RIO31_GCLK_P	62
RIO30_N	63	RIO31_GCLK_N	64

Table 2-6 J16 XMC User Signals (Rear I/O)

Pin Description	Number	Pin Description	Number
DP00_P	A1	DP01_P	D1
GND	A2	GND	D2
DP02_P	A3	DP03_P	D3
GND	A4	GND	D4
DP04_P	A5	DP05_P	D5
GND	A6	GND	D6
DP06_P	A7	DP07_P	D7
GND	A8	GND	D8
DP08_P	A9	DP09_P	D9
GND	A10	GND	D10
DP10_P	A11	DP11_P	D11
GND	A12	GND	D12
DP12_P	A13	DP13_P	D13
GND	A14	GND	D14
DP14_P	A15	DP15_P	D15
GND	A16	GND	D16
DP16_P	A17	DP17_P	D17
GND	A18	GND	D18
DP18_P	A19	DP19_P	D19
DP00_N	B1	DP01_N	E1
GND	B2	GND	E2
DP02_N	B3	DP03_N	E3
GND	B4	GND	E4
DP04_N	B5	DP05_N	E5
GND	B6	GND	E6
DP06_N	B7	DP07_N	E7
GND	B8	GND	E8
DP08_N	B9	DP09_N	E9
GND	B10	GND	E10
DP10_N	B11	DP11_N	E11
GND	B12	GND	E12
DP12_N	B13	DP13_N	E13
GND	B14	GND	E14
DP14_N	B15	DP15_N	E15
GND	B16	GND	E16
DP16_N	B17	DP17_N	E17
GND	B18	GND	E18
DP18_N	B19	DP19_N	E19
SIO18_GCLK_N	C1	SIO18_GCLK_P	F1
SIO16_N	C2	SIO17_N	F2
SIO16_P	C3	SIO17_P	F3
SIO14_N	C4	SIO15_N	F4
SIO14_P	C5	SIO15_P	F5

Pin Description	Number	Pin Description	Number
SIO12_N	C6	SIO13_N	F6
SIO12_P	C7	SIO13_P	F7
SIO10_N	C8	SIO11_N	F8
SIO10_P	C9	SIO11_P	F9
SIO8_N	C10	SIO9_N	F10
SIO8_P	C11	SIO9_P	F11
SIO6_N	C12	SIO7_N	F12
SIO6_P	C13	SIO7_P	F13
SIO4_N	C14	SIO5_N	F14
SIO4_P	C15	SIO5_P	F15
SIO2_N	C16	SIO3_N	F16
SIO2_P	C17	SIO3_P	F17
SIO0_GCLK_N	C18	SIO1_N	F18
SIO0_GCLK _P	C19	SIO1_P	F19

Table 2-7 P2 Board to Board Cable Connection to J16 User Signals

Pin Description	Number	Pin Description	Number
DP00_P	1	DP10_P	2
DP00_N	3	DP10_N	4
DP01_P	5	DP11_P	6
DP01_N	7	DP11_N	8
DP02_P	9	DP12_P	10
DP02_N	11	DP12_N	12
DP03_P	13	DP13_P	14
DP03_N	15	DP13_N	16
DP08_P	17	DP09_P	18
DP08_N	19	DP09_N	20
SIO0_GCLK_P	21	SIO1_P	22
SIO0_GCLK_N	23	SIO1_N	24
SIO2_P	25	SIO3_P	26
SIO2_N	27	SIO3_N	28
SIO4_P	29	SIO5_P	30
SIO4_N	31	SIO5_N	32
SIO6_P	33	SIO7_P	34
SIO6_N	35	SIO7_N	36
SIO8_P	37	SIO9_P	38
SIO8_N	39	SIO9_N	40
GND	41		

Table 2-8 P3 Board to Board Cable Connection to J16 User Signals

Pin Description	Number	Pin Description	Number
DP04_P	1	DP14_P	2
DP04_N	3	DP14_N	4
DP05_P	5	DP15_P	6
DP05_N	7	DP15_N	8
DP06_P	9	DP16_P	10
DP06_N	11	DP16_N	12
DP07_P	13	DP17_P	14
DP07_N	15	DP17_N	16
DP18_P	17	DP19_P	18
DP18_N	19	DP19_N	20
SIO10_P	21	SIO11_P	22
SIO10_N	23	SIO11_N	24
SIO12_P	25	SIO13_P	26
SIO12_N	27	SIO13_N	28
SIO14_P	29	SIO15_P	30
SIO14_N	31	SIO15_N	32
SIO16_P	33	SIO18_GCLK_P	34
SIO16_N	35	SIO18_GCLK_N	36
SIO17_P	37	NC[1]	38
SIO17_N	39	NC[1]	40
GND	41		

Notes (Table 2-8):

1. NC – Not Connected

Table 2-9 P4 Fan Power

Pin Description	Number	Pin Description	Number
GND	1	+12V	2
NC[1]	3		

Notes (Table 2-9):

1. NC – Not Connected

Table 2-10 P5 Programming Connector

Pin Description	Number	Pin Description	Number
NC[1]	1	VREF	2
GND	3	TMS	4
GND	5	TCK	6
GND	7	TDO	8
GND	9	TDI	10
GND	11	NC[1]	12
NC[1]	13	NC[1]	14

Notes (Table 2-10):

1. NC – Not Connected

Table 2-11 5025-917 Crossover Cable P2 Connections

Carrier 1 Signal Name	Carrier 1 P2 Pin	Carrier 2 Signal Name	Carrier 2 P2 Pin
DP00_P	1	DP10_P	2
DP00_N	3	DP10_N	4
DP01_P	5	DP11_P	6
DP01_N	7	DP11_N	8
DP02_P	9	DP12_P	10
DP02_N	11	DP12_N	12
DP03_P	13	DP13_P	14
DP03_N	15	DP13_N	16
DP08_P	17	DP09_P	18
DP08_N	19	DP09_N	20
SIO0_GCLK_P	21	SIO1_P	22
SIO0_GCLK_N	23	SIO1_N	24
SIO2_P	25	SIO3_P	26
SIO2_N	27	SIO3_N	28
SIO4_P	29	SIO5_P	30
SIO4_N	31	SIO5_N	32
SIO6_P	33	SIO7_P	34
SIO6_N	35	SIO7_N	36
SIO8_P	37	SIO9_P	38
SIO8_N	39	SIO9_N	40
GND	41	GND	41
DP10_P	2	DP00_P	1
DP10_N	4	DP00_N	3
DP11_P	6	DP01_P	5
DP11_N	8	DP01_N	7
DP12_P	10	DP02_P	9
DP12_N	12	DP02_N	11
DP13_P	14	DP03_P	13
DP13_N	16	DP03_N	15
DP09_P	18	DP08_P	17
DP09_N	20	DP08_N	19
SIO1_P	22	SIO0_GCLK_P	21
SIO1_N	24	SIO0_GCLK_N	23
SIO3_P	26	SIO2_P	25
SIO3_N	28	SIO2_N	27
SIO5_P	30	SIO4_P	29
SIO5_N	32	SIO4_N	31
SIO7_P	34	SIO6_P	33
SIO7_N	36	SIO6_N	35
SIO9_P	38	SIO8_P	37
SIO9_N	40	SIO8_N	39

Table 2-12 5025-917 Crossover Cable P3 Connections

Carrier 1 Signal Name	Carrier 1 P3 Pin	Carrier 2 Signal Name	Carrier 2 P3 Pin
DP04_P	1	DP14_P	2
DP04_N	3	DP14_N	4
DP05_P	5	DP15_P	6
DP05_N	7	DP15_N	8
DP06_P	9	DP16_P	10
DP06_N	11	DP16_N	12
DP07_P	13	DP17_P	14
DP07_N	15	DP17_N	16
DP18_P	17	DP19_P	18
DP18_N	19	DP09_N	20
SIO10_P	21	SIO11_P	22
SIO10_N	23	SIO11_N	24
SIO12_P	25	SIO13_P	26
SIO12_N	27	SIO13_N	28
SIO14_P	29	SIO15_P	30
SIO14_N	31	SIO15_N	32
SIO16_P	33	SIO18_GCLK_P	34
SIO16_N	35	SIO18_GCLK_N	36
SIO17_P	37	NC[1]	38
SIO17_N	39	NC[1]	40
GND	41	GND	41
DP14_P	2	DP04_P	1
DP14_N	4	DP04_N	3
DP15_P	6	DP05_P	5
DP15_N	8	DP05_N	7
DP16_P	10	DP06_P	9
DP16_N	12	DP06_N	11
DP17_P	14	DP07_P	13
DP17_N	16	DP07_N	15
DP19_P	18	DP18_P	17
DP19_N	20	DP18_N	19
SIO11_P	22	SIO10_P	21
SIO11_N	24	SIO10_N	23
SIO13_P	26	SIO12_P	25
SIO13_N	28	SIO12_N	27
SIO15_P	30	SIO14_P	29
SIO15_N	32	SIO14_N	31
SIO18_GLCK_P	34	SIO16_P	33
SIO18_GCLK_N	36	SIO16_N	35
NC[1]	38	SIO17_P	37

Carrier 1 Signal Name	Carrier 1 P3 Pin	Carrier 2 Signal Name	Carrier 2 P3 Pin
NC[1]	40	SIO17_N	39

Notes (Table 2-12):

1. NC – Not Connected

PCI Express Bus Connections

Table 2-13 indicates the pin assignments for the PCIe bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. "B" is on the component side of the carrier board while "A" is on the solder side. Connector "gold finger" numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals.

Table 2-13 PCIe Bus P1 CONNECTIONS

Signal	Pin	Pin	Signal
+12V	B01	A01	PRSNT*
+12V	B02	A02	+12V
+12V	B03	A03	+12V
GND	B04	A04	GND
SMCLK	B05	A05	***TCK***
SMDAT	B06	A06	***TDI***
GND	B07	A07	***TDO***
+3.3V	B08	A08	***TMS***
TRST*	B09	A09	+3.3V
+3.3Vaux	B10	A10	+3.3V
WAKE*	B11	A11	PERST*
RSVD	B12	A12	GND
GND	B13	A13	REFCLKp
PET0p	B14	A14	REFCLKn
PET0n	B15	A15	GND
GND	B16	A16	PER0p
PRSNTx1*	B17	A17	PER0n
GND	B18	A18	GND
PET1p	B19	A19	***RSVD***
PET1n	B20	A20	GND
GND	B21	A21	PER1p
GND	B22	A22	PER1n
PET2p	B23	A23	GND
PET2n	B24	A24	GND

Signal	Pin	Pin	Signal
GND	B25	A25	PER2p
GND	B26	A26	PER2n
PET3p	B27	A27	GND
PET3n	B28	A28	GND
GND	B29	A29	PER3p
RSVD	B30	A30	PER3n
PRSNTx4*	B31	A31	GND
GND	B32	A32	GND
PET4p	B33	A33	***RSVD***
PET4n	B34	A34	***RSVD***
GND	B35	A35	PER4p
GND	B36	A36	PER4n
PET5p	B37	A37	GND
PET5n	B38	A38	GND
GND	B39	A39	PER5p
GND	B40	A40	PER5n
PET6p	B41	A41	GND
PET6n	B42	A42	GND
GND	B43	A43	PER6p
GND	B44	A44	PER6n
PET7p	B45	A45	GND
PET7n	B46	A46	GND
GND	B47	A47	PER7p
PRSNTx8*	B48	A48	PER7n
GND	B49	A49	GND

Notes (Table 2-13):

1. Asterisk (*) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.

FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each XMC module. This provides maximum filtering and signal decoupling between the XMC modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the PCIe bus and the XMC module power supply returns. Therefore, unless isolation is provided on the XMC module itself, the field I/O connections are not isolated from the PCIe bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the XMC input/output modules.

3. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 0, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

Application Notes

Frequently Asked Questions (FAQ’s)

Product Knowledge Base

Tutorials

Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

4. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length .....12.283 inches (312.0 mm)
Height.....4.200 inches (106.68 mm)
Width .....occupies 2 slots with fan installed (fan is mounted on solder side, height is 10 mm),
occupies 1 slot with fan removed

Connectors

P1 .....PCI Express V1.1 x8 lanes card edge
J3 .....Auxiliary power connector (PCIe Graphics)
P4 .....Fan Power
P5 .....JTAG (Xilinx programming adapter)
J14 and J16 .....XMC user signals (Rear I/O)
J15.....XMC PCIe signals
P2 and P3 .....board to board cable connection to XMC J16 user signals
J1 .....board to board cable connection to XMC J14 user signals

Jumpers

JP1.....Power source selection, PCIe card edge or PCIe graphics power connector
JP2.....JTAG I/O voltage selection, +3.3 or +2.5 Volts

Power

Board power requirements are a function of the installed XMC module. This specification lists currents for the carrier board only. The carrier board provides +3.3V, +12V and -12V power to the XMC module. +12V power can be supplied either from the PCIe bus +12V supply or from the PCIe graphics power connector. The +12V power source for the XMC module is selected by jumper J1. The DC/DC converter generates the -12V supply from the selected +12V source. Note that the maximum amount of current provided to the carrier card via the PCIe bus varies with each system. Refer to your system documentation for more information on PCIe power specifications.

Currents specified are for the carrier board only for Model APCe8675, add the XMC module currents for the total current required from each supply.

+3.3 Volts .....0 mA
+12 Volts .....300 mA max with fan operating

PCIe BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI Express specifications per revision 1.1 dated March 28, 2005. Note: PCIe Gen 2 signal rates exceed the rated bandwidth of the XMC connectors.

ENVIRONMENTAL

Operating Temperature.....0 to +70°C
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C
Non-Isolated .....The PCIe bus and the XMC module commons have a direct electrical connection. As such unless the XMC module provides isolation between the logic and user I/O signals, the user I/O signals are not isolated from the PCIe bus.

Electromagnetic Compatibility

Immunity per EN 61000-6-2:

Electrostatic Discharge Immunity..IEC6100-4-2
Radiated Field Immunity.....IEC61000-4-4
Electric Fast Transient Immunity ...IEC61000-4-4
Surge Immunity.....IEC 61000-4-5
Conducted R F Immunity IEC6100-4-6

Emissions per EN 61000-6-4:

Enclosure Port.....per CISPR 16
Low Voltage AC Mains Port .....per CISPR 16
Telecom / Network Port .....per CISPR 22

WARNING: This is a Class A product. In a domestic environment, this product may cause radio interference in which the user may be required to take adequate measures.

AGENCY APPROVALS

Electromagnetic Compatibility (EMC):

EMC Directive 2004/108/EC.

Federal Communications Commission (FCC):

FCC PART 15, Class A.

Certificate of Volatility

Certificate of Volatility				
Acromag Model APCe8675	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) □ Yes ■ No				
Acromag Representative				
Name: Russ Nieves	Title: Dir. Of Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

5. Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
23-AUG-13	A	JCL	Initial Acromag release.
6-SEP-13	B	JCL	Added Certificate of Volatility
12-DEC-13	C	JCL/ARP	Removed P.O. Box from address on cover page. Assigned new numbers to Buy/Resell products: changed F68-11M68-50-1007 to 5025-913; changed HQDP-020-03.00-SBL-STR-2-B to 5025-917.
13-JAN-14	D	JCL	Updated EMC compliance statements in Environmental section.
11-MAR-14	E	JCL	Updated EMC compliance statements. Added radio interference warning. Added Agency approvals section.
22-SEP-14	F	FJM/ARP	Correct model number on Certificate of Volatility.
04-MAY-17	G	CAB/ARP	Correct tables 2-8 and 2-12. Update contact info in COV.
03 AUG 2017	H	CAP/JAA	Removed CE Mark due to non-RoHS compliant part. Refer to ECO # 17G016.

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