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Carrier Card Series

APCe8670 PCI Express Bus PMC Carrier

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1. GENERAL INFORMATION

The APCe8670 card is a Peripheral Component Interconnect Express (PCIe) bus card carrier for a PMC module. The carrier enables the use of PMC mezzanine I/O modules in a standard desktop computer. The carrier card acts as an adapter to bridge between the PCIe bus of your PC and the PCI bus of a PMC module card. Access to PMC P4 rear I/O is provided through connector J6. PMC modules with front I/O can be accessed though the front mounting bracket. A cable is available to connect the J6 rear I/O to a front panel bracket mounted connector located in an adjacent slot.

Model	Board Size (Length)	Operating Temperature Range
APCe8670	9.342 inches	0 to +70°C

KEY APCe8670 FEATURES

PCI Express Carrier: Four PCI Express lanes connect the PCIe bus to the TSI-384 PCIe to PCI bridge.

PCI Features: 32/64 bit addressing, 32/64 bit data bus, 25, 33, 50, and 66 MHz operation, 4KB read completion buffer, up to eight outstanding read requests.

PCI-X Features: 32/64 bit addressing, 32/64 bit data bus, 50, 66, and 100 MHz operation, 4KB read completion buffer, up to eight outstanding read requests.

Removable Fan: For applications that do not require the cooling fan, the fan can be easily removed. With the fan removed the APCe8670 will fit in the space of a single slot.

Rear I/O: 32 differential pairs are routed from the PMC P4 connector to an MD68 (internal SCSI) male connector. With an optional cable, these signals may be connected to a panel mount connector in a PCI card bracket installed in an adjacent slot.

Auxiliary Power Connection: 12 Volt power may be optionally supplied through a PCI express graphics power connector if the PMC card requires more power than what is available from the PCIe card slot.

JTAG Programming Header: The APCe8670 carrier includes a programming connector that mates with a Xilinx programmer for programming Acromag FPGA products. Acromag PMC FPGA boards can be configured to route the JTAG programming signals through the PMC P1 and P2 connectors.

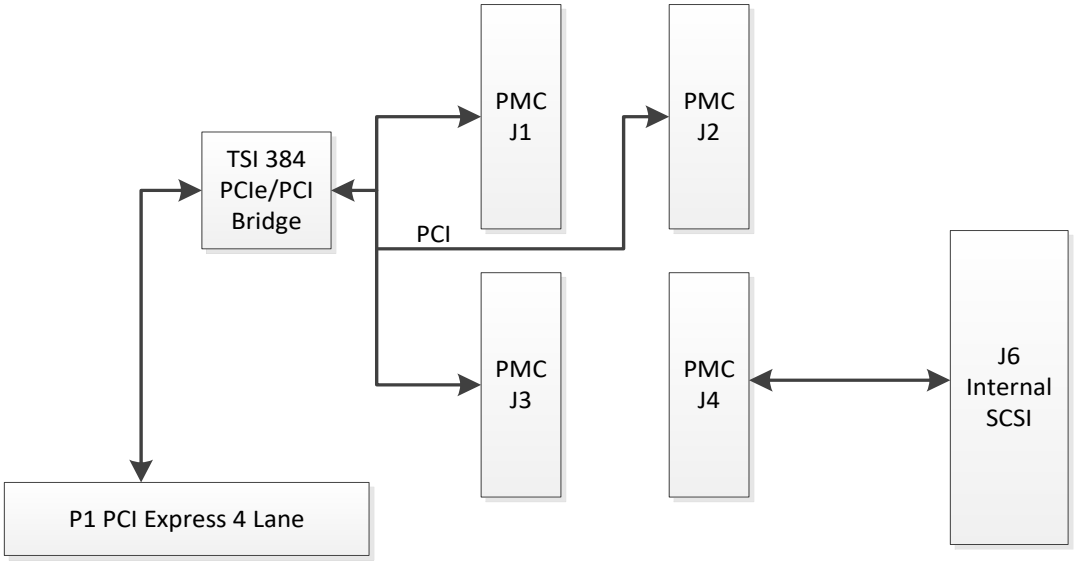


Figure 1 Block Diagram Showing Data Paths

SIGNAL INTERFACE PRODUCTS

Cables

Acromag offers a cable that makes the PMC rear I/O signals accessible from the back panel of a PC. This cable connects J6 to a MD68 connector mounted on a PCI card bracket. The Acromag part number is 5025-913.

2. PREPARATION FOR USE

UNPACKING AND INSPECTION



Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the

board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed PMC module, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Board Configuration

Power should be removed from the board when changing jumper configurations or when installing a PMC module, cables and field wiring.

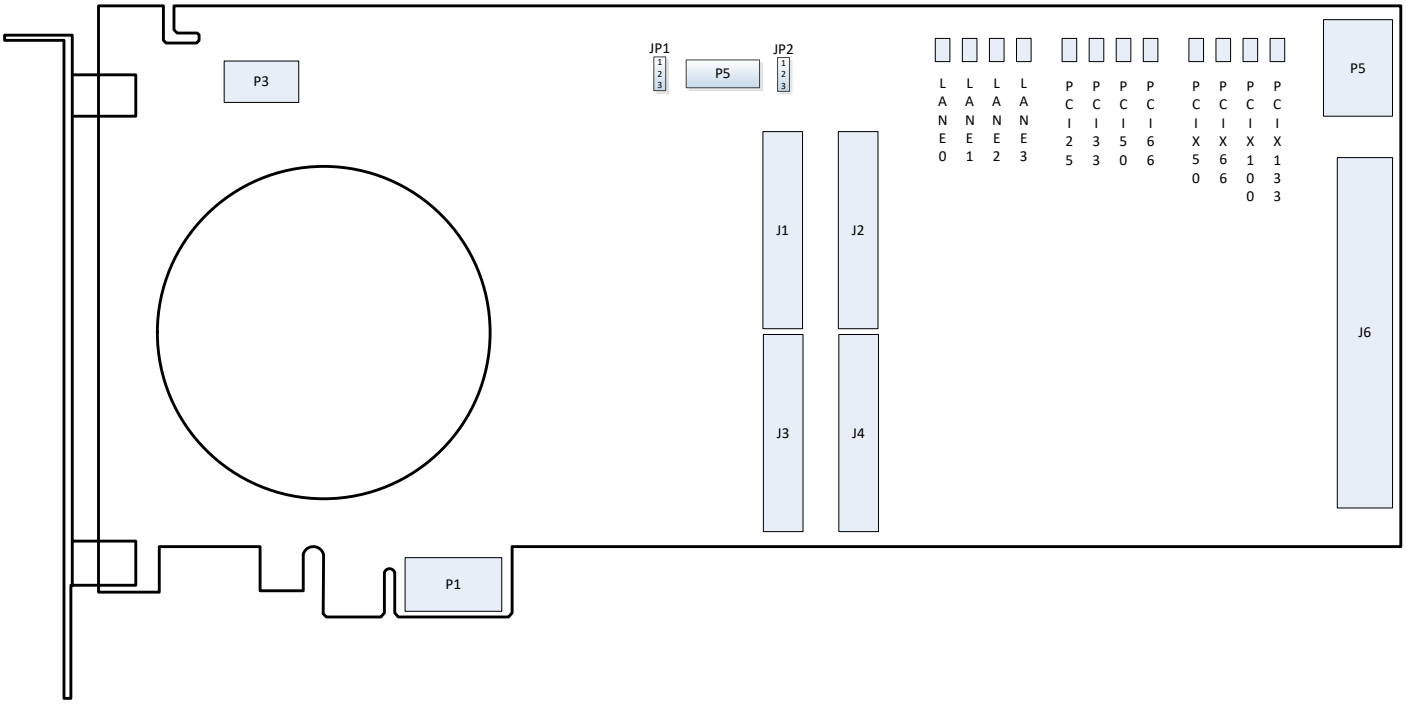


Figure 2 Connector and Status Indicator Location

JUMPERS

Refer to Figure 2 Connector and Status Indicator Location". Jumper JP1 selects the source of +12 Volt power. The jumper must be present in one of the two configurations for proper board operation.

Table 2-1 JP1 +12V Power Source Select Jumper

Power Source	Jumper Position
PCIe Card Edge	1 - 2
PCIe Graphics Power	2 - 3

Jumper JP2 provides the option to operate the PCI bus clock at a lower frequency. The PCI bus clock frequency is controlled by a combination of the JP2 jumper position, the logic level of the PCI bus M66EN signal and the logic level of the PCI bus PCIXCAP signal (see Table 2-3). For convenience, the PCI bus clock frequency is indicated by LEDs located near the top edge of the board.

Table 2-2 JP2 PCI Clock Frequency Select Jumper

PCI Clock	Jumper Position
25, 50, 100 MHz	1 - 2
33, 66, 133 MHz	2 - 3

Table 2-3 PCI Clock Frequency

PCI Clock Frequency	JP2 Position	M66EN	PCIXCAP
100 MHz	1 - 2	H	H
50 MHz	1 - 2	H	L
25 MHz	1 - 2	L	X
133 MHz[1]	2 - 3	H	H
66 MHz	2 - 3	H	L
33 MHz	2 - 3	L	X

Notes (Table 2-3):

1. Operation at 133 MHz PCI bus clock frequency has not been validated.

STATUS INDICATORS

LED indicators located at the top edge of the board display the status of the PCIe lanes, the PCI bus operating mode, and the clock frequency (see Figure 2). The PCIe lane status LEDs report the number for active lanes x1, x2, or x4. The remaining LEDs report the PCI bus mode and clock frequency. Only one of these LEDs will be lit to indicate the current operating state.

CONNECTORS

Refer to Figure 2 Connector and Status Indicator Location". The APCe8670 carrier provides the following connectors:

J1, J2 and J3.....PMC PCI/X signals
J4.....PMC user signals (Rear I/O)
J5.....auxiliary power connector (PCIe graphics)
J6.....cable connection to J14 user signals
P1.....PCI Express v1.1 x4 lanes card edge
P3.....fan power
P4.....JTAG (Xilinx programming adapter)

Table 2-4 J1 PMC PCI/X signals Connector

Pin Description	Number	Pin Description	Number
TCK	1	-12V	2
GND	3	INTA#	4
INTB#	5	INTC#	6
BUSMODE1#	7	+5V	8
INTD#	9	NC[1]	10
GND	11	+3.3VAUX	12
CLK	13	GND	14
GND	15	GNT#	16
REQ#	17	+5V	18
+3.3V	19	AD31	20
AD28	21	AD27	22
AD25	23	GND	24
GND	25	C/BE3#	26
AD22	27	AD21	28
AD19	29	+5V	30
+3.3V	31	AD17	32
FRAME#	33	GND	34
GND	35	IRDY#	36
DEVSEL#	37	+5V	38
PCIXCAP	39	LOCK#	40
NC[1]	41	NC[1]	42
PAR	43	GND	44
+3.3V	45	AD15	46
AD12	47	AD11	48
AD9	49	+5V	50
GND	51	C/BE0#	52
AD6	53	AD5	54
AD4	55	GND	56
+3.3V	57	AD3	58
AD2	59	AD1	60
AD0	61	+5V	62
GND	63	REQ64#	64

Notes (Table 2-4):

1. NC – Not Connected

Table 2-5 J2 PMC PCI/X signals Connector

Pin Description	Number	Pin Description	Number
+12V	1	TRST#	2
TMS	3	TDO	4
TDI	5	GND	6
GND	7	NC[1]	8
NC[1]	9	NC[1]	10
BUSMODE2#	11	+3.3V	12
RST#	13	BUSMODE3#	14
+3.3V	15	BUSMODE4#	16
PME#	17	GND	18
AD30	19	AD29	20
GND	21	AD26	22
AD24	23	+3.3V	24
IDSEL	25	AD23	26
+3.3V	27	AD20	28
AD18	29	GND	30
AD16	31	C/BE2#	32
GND	33	NC[1]	34
TRDY#	35	+3.3V	36
GND	37	STOP#	38
PERR#	39	GND	40
+3.3V	41	SERR#	42
C/BE1#	43	GND	44
AD14	45	AD13	46
M66EN	47	AD10	48
AD8	49	+3.3V	50
AD7	51	NC[1]	52
+3.3V	53	NC[1]	54
NC[1]	55	GND	56
NC[1]	57	NC[1]	58
GND	59	NC[1]	60
ACK64#	61	+3.3V	62
GND	63	NC[1]	64

Notes (Table 2-5):

1. NC – Not Connected

Table 2-6 J3 PMC PCI/X signals Connector

Pin Description	Number	Pin Description	Number
NC[1]	1	GND	2
GND	3	C/BE7#	4
C/BE6#	5	C/BE5#	6
C/BE4#	7	GND	8
+3.3V	9	PAR64	10
AD63	11	AD62	12
AD61	13	GND	14
GND	15	AD60	16
AD59	17	AD58	18
AD57	19	GND	20
+3.3V	21	AD56	22
AD55	23	AD54	24
AD53	25	GND	26
GND	27	AD52	28
AD51	29	AD50	30
AD49	31	GND	32
GND	33	AD48	34
AD47	35	AD46	36
AD45	37	GND	38
+3.3V	39	AD44	40
AD43	41	AD42	42
AD41	43	GND	44
GND	45	AD40	46
AD39	47	AD38	48
AD37	49	GND	50
GND	51	AD36	52
AD35	53	AD34	54
AD33	55	GND	56
+3.3V	57	AD32	58
NC[1]	59	NC[1]	60
NC[1]	61	GND	62
GND	63	NC[1]	64

Notes (Table 2-6):

1. NC – Not Connected

Table 2-7 J4 PMC Connector User Signals (Rear I/O)

Pin Description	Number	Pin Description	Number
RIO0_GCLK_P	1	RIO1_P	2
RIO0_GCLK_N	3	RIO1_N	4
RIO2_P	5	RIO3_P	6
RIO2_N	7	RIO3_N	8
RIO4_P	9	RIO5_P	10
RIO4_N	11	RIO5_N	12
RIO6_P	13	RIO7_P	14
RIO6_N	15	RIO7_N	16
RIO8_P	17	RIO9_P	18
RIO8_N	19	RIO9_N	20
RIO10_P	21	RIO11_P	22
RIO10_N	23	RIO11_N	24
RIO12_P	25	RIO13_P	26
RIO12_N	27	RIO13_N	28
RIO14_P	29	RIO15_P	30
RIO14_N	31	RIO15_N	32
RIO16_P	33	RIO17_P	34
RIO16_N	35	RIO17_N	36
RIO18_P	37	RIO19_P	38
RIO18_N	39	RIO19_N	40
RIO20_P	41	RIO21_P	42
RIO20_N	43	RIO21_N	44
RIO22_P	45	RIO23_P	46
RIO22_N	47	RIO23_N	48
RIO24_P	49	RIO25_P	50
RIO24_N	51	RIO25_N	52
RIO26_P	53	RIO27_P	54
RIO26_N	55	RIO27_N	56
RIO28_P	57	RIO29_P	58
RIO28_N	59	RIO29_N	60
RIO30_P	61	RIO31_GCLK_P	62
RIO30_N	63	RIO31_GCLK_N	64

Table 2-8 J5 PCIe Graphics Power

Pin Description	Number	Pin Description	Number
+12V_AUX	1	+12V_AUX	2
+12V_AUX	3	GND	4
GND	5	GND	6
GND	7	GND	8

Table 2-9 J6 Board to Board Connector (Rear I/O)

Pin Description	Number	Pin Description	Number
RIO0_GCLK_P	1	RIO0_GCLK_N	35
RIO1_P	2	RIO1_N	36
RIO2_P	3	RIO2_N	37
RIO3_P	4	RIO3_N	38
RIO4_P	5	RIO4_N	39
RIO5_P	6	RIO5_N	40
RIO6_P	7	RIO6_N	41
RIO7_P	8	RIO7_N	42
RIO8_P	9	RIO8_N	43
RIO9_P	10	RIO9_N	44
RIO10_P	11	RIO10_N	45
GND	12	GND	46
RIO11_P	13	RIO11_N	47
RIO12_P	14	RIO12_N	48
RIO13_P	15	RIO13_N	49
RIO14_P	16	RIO14_N	50
RIO15_P	17	RIO15_N	51
RIO16_P	18	RIO16_N	52
RIO17_P	19	RIO17_N	53
RIO18_P	20	RIO18_N	54
RIO19_P	21	RIO19_N	55
RIO20_P	22	RIO20_N	56
GND	23	GND	57
RIO21_P	24	RIO21_N	58
RIO22_P	25	RIO22_N	59
RIO23_P	26	RIO23_N	60
RIO24_P	27	RIO24_N	61
RIO25_P	28	RIO25_N	62
RIO26_P	29	RIO26_N	63
RIO27_P	30	RIO27_N	64
RIO28_P	31	RIO28_N	65
RIO29_P	32	RIO29_N	66
RIO30_P	33	RIO30_N	67
RIO31_GCLK_P	34	RIO31_GCLK_N	68

Table 2-10 P3 Fan Power

Pin Description	Number	Pin Description	Number
GND	1	+12V	2
NC[1]	3		

Notes (Table 2-10):

1. NC – Not Connected

Table 2-11 P4 Programming Connector

Pin Description	Number	Pin Description	Number
NC[1]	1	VREF	2
GND	3	TMS	4
GND	5	TCK	6
GND	7	TDO	8
GND	9	TDI	10
GND	11	NC[1]	12
NC[1]	13	NC[1]	14

Notes (Table 2-11):

1. NC – Not Connected

PCI Express Bus Connections

Table 2-12 indicates the pin assignments for the PCIe bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. "B" is on the component side of the carrier board while "A" is on the solder side. Connector "gold finger" numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals.

Table 2-12 P1 PCIe Bus Connector

Signal	Pin	Pin	Signal
+12V	B01	A01	PRSNT*
+12V	B02	A02	+12V
+12V	B03	A03	+12V
GND	B04	A04	GND
SMCLK	B05	A05	***TCK***
SMDAT	B06	A06	***TDI***
GND	B07	A07	***TDO***
+3.3V	B08	A08	***TMS***
TRST*	B09	A09	+3.3V
+3.3Vaux	B10	A10	+3.3V
WAKE*	B11	A11	PERST*
RSVD	B12	A12	GND
GND	B13	A13	REFCLKp
PET0p	B14	A14	REFCLKn
PET0n	B15	A15	GND
GND	B16	A16	PER0p
PRSNTx1*	B17	A17	PER0n
GND	B18	A18	GND
PET1p	B19	A19	***RSVD***
PET1n	B20	A20	GND
GND	B21	A21	PER1p
GND	B22	A22	PER1n
PET2p	B23	A23	GND
PET2n	B24	A24	GND
GND	B25	A25	PER2p
GND	B26	A26	PER2n
PET3p	B27	A27	GND
PET3n	B28	A28	GND
GND	B29	A29	PER3p
RSVD	B30	A30	PER3n
PRSNTx4*	B31	A31	GND
GND	B32	A32	GND

Notes (Table 2-12):

1. Asterisk (*) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.

FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each PMC module. This provides maximum filtering and signal decoupling between the PMC modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the PCIe

bus and the PMC module power supply returns. Therefore, unless isolation is provided on the PMC module itself, the field I/O connections are not isolated from the PCIe bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the PMC input/output modules.

3. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 0, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

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Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

4. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length .....9.342 inches (237.28 mm)
Height.....4.200 inches (106.68 mm)
Width .....occupies 2 slots with fan installed (fan is mounted on solder side, height is 10 mm),
occupies 1 slot with fan removed

Connectors

P1 .....PCI Express V1.1 x4 lanes card edge
P3 .....Fan Power
P4 .....JTAG (Xilinx programming adapter)
J1, J2, J3.....PMC PCI/X signals
J4 .....PMC user signals (Rear I/O)
J5 .....Auxiliary power connector (PCIe Graphics)
J6 .....board to board cable connection to PMC J4 user signals

Jumpers

JP1.....Power source selection, PCIe card edge or PCIe graphics power connector (see Table 2-1)
JP2.....PCI bus clock frequency selection (see Table 2-2)

Power

Board power requirements are a function of the installed PMC module. This specification lists currents for the carrier board only. The carrier board provides +3.3V, +5V, +12V and -12V power to the PMC module. +12V power can be supplied either from the PCIe bus +12V supply or from the PCIe graphics power connector. The +12V power source for the PMC module is selected by jumper JP1. A DC/DC converter generates the +5V and -12V supplies from the selected +12V source. Note that the maximum amount of current provided to the carrier card via the PCIe bus varies with each system. Refer to your system documentation for more information on PCIe power specifications.

Currents specified are for the APCe8670 carrier board only, add the PMC module currents for the total current required from each supply.

+3.3 Volts .....350 mA typical
+3.3V_AUX .....0 mA
+12 Volts .....280 mA maximum with fan operating
140 mA maximum with fan disconnected

PCIe BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI Express specifications per revision 1.1 dated March 28, 2005.

ENVIRONMENTAL

Operating Temperature.....0 to +70°C
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C
Non-Isolated .....The PCIe bus and the PMC module commons have a direct electrical connection. As such unless the PMC module provides isolation between the logic and user I/O signals, the user I/O signals are not isolated from the PCIe bus.

Electromagnetic Compatibility

Immunity per EN 61000-6-2:

Electrostatic Discharge Immunity..IEC6100-4-2
Radiated Field Immunity.....IEC61000-4-4
Electric Fast Transient Immunity ...IEC61000-4-4
Surge Immunity.....IEC 61000-4-5
Conducted R F Immunity IEC6100-4-6

Emissions per EN 61000-6-4:

Enclosure Port.....per CISPR 16
Low Voltage AC Mains Port .....per CISPR 16
Telecom / Network Port .....per CISPR 22

WARNING: This is a Class A product. In a domestic environment, this product may cause radio interference in which the user may be required to take adequate measures.

AGENCY APPROVALS

Electromagnetic Compatibility (EMC):

EMC Directive 2004/108/EC.

Federal Communications Commission (FCC):

FCC PART 15, Class A.

Certificate of Volatility

Certificate of Volatility				
Acromag Model APCe8670	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type (EEPROM, FLASH etc.) EEPROM	Size: 32K bits	User Modifiable Yes	Function: Storage of configuration data for TSI384 bridge	Process to Sanitize: Erase EEPROM by writing commands to EEPROM control register in TSI384 bridge via program running on host processor.
Acromag Representative				
Name: Joseph Primeau	Title: Dir. of Sales and Marketing	Email: jprimeau@acromag.com	Office Phone: 248-295-0823	Office Fax: 248-624-9234

5. Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
23-AUG-13	A	JCL	Initial Acromag release.
18-OCT-13	B	JCL	Added Certificate of Volatility
12-DEC-13	C	JCL/ARP	Removed P.O. Box from address on cover page. Assigned new number to Buy/Resell product: changed F68-11M68-50-1007 to 5025-913.
13-JAN-14	D	JCL	Updated EMC compliance statements in Environmental section. Added detail to Certificate of Volatility.
11-MAR-14	E	JCL	Updated EMC compliance statements. Added radio interference warning. Added Agency approvals section.
4-AUG-2017	F	CAP/ARP	Removed CE Mark due to non-RoHS compliant part. Refer to ECO # 17G016.

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