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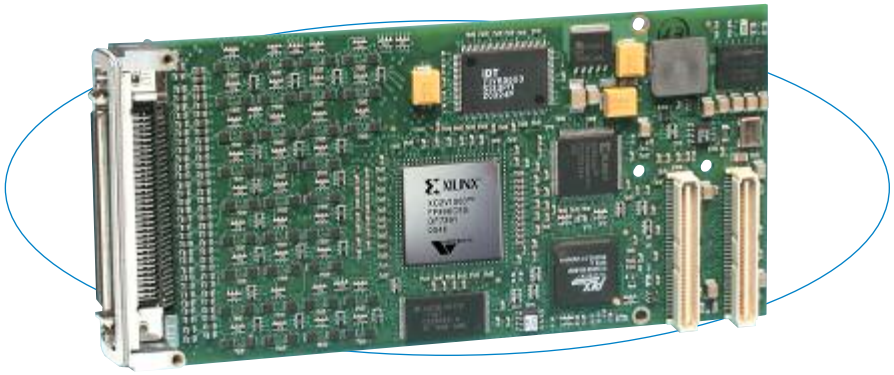
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Find the *Acromag / Xembedded / Xycom PMC-DX2003* at our website: *Click HERE*

Acromag
THE LEADER IN INDUSTRIAL I/O

PMC-DX503/DX2003 Reconfigurable FPGA with TTL and Differential I/O



Download your own logic programs and algorithms into the on-board user-configured FPGA to quickly create a custom digital I/O module.

- PMC-DX503: 24 diff. I/O, 16 TTL I/O, 6,912 logic cells
- PMC-DX2003: 24 diff. I/O, 16 TTL I/O, 24,192 logic cells

(NOTE: Rear I/O models have 23 diff. channels)

PMC-DX503 and PMC-DX2003 modules provide users with the capability to implement complex, customized digital I/O board solutions. Application-specific logic routines and algorithms can be downloaded into the on-board reconfigurable FPGA to control operation of the I/O channels.

These modules are ideal for advanced TTL and differential RS422/485 I/O functions. Typical uses include hardware simulation, in-circuit diagnostics, and communication processing. Modules are able to generate recipe-based responses to input stimulus and to translate communication protocols.

Powerful and versatile, these PMC modules are designed around a reconfigurable FPGA, the Xilinx® Virtex®-II. The PMC-DX503 has the 6,912 logic cell package, while the PMC-DX2003 uses the 24,192 logic cell version. Both DSP-capable FPGAs feature versatile logic resources, large on-chip memories, and a high-speed interface.

The PCI bus interface is handled by a PLX® PCI 9056 device which provides 32-bit 66MHz bus mastering with dual-channel DMA support.

Features

- 16 bi-directional TTL I/O lines
  24 bi-directional RS422/485 differential I/O lines
- Front or rear I/O connection
- Customizable FPGA with 6,912 or 24,192 logic cells (Xilinx Virtex-II XC2V500 or XC2V2000)
- FPGA code loads from PCI bus or flash memory
- 256K x 36-bit SRAM memory
- Supports dual DMA channel data transfer to CPU
- Supports both 5V and 3.3V signalling
- Extended temperature option (-40 to 85°C)

Specifications

FPGA

FPGA: Xilinx Virtex-II FPGA
PMC-DX503: XC2V500 FPGA with 6,912 logic cells
PMC-DX2003: XC2V2000 FPGA with 24,192 logic cells

FPGA configuration: Downloadable via PCI bus or from flash memory.

Example FPGA program: VHDL provided implements interface to PCI bus IC, interface to SRAM, PLL control, and digital I/O control. Program requires user proficiency with Xilinx software tools. See Engineering Design Kit.

Differential Digital I/O

I/O channel configuration: 24 bidirectional differential signals (rear I/O models have 23 channels). Direction is controlled independently.

Differential driver output voltage with 50 ohm load: 2V minimum, 5V maximum.

Common mode output voltage: 3V maximum:

Minimum input resistance: 12K ohms.

Termination resistors: 120 ohm termination resistor networks are installed in sockets.

TTL Digital I/O

I/O channel configuration: 16 bidirectional TTL transceivers with direction controlled as signal pairs.

Reset/power-up condition: All channels default to input.

Digital Input

Input voltage range: 0 to 5V DC.

Input signal threshold, low to high: 3.5V typical.

Input signal threshold, high to low: 1.5V typical.

Input response time: 10 nanoseconds, typical.

Digital Output

Output voltage range: 0 to 5V DC.

Output ON current range: -32 to 32mA.

Output pullups: 4.7K ohm socketed resistors.

Turn on/off time: 10nS.

Input Interrupts

8 channels of interrupts are available for high-to-low, low-to-high, or any change-of-state event type.

PMC Compliance

Conforms to PCI Local Bus Specification, Revision 2.2 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI bus clock frequency: 66MHz.

32-bit PCI Master: Implemented by PLX PCI 9056 device.

Signaling: 5V and 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E versions)
Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: 1,125,663 hrs. at 25°C, MIL-HDBK-217F, Notice 2.

Ordering Information

PMC FPGA Modules *(rear I/O models have 23 diff. chan.)*
PMC-DX503: TTL/differential I/O with 6,912 logic cells
PMC-DX503R: PMC-DX503 except with rear I/O connector

PMC-DX503E: PMC-DX503 with extended temp. range
PMC-DX503RE: PMC-DX503E except w/ rear I/O connector

PMC-DX2003: TTL/differential I/O with 24,192 logic cells
PMC-DX2003R: PMC-DX2003 except w/ rear I/O connector

PMC-DX2003E: PMC-DX2003 with extended temp. range
PMC-DX2003RE: PMC-DX2003E except w/ rear I/O connector

Accessories *(see accessories documentation for details)*
5025-288: Termination panel, SCSI-3 connector, 68 screw terminals
5028-432: Cable, shielded, SCSI-3 connector both ends

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