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VPX4500/CC 3U AcroPack Carrier

USER'S MANUAL

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1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

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Radio Frequency Interference Statement

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

VPX4500E/CC-LF Overview

The VPX4500 is a 3U VPX carrier for Acromag AcroPack (AP) mezzanine board modules. The carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. AP modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with AP modules may replace several dedicated function VPX boards. The VPX4500 carrier board provides impressive functionality at low cost.

Model VPX4500E-LF is an air-cooled product that supports three AcroPack sites. Two of the sites provide field I/O connections through front panel mounted 50 pin shielded connectors. The third site provides field I/O connections through the VPX backplane.

Model VPX4500-CC-LF is a conduction-cooled product that supports three AcroPack sites. Two of the sites provide field I/O connections through 50 pin ribbon cable connectors. The third site provides field I/O connections to the VPX backplane.

Model VPX4500-RTM-LF is a rear transition module used with both the VPX4500-E-LF and the VPX4500-CC-LF carriers to provide access to the slot C AcroPack field I/O signals.

Model	Supported AP Slots	Operating Temperature Range
VPX4500E-LF	3(A,B,C)	-40 to +85°C
VPX4500-CC-LF	3(A,B,C)	-40 to +85°C
VPX4500-RTM-LF		-40 to +85°C

KEY FEATURES

VPX Profile: - 3U SLOT3-PER-1F-14.3.2 provides a PCIe bus interface to control and communicate with industry standard AP modules.

Interface for AcroPack Modules – The VPX4500 provides an electrical and mechanical interface for up to three AcroPack modules. AcroPack Modules (AP) are available from Acromag in a wide variety of input/output configurations to meet the needs of varied applications.

PCI Express Version 2.1 Compliant Carrier: - Includes a PCIe switch to allow three PCIe devices (AcroPack or mini-PCIe) to share a single slot in a 3U VPX chassis**.** The PCIe switch connects to the VPX backplane via four Gen 2 PCIe lanes.

Board Identification – A unique carrier and site number are set for each AcroPack site. This feature provides the capability to distinguish a particular AcroPack module from others when multiple instances of the same module are used in a system.

JTAG Programming Header – A standard 14-pin Xilinx JTAG programming header is provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the three AcroPack modules are daisy-chained.

Individually Fused Power - Fused +1.5V, +3.3V, +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each AcroPack module. Fuses F1-F3, F6-F8 and F11-F13 are user replaceable (see Figure 3). Fuses F4, F5, F9, F10, F14 and F15 are not user replaceable, you must return the board to Acromag to replace these fuses.

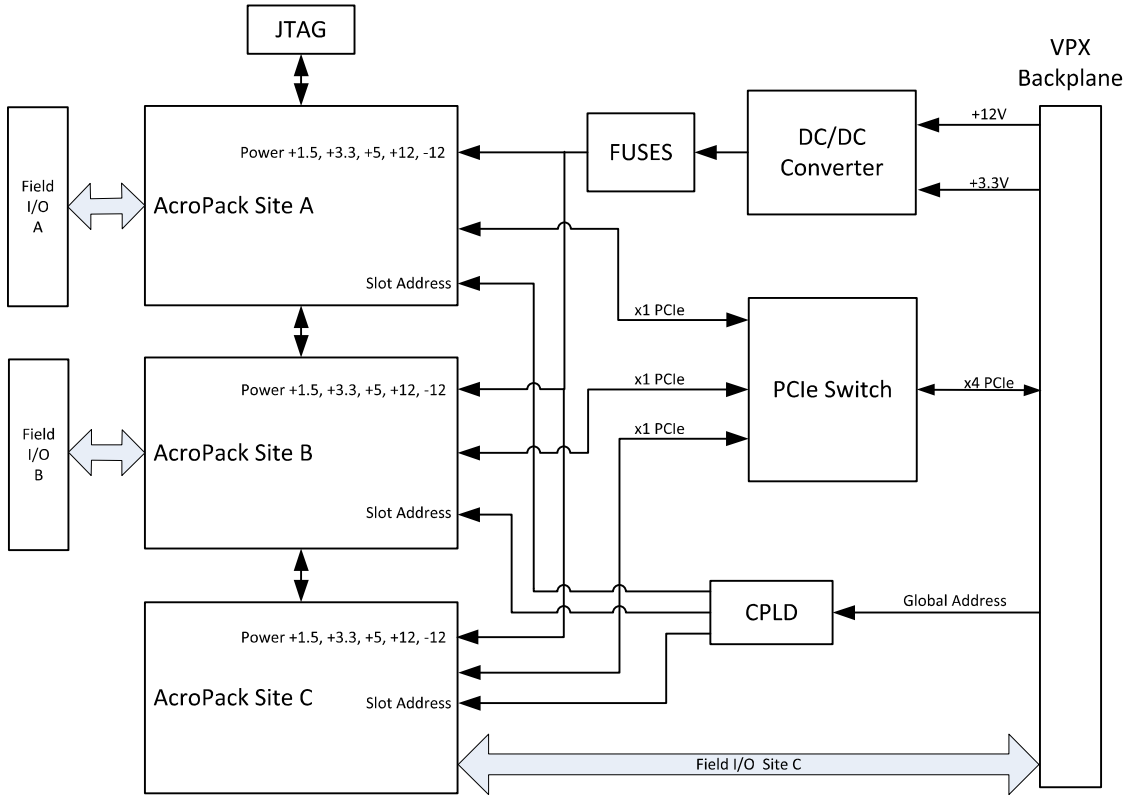


Figure 1 VPX4500 Block Diagram

SIGNAL INTERFACE PRODUCTS

This AP carrier board will mate directly to all AP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual AP modules):

VPX4500E-LF and VPX4500-RTM-LF Cables

For connecting to the two front panel connectors on the VPX4500E-LF and to the VPX4500-RTM-LF: Model 5028-372 Round cable, shielded, SCSI-2 to CHAMP 0.8mm, 2 meters long.

Termination Panel

Model 5028-378: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to carrier boards, via round 50-pin shielded cable (Model 5028-372).

VPX-4500-CC-LF Cables

For connecting to the VPX4500CC-LF slots A and B: Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin

cable with female connectors at both ends for connecting carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

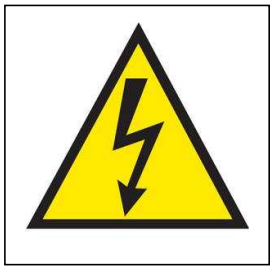
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS





It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

WARNING: This AcroPack carrier does not provide isolation between the AcroPack Field I/O signals and the host. It is not intended to be used with isolated AcroPack modules.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

Power and Cooling Considerations

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements

of the carrier board, plus the installed AcroPack modules within the voltage tolerances specified.

CAUTION: Acromag has used pins labeled as reserved in the Mini-PCIe specification for additional power connections. If you are installing a Mini-PCIe card from another manufacturer remove fuses F1, F2 and F3 for slot A, fuses F6, F7 and F8 for slot B, or F11, F12, and F13 for slot C.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis could be a cause for some concern. Most, if not all computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the AcroPack modules to the carrier board alone results in elevated module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Board Configuration

Board configuration consists of selecting the source of the PCIe reference clock and the source of power for the System Management bus components.

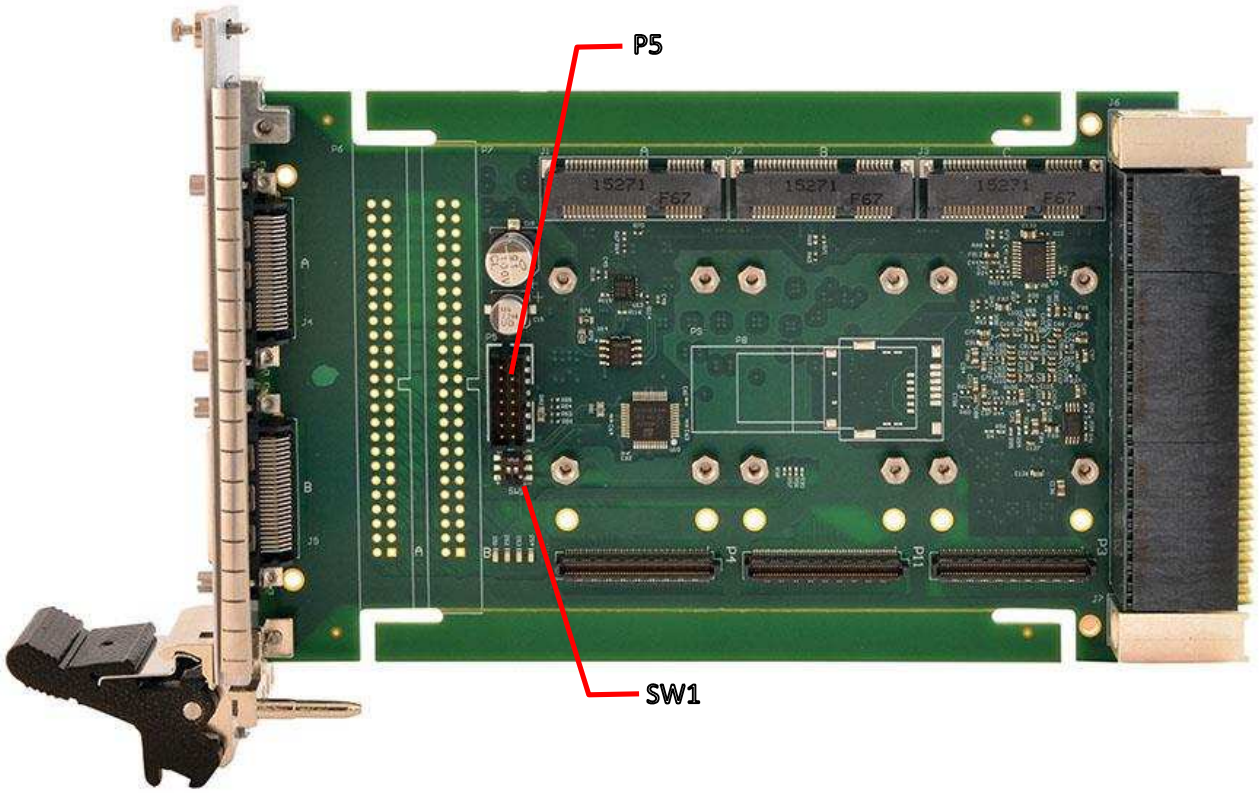


Figure 2 Switch and JTAG Connector Location

Switch SW1 is located on the top side of the board as shown in Figure 2. It contains two switches. It selects the PCIe reference clock source and the source of power for the system management bus devices. Table 1 details the function of the switches.

Table 1 Switch SW1 Functions

Function	Switch location	Switch Position Up	Switch Position Down
SM bus device power source select	right	+3.3 V	+3.3V Aux
PCIe reference clock source select	left	VPX Backplane	On-board oscillator

ACROPACK MODULE INSTALLATION

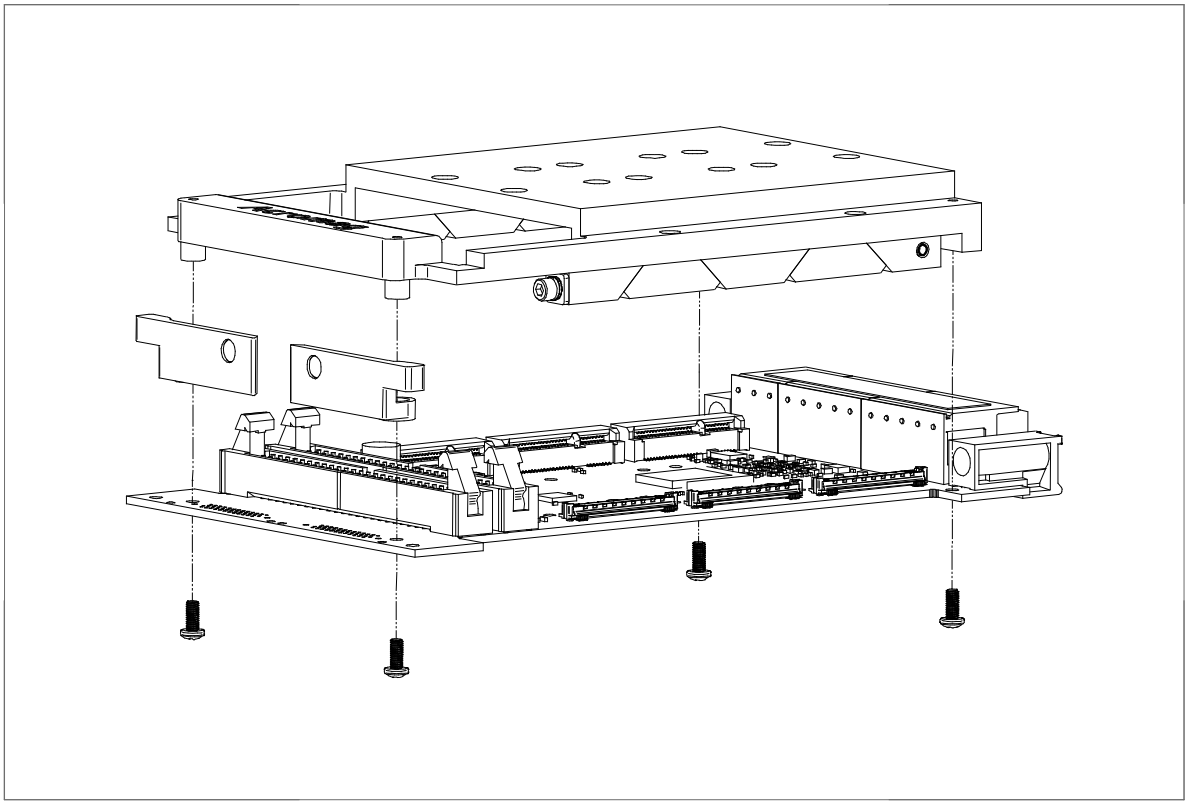
Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring.

AcroPack Module and Heatsink Installation

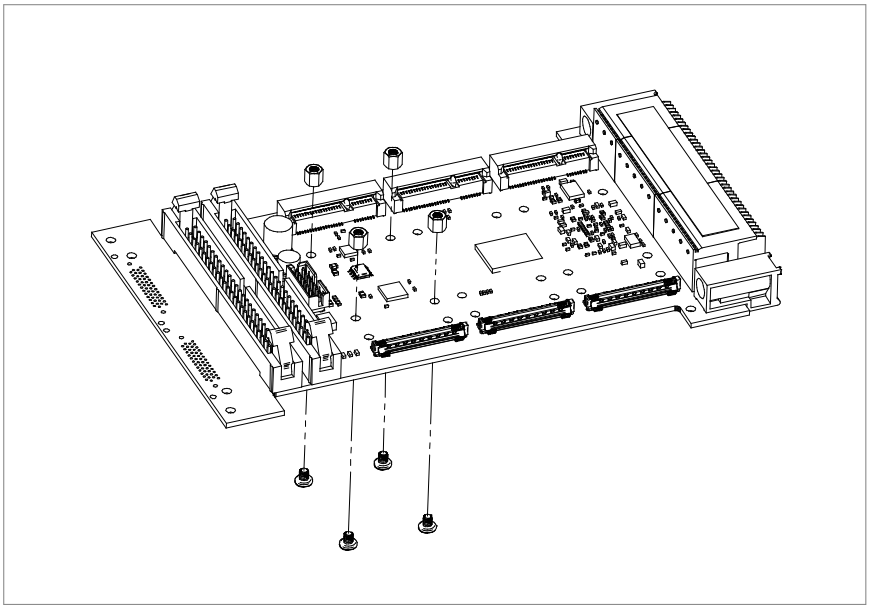
The VPX 4500 carriers support three sites for AcroPack modules. A heatsink is required for each AcroPack module installed on the conduction cooled VPX4500-CC-LF carrier. A heatsink may be necessary on some AcroPack modules installed on the air-cooled VPX4500E-LF carrier in order to extend the upper temperature limit. Refer to the users' manuals of the AcroPack modules you plan to install to determine if this is the case. The AP-CC-01 is a heatsink kit for AcroPack modules.

These instructions will guide you in the installation of the AcroPack module and the heatsink kit. The instructions show the conduction cooled version of the carrier. The installation process for the air cooled carrier is similar, just skip steps 1, 5 and 6 (note: if an AP-CC-01 heatsink is not needed, only two standoffs are used).

Step 1: Remove the 4 (M2.5 x 6mm) pan head screws that secure the conduction heatsink to the VPX4500 board. Remove the VPX4500 Conduction Cooled Heatsink and handles.

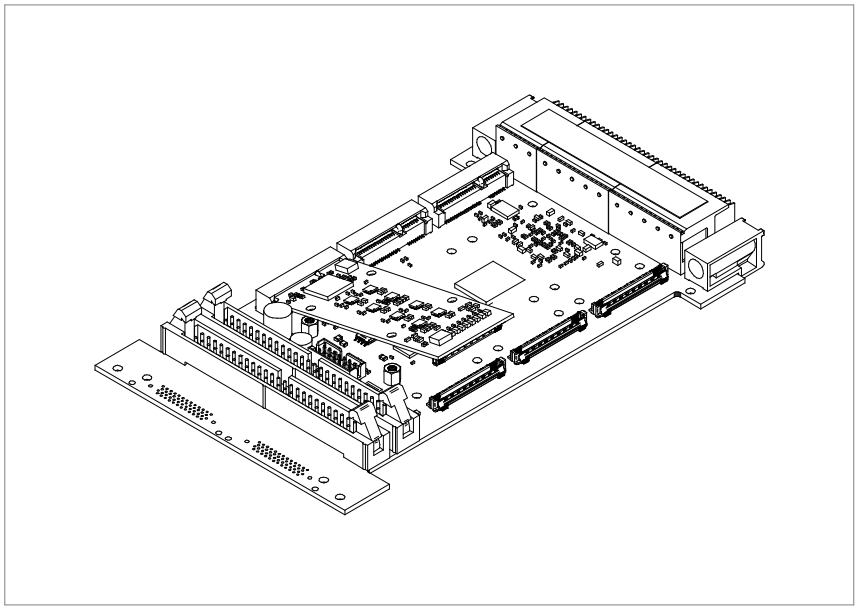


Step 2: Install the 4 (M2.5 x 4.5mm) standoffs as shown



Step 3: Insert the gold card edge finger end of the AcroPack module into the right angle carrier socket.

Make sure connector alignment is correct before carefully pressing the opposite end of the AcroPack module down to seat the bottom side connector into the vertical carrier socket.



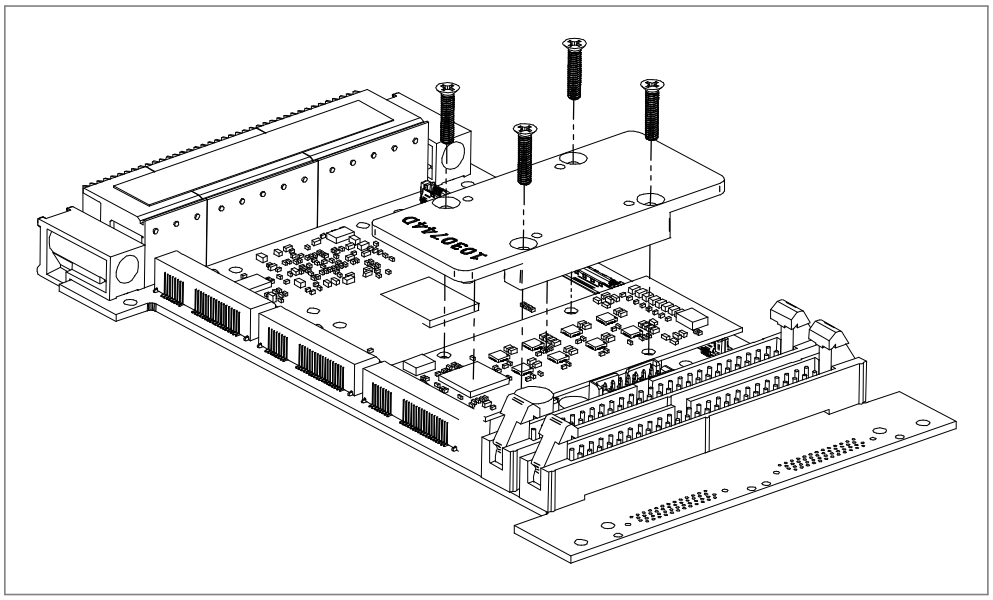
Step 4: Place the heatsink onto the AcroPack Module as shown.

NOTE: See the orientation of the part number on the AcroPack Heatsink.

The Heatsink Conduction Pad must come in contact with the large IC on the AcroPack module.

Secure with 4 (M2.5 x 12mm) Flat head screws.

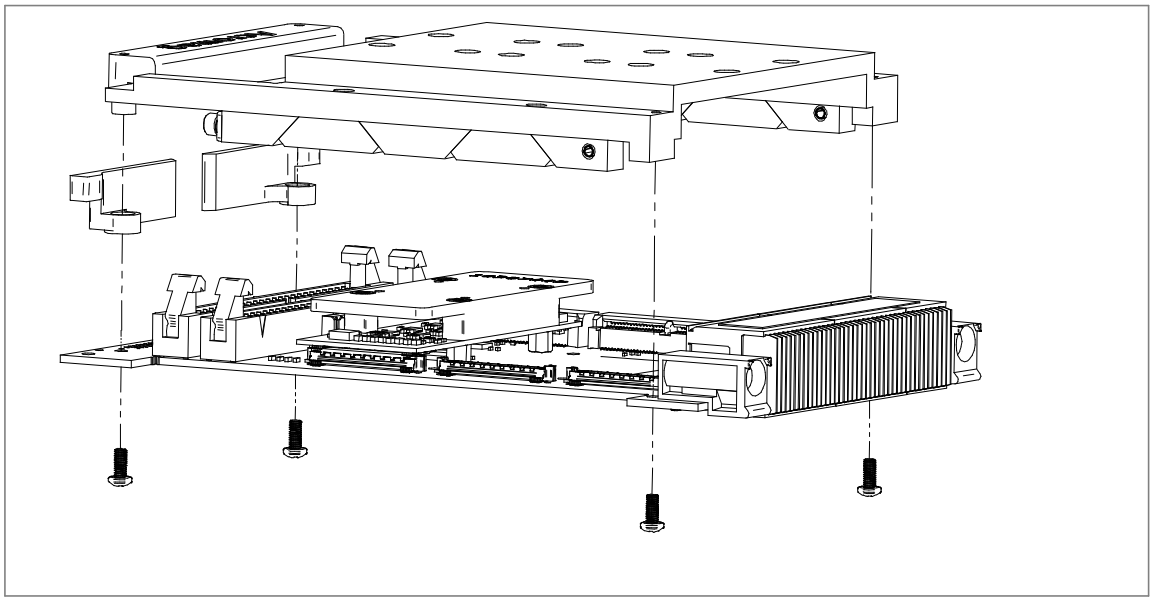
Repeat for each AcroPack module site as needed.



Step 5: Install the right and left Handles as shown.

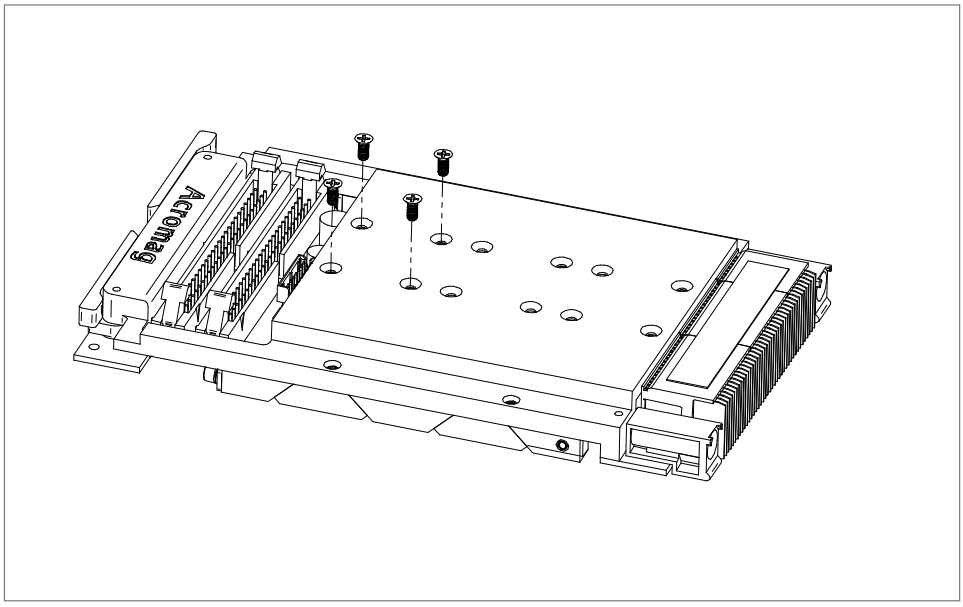
Install the VPX4500 Conduction Cooled Heatsink.

Secure with 4 (M2.5 x 6mm) pan head screws.



Step 6: Install the 4 (M2.5 x 6mm) flat head screws that secure the AcroPack heatsink to the VPX4500 Conduction Cooled Heatsink.

Repeat for each installed AcroPack module.



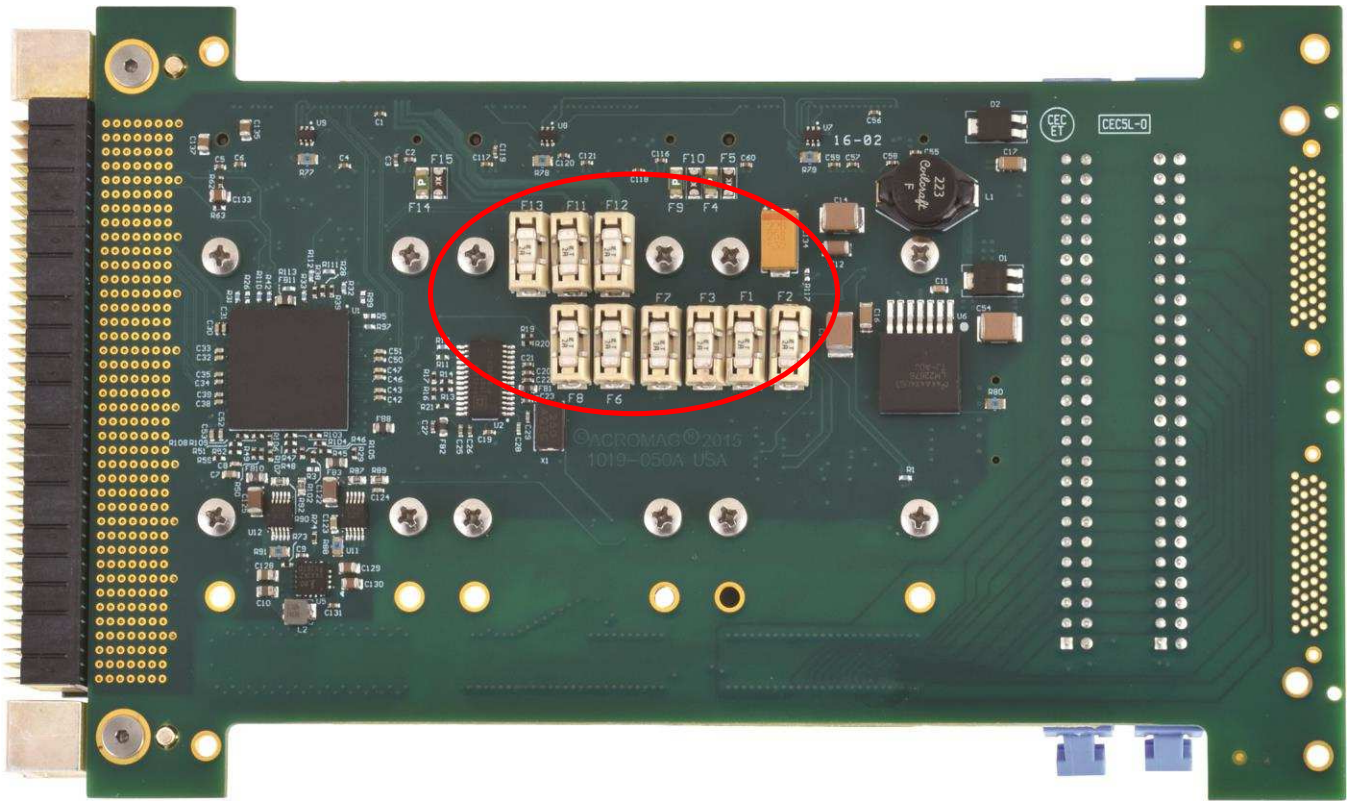


Figure 3 Fuse Locations

FUSE LOCATIONS

Figure 3 shows the view of the bottom side of the carrier board with the replaceable fuses circled in red. Table 2 shows the reference designators corresponding to the AcroPack slot and power rail. Fuses F1-F3, F7-F8 and F11-F13 can be removed by the user. These fuses should be removed when installing a Mini-PCIe card form another vendor.

Table 2 Fuse Reference Designators

Slot	-12 V	1.5 V	3.3 V	5 V	12 V
A	F3	F5	F4	F2	F1
B	F8	F10	F9	F7	F6
C	F13	F15	F14	F12	F11

CONNECTORS

Connectors of the VPX4500 carrier consist of three carrier AP module field I/O connectors, three AP module Mini-PCIe connectors, two front field I/O connectors (50 pin champ on VPX4500E-LF, or 50 pin ribbon cable on

VPX4500-CC-LF), a JTAG programming connector, and three VPX backplane connectors. These interface connectors are discussed in the following sections.

Carrier Field I/O Connectors (AP modules A through B)

Field I/O connections are made via 50 pin 3M ribbon cable connectors A, B, C, and D for AP modules in positions A through D. AP module assignment is marked on the board for easy identification (see AP location drawing 4502-135 for physical locations of the AP modules). Flat cable assemblies and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors. Pin assignments are defined by the AP module employed since the pins from the AP module field side correspond identically to the pin numbers of the 50 pin connectors.

Carrier field I/O connectors A through B are 3M Low Profile 50-pin headers (3M P/N P50LE-050P1-R1-DA) and they mate to ejector equipped ribbon cable connectors (P25LE-050S-DA).

AP Site Field I/O Connectors (AP modules A through C)

The field side connectors of AP modules A through C mate to Samtec SS5-50-3.00-L-D-K-TR connectors on the carrier board. AP slot locations are labeled on the board for easy identification. The field I/O signals for slots A and B are routed to front panel mounted connectors J4 and J5 on the VPX4500E model or ribbon cable connectors P6 and P7 on the VPX4500CC model. Slot C field I/O signals are routed to the rear of the carrier to the VPX P2 connector on both the VPX4500 and VPX4500CC models.

The Samtec SS5-50-3.00-L-D-K-TR connectors on the carrier mate to Samtec ST5-50-1.50-L-D-P-TR connectors on the AP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag AP modules) provide additional stability for harsh environments (see ACROPACK MODULE INSTALLATION for assembly details).

Pin assignments for these connectors are made by the specific AP model used.

Table 3 Field I/O Pin Assignments

Carrier J4, J5 and Termination Panel (Champ)	Carrier P6, P7 (Ribbon)	Carrier P2 (VPX)	Carrier P3, P4, P11	Module Pin Number	Field I/O Signal
1	1	A1	2	2	Field I/O 1
26	2	B1	1	1	Field I/O 2
			4	4	Reserved
			3	3	Reserved

Carrier J4, J5 and Termination Panel (Champ)	Carrier P6, P7 (Ribbon)	Carrier P2 (VPX)	Carrier P3, P4, P11	Module Pin Number	Field I/O Signal
2	3	D1	6	6	Field I/O 3
27	4	E1	5	5	Field I/O 4
			8	8	Reserved
			7	7	Reserved
3	5	B2	10	10	Field I/O 5
28	6	C2	9	9	Field I/O 6
			12	12	Reserved
			11	11	Reserved
4	7	E2	14	14	Field I/O 7
29	8	F2	13	13	Field I/O 8
			16	16	Reserved
			15	15	Reserved
5	9	A3	18	18	Field I/O 9
30	10	B3	17	17	Field I/O 10
			20	20	Reserved
			19	19	Reserved
6	11	D3	22	22	Field I/O 11
31	12	E3	21	21	Field I/O 12
			24	24	Reserved
			23	23	Reserved
7	13	B4	26	26	Field I/O 13
32	14	C4	25	25	Field I/O 14
			28	28	Reserved
			27	27	Reserved
8	15	E4	30	30	Field I/O 15
33	16	F4	29	29	Field I/O 16
			32	32	Reserved
			31	31	Reserved
9	17	A5	34	34	Field I/O 17
34	18	B5	33	33	Field I/O 18
			36	36	Reserved
			35	35	Reserved
10	19	D5	38	38	Field I/O 19

Carrier J4, J5 and Termination Panel (Champ)	Carrier P6, P7 (Ribbon)	Carrier P2 (VPX)	Carrier P3, P4, P11	Module Pin Number	Field I/O Signal
35	20	E5	37	37	Field I/O 20
			40	40	Reserved
			39	39	Reserved
11	21	B6	42	42	Field I/O 21
36	22	C6	41	41	Field I/O 22
			44	44	Reserved
			43	43	Reserved
12	23	E6	46	46	Field I/O 23
37	24	F6	45	45	Field I/O 24
			48	48	Reserved
			47	47	Reserved
13	25	A7	50	50	Field I/O 25
38	26	B7	49	49	Field I/O 26
			52	52	Reserved
			51	51	Reserved
14	27	D7	54	54	Field I/O 27
39	28	E7	53	53	Field I/O 28
			56	56	Reserved
			55	55	Reserved
15	29	B8	58	58	Field I/O 29
40	30	C8	57	57	Field I/O 30
			60	60	Reserved
			59	59	Reserved
16	31	E8	62	62	Field I/O 31
41	32	F8	61	61	Field I/O 32
			64	64	Reserved
			63	63	Reserved
17	33	A9	66	66	Field I/O 33
42	34	B9	65	65	Field I/O 34
			68	68	Reserved
			67	67	Reserved
18	35	D9	70	70	Field I/O 35
22	36	E9	69	69	Field I/O 36

Carrier J4, J5 and Termination Panel (Champ)	Carrier P6, P7 (Ribbon)	Carrier P2 (VPX)	Carrier P3, P4, P11	Module Pin Number	Field I/O Signal
			72	72	Reserved
			71	71	Reserved
19	37	B10	74	74	Field I/O 37
44	38	C10	73	73	Field I/O 38
			76	76	Reserved
			75	75	Reserved
20	39	E10	78	78	Field I/O 39
45	40	F10	77	77	Field I/O 40
			80	80	Reserved
			79	79	Reserved
21	41	A11	82	82	Field I/O 41
46	42	B11	81	81	Field I/O 42
			84	84	Reserved
			83	83	Reserved
22	43	D11	86	86	Field I/O 43
47	44	E11	85	85	Field I/O 44
			88	88	Reserved
			87	87	Reserved
23	45	B12	90	90	Field I/O 45
48	46	C12	89	89	Field I/O 46
			92	92	Reserved
			91	91	Reserved
24	47	E12	94	94	Field I/O 47
49	48	F12	93	93	Field I/O 48
			96	96	Reserved
			95	95	Reserved
25	49	A13	98	98	Field I/O 49
50	50	B13	97	97	Field I/O 50
			100	100	Reserved
			99	99	Reserved

AP Site Mini-PCIe Connectors (AP modules A through C)

The AcroPack Mini-PCIe connectors mate to TE Connectivity 1759457-1 connectors on the carrier board. AcroPack locations are labeled on the board for easy identification.

Pin assignments for these connectors are based on the Mini-PCIe specification with the exceptions noted in Table 4.

Table 4 AP Module Mini PCIE Bus Connectors J1, J2, and J3

Pin #	Name	Pin #	Name
51	**+5V**[3]	52	+3.3V[4]
49	**+12V**[3]	50	GND
47	**-12V**[3]	48	+1.5V
45	**Present**	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[4]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[4]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1,2]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1,2]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C. (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[4]

Notes (Table 4):

1. The following mini-PCIe signals are not supported: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR.
2. TDI is tied to TDO on modules that do not use JTAG.
3. +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. Remove the fuses on these power

supplies for mini-PCIe cards from other vendors that cannot tolerate power applied to these reserved pins.

4. All +3.3Vaux power pins are changed to system +3.3V power.
5. The SM bus signals SMB_CLK and SMB_DATA are used to communicate with a CPLD on the carrier that reports slot ID. These signals will be under the control of the AcroPack module.

VPX Connectors

Table 5 and Table 6 show the pin assignments for the VPX P0 and P1 connectors for reference. Refer to ANSI/VITA 46.0 VPX Baseline Standard for complete signal descriptions for connector P0. Refer to ANSI/VITA 46.4 PCI Express® on the VPX Fabric Connector for connector P1 signal descriptions.

Table 5 VPX P0 Connector Pin Assignment

Pin #	Name	Pin #	Name
A1	+3.3V	E1	+12V
A2	+3.3V	E2	+12V
A3	+5V	E3	+5V
A4	NVRAM_LOCK	E4	GND
A5	SMD_DATA	E5	GND
A6	GA0	E6	GND
A7	N.C.	E7	JTAG_BYPASS[2]
A8	GND	E8	VPX_REFCLK_P
B1	+3.3V	F1	+12V
B2	+3.3V	F2	+12V
B3	+5V	F3	+5V
B4	VPX_PERST	F4	N.C.
B5	SMB_CLK	F5	GA4
B6	GA1	F6	GA2
B7	N.C.[1]	F7	GND
B8	N.C.	F8	VPX_REFCLK_N
C1	+3.3V	G1	+12V
C2	+3.3V	G2	+12V
C3	+5V	G3	+5V
C4	GND	G4	N.C.
C5	GND	G5	N.C.
C6	GND	G6	GA3
C7	GND	G7	N.C.
C8	N.C.	G8	GND
D1	N.C.		
D2	N.C.		
D3	N.C.		
D4	N.C.		
D5	+3.3V_AUX		
D6	N.C.		

Pin #	Name	Pin #	Name
D7	JTAG_BYPASS[2]		
D8	GND		

Notes (Table 5):

1. N.C. – not connected
2. VPX JTAG signal TDO is connected directly to TDI

Table 6 VPX P1 Connector Pin Assignment

Pin #	Name	Pin #	Name
A1	VPX_PER0_P	E1	VPX_PET0_N
A2	GND	E2	VPX_PET1_P
A3	N.C.	E3	VPX_PET2_N
A4	GND	E4	VPX_PET3_P
A5	N.C.	E5	N.C.
A6	GND	E6	N.C.
A7	N.C.	E7	N.C.
A8	GND	E8	N.C.
A9	N.C.	E9	N.C.
A10	GND	E10	N.C.
A11	N.C.	E11	N.C.
A12	GND	E12	N.C.
A13	N.C.	E13	N.C.
A14	GND	E14	N.C.
A15	N.C.	E15	N.C.
A16	GND	E16	N.C.
B1	VPX_PER0_N	F1	GND
B2	VPX_PER1_P	F2	VPX_PET1_N
B3	VPX_PER2_N	F3	GND
B4	VPX_PER3_P	F4	VPX_PET3_N
B5	N.C.	F5	GND
B6	N.C.	F6	N.C.
B7	N.C.	F7	GND
B8	N.C.	F8	N.C.
B9	N.C.	F9	GND
B10	N.C.	F10	N.C.
B11	N.C.	F11	GND
B12	N.C.	F12	N.C.
B13	N.C.	F13	GND
B14	N.C.	F14	N.C.
B15	N.C.	F15	GND
B16	N.C.	F16	N.C.
C1	GND	G1	N.C.
C2	VPX_PER1_N	G2	GND
C3	GND	G3	N.C.

Pin #	Name	Pin #	Name
C4	VPX_PER3_N	G4	GND
C5	GND	G5	N.C.
C6	N.C.	G6	GND
C7	GND	G7	N.C.
C8	N.C.	G8	GND
C9	GND	G9	N.C.
C10	N.C.	G10	GND
C11	GND	G11	N.C.
C12	N.C.	G12	GND
C13	GND	G13	N.C.
C14	N.C.	G14	GND
C15	GND	G15	N.C.
C16	N.C.	G16	GND
D1	VPX_PET0_P		
D2	GND		
D3	VPX_PET2_P		
D4	GND		
D5	N.C.		
D6	GND		
D7	N.C.		
D8	GND		
D9	N.C.		
D10	GND		
D11	N.C.		
D12	GND		
D13	N.C.		
D14	GND		
D15	N.C.		
D16	GND		

JTAG Programming/Debug Connector

A JTAG programming/debug connector is provided for developing applications that use Acromag's FPGA AcroPack modules. See reference designator P5 in Figure 2. This is a standard 14-pin Xilinx programming header for connecting a Xilinx Platform USB II programming device (or equivalent). The pin assignment for P5 is shown in Table 7. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to bypass the TDI and TDO signals. A CPLD on the carrier is included in the JTAG chain. The Xilinx Vivado tools can detect the presence of the CPLD in the JTAG chain, and skip it when accessing the FPGAs on the AcroPack modules.

Table 7 JTAG Programming/Debug Connector Pin Assignment

Signal	Pin	Pin	Signal
N.C.[1]	1	2	+3.3V
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	N.C. [1]
N.C. [1]	13	14	N.C. [1]

Notes (Table 7):

1. N.C. – not connected

TMS – **JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.

TCK – **JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.

TDO – **JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.

TDI – **JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

+3.3V – The target reference voltage V_{REF} is 3.3 Volts

GND - Ground.

FIELD GROUNDING CONSIDERATIONS

Care should be taken to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AcroPack input/output modules.

3. PROGRAMMING INFORMATION

This VPX4500 carrier board has no end user programmable components. The PCIe switch on the carrier is transparent to the end user.

4. THEORY OF OPERATION

This section describes the functionality of the circuitry used on the carrier board. Refer to Figure 1 VPX4500 Block Diagram as you review this material.

PCIe Switch

The PCIe switch is a 6 port 8 lane PCIe Gen 2 switch. It expands the single host PCIe port to three ports, one for each AcroPack site. The host port consists of four PCIe lanes, each of the AcroPack sites have one lane each.

PCIe Bus Interface

The PCIe bus interface is implemented in the logic of the carrier board's PCIe bus target interface chip. Note that the VPX4500 board is not hot-swappable.

DC/DC Converter

The VPX4500 carriers have two DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present at the host interface. The +1.5 Volt supply is sourced from the +5 Volt host power. The -12 Volt supply is sourced from +12 Volt host power.

Slot Addressing

The VPX4500 carriers assign a unique slot address to each of the AcroPack sites. The slot address is 8 bits long. It consists of 3 bits to identify the site on the carrier where the AcroPack module is installed, and 5 bits that are determined by the global address lines on the VPX backplane. The CPLD will serialize the slot address and transmit the address to the AcroPack module as requested by the AcroPack module. The process of reading the slot address is typically initiated by host software.

JTAG

A JTAG interface is provided for programming and debugging FPGAs on AcroPack modules. It is intended to be used with a Xilinx Platform USB II programming device. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to complete the JTAG chain. The slot address CPLD is also included in the JTAG chain for factory programming.

Power Supply Fuses

The power supplies to each AcroPack module are individually fused. A blown fuse can be identified by visible inspection or by use of an ohm meter. The locations of the fuses are shown in Figure 3. The current rating for each of the fuses is listed in the Fuses paragraph in section 6.

5. SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in Section 2 PREPARATION FOR USE have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or AcroPack with one that is known to work correctly is a good technique to isolate a faulty board.

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes
- Frequently Asked Questions (FAQ’s)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag’s application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length .....6.299 inches (160.0 mm)
Height.....3.937 inches (100.0 mm)
Board thickness.....0.063 inches (1.60 mm)
Max component height .....0.394 inches (10 mm)
Max component height under AP modules
0.069 inches (1.75 mm)

Connectors

P0 (VPX) .....TE Connectivity 1410189-3
P1,2 (VPX) .....TE Connectivity 1410187-3

J4,5 (VPX4500E-LF Carrier Field I/O)
50 pin champ (TE Connectivity 6658751-1)
P6,7 (VPX4500-CC-LF Carrier Field I/O)
50 pin male plug header (TE Connectivity 1-1761685-5)
P3,4,11 (AP Field I/O).....100-pin SMT socket (Samtec SS5-50-3.00-L-D-K-TR)
J1,2,3 (AP Logic) .....50-pin male plug header (TE Connectivity 1759457-1)
P5 (JTAG programmer) .....14-pin male plug header (Molex 87832-1420)

Isolation

This AcroPack carrier does not provide isolation between the AcroPack Field I/O signals and the host. It is not intended to be used with isolated AcroPack modules.

Power

Board power requirements are a function of the installed AP modules. This specification lists currents for the carrier board only. The carrier board provides +1.5V, +3.3V, +5V, +12V and -12V power to each AP module. The VPX4500 contains DC/DC converters, which generate the +1.5V and -12V from the +5V and +12V VPX power rails. Each AP module supply line is individually fused. Additionally, the carrier board utilizes +3.3V VPX power for logic.

Fuses

+1.5 .....1.1 Amps (F5, F10 and F15) Raychem NANOSMDC110F-2
+3.3V..... 3 Amps (F4, F9 and F14) Littelfuse 0466003.NR
+5V, +12V, -12V ..... 2 Amps (F1, F3, F3, F6, F8, F11 and F13) Littelfuse 0453002.MR

Currents specified are for the carrier board only for Model VPX4500(E), add the AP module currents for the total current required from each supply.

+3.3 Volts (±10%).....0.55 A Typical
+5 Volts (±5%).....6.5 mA Typical

+12 Volts (±5%).....25 mA Typical

PCIe BUS COMPLIANCE

Industry Specifications Compliance
PCI Express® Base Specification, Revision 2.1

ENVIRONMENTAL

Operating Temperature.....-40 to +70°C (VPX4500)
-40 to +85°C (VPX4500E)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C.
Non-Isolated .....The PCIe bus and the AP module commons have a direct electrical connection. As such unless the AP module provides isolation between the logic and field side, the field I/O signals are not isolated from the PCIe bus.

EMC Compliance

Immunity.....per EN 61000-6-2
Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
Radiated Field Immunity (RFI), per IEC 61000-4-3
Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
Surge Immunity, per IEC 61000-4-5
Conducted RF Immunity (CRFI), per IEC 61000-4-6
Emissions .....per EN61000-6-4
Enclosure Port, per CISPR 16
Low Voltage AC Mains Port, per CISPR 16
Note: This is a Class A product

Vibration and Shock Standard

The VPX4500 carriers are designed to pass the following Vibration and Shock standards.
Vibration, Sinusoidal Operating ...Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating .....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating.....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

7. CERTIFICATE OF VOLATILITY

Certificate of Volatility				
Acromag Models VPX4500E-LF, VPX4500-CC-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, FLASH etc.) FLASH	Size: 1 Mbit	User Modifiable Yes	Function: PCIe switch configuration	Process to Sanitize: Overwrite FLASH contents.
Type(EEPROM, FLASH etc.) EEPROM	Size: 2 Kbit	User Modifiable Yes	Function: I/O expander general purpose non-volatile memory	Process to Sanitize: Overwrite EEPROM contents.
Acromag Representative				
Name: Russ Nieves	Title: Dir. of Sales and Marketing	Email: rnieves@acromag.com	Office Phone: 248-295-0838	Office Fax: 248-624-9234

8. REVISION HISTORY

Release Date	Version	EGR/DOC	Description of Revision
15 NOV 2016	A	JCL/MJO	Initial Acromag release.
05 JAN 2017	B	JCL/MJO	Corrected error identifying switch functions (***Table 1 Switch SW1 Functions***)

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