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Carrier Card Series

VPX4821A/VPX4821A-CC VPX XMC/PMC Carrier

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1. GENERAL INFORMATION

The VPX4821A card is a 6U VPX non-intelligent XMC/PMC carrier board designed for PCIe bus connection to the VPX Data Plane. The board supports up to a 8x PCIe connection that is selectable via jumpers. The carrier enables the use of XMC and PMC mezzanine I/O modules. The carrier card acts as an adapter to route PCIe bus signals between the PCIe bus of your backplane and either P15 connector of an XMC module card or P11 and P12 of a PMC Card. Access to rear I/O is provided through connections to the backplane. XMC and PCM modules with front I/O can be accessed though the front mounting bracket.

The VPX4821A series is a 6U VPX Non-Intelligent XMC/PMC carrier board designed for 4x/8x PCIe bus connection. The carrier card uses a PLX Technology® PCIe Switch Chip (PEX 8734) and IDT Technology® PCIe to PCI Bridge Chip (TSI384) to interface between the VPX PCIe bus and one XMC/PMC mezzanine I/O module card.

Model VPX4821A-XX-LF is an air-cooled product which can be used for front and rear I/O XMC/PMC mezzanine modules.

Model VPX4821A-XX-CC-LF is an extended temperature conduction-cooled product which supports all Acromag FPGA modules. It only supports Rear I/O.

Model	Description	Temp Range
VPX4821A-42-LF	*Air-cooled 6U VPX XMC/PMC Carrier for Data Plane with VITA 42*	0 to +70°C
VPX4821A-42-CC-LF	*Conduction-cooled 6U VPX XMC/PMC Carrier for Data Plane with VITA 42*	-40 to +85°C[1]
VPX4821A-61-LF	*Air-cooled 6U VPX XMC/PMC Carrier for Data Plane with VITA 61*	0 to +70°C
VPX4821A-61-CC-LF	*Conduction-cooled 6U VPX XMC/PMC Carrier for Data Plane with VITA 61*	-40 to +85°C[1]

1. See Power Specifications for further information including power rating.

KEY VPX4821A FEATURES

PCI Express Interface: Up to Sixteen PCI Express Gen 1 or Gen 2 lanes are connected to the VPX P1 connecter. This is the Data Plane. Lane configuration is jumper selectable.

PCI Express Configuration: Jumper selectable for two x8 ports, four x4 ports, or one x8 port and two x4 ports.

PCI and PC-X Compliant: Each slot supports up to 133MHz 64 bit PCI-X.

Upstream and NT Port Configuration: Selectable via jumper.

I/O: Support both Front and Rear I/O. CC model is Rear I/O only.

Single Power Supply: The carrier only requires VPX to provide +12V to PS1. The carrier will generate and supply the PMC/XMC modules with +5V and +3.3V. The XMC VPWR pins are connected to +12V. This board can also run off only the VPX PS3 +5V supply. Please contact the factory for details. All AUX supplies are optional and are only required if used by the XMC/PMC modules.

JTAG Programming Header: The VPX4821A carrier includes a programming connector that mates with a Xilinx programmer for programming Acromag FPGA products. Acromag XMC FPGA boards can be configured to route the JTAG programming signals through the XMC P15/P25 connectors.

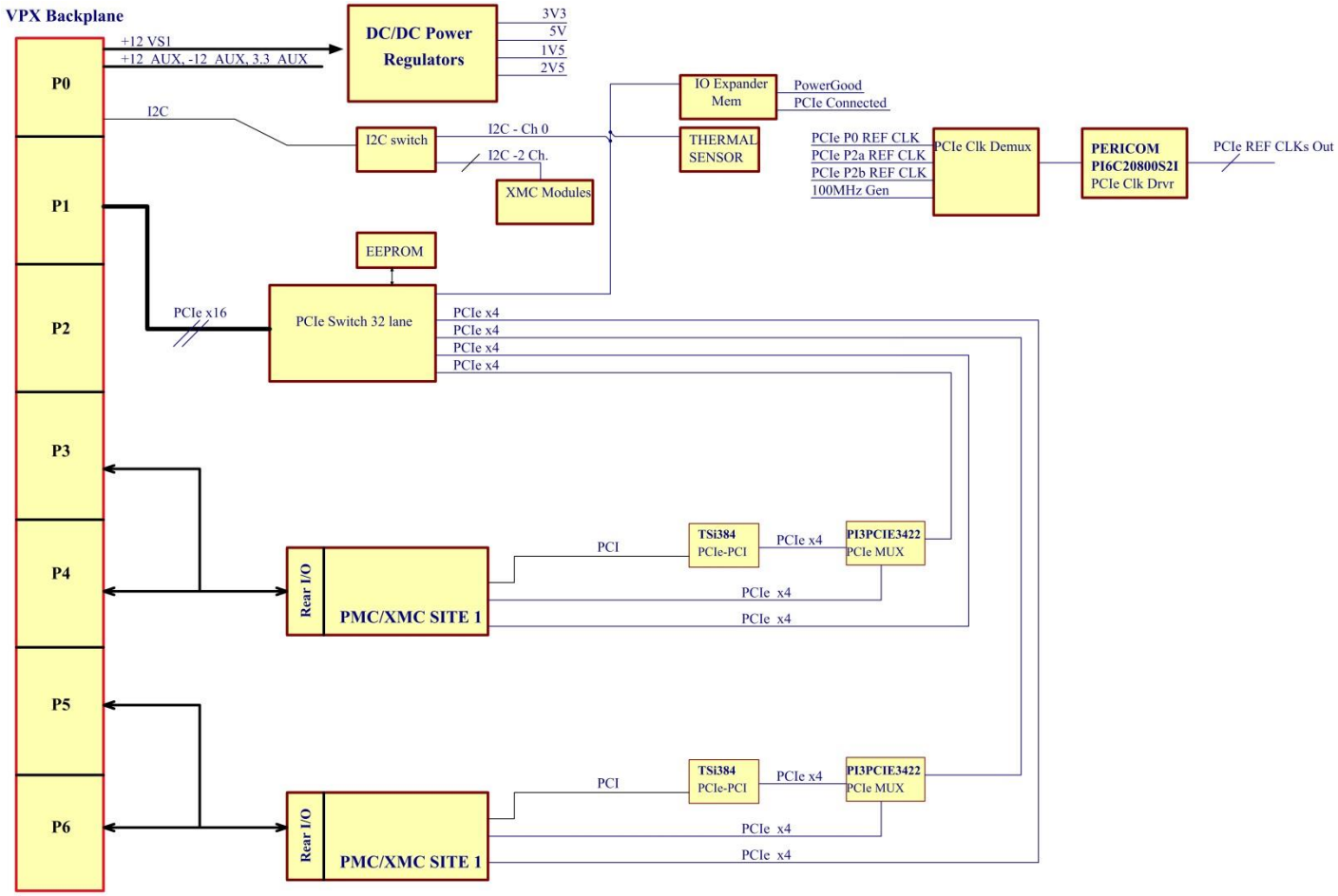


Figure 1: Block Diagram

2. PREPARATION FOR USE

UNPACKING AND INSPECTION



Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed PMC/XMC modules, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Board Configuration

Power should be removed from the board when changing jumper configurations or when installing an XMC or PMC module, cables and field wiring.

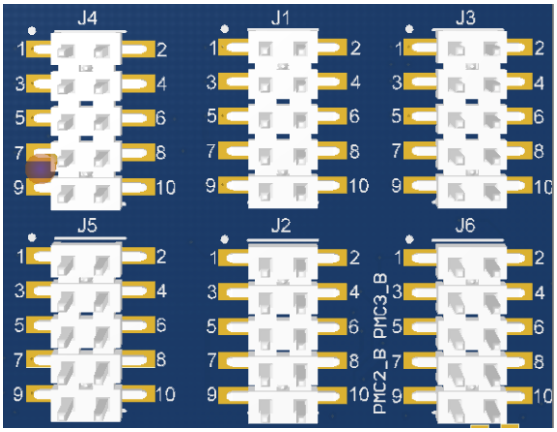


Figure 2: Jumper Diagram

JUMPERS

There are six jumper blocks located on the board. The jumper blocks are labeled J1, J2, J3, J4, J5, and J6. Within each jumper block there are multiple jumper settings. A jumper can be used to shout post horizontally and vertically. The jumper position is OPEN if no jumper is present. The jumper position is SET if a jumper is present across the two pins. The description for each jumper is described in the tables that follow. **Bold Selections are the factory default setting.**

For rugged designs all jumpers can be replaced with 0 Ohm resistors. Please contact the factory for details.

PCIe Lane Configuration

The VPX P1 PCIe lane configuration is selectable via the J1 jumper. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8734.

Table 2-1 PCIe Lane Jumper Configuration

PCIe Lane Configuration	J1 Jumper Configuration					
	5-6	5-7	6-8	1-2	1-3	2-4
8x-8x	O	S	O	S	O	O
4x-4x-4x-4x	**O**	**O**	**S**	**O**	**O**	**S**
8x-4x-4x	O	O	S	O	S	O

Default setting is 4x-4x-4x-4x with vertical jumbers J1 2-4 and 6-8 set.

The PCIe lane configuration determined the PCIe switch port naming convention. Use Table 2-2 as a reference when selecting the upstream and downstream port.

Table 2-2 PCIe Port Naming Convention

PCIe Lane Configuration	Port Naming			
	L0-L3	L4-L7	L8-L11	L12-L15
8x-8x	Port 0		Port 1	
4x-4x-4x-4x	Port 0	Port 1	Port 2	Port 3
8x-4x-4x	Port 0		Port 1	Port 2

PCIe Upstream Port Select

The PCIe Upstream port is selectable via the J3 jumper. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8734.

Table 2-3 PCIe Upstream Port Jumper Selection

PCIe Lane Configuration	J3 Jumper Configuration					
	5-6	5-7	6-8	1-2	1-3	2-4
Port 0	**O**	**S**	**O**	**O**	**S**	**O**
Port 1	O	S	O	O	O	S
Port 2	O	S	O	S	O	O
Port 3	O	O	S	O	S	O

Default setting is Port 0 with vertical J3 jumbers 1-3 and 5-7 set.

Fan-Out Enable

Enable peer-to-peer (Downstream endpoint-to-Downstream endpoint) traffic with jumper J5 9-10 set. If peer-to-peer (Downstream endpoint-to-Downstream endpoint) traffic is not needed, this jumper can be left open.

Table 2-4 Fan-Out Enable Jumper Setting

Fan-Out Enable	J5 9-10
Enable	**SET**
Disable	OPEN

Default Fan-Out Enabled setting horizontal J5 jumber 9-10 set.

PCIe NT Port Enable/Select

To Enable the Non-Transparent (NT) Port of the PCIe switch, SET J5 and J2 jumpers as listed in table 2-5. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8734. Non-Transparent selected presents a processor as an endpoint rather than another memory system.

Table 2-5 NT Enabled Jumper Settings

Select NT Upstream Port	Jumper Configuration								
	J5						J2		
	1-2	1-3	2-4	5-6	5-7	6-8	1-2	1-3	2-4
Port 0	O	S	O	O	S	O	O	S	O
Port 1	O	S	O	O	S	O	O	O	S
Port 2	O	S	O	O	S	O	S	O	O
Port 3	O	S	O	O	O	S	O	S	O
NT Disable	**S**	**O**	**O**	**S**	**O**	**O**	**S**	**O**	**O**

Default setting is NT Disable with horizontal J5 jumber 1-2 set, 5-6 set, and J2 jumper 1-2 set.

+3.3_AUX Power

The 3.3V_AUX power is required for proper operation of this board. For users without this power supply available on the VPX backplane you can alternatively use the onboard generated 3.3V.

Table 2-6 +3.3V_AUX Power Select Jumper Settings

Source of +3.3V-AUX	J6 7-8	J6 9-10
Onboard +3.3V	OPEN	SET
Backplane	**SET**	**OPEN**

WARNING! The J6 7-8 and J6 9-10 jumpers should both never be set. This could cause damage to either the board or chassis power supply.

Default setting is +3.3V_AUX from Backplane with horizontal J6 7-8 jumber set.

JTAG Reference Power

The pull-up voltage on the JTAG pins to XMC P15 and P25 can be selected as either +2.5V or +3.3V. Refer to the XMC User's Manual for proper voltage selection. The jumper J3 9-10 is for slot A and the jumper J1 9-10 is for slot B.

Table 2-7 JTAG Power Select Jumper Settings

JTAG Ref Voltage		
Slot	**LOC**	**Setting**
Slot A	J3 9-10	**OPEN +3.3V** SET +2.5V
Slot B	J1 9-10	**OPEN +3.3V** SET +2.5V

Default setting is +3.3V JTAG Ref with J3 9-10 jumber OPEN and J1 9-10 jumper OPEN.

Clock Settings

There are several clock options available for the user. These options are set on J4 1-2, J4 3-4, and J4 5-6 jumpers. The default selection is to use the on-board crystal to generate the 100MHz PCIe clock. This frequency is propagated to all parts and XMC/PMC modules. Users also have the option to use a clock from the VPX backplane. Note that this must be a 100MHz clock for proper

operation. Refer to the table below for jumper settings. Spread spectrum clocking is enabled when J4 3-4 is Set. Spread spectrum clocking should always be disabled.

Table 2-8 Clock Jumper Settings

Global Clock Source	J4 1-2	J4 3-4	J4 5-6
On Board Crystal	**OPEN**	**OPEN**	**OPEN**
VPX SYSCLK	SET	OPEN	OPEN
Disable all CLK's	OPEN	OPEN	SET

Default setting is On Board Crystal with J4 1-2, J4 3-4, and J4 5-6 jumpers OPEN.

Reset

The reset delay circuit is enabled/disabled via configuration jumper J6. This system reset is propagated to all parts XMC/PMC modules and backplane.

Configuration jumper J2 is used to configure the on-board system reset delay circuit. When enabled, the VPX SYSRESET signal will be held down on power-up for a configurable amount of time. This can be used to allow extra time for a particularly large FPGA program to load before reset is de-asserted and the PCIe bus is enumerated, for instance.

Refer to the table below for jumper settings.

Table 2-9 Reset Output Generator Jumper Settings

Reset Output Generator	J6 1-2	J6 3-4
System Reset	**OPEN**	**SET**
Delay Circuit Reset	**SET**	**OPEN**

RESET OUTPUT TIME	JUMPER POSITION		
	J2 5-6	J2 7-8	J2 9-10
20ms	OPEN	OPEN	OPEN
189ms	OPEN	OPEN	SET
300ms	SET	OPEN	OPEN
572ms	OPEN	SET	OPEN
761ms	OPEN	SET	SET

I^2C PROGRAMMING

The PEX8734 PCI switch can alternately be programmed via a simple I^2C bus. The I^2C is accessed via the System Bus pins on the VPX backplane. Furthermore the I^2C bus is connected to both XMC modules. For further information on programming using the I^2C bus contact the factory.

NVROM

The NVROM signal from the VPX Backplane is routed to the PCIe Switch EEPROM as well as both XMC modules.

LED's

The VPX4821A has several status LEDS. These LED's are primarily used for initial power-up status. The LEDs are located on the front of the card near the J1 to J6 jumpers. The table below describes the functionality.

Table 2-10 LED

LED	Color	Description
DS1	Green	All power supplies are good.
DS2	Red	PMC A Only – PCIe Lane 1 has connected.
DS3	Red	PMC A Only – PCIe Lane 2 has connected.
DS4	Red	PMC A Only – PCIe Lane 3 has connected.
DS5	Red	PMC A Only – PCIe Lane 4 has connected.
DS6	Red	PMC B Only – PCIe Lane 1 has connected.
DS7	Red	PMC B Only – PCIe Lane 2 has connected.
DS8	Red	PMC B Only – PCIe Lane 3 has connected.
DS9	Red	PMC B Only – PCIe Lane 4 has connected.
DS10	Green	VPX PCIe Port 0 has successfully connected
DS11	Green	VPX PCIe Port 1 has successfully connected
DS12	Green	VPX PCIe Port 2 has successfully connected
DS13	Green	VPX PCIe Port 3 has successfully connected
DS14	Green	A Connection has been made to XMC/PMC Slot A.
DS15	Green	A Connection has been made to XMC/PMC Slot B.
DS16	Red	Fatal Error (non-recoverable)
DS17	Green	PCI INTA

BACKPLANE KEY

The VPX4821A is not keyed and will plug into any VPX backplane. Prior to powerup, verify that VS1 is +12V. Any other voltage on VS1 may damage the board.

CONNECTORS

Refer to Figure 3 for connector locations. Connectors on the VPX4821A carrier consist of six VPX Backplane connectors, then 2 XMC connectors, and four PMC connectors for each slot. These interface connectors are discussed in the following sections.

J11/J12/J13/J21/J22/J23.....PMC PCI signals
J14/J25 .....PMC user signals (Rear I/O)
J15/J25 .....XMC PCIe signals
J16/J26 .....XMC user signals (Rear I/O)
P0 .....VPX Power and system signals.
P1……VPX Data Plane. This connects to all PCIe lanes.
P2 .....VPX Expansion plane. This connector is not populated.
P3/P4.....PMC/XMC Slot A Rear I/O.
P5/P6.....PMC/XMC Slot B Rear I/O.

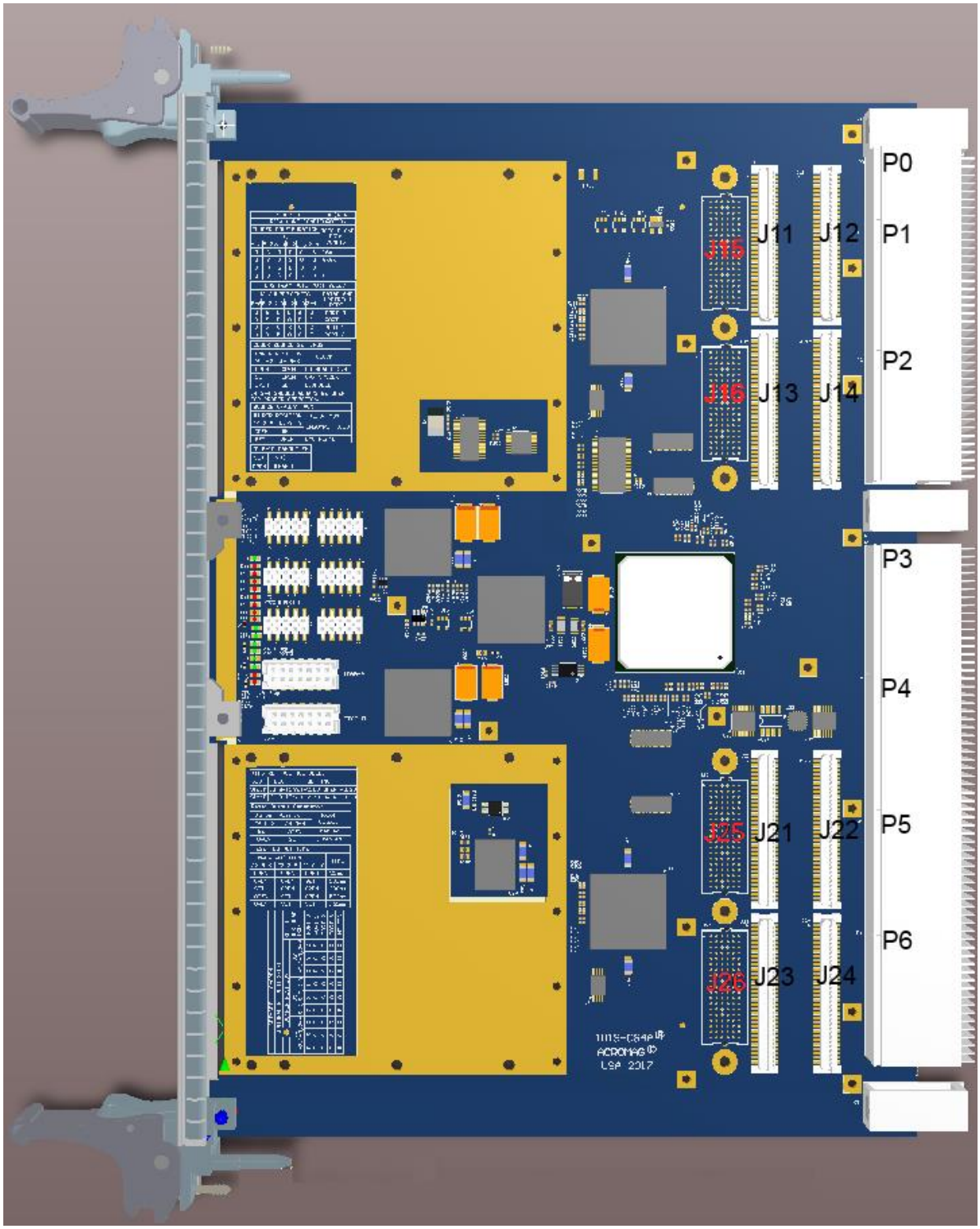


Figure 3: Connector Locations

VPX Connectors

Table 2-11 P0 – VPX Utility Signals

Pin	A	B	C	D	E	F	G
1	VS2	VS2	VS2	NC	+12V	+12V	+12V
2	VS2	VS2	VS2	NC	+12V	+12V	+12V
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	NVMRO	P0_SYSRESET	GND	-12V_AUX	GND	SM3	SM2
5	I2C_DAT	I2C_CLK	GND	+3.3V_AUX	GND	GA4	GAP
6	GA0	GA1	GND	+12V_AUX	GND	GA2	GA3
7	JTAG_TRST	JTAG_TMS	GND	JTAG_TDI	JTAG_TDO	GND	JTAG_TCK
8	GND	REF_BUS_P	REF_BUS_N	GND	P0_REFCLK_P	P0_REFCLK_N	GND

All blue colored cells are Not Used in this design.

Table 2-12 P1 – VPX Data Plane

Pin	A	B	C	D	E	F	G
1	PCIE_L0_RXP	PCIE_L0_RXN	Gnd	PCIE_L0_TXP	PCIE_L0_TXN	Gnd	
2	Gnd	PCIE_L1_RXP	PCIE_L1_RXN	Gnd	PCIE_L1_TXP	PCIE_L1_TXN	Gnd
3	PCIE_L2_RXP	PCIE_L2_RXN	Gnd	PCIE_L2_TXP	PCIE_L2_TXN	Gnd	
4	Gnd	PCIE_L3_RXP	PCIE_L3_RXN	Gnd	PCIE_L3_TXP	PCIE_L3_TXN	Gnd
5	PCIE_L4_RXP	PCIE_L4_RXN	Gnd	PCIE_L4_TXP	PCIE_L4_TXN	Gnd	
6	Gnd	PCIE_L5_RXP	PCIE_L5_RXN	Gnd	PCIE_L5_TXP	PCIE_L5_TXN	Gnd
7	PCIE_L6_RXP	PCIE_L6_RXN	Gnd	PCIE_L6_TXP	PCIE_L6_TXN	Gnd	
8	Gnd	PCIE_L7_RXP	PCIE_L7_RXN	Gnd	PCIE_L7_TXP	PCIE_L7_TXN	Gnd
9	PCIE_L8_RXP	PCIE_L8_RXN	Gnd	PCIE_L8_TXP	PCIE_L8_TXN	Gnd	
10	Gnd	PCIE_L9_RXP	PCIE_L9_RXN	Gnd	PCIE_L9_TXP	PCIE_L9_TXN	Gnd
11	PCIE_L10_RXP	PCIE_L10_RXN	Gnd	PCIE_L10_TXP	PCIE_L10_TXN	Gnd	
12	Gnd	PCIE_L11_RXP	PCIE_L11_RXN	Gnd	PCIE_L11_TXP	PCIE_L11_TXN	Gnd
13	PCIE_L12_RXP	PCIE_L12_RXN	Gnd	PCIE_L12_TXP	PCIE_L12_TXN	Gnd	
14	Gnd	PCIE_L13_RXP	PCIE_L13_RXN	Gnd	PCIE_L13_TXP	PCIE_L13_TXN	Gnd
15	PCIE_L14_RXP	PCIE_L14_RXN	Gnd	PCIE_L14_TXP	PCIE_L14_TXN	Gnd	
16	Gnd	PCIE_L15_RXP	PCIE_L15_RXN	Gnd	PCIE_L15_TXP	PCIE_L15_TXN	Gnd

All blue colored cells are Not Used in this design.

Table 2-13 P3 – PMC SLOT A Rear I/O

Pin	A	B	C	D	E	F	G
1	PMC1_RIO1_N	PMC1_RIO1_P	Gnd	PMC1_RIO0_N	PMC1_RIO0_P	Gnd	
2	Gnd	PMC1_RIO3_N	PMC1_RIO3_P	Gnd	PMC1_RIO2_N	PMC1_RIO2_P	Gnd
3	PMC1_RIO5_N	PMC1_RIO5_P	Gnd	PMC1_RIO4_N	PMC1_RIO4_P	Gnd	
4	Gnd	PMC1_RIO7_N	PMC1_RIO7_P	Gnd	PMC1_RIO6_N	PMC1_RIO6_P	Gnd
5	PMC1_RIO9_N	PMC1_RIO9_P	Gnd	PMC1_RIO8_N	PMC1_RIO8_P	Gnd	
6	Gnd	PMC1_RIO11_N	PMC1_RIO11_P	Gnd	PMC1_RIO10_N	PMC1_RIO10_P	Gnd
7	PMC1_RIO13_N	PMC1_RIO13_P	Gnd	PMC1_RIO12_N	PMC1_RIO12_P	Gnd	
8	Gnd	PMC1_RIO15_N	PMC1_RIO15_P	Gnd	PMC1_RIO14_N	PMC1_RIO14_P	Gnd
9	PMC1_RIO17_N	PMC1_RIO17_P	Gnd	PMC1_RIO16_N	PMC1_RIO16_P	Gnd	
10	Gnd	PMC1_RIO19_N	PMC1_RIO19_P	Gnd	PMC1_RIO18_N	PMC1_RIO18_P	Gnd
11	PMC1_RIO21_N	PMC1_RIO21_P	Gnd	PMC1_RIO20_N	PMC1_RIO20_P	Gnd	
12	Gnd	PMC1_RIO23_N	PMC1_RIO23_P	Gnd	PMC1_RIO22_N	PMC1_RIO22_P	Gnd
13	PMC1_RIO25_N	PMC1_RIO25_P	Gnd	PMC1_RIO24_N	PMC1_RIO24_P	Gnd	
14	Gnd	PMC1_RIO27_N	PMC1_RIO27_P	Gnd	PMC1_RIO26_N	PMC1_RIO26_P	Gnd
15	PMC1_RIO29_N	PMC1_RIO29_P	Gnd	PMC1_RIO28_N	PMC1_RIO28_P	Gnd	
16	Gnd	PMC1_RIO31_N	PMC1_RIO31_P	Gnd	PMC1_RIO30_N	PMC1_RIO30_P	Gnd

All blue colored cells are Not Used in this design.

Table 2-14 P4 – XMC SLOT A Rear I/O

Pin	A	B	C	D	E	F	G
1	XMC1_DP05_N	XMC1_DP05_P	Gnd	XMC1_DP04_N	XMC1_DP04_P	Gnd	
2	Gnd	XMC1_DP07_N	XMC1_DP07_P	Gnd	XMC1_DP06_N	XMC1_DP06_P	Gnd
3	XMC1_DP09_N	XMC1_DP09_P	Gnd	XMC1_DP08_N	XMC1_DP08_P	Gnd	
4	Gnd	XMC1_DP15_N	XMC1_DP15_P	Gnd	XMC1_DP14_N	XMC1_DP14_P	Gnd
5	XMC1_DP17_N	XMC1_DP17_P	Gnd	XMC1_DP16_N	XMC1_DP16_P	Gnd	
6	Gnd	XMC1_DP19_N	XMC1_DP19_P	Gnd	XMC1_IO_B19	XMC1_IO_A19	Gnd
7	XMC1_DP01_N	XMC1_DP01_P	Gnd	XMC1_DP00_N	XMC1_DP00_P	Gnd	
8	Gnd	XMC1_DP03_N	XMC1_DP03_P	Gnd	XMC1_DP02_N	XMC1_DP02_P	Gnd
9	XMC1_DP11_N	XMC1_DP11_P	Gnd	XMC1_DP10_N	XMC1_DP10_P	Gnd	
10	Gnd	XMC1_DP13_N	XMC1_DP13_P	Gnd	XMC1_DP12_N	XMC1_DP12_P	Gnd
11			Gnd			Gnd	
12	Gnd			Gnd			Gnd
13			Gnd			Gnd	
14	Gnd			Gnd			Gnd
15			Gnd			Gnd	
16	Gnd			Gnd			Gnd

All blue colored cells are Not Used in this design.

Table 2-15 P5 – PMC SLOT B Rear I/O

Pin	A	B	C	D	E	F	G
1	PMC2_RIO1_N	PMC2_RIO1_P	Gnd	PMC2_RIO0_N	PMC2_RIO0_P	Gnd	
2	Gnd	PMC2_RIO3_N	PMC2_RIO3_P	Gnd	PMC2_RIO2_N	PMC2_RIO2_P	Gnd
3	PMC2_RIO5_N	PMC2_RIO5_P	Gnd	PMC2_RIO4_N	PMC2_RIO4_P	Gnd	
4	Gnd	PMC2_RIO7_N	PMC2_RIO7_P	Gnd	PMC2_RIO6_N	PMC2_RIO6_P	Gnd
5	PMC2_RIO9_N	PMC2_RIO9_P	Gnd	PMC2_RIO8_N	PMC2_RIO8_P	Gnd	
6	Gnd	PMC2_RIO11_N	PMC2_RIO11_P	Gnd	PMC2_RIO10_N	PMC2_RIO10_P	Gnd
7	PMC2_RIO13_N	PMC2_RIO13_P	Gnd	PMC2_RIO12_N	PMC2_RIO12_P	Gnd	
8	Gnd	PMC2_RIO15_N	PMC2_RIO15_P	Gnd	PMC2_RIO14_N	PMC2_RIO14_P	Gnd
9	PMC2_RIO17_N	PMC2_RIO17_P	Gnd	PMC2_RIO16_N	PMC2_RIO16_P	Gnd	
10	Gnd	PMC2_RIO19_N	PMC2_RIO19_P	Gnd	PMC2_RIO18_N	PMC2_RIO18_P	Gnd
11	PMC2_RIO21_N	PMC2_RIO21_P	Gnd	PMC2_RIO20_N	PMC2_RIO20_P	Gnd	
12	Gnd	PMC2_RIO23_N	PMC2_RIO23_P	Gnd	PMC2_RIO22_N	PMC2_RIO22_P	Gnd
13	PMC2_RIO25_N	PMC2_RIO25_P	Gnd	PMC2_RIO24_N	PMC2_RIO24_P	Gnd	
14	Gnd	PMC2_RIO27_N	PMC2_RIO27_P	Gnd	PMC2_RIO26_N	PMC2_RIO26_P	Gnd
15	PMC2_RIO29_N	PMC2_RIO29_P	Gnd	PMC2_RIO28_N	PMC2_RIO28_P	Gnd	
16	Gnd	PMC2_RIO31_N	PMC2_RIO31_P	Gnd	PMC2_RIO30_N	PMC2_RIO30_P	Gnd

All blue colored cells are Not Used in this design.

Table 2-16 P6 – XMC SLOT B Rear I/O

Pin	A	B	C	D	E	F	G
1	XMC2_DP05_N	XMC2_DP05_P	Gnd	XMC2_DP04_N	XMC2_DP04_P	Gnd	
2	Gnd	XMC2_DP07_N	XMC2_DP07_P	Gnd	XMC2_DP06_N	XMC2_DP06_P	Gnd
3	XMC2_DP09_N	XMC2_DP09_P	Gnd	XMC2_DP08_N	XMC2_DP08_P	Gnd	
4	Gnd	XMC2_DP15_N	XMC2_DP15_P	Gnd	XMC2_DP14_N	XMC2_DP14_P	Gnd
5	XMC2_DP17_N	XMC2_DP17_P	Gnd	XMC2_DP16_N	XMC2_DP16_P	Gnd	
6	Gnd	XMC2_DP19_N	XMC2_DP19_P	Gnd	XMC2_IO_B19	XMC2_IO_A19	Gnd
7	XMC2_DP01_N	XMC2_DP01_P	Gnd	XMC2_DP00_N	XMC2_DP00_P	Gnd	
8	Gnd	XMC2_DP03_N	XMC2_DP03_P	Gnd	XMC2_DP02_N	XMC2_DP02_P	Gnd
9	XMC2_DP11_N	XMC2_DP11_P	Gnd	XMC2_DP10_N	XMC2_DP10_P	Gnd	
10	Gnd	XMC2_DP13_N	XMC2_DP13_P	Gnd	XMC2_DP12_N	XMC2_DP12_P	Gnd
11			Gnd			Gnd	
12	Gnd			Gnd			Gnd
13			Gnd			Gnd	
14	Gnd			Gnd			Gnd
15			Gnd			Gnd	
16	Gnd			Gnd			Gnd

All blue colored cells are Not Used in this design.

PMC Connectors

Table 2-17 Jx1 PMC PCI Signals

Pin Description	Number	Pin Description	Number
TCK	1	-12V	2

Pin Description	Number	Pin Description	Number
GND	3	INTA#	4
INTB#	5	INTC#	6
BUSMODE1#	7	+5V	8
INTD#	9	NC[1]	10
GND	11	+3.3VAUX	12
CLK	13	GND	14
GND	15	GNT#	16
REQ#	17	+5V	18
+3.3V	19	AD31	20
AD28	21	AD27	22
AD25	23	GND	24
GND	25	C/BE3#	26
AD22	27	AD21	28
AD19	29	+5V	30
+3.3V	31	AD17	32
FRAME#	33	GND	34
GND	35	IRDY#	36
DEVSEL#	37	+5V	38
PCIXCAP	39	LOCK#	40
NC[1]	41	NC[1]	42
PAR	43	GND	44
+3.3V	45	AD15	46
AD12	47	AD11	48
AD9	49	+5V	50
GND	51	C/BE0#	52
AD6	53	AD5	54
AD4	55	GND	56
+3.3V	57	AD3	58
AD2	59	AD1	60
AD0	61	+5V	62
GND	63	REQ64#	64

1. NC- Not used.

Table 2-18 Jx2 PMC PCI Signals

Pin Description	Number	Pin Description	Number
+12V	1	TRST#	2
TMS	3	TDO	4
TDI	5	GND	6
GND	7	NC[1]	8
NC[1]	9	NC[1]	10
BUSMODE2#	11	+3.3V	12
RST#	13	BUSMODE3#	14
+3.3V	15	BUSMODE4#	16
PME#	17	GND	18

Pin Description	Number	Pin Description	Number
AD30	19	AD29	20
GND	21	AD26	22
AD24	23	+3.3V	24
IDSEL	25	AD23	26
+3.3V	27	AD20	28
AD18	29	GND	30
AD16	31	C/BE2#	32
GND	33	NC[1]	34
TRDY#	35	+3.3V	36
GND	37	STOP#	38
PERR#	39	GND	40
+3.3V	41	SERR#	42
C/BE1#	43	GND	44
AD14	45	AD13	46
M66EN	47	AD10	48
AD8	49	+3.3V	50
AD7	51	NC[1]	52
+3.3V	53	NC[1]	54
NC[1]	55	GND	56
NC[1]	57	NC[1]	58
GND	59	NC[1]	60
ACK64#	61	+3.3V	62
GND	63	NC[1]	64

1. NC- Not used.

Table 2-19 Jx3 PMC PCI Signals

Pin Description	Number	Pin Description	Number
NC[1]	1	GND	2
GND	3	C/BE7#	4
C/BE6#	5	C/BE5#	6
C/BE4#	7	GND	8
+3.3V	9	PAR64	10
AD63	11	AD62	12
AD61	13	GND	14
GND	15	AD60	16
AD59	17	AD58	18
AD57	19	GND	20
+3.3V	21	AD56	22
AD55	23	AD54	24
AD53	25	GND	26
GND	27	AD52	28
AD51	29	AD50	30
AD49	31	GND	32

Pin Description	Number	Pin Description	Number
GND	33	AD48	34
AD47	35	AD46	36
AD45	37	GND	38
+3.3V	39	AD44	40
AD43	41	AD42	42
AD41	43	GND	44
GND	45	AD40	46
AD39	47	AD38	48
AD37	49	GND	50
GND	51	AD36	52
AD35	53	AD34	54
AD33	55	GND	56
+3.3V	57	AD32	58
NC[1]	59	NC[1]	60
NC[1]	61	GND	62
GND	63	NC[1]	64

1. NC- Not used.

Table 2-20 Jx4 PMC PCI Rear I/O Signals

Pin Description	Number	Pin Description	Number
RIO0_P	1	RIO1_P	2
RIO0_N	3	RIO1_N	4
RIO2_P	5	RIO3_P	6
RIO2_N	7	RIO3_N	8
RIO4_P	9	RIO5_P	10
RIO4_N	11	RIO5_N	12
RIO6_P	13	RIO7_P	14
RIO6_N	15	RIO7_N	16
RIO8_P	17	RIO9_P	18
RIO8_N	19	RIO9_N	20
RIO10_P	21	RIO11_P	22
RIO10_N	23	RIO11_N	24
RIO12_P	25	RIO13_P	26
RIO12_N	27	RIO13_N	28
RIO14_P	29	RIO15_P	30
RIO14_N	31	RIO15_N	32
RIO16_P	33	RIO17_P	34
RIO16_N	35	RIO17_N	36
RIO18_P	37	RIO19_P	38
RIO18_N	39	RIO19_N	40
RIO20_P	41	RIO21_P	42
RIO20_N	43	RIO21_N	44
RIO22_P	45	RIO23_P	46

Pin Description	Number	Pin Description	Number
RIO22_N	47	RIO23_N	48
RIO24_P	49	RIO25_P	50
RIO24_N	51	RIO25_N	52
RIO26_P	53	RIO27_P	54
RIO26_N	55	RIO27_N	56
RIO28_P	57	RIO29_P	58
RIO28_N	59	RIO29_N	60
RIO30_P	61	RIO31_P	62
RIO30_N	63	RIO31_N	64

1. In VPX Connector pinouts P3/P5 the name is preceded by PMC1 or PMC2 depending on Slot.

XMC Connectors

Table 2-21 Jx5 XMC PCIe Signals

Pin Description	Number	Pin Description	Number
PET0p0	A1	PET0p1	D1
GND	A2	GND	D2
PET0p2	A3	PET0p3	D3
GND	A4	GND	D4
PET0p4	A5	PET0p5	D5
GND	A6	GND	D6
PET0p6	A7	PET0p7	D7
GND	A8	GND	D8
NC	A9	NC	D9
GND	A10	GND	D10
PER0p0	A11	PER0p1	D11
GND	A12	GND	D12
PER0p2	A13	PER0p3	D13
GND	A14	GND	D14
PER0p4	A15	PER0p5	D15
GND	A16	GND	D16
PER0p6	A17	PER0p7	D17
GND	A18	GND	D18
REFCLK+0	A19	WAKE#[1]	D19
PET0n0	B1	PET0n1	E1
GND	B2	GND	E2
PET0n2	B3	PET0n3	E3
GND	B4	GND	E4
PET0n4	B5	PET0n5	E5
GND	B6	GND	E6
PET0n6	B7	PET0n7	E7
GND	B8	GND	E8

Pin Description	Number	Pin Description	Number
NC	B9	NC	E9
GND	B10	GND	E10
PER0n0	B11	PER0n1	E11
GND	B12	GND	E12
PER0n2	B13	PER0n3	E13
GND	B14	GND	E14
PER0n4	B15	PER0n5	E15
GND	B16	GND	E16
PER0n6	B17	PER0n7	E17
GND	B18	GND	E18
REFCLK-0	B19	ROOT0#[1]	E19
3.3V	C1	VPWR	F1
TRST#	C2	MRSTI#	F2
3.3V	C3	VPWR	F3
TCK	C4	MRSTO#[1]	F4
3.3v	C5	VPWR	F5
TMC	C6	+12V	F6
3.3v	C7	VPWR	F7
TDI	C8	-12V	F8
NC	C9	VPWR	F9
TDO	C10	GA0	F10
MBIST#	C11	VPWR	F11
GA1	C12	MPRESENT#	F12
3.3V AUX	C13	VPWR	F13
GA2	C14	MSDA	F14
NC	C15	VPWR	F15
MVMRO	C16	MSCL	F16
NC	C17	NC	F17
NC	C18	NC	F18
NC	C19	NC	F19

Table 2-22 Jx6 XMC Rear I/O Signals[1]

Pin Description	Number	Pin Description	Number
DP00_P	A1	DP01_P	D1
GND	A2	GND	D2
DP02_P	A3	DP03_P	D3
GND	A4	GND	D4
DP04_P	A5	DP05_P	D5
GND	A6	GND	D6
DP06_P	A7	DP07_P	D7
GND	A8	GND	D8
DP08_P	A9	DP09_P	D9
GND	A10	GND	D10

Pin Description	Number	Pin Description	Number
DP10_P	A11	DP11_P	D11
GND	A12	GND	D12
DP12_P	A13	DP13_P	D13
GND	A14	GND	D14
DP14_P	A15	DP15_P	D15
GND	A16	GND	D16
DP16_P	A17	DP17_P	D17
GND	A18	GND	D18
DP18_P	A19	DP19_P	D19
DP00_N	B1	DP01_N	E1
GND	B2	GND	E2
DP02_N	B3	DP03_N	E3
GND	B4	GND	E4
DP04_N	B5	DP05_N	E5
GND	B6	GND	E6
DP06_N	B7	DP07_N	E7
GND	B8	GND	E8
DP08_N	B9	DP09_N	E9
GND	B10	GND	E10
DP10_N	B11	DP11_N	E11
GND	B12	GND	E12
DP12_N	B13	DP13_N	E13
GND	B14	GND	E14
DP14_N	B15	DP15_N	E15
GND	B16	GND	E16
DP16_N	B17	DP17_N	E17
GND	B18	GND	E18
DP18_N	B19	DP19_N	E19
User_SEU1	C1	NC	F1
User_SEU2	C2	NC	F2
NC	C3	NC	F3
NC	C4	NC	F4
NC	C5	NC	F5
NC	C6	NC	F6
NC	C7	NC	F7
NC	C8	NC	F8
NC	C9	NC	F9
NC	C10	NC	F10
NC	C11	NC	F11
NC	C12	NC	F12
NC	C13	NC	F13
NC	C14	NC	F14
NC	C15	NC	F15

Pin Description	Number	Pin Description	Number
NC	C16	NC	F16
NC	C17	NC	F17
NC	C18	NC	F18
NC	C19	NC	F19

1. In VPX Connector pinouts P4/P6 the name is preceded by XMC1 or XMC2 depending on Slot.

FIELD GROUNDING CONSIDERATIONS

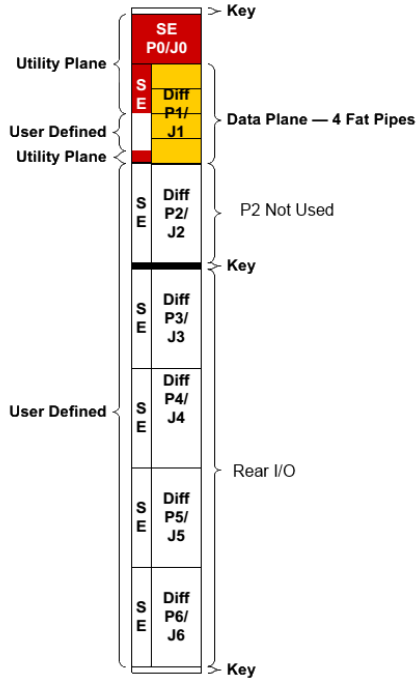
Carrier boards are designed with passive filters on each supply line to each XMC/PMC module. This provides maximum filtering and signal decoupling between the XMC modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the PCIe bus and the XMC module power supply returns. Therefore, unless isolation is provided on the XMC module itself, the field I/O connections are not isolated from the PCIe bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the XMC input/output modules.

All metalwork on this product will be connected to chassis ground which is isolated from the board ground. However this does not guarantee isolation as other components in your system may interconnect these two grounds. All system integrators should check all ground connections to prevent any current from running though the VPX4821A chassis ground.

3. VPX CONNECTIVITY

VITA 65 PROFILES

The VPX4821A and VPX4821ACC match the following VITA 65 Module Profiles: MOD6-PER-4F-12.3.1-2, MOD6-PER-4F-12.3.1-3, MOD6-PER-2F-12.3.2-1, MOD6-PER-2F-12.3.2-2, MOD6-PER-1U-12.3.3-1, MOD6-PER-1U-12.3.3-2, MOD6-PER-1F-12.3.4-1, and MOD6-PER-1F-12.3.4-2.
The profile chart for MOD6-PER-4F-12.3.1-2 is as follows.



The customer is responsible for checking compatibility of the VPX4821A with their VPX backplane as well as managing the interconnect between boards. All the PCIe lanes are connected to P1, the data plane. Further information can be found in VITA 65.

REAR I/O

The Rear is mapped per VITA 46.9, method P64s+X12d+X8D. This mapping is shown in the diagram on the following page. Note per the errata attached to VITA 46.9 that the polarity of the XMC twisted pairs is reversed compared to the VITA 42 specification. Please refer to VITA 46.9 for further information.

XMC Rear I/O is routed differentially with 100 Ohm impedance and matched length.

PMC Rear I/O is routed differentially with 100 Ohm impedance and best effort to match length. Match lengths will be done in groups of four.

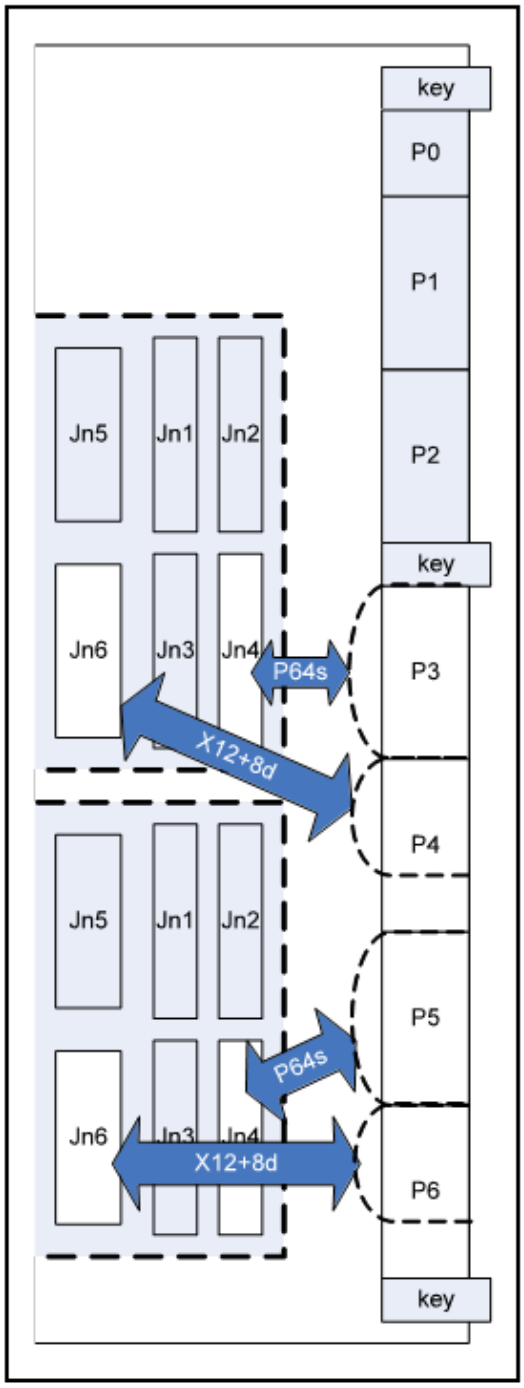


Figure 4: 6U Carrier P64s+X12d+X8d Mapping Diagram

4. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the carrier and/or XMC/PMC with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at https://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

Application Notes

Frequently Asked Questions (FAQ’s)

Product Knowledge Base

Tutorials

Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

5. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length .....9.187 inches (233.35 mm) Maximum
Height.....6.299 inches (159.99 mm) Maximum
Width .....VPX4821A-XX-LF 0.8" inch air cooled. 1.0" front panels available upon request.
.....VPX4821A-XX-CC-LF 0.8" Conduction Cooled.
Unit Weight.....1.435 lb (0.651 kg) (does not include shipping material)

Connectors

Refer to the Connector Section located early in this manual for pin outs.

Jumpers

J1, J2, J3, J4, J5, and J6 .....Control PCIe strapping signals, clk setup, and JTAG power settings. Refer to the Jumper section located earlier in this manual for more information.

POWER

Board power requirements are a function of the installed XMC module and of the carrier card. The carrier board supports up to four power supplies from the VPX Backplane +12V, +3.3V_AUX, +12V_AUX, -12V_AUX. The +5V and +3.3V supplies for the XMC/PMC modules are generated by on-board DC/DC converters from the +12V backplane supply.

Currents specified are for the carrier board only for Model VPX4821A, add the XMC module currents for the total current required from each supply. The major power components are listed below to assist with power calculations

Table 5-1 VPX4821A Internal Power usage typical.

Voltage	PCIe Switch[2]	PCIe-PCI Bridge[3]	Watts	Power from +12V[1]
+0.9V	3.264A		2.938W	3.53W
+1.8V	0.383A		0.69W	0.83W
+1.2V		0.61A	1.81W	2.17W
+3.3V		0.17A	0.56W	0.672W

1. Assume 83% from on board DC/DC
2. Assume 8 lane operation,Gen 2. Typical.
3. Per PMC Slot Used. Typical

+12 Volts (±5%).....900 mA typ, 2A Maximum.
+12V_AUX, -12V_AUX.....not used Supplied to PMC/XMC modules only.
+3.3V_AUX.....25mA typical, 50mA maximum.
Sequencing.....All power supplies will ramp up with 400us of bus power. Onboard supplies will ramp up together once **VS1 (+12V)** has exceeded 2.5V. Note that there is no onboard detection to determine if +12V is within specification.

XMC/PMC Power

The maximum power provided to the XMC/PMC modules is limited due to onboard DC/DC converters. Both the +3.3V and +5V supplies are generated on the carrier board. The total limits for the supplies are provided in the table below. Be sure to add up supplies for both XMC/PMC and do not exceed the limits below. Note that each DC/DC can provide up to 12A inrush. Exceeding these limits will cause the on-board supplies to automatically shut down. Furthermore, never exceed using more then 1A per power pin on the PMC/XMC modules. Resistance losses can mount when more then 1A per power pin is used and Acromag can no longer guarantee that the voltage falls within specification.

Table 5-2 Total Power Available for PMC/XMC modules

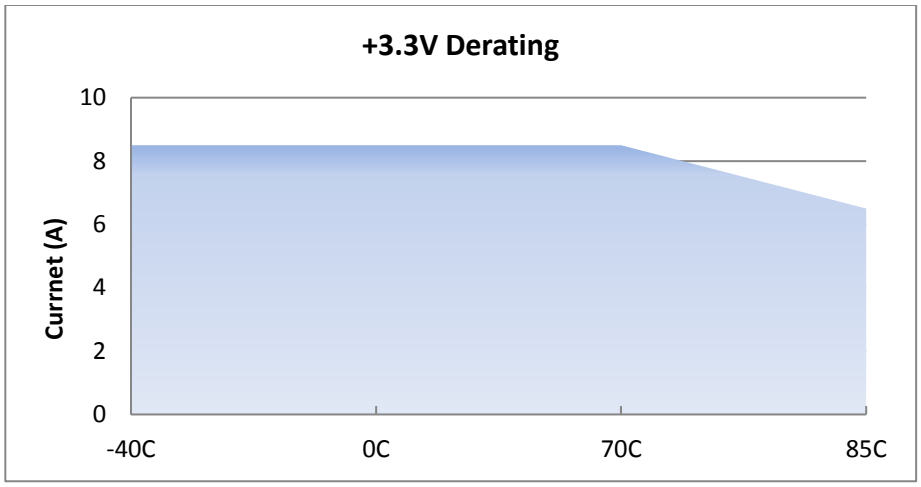
Voltage	Total Power Available	On-board usage	Derating[2] above
+3.3V	8A	0.5A	70°C
+5V	8A	0A	70°C
+12V	6A[1]	0.9A	NA
+12V_AUX	1A	0A	NA
-12V_AUX	1A	0A	NA
+3.3V_AUX	1A	0.05A	NA

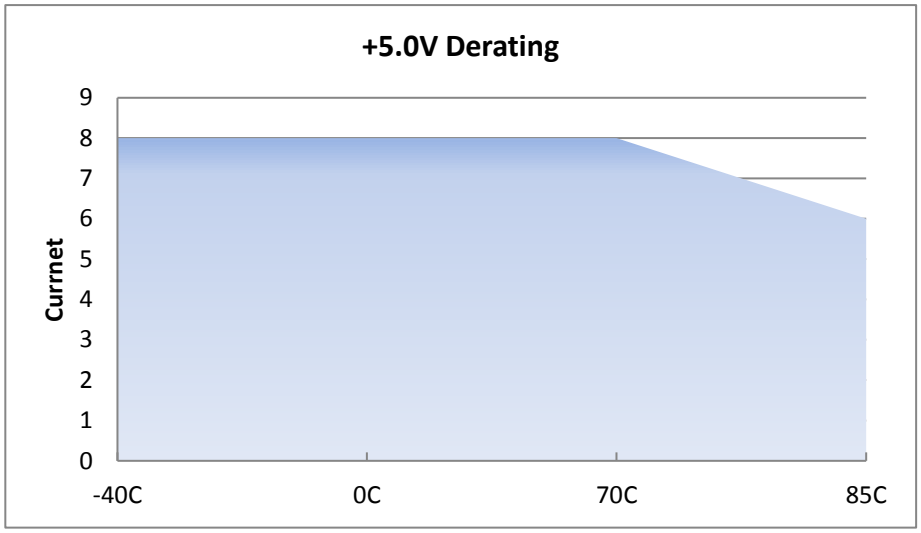
1. +12V From backplane, Assume 6A available (72W) to generate +3.3, +5.0V supplies.
2. Derating is required above this temperature due to DC/DC. See Power dissipation section below. Note that extra allowance of 0.5A is available on the CC modules due to the addition of a heat sink.

Power Dissipation

Power dissipation is a complicated issue on the carrier card. The maximum allowable die temperature is 125°C for the critical components on the board. Beyond this point, the DC/DC and the PCIe switch will automatically be disabled to prevent overheating. Furthermore thermal restrictions on the DC/DC IC's for +3.3V and +5.0V supplies will limit supply current to the XMC/PMC modules dependent on ambient temperature. As such as you proceed to calculate maximum power dissipation you take into consideration how much +3.3V and +5.0V power you are using as well as the overall power usage.

The first two charts give the Amperage derating for +3.3V and +5.0V supplies. For conduction cooled boards Acromag limits the maximum power to 0.5A above the 85C limit. This will guarantee full functionality over the full power rating of the XMC/PMC modules.





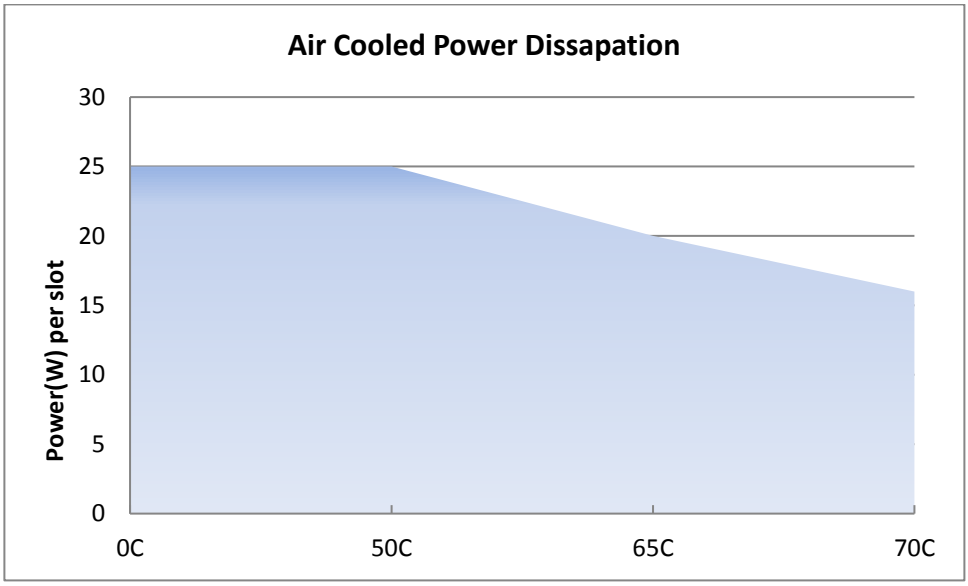
Assuming that your XMC/PMC current supply requirements are met then you can move to the total XMC/PMC power dissipation calculation.

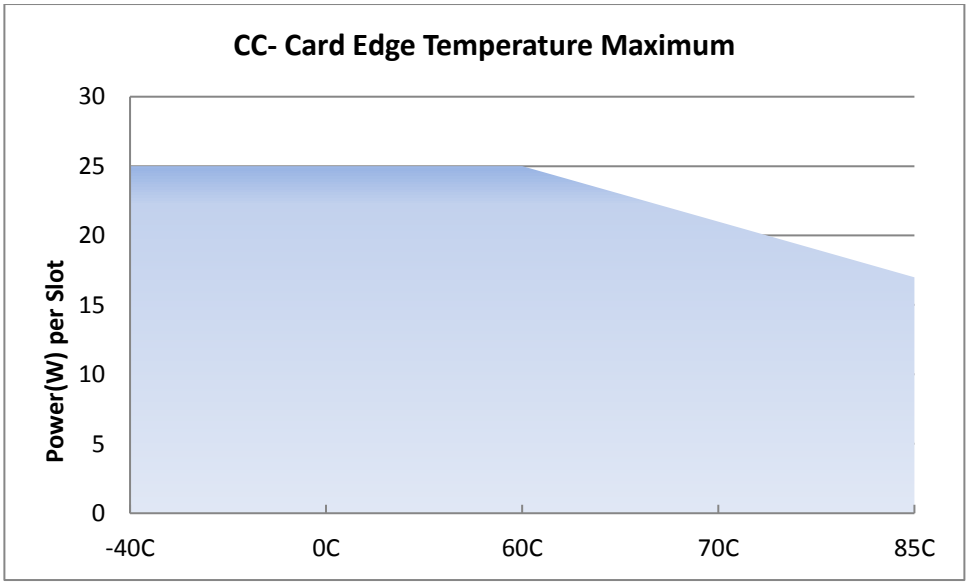
Power Dissipation .....25W Maximum per XMC/PMC. See derating information below.

While Acromag can test temperature with a given thermal dissipation we do not guarantee that the individual chips on the XMC/PMC boards will not go into thermal shutdown. Each XMC/PMC module used must be fully rated at the temperature and power usage specified and MUST be connected to the midplane on conduction cooled frame for maximum effectiveness.

The two charts below give the maximum power dissipation (per slot) for both air cooled and conduction cooled boards. For air cooled boards it is assume air flow of at least 200cfm across the module. Conduction cooled conditions assume a 6U Conduction cooled chassis with the first 3 adjacent slots populate with power board, CPU, and the VPX4821A. The test board was an XMC and PMC module modified with power resistors to induce specific

currents. The Resistors are provided a direct cooling path to either the conduction cooled ring or the midplane.





PCIe BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI Express specifications per revision 2.0. *Note: PCIe Gen 2 signal rates exceed the rated bandwidth of the XMC connectors. While testing to Gen2 signals was completed, Acromag cannot certify Gen2 compliance with non-Acromag products.*

Switch.....A PLX Tech PEX8734 Gen 2.0 PCIe switch is used for the routing of PCIe signals.

Maximum PCIe trace length on XMC module... 500mils Recommended for Gen2 compliance.

Clock…..Jumper selectable between VPX P0 SYSCLK and an on board generated clock.
SYSCLK Requirements (if used)…….100MHz 200ppm, J_{RMS-HF} 3.1ps RMS, J_{RMS-LF} 3.0ps RMS

PCI BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI specifications per revision 3.0 and PCI-X revision 2.0. PCI will operate at 33Mhz or 66HZ. PCI-X will operation at 66MHz or 133MHz at either 32 or 64 bits. Other operational frequencies are available, contact the factory for details.

XMC/PMC Slot Selection

Auto negotiate…… ..PCIe, PCI-X, and PCI offer auto negotiation for bus width and speed. If you insert and XMC module it will automatically be detected via the MPRESENT# signal and disable the PMC PCI interface. Vice versa if no XMC is present, the PCI Interface to the PMC module is enable. If no PMC module is detected, then the PCIe to PCI bridge will go into low power mode since it is unused.

Rear I/O

Specification….....Rear I/O is compliant to VITA 46.9. Slot A is mapped P3w1-P64s+P4w1-X12d+X8d Slot B is mapped P5w1-P64s+P6w1-X12d+X8d.

ENVIRONMENTAL

ENVIRONMENTAL

Operating Temperature.....VPX4821A-XX-LF 0 to +70°C
.....VPX4821A-XX-CC-LF -40°C to +85°C. Max card edge temp 85°C
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +100°C

EMC Compliance

Radiated Field Immunity.....Designed to comply with IEC61000-4-3 class A
Surge Immunity.....Not required for signal I/O per European Norm EN61000-6-1
Electric Fast Transient Immunity…Designed to comply with IEC61000-4-4 class A
Radiated Emissions .....Designed to comply with CISPR 16-2-3 class A
Electrostatic Discharge .....Designed to comply with IEC6100-4-2 Level 2
Conducted Radio Frequency Interference
Designed to comply with IEC6100-4-6 class A

PCIe Non-Isolated .....The PCIe bus and the XMC module commons have a direct electrical connection. As such unless the XMC module provides isolation between the logic and user I/O signals, the user I/O signals are not isolated from the PCIe bus.
Chassis Ground…….Chassis Ground is electrical isolated (floating) from all digital (power) grounds on the board. All metal work is attached is chassis ground.

Certificate of Volatility

Certificate of Volatility				
Acromag Model VPX4821A-XX-LF VPX4821A-XX-CC-LF ACRO5392-CC	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) EEPROM	Size: 2kb	User Modifiable ■ Yes □ No	Function: Storage of Code IPMI information	Process to Sanitize: Clear Memory by erasing. Note device is empty when first shipped.
Type(EEPROM, Flash, etc.) EEPROM	Size: 4096x8-bit	User Modifiable ■ Yes □ No	Function: Storage for initialization of PCIe Switch PEX8734	Process to Sanitize: Clear Memory by erasing. Note device is empty when first shipped.
Type(EEPROM, Flash, etc.) EEPROM	Size: 4096x8-bit	User Modifiable □ Yes ■ No	Function: Storage of Code for PCIe/PCI bridge TSI384 (Device is not populated in default build)	Process to Sanitize: Not Applicable

6. REVISION HISTORY

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
18 AUG 2014	A	CAB	INITIAL RELEASE
13 JUN 2017	B	LMP/MJO	Updates for new PEX8743 Switch of VPX4821A
19 APR 2019	C	RMG/LMP/ARP	Fixed “Error” messages, table numbering and contact information. Updated “Reset” section.
3-SEPT-2019	D	LMP/ARP	Change Ordering Information.

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