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# XMCAP2022 XMC AcroPack Carrier Boards

## For ARCX Applications

# USER'S MANUAL

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# 1. GENERAL INFORMATION

## Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

## Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

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## Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

## XMCAP2022 OVERVIEW

The XMCAP2022 is a carrier for mini-PCIe or AcroPack mezzanine modules in an XMC form factor. This carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. AcroPack modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with AcroPack modules may replace several dedicated function XMC modules.

### Ordering Information

The XMCAP2022-LF was designed for use in the ARCX4000 series. It is the same as the XMCAP2021-LF but with different routing to the Rear I/O connectors P14 and P16.

| Model | I/O Type |
|---|---|
| XMCAP2022-LF | Rear (P14 & P16) For ARCX4000 applications |

## KEY XMCAP2022 FEATURES

**Interface for AcroPack modules** – The XMCAP2022 provides an electrical and mechanical interface for up to two industry standard mini-PCIe or AcroPack modules. AcroPack modules are available from Acromag. Mini-PCIe cards are available from other vendors in a wide variety of input/output configurations to meet the needs of varied applications.

**PCI Express Version 2.1 Compliant Carrier: -** Includes a PCIe switch to allow two PCIe devices (AcroPack or mini-PCIe) to share a single XMC slot on the XMC carrier.

**Board Identification –** A unique carrier and site number can be set for each AcroPack site automatically by geographical address bits or by DIP switch. This feature provides the capability to distinguish a particular AcroPack module from others when multiple instances of the same module are used in a system.

**JTAG Programming Header –** JTAG programming is supported both through the XMC P15 connector, as well as through a Molex 78171-5006 6-pin micro connector (J3). This connection is provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the two AcroPack modules are daisy-chained.

## SIGNAL INTERFACE PRODUCTS

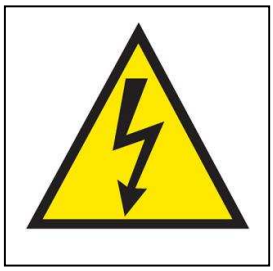
This AcroPack carrier board will mate directly to most industry standard mini-PCIe and AcroPack modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual AcroPack modules):

### JTAG Adapter Cable

Model 5028-564 JTAG Adapter Cable connects between J3 and a Xilinx USB programmer. This cable is only required if JTAG is not available on the XMC carrier through the P15 XMC connector.

## 2. PREPARATION FOR USE

### IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS





It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

***WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.*** This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

### UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

## BOARD CONFIGURATION

Power should be removed from the board when changing switch configurations or when installing AcroPack modules, cables and field wiring.

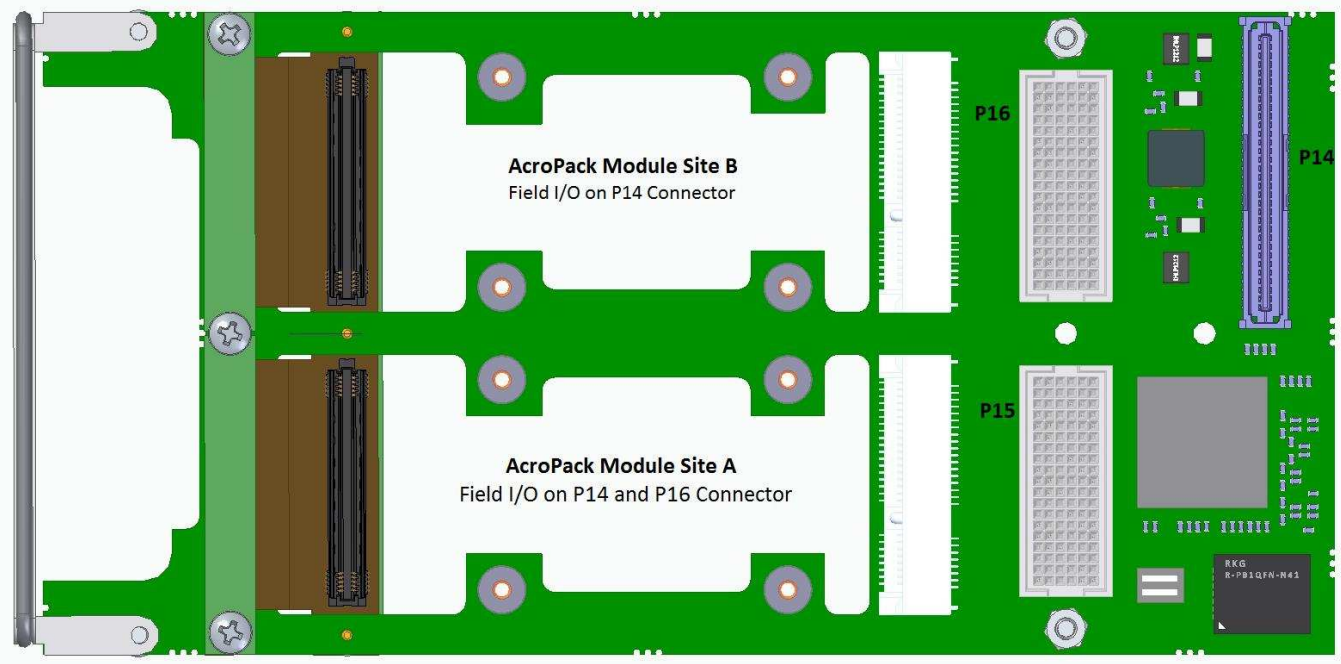



**Figure 1 XMCAP2022 Primary Side**

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed AcroPack modules within the voltage tolerances specified.

**IMPORTANT: Adequate thermos conduction must be provided to prevent a temperature rise above the maximum operating temperature.**

The lack of thermo conduction from the XMC carrier could be a cause for some concern. Adequate thermo conduction must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics.

## CARRIER ADDRESS ASSIGNMENT

Following are the instructions for setting the slot address of the carrier. By assigning a unique address to each carrier, system software can distinguish this carrier from other similarly configured carriers installed in a system.

Address bits A0, A1, and A2 are connected to the corresponding Geographical Addressing (GA) bits of the XMC P15 connector. This should automatically assign a unique address to the XMCAP2022 board.

If the GA bits are not supplied by the XMC carrier onto which the XMCAP2022 board is installed, SW1 may be used to select address bits A3 and A4. Figure 1 shows the location of switch SW1. Set the switch state as shown in Table 1 below to assign a unique slot address to this carrier.

**Table 1 Switch SW1 assignments**

| SW1 Position | Address Bit | Value |
|---|---|---|
| 1-2 | A3 | 1 |
| 2-3 | | 0 |
| 4-5 | A4 | 1 |
| 5-6 | | 0 |

## ACROPACK HEATSINKING

Most applications require the use of a nonstandard heatsink. Consult the factory for each application. See Appendix A for the installation of the heatsink.

Available XMCAP202x heatsinks for use in ARCX box applications:

- AP-CC-02: Dual generic AcroPack (left rail or single wide ARCX)
- AP-CC-03: AP57x with generic AP (left rail or single wide ARCX)
- AP-CC-05: Dual generic AP (right rail)

Where “generic” AcroPack refers to:

- AP220-16E-LF
- AP225-16E-LF
- AP226-8E-LF
- AP231-16E-LF
- AP235-16E-LF
- AP236-8E-LF
- AP323E-LF
- AP341E-LF
- AP342E-LF
- AP408E-LF

- AP418E-LF
- AP445E-LF
- AP471E-LF
- AP482/3/4E-LF
- AP500E-LF
- AP512E-LF
- AP520-64E-LF
- AP521-64E-LF
- AP522E-LF
- APA7-201/2/3/4E-LF
- APA7-501/2/3/4E-LF

## ACROPACK MODULE INSTALLATION

Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring. Refer to Figure 4 while reading this section. Place the XMCAP2022 flat on an anti-static surface for support. To install, first insert the edge of the AcroPack module into the carrier connector at an angle similar to that shown in the figure. Next, using a rocking motion while gently applying force to keep the edge of the board against the back of the carrier connector, position the module such that the field I/O connector is just above the mating connector. Verify that the two connectors are properly aligned. Once alignment is achieved, you can fully seat the connector. It will snap into place. Install four M2.5 screws as shown.

Refer to Appendix B for the installation of the XMC card into the ARCX XMC site.

**Note: The AP441E-LF is not recommended for use with the XMC AcroPack carrier.**

***WARNING: When installing a commercial mini-PCIe module onto the XMCAP2022 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.***

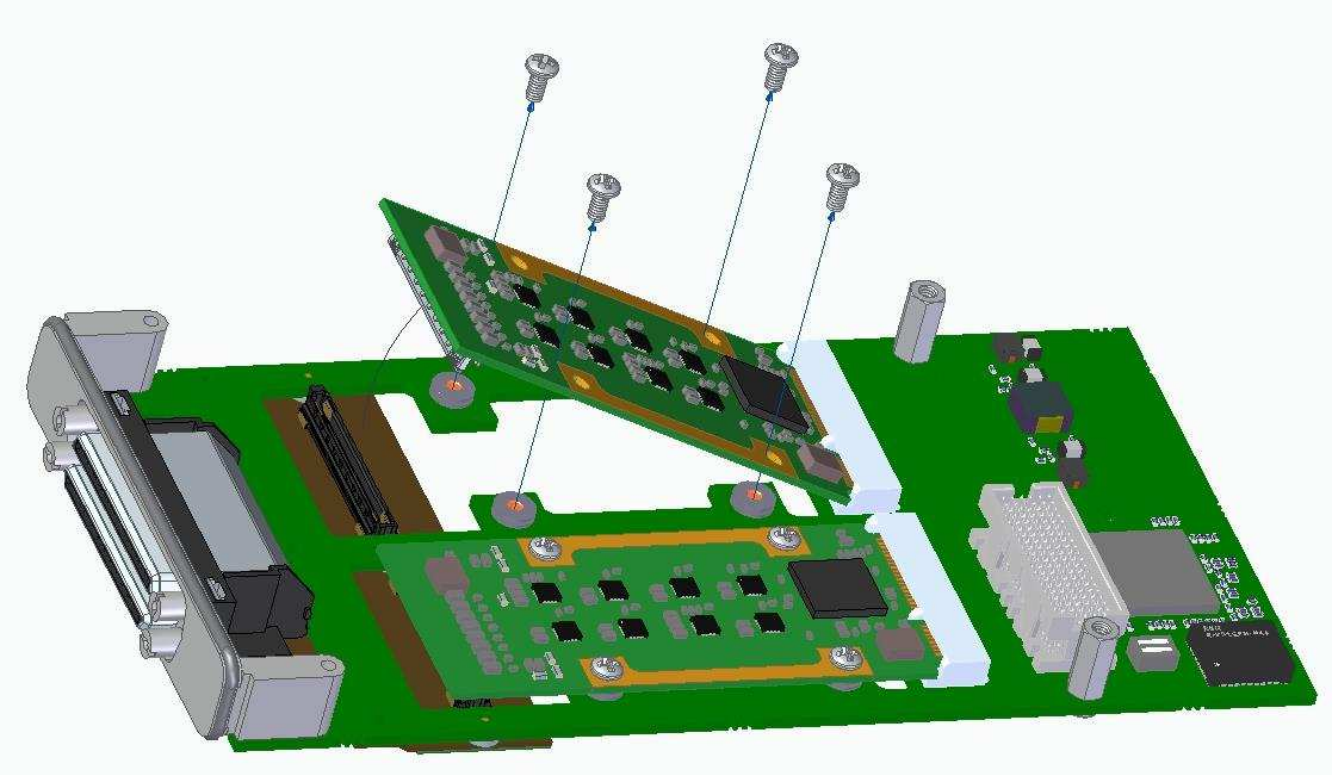


**Figure 4 AcroPack Module Installation**

## FIELD GROUNDING CONSIDERATIONS

Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AcroPack input/output modules.

## CONNECTORS

The XMCAP2022 carrier uses two AcroPack module field I/O connectors, two mini-PCIe connectors, two field I/O connectors (rear P14 & P16 connectors for XMCAP2022) and one XMC bus interface connector. These are discussed in the following sections.

### Rear Field I/O Connectors

Field I/O connections on the XMCAP2022 model are made via the P14 and P16 connectors. The Field I/O connections from the AcroPack module in Site A are available through the XMC P16 and PMC P14 connector. The Field I/O connections from the AcroPack module in Site B are available through the PMC P14 connector.

See Table 2.A below for pin assignments for Slot A and Table 2.B for pin assignments for Slot B.

### AcroPack Field I/O Connectors

The field side connector of AcroPack modules mate to Samtec SS5-50-3.00-L-D-K-TR socket connectors on the carrier board.

This provides excellent connection integrity due to the gold plating in the mating area. M2.5 screws and spacers provide additional stability for harsh environments.

The functions of each of the Field I/O signals are defined by the installed AcroPack model.

**Table 2.A Field I/O Pin Assignments AcroPack A**

| XMCAP2022 Rear I/O Connection (Site A - P16) | XMCAP2022 Rear I/O Connection (Site A - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR | Module Pin Number | Field A I/O Signal |
|---|---|---|---|---|
| C3 | | 2 | 2 | Field A I/O 1 |
| C2 | | 1 | 1 | Field A I/O 2 |
| | | 4 | 4 | Reserved/isolation |
| | | 3 | 3 | Reserved/isolation |
| C5 | | 6 | 6 | Field A I/O 3 |
| C4 | | 5 | 5 | Field A I/O 4 |
| | | 8 | 8 | Reserved/isolation |
| | | 7 | 7 | Reserved/isolation |
| F5 | | 10 | 10 | Field A I/O 5 |
| F4 | | 9 | 9 | Field A I/O 6 |
| | | 12 | 12 | Reserved/isolation |
| | | 11 | 11 | Reserved/isolation |
| F7 | | 14 | 14 | Field A I/O 7 |
| F6 | | 13 | 13 | Field A I/O 8 |
| | | 16 | 16 | Reserved/isolation |
| | | 15 | 15 | Reserved/isolation |
| F19 | | 18 | 18 | Field A I/O 9 |
| F18 | | 17 | 17 | Field A I/O 10 |
| | | 20 | 20 | Reserved/isolation |
| | | 19 | 19 | Reserved/isolation |
| C19 | | 22 | 22 | Field A I/O 11 |
| C18 | | 21 | 21 | Field A I/O 12 |
| | | 24 | 24 | Reserved/isolation |
| | | 23 | 23 | Reserved/isolation |

| XMCAP2022 Rear I/O Connection (Site A - P16) | XMCAP2022 Rear I/O Connection (Site A - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR | Module Pin Number | Field A I/O Signal |
|---|---|---|---|---|
| C7 | | 26 | 26 | Field A I/O 13 |
| C6 | | 25 | 25 | Field A I/O 14 |
| | | 28 | 28 | Reserved/isolation |
| | | 27 | 27 | Reserved/isolation |
| F1 | | 30 | 30 | Field A I/O 15 |
| C1 | | 29 | 29 | Field A I/O 16 |
| | | 32 | 32 | Reserved/isolation |
| | | 31 | 31 | Reserved/isolation |
| C9 | | 34 | 34 | Field A I/O 17 |
| C8 | | 33 | 33 | Field A I/O 18 |
| | | 36 | 36 | Reserved/isolation |
| | | 35 | 35 | Reserved/isolation |
| F3 | | 38 | 38 | Field A I/O 19 |
| F2 | | 37 | 37 | Field A I/O 20 |
| | | 40 | 40 | Reserved/isolation |
| | | 39 | 39 | Reserved/isolation |
| F11 | | 42 | 42 | Field A I/O 21 |
| F10 | | 41 | 41 | Field A I/O 22 |
| | | 44 | 44 | Reserved/isolation |
| | | 43 | 43 | Reserved/isolation |
| F8 | | 46 | 46 | Field A I/O 23 |
| F9 | | 45 | 45 | Field A I/O 24 |
| | | 48 | 48 | Reserved/isolation |
| | | 47 | 47 | Reserved/isolation |
| | 62 | 50 | 50 | Field A I/O 25 |
| | 64 | 49 | 49 | Field A I/O 26 |
| | | 52 | 52 | Reserved/isolation |
| | | 51 | 51 | Reserved/isolation |
| | 56 | 54 | 54 | Field A I/O 27 |
| | 54 | 53 | 53 | Field A I/O 28 |
| | | 56 | 56 | Reserved/isolation |
| | | 55 | 55 | Reserved/isolation |
| F13 | | 58 | 58 | Field A I/O 29 |
| F12 | | 57 | 57 | Field A I/O 30 |
| | | 60 | 60 | Reserved/isolation |

| XMCAP2022 Rear I/O Connection (Site A - P16) | XMCAP2022 Rear I/O Connection (Site A - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR | Module Pin Number | Field A I/O Signal |
|---|---|---|---|---|
| | | 59 | 59 | Reserved/isolation |
| C10 | | 62 | 62 | Field A I/O 31 |
| C11 | | 61 | 61 | Field A I/O 32 |
| | | 64 | 64 | Reserved/isolation |
| | | 63 | 63 | Reserved/isolation |
| | 58 | 66 | 66 | Field A I/O 33 |
| | 60 | 65 | 65 | Field A I/O 34 |
| | | 68 | 68 | Reserved/isolation |
| | | 67 | 67 | Reserved/isolation |
| C15 | | 70 | 70 | Field A I/O 35 |
| C14 | | 69 | 69 | Field A I/O 36 |
| | | 72 | 72 | Reserved/isolation |
| | | 71 | 71 | Reserved/isolation |
| F15 | | 74 | 74 | Field A I/O 37 |
| F14 | | 73 | 73 | Field A I/O 38 |
| | | 76 | 76 | Reserved/isolation |
| | | 75 | 75 | Reserved/isolation |
| | 59 | 78 | 78 | Field A I/O 39 |
| | 57 | 77 | 77 | Field A I/O 40 |
| | | 80 | 80 | Reserved/isolation |
| | | 79 | 79 | Reserved/isolation |
| | 50 | 82 | 82 | Field A I/O 41 |
| | 52 | 81 | 81 | Field A I/O 42 |
| | | 84 | 84 | Reserved/isolation |
| | | 83 | 83 | Reserved/isolation |
| C13 | | 86 | 86 | Field A I/O 43 |
| C12 | | 85 | 85 | Field A I/O 44 |
| | | 88 | 88 | Reserved/isolation |
| | | 87 | 87 | Reserved/isolation |
| F17 | | 90 | 90 | Field A I/O 45 |
| F16 | | 89 | 89 | Field A I/O 46 |
| | | 92 | 92 | Reserved/isolation |
| | | 91 | 91 | Reserved/isolation |
| | 63 | 94 | 94 | Field A I/O 47 |
| | 61 | 93 | 93 | Field A I/O 48 |

| XMCAP2022 Rear I/O Connection (Site A - P16) | XMCAP2022 Rear I/O Connection (Site A - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR | Module Pin Number | Field A I/O Signal |
|---|---|---|---|---|
| | | 96 | 96 | Reserved/isolation |
| | | 95 | 95 | Reserved/isolation |
| | 55 | 98 | 98 | Field A I/O 49 |
| | 53 | 97 | 97 | Field A I/O 50 |
| | | 100 | 100 | Reserved/isolation |
| | | 99 | 99 | Reserved/isolation |

### Table 2.B Field I/O Pin Assignments AcroPack B

| XMCAP2022 Rear I/O Connection (Site B - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K- | Module Pin Number | Field B I/O Signal |
|---|---|---|---|
| 1 | 2 | 2 | Field B I/O 1 |
| 3 | 1 | 1 | Field B I/O 2 |
| | 4 | 4 | Reserved/isolation |
| | 3 | 3 | Reserved/isolation |
| 2 | 6 | 6 | Field B I/O 3 |
| 4 | 5 | 5 | Field B I/O 4 |
| | 8 | 8 | Reserved/isolation |
| | 7 | 7 | Reserved/isolation |
| 5 | 10 | 10 | Field B I/O 5 |
| 7 | 9 | 9 | Field B I/O 6 |
| | 12 | 12 | Reserved/isolation |
| | 11 | 11 | Reserved/isolation |
| 6 | 14 | 14 | Field B I/O 7 |
| 8 | 13 | 13 | Field B I/O 8 |
| | 16 | 16 | Reserved/isolation |
| | 15 | 15 | Reserved/isolation |
| 9 | 18 | 18 | Field B I/O 9 |
| 11 | 17 | 17 | Field B I/O 10 |
| | 20 | 20 | Reserved/isolation |
| | 19 | 19 | Reserved/isolation |
| 10 | 22 | 22 | Field B I/O 11 |
| 12 | 21 | 21 | Field B I/O 12 |
| | 24 | 24 | Reserved/isolation |

| XMCAP2022 Rear I/O Connection (Site B - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K- | Module Pin Number | Field B I/O Signal |
|---|---|---|---|
| | 23 | 23 | Reserved/isolation |
| 13 | 26 | 26 | Field B I/O 13 |
| 15 | 25 | 25 | Field B I/O 14 |
| | 28 | 28 | Reserved/isolation |
| | 27 | 27 | Reserved/isolation |
| 14 | 30 | 30 | Field B I/O 15 |
| 16 | 29 | 29 | Field B I/O 16 |
| | 32 | 32 | Reserved/isolation |
| | 31 | 31 | Reserved/isolation |
| 17 | 34 | 34 | Field B I/O 17 |
| 19 | 33 | 33 | Field B I/O 18 |
| | 36 | 36 | Reserved/isolation |
| | 35 | 35 | Reserved/isolation |
| 18 | 38 | 38 | Field B I/O 19 |
| 20 | 37 | 37 | Field B I/O 20 |
| | 40 | 40 | Reserved/isolation |
| | 39 | 39 | Reserved/isolation |
| 21 | 42 | 42 | Field B I/O 21 |
| 23 | 41 | 41 | Field B I/O 22 |
| | 44 | 44 | Reserved/isolation |
| | 43 | 43 | Reserved/isolation |
| 22 | 46 | 46 | Field B I/O 23 |
| 24 | 45 | 45 | Field B I/O 24 |
| | 48 | 48 | Reserved/isolation |
| | 47 | 47 | Reserved/isolation |
| 25 | 50 | 50 | Field B I/O 25 |
| 27 | 49 | 49 | Field B I/O 26 |
| | 52 | 52 | Reserved/isolation |
| | 51 | 51 | Reserved/isolation |
| 26 | 54 | 54 | Field B I/O 27 |
| 28 | 53 | 53 | Field B I/O 28 |
| | 56 | 56 | Reserved/isolation |
| | 55 | 55 | Reserved/isolation |
| 29 | 58 | 58 | Field B I/O 29 |
| 31 | 57 | 57 | Field B I/O 30 |

| XMCAP2022 Rear I/O Connection (Site B - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K- | Module Pin Number | Field B I/O Signal |
|---|---|---|---|
| | 60 | 60 | Reserved/isolation |
| | 59 | 59 | Reserved/isolation |
| 30 | 62 | 62 | Field B I/O 31 |
| 32 | 61 | 61 | Field B I/O 32 |
| | 64 | 64 | Reserved/isolation |
| | 63 | 63 | Reserved/isolation |
| 33 | 66 | 66 | Field B I/O 33 |
| 35 | 65 | 65 | Field B I/O 34 |
| | 68 | 68 | Reserved/isolation |
| | 67 | 67 | Reserved/isolation |
| 34 | 70 | 70 | Field B I/O 35 |
| 36 | 69 | 69 | Field B I/O 36 |
| | 72 | 72 | Reserved/isolation |
| | 71 | 71 | Reserved/isolation |
| 37 | 74 | 74 | Field B I/O 37 |
| 39 | 73 | 73 | Field B I/O 38 |
| | 76 | 76 | Reserved/isolation |
| | 75 | 75 | Reserved/isolation |
| 38 | 78 | 78 | Field B I/O 39 |
| 40 | 77 | 77 | Field B I/O 40 |
| | 80 | 80 | Reserved/isolation |
| | 79 | 79 | Reserved/isolation |
| 41 | 82 | 82 | Field B I/O 41 |
| 43 | 81 | 81 | Field B I/O 42 |
| | 84 | 84 | Reserved/isolation |
| | 83 | 83 | Reserved/isolation |
| 42 | 86 | 86 | Field B I/O 43 |
| 44 | 85 | 85 | Field B I/O 44 |
| | 88 | 88 | Reserved/isolation |
| | 87 | 87 | Reserved/isolation |
| 45 | 90 | 90 | Field B I/O 45 |
| 47 | 89 | 89 | Field B I/O 46 |
| | 92 | 92 | Reserved/isolation |
| | 91 | 91 | Reserved/isolation |
| 46 | 94 | 94 | Field B I/O 47 |

| XMCAP2022 Rear I/O Connection (Site B - P14) | Carrier P1, P2 Samtec SS5-50-3.00-L-D-K- | Module Pin Number | Field B I/O Signal |
|---|---|---|---|
| 48 | 93 | 93 | Field B I/O 48 |
| | 96 | 96 | Reserved/isolation |
| | 95 | 95 | Reserved/isolation |
| 49 | 98 | 98 | Field B I/O 49 |
| 51 | 97 | 97 | Field B I/O 50 |
| | 100 | 100 | Reserved/isolation |
| | 99 | 99 | Reserved/isolation |

### ARCX 4000 Series Cross Reference

The Table below is a cross-reference for the ARCX box connections.

| Pin 38999 J3/J5* | Pin PMC J14/J24* | Pin XMC J16/J26* | XMCAP2022 Signal Name |
|---|---|---|---|
| 1 | 1 | | Field B I/O 1 |
| 2 | 3 | | Field B I/O 2 |
| 3 | 2 | | Field B I/O 3 |
| 4 | 4 | | Field B I/O 4 |
| 5 | 5 | | Field B I/O 5 |
| 6 | 7 | | Field B I/O 6 |
| 7 | 6 | | Field B I/O 7 |
| 8 | 8 | | Field B I/O 8 |
| 9 | N/A | | #N/A |
| 10 | 9 | | Field B I/O 9 |
| 11 | 11 | | Field B I/O 10 |
| 12 | N/A | | #N/A |
| 13 | 10 | | Field B I/O 11 |
| 14 | 12 | | Field B I/O 12 |
| 15 | N/A | | #N/A |
| 16 | 13 | | Field B I/O 13 |
| 17 | 15 | | Field B I/O 14 |
| 18 | 14 | | Field B I/O 15 |
| 19 | 16 | | Field B I/O 16 |
| 20 | 17 | | Field B I/O 17 |
| 21 | 19 | | Field B I/O 18 |
| 22 | 18 | | Field B I/O 19 |
| 23 | 20 | | Field B I/O 20 |
| 24 | 21 | | Field B I/O 21 |

| Pin 38999 J3/J5* | Pin PMC J14/J24* | Pin XMC J16/J26* | XMCAP2022 Signal Name |
|---|---|---|---|
| 25 | 23 | | Field B I/O 22 |
| 26 | N/A | | #N/A |
| 27 | 22 | | Field B I/O 23 |
| 28 | 24 | | Field B I/O 24 |
| 29 | 25 | | Field B I/O 25 |
| 30 | 27 | | Field B I/O 26 |
| 31 | N/A | | #N/A |
| 32 | 26 | | Field B I/O 27 |
| 33 | 28 | | Field B I/O 28 |
| 34 | 29 | | Field B I/O 29 |
| 35 | 31 | | Field B I/O 30 |
| 36 | N/A | | #N/A |
| 37 | 30 | | Field B I/O 31 |
| 38 | 32 | | Field B I/O 32 |
| 39 | N/A | | #N/A |
| 40 | N/A | | #N/A |
| 41 | 33 | | Field B I/O 33 |
| 42 | 35 | | Field B I/O 34 |
| 43 | 34 | | Field B I/O 35 |
| 44 | 36 | | Field B I/O 36 |
| 45 | N/A | | #N/A |
| 46 | N/A | | #N/A |
| 47 | 37 | | Field B I/O 37 |
| 48 | 39 | | Field B I/O 38 |
| 49 | N/A | | #N/A |
| 50 | 38 | | Field B I/O 39 |
| 51 | 40 | | Field B I/O 40 |
| 52 | 41 | | Field B I/O 41 |
| 53 | 43 | | Field B I/O 42 |
| 54 | N/A | | #N/A |
| 55 | 42 | | Field B I/O 43 |
| 56 | 44 | | Field B I/O 44 |
| 57 | 45 | | Field B I/O 45 |
| 58 | 47 | | Field B I/O 46 |
| 59 | N/A | | #N/A |
| 60 | 46 | | Field B I/O 47 |
| 61 | 48 | | Field B I/O 48 |
| 62 | 49 | | Field B I/O 49 |

| Pin 38999 J3/J5* | Pin PMC J14/J24* | Pin XMC J16/J26* | XMCAP2022 Signal Name |
|---|---|---|---|
| 63 | 51 | | Field B I/O 50 |
| 64 | N/A | | #N/A |
| 65 | 50 | | Field A I/O 41 |
| 66 | 52 | | Field A I/O 42 |
| 67 | 53 | | Field A I/O 50 |
| 68 | 55 | | Field A I/O 49 |
| 69 | N/A | | #N/A |
| 70 | 54 | | Field A I/O 28 |
| 71 | 56 | | Field A I/O 27 |
| 72 | 57 | | Field A I/O 40 |
| 73 | 59 | | Field A I/O 39 |
| 74 | N/A | | #N/A |
| 75 | 58 | | Field A I/O 33 |
| 76 | 60 | | Field A I/O 34 |
| 77 | N/A | | #N/A |
| 78 | 61 | | Field A I/O 48 |
| 79 | 63 | | Field A I/O 47 |
| 80 | N/A | | #N/A |
| 81 | 62 | | Field A I/O 25 |
| 82 | 64 | | Field A I/O 26 |
| 83 | N/A | | #N/A |
| 84 | | C19 | Field A I/O 11 |
| 85 | | C18 | Field A I/O 12 |
| 86 | | F19 | Field A I/O 9 |
| 87 | | F18 | Field A I/O 10 |
| 88 | | C17 | #N/A |
| 89 | | C16 | #N/A |
| 90 | | F17 | Field A I/O 45 |
| 91 | | F16 | Field A I/O 46 |
| 92 | | C15 | Field A I/O 35 |
| 93 | | C14 | Field A I/O 36 |
| 94 | | N/A | #N/A |
| 95 | | F15 | Field A I/O 37 |
| 96 | | F14 | Field A I/O 38 |
| 97 | | N/A | #N/A |
| 98 | | C13 | Field A I/O 43 |
| 99 | | C12 | Field A I/O 44 |
| 100 | | N/A | #N/A |

| Pin 38999 J3/J5* | Pin PMC J14/J24* | Pin XMC J16/J26* | XMCAP2022 Signal Name |
|---|---|---|---|
| 101 | | F13 | Field A I/O 29 |
| 102 | | F12 | Field A I/O 30 |
| 103 | | C11 | Field A I/O 32 |
| 104 | | C10 | Field A I/O 31 |
| 105 | | N/A | #N/A |
| 106 | | F11 | Field A I/O 21 |
| 107 | | F10 | Field A I/O 22 |
| 108 | | C9 | Field A I/O 17 |
| 109 | | C8 | Field A I/O 18 |
| 110 | | N/A | #N/A |
| 111 | | F9 | Field A I/O 24 |
| 112 | | F8 | Field A I/O 23 |
| 113 | | N/A | #N/A |
| 114 | | C7 | Field A I/O 13 |
| 115 | | C6 | Field A I/O 14 |
| 116 | | N/A | #N/A |
| 117 | | F7 | Field A I/O 7 |
| 118 | | F6 | Field A I/O 8 |
| 119 | | N/A | #N/A |
| 120 | | C5 | Field A I/O 3 |
| 121 | | C4 | Field A I/O 4 |
| 122 | | N/A | #N/A |
| 123 | | F5 | Field A I/O 5 |
| 124 | | F4 | Field A I/O 6 |
| 125 | | C3 | Field A I/O 1 |
| 126 | | C2 | Field A I/O 2 |
| 127 | | F3 | Field A I/O 19 |
| 128 | | F2 | Field A I/O 20 |
| 129 | | F1 | Field A I/O 15 |
| 130 | | C1 | Field A I/O 16 |

*J5, J24 and J26 are only available on ARCX-4120 double-wide enclosures.

### Mini-PCIe Connectors

The AcroPack Mini-PCIe connectors mate to TE Connectivity 1759457-1 connectors on the carrier board. AcroPack locations A and B are labeled on the board for easy identification.

Pin assignments for these connectors are based on the Mini-PCIe specification with the exceptions noted in Table 3.

***WARNING: When installing a commercial mini-PCIe module onto the XMCAP2022 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.***

**Table 3 Mini-PCIe Connectors J1 and J2 Pin Assignments**

| Pin # | Name | Pin # | Name |
|---|---|---|---|
| 51 | **+5V**[3] | 52 | +3.3V[4] |
| 49 | **+12V**[3] | 50 | GND |
| 47 | **-12V**[3] | 48 | +1.5V |
| 45 | **Present***[3] | 46 | N.C. (LED_WPAN#)[1] |
| 43 | GND | 44 | N.C. (LED_WLAN#)[1] |
| 41 | +3.3V[4] | 42 | N.C. (LED_WWAN#)[1] |
| 39 | +3.3V[4] | 40 | GND |
| 37 | GND | 38 | N.C. (USB_D+)[1] |
| 35 | GND | 36 | N.C. (USB_D-)[1] |
| 33 | PETX0_P | 34 | GND |
| 31 | PETX0_N | 32 | SMB_DATA[5] |
| 29 | GND | 30 | SMB_CLK[5] |
| 27 | GND | 28 | +1.5V |
| 25 | PERX0_P | 26 | GND |
| 23 | PERX0_N | 24 | +3.3V[4] |
| 21 | GND | 22 | PERST# |
| 19 | **TDI** (UIM_C4)[1,2] | 20 | N.C. (W_DISABLE#)[1] |
| 17 | **TDO** (UIM_C8)[1,2] | 18 | GND |
| 15 | GND | 16 | N.C. (UIM_VPP)[1] |
| 13 | REFCLK_P | 14 | N.C. (UIM_RESET)[1] |
| 11 | REFCLK_N | 12 | N.C. (UIM_CLK)[1] |
| 9 | GND | 10 | N.C. (UIM_DATA)[1] |
| 7 | CLKREQ# | 8 | N.C. (UIM_PWR)[1] |
| 5 | **TCK** (COEX2)[1] | 6 | +1.5V |
| 3 | **TMS** (COEX1)[1] | 4 | GND |
| 1 | N.C. (WAKE#)[1] | 2 | +3.3V[4] |

**Notes:**

1. The following mini-PCIe signals are not supported: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR. The following signals UIM_C4, UIM_C8, COEX2 and COEX1 are repurposed for JTAG.
2. TDI is tied to TDO on modules that do not use JTAG.
3. +5, +12, and -12 Volt power supplies and their control signal have been assigned to pins that are reserved in the mini-PCIe specification. This power is switched

and only supplied when The Present* Pin (45) of the AcroPack module is seen to be grounded.

4. All +3.3Vaux power pins are changed to system +3.3V power.
5. The SM bus signals SMB_CLK and SMB_DATA are used to communicate with a CPLD on the carrier that reports slot ID. These signals will be under the control of the AcroPack module.

### XMC/PCIe Bus Connections

Table4 indicates the pin assignments for the PCIe bus signals at the XMC VITA 42.3 connector P15.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals.

**Table 4 XMC/PCIe Bus P15 CONNECTIONS**

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| **1** | PETX0_P | PETX0_N | +3.3V | PETX1_P | PETX1_N | VPWR |
| **2** | GND | GND | No Connect | GND | GND | PERST* |
| **3** | PETX2_P | PETX2_N | +3.3V | PETX3_P | PETX3_N | VPWR |
| **4** | GND | GND | TCK | GND | GND | No Connect |
| **5** | PETX4_P | PETX4_N | +3.3V | PETX5_P | PETX5_N | VPWR |
| **6** | GND | GND | TMS | GND | GND | +12V_AUX (NC)[3] |
| **7** | PETX6_P | PETX6_N | +3.3V | PETX7_P | PETX7_N | VPWR |
| **8** | GND | GND | TDI | GND | GND | -12V_AUX (NC)[3] |
| **9** | No Connect | No Connect | No Connect | No Connect | No Connect | VPWR |
| **10** | GND | GND | TDO | GND | GND | GA0 |
| **11** | No Connect | No Connect | No Connect | No Connect | No Connect | VPWR |
| **12** | GND | GND | GA1 | GND | GND | GND |
| **13** | No Connect | No Connect | +3.3V_AUX (NC)[2] | No Connect | No Connect | VPWR |
| **14** | GND | GND | GA2 | GND | GND | No Connect |
| **15** | No Connect | No Connect | No Connect | No Connect | No Connect | VPWR |
| **16** | GND | GND | MVMRO* | GND | GND | No Connect |
| **17** | No Connect | No Connect | No Connect | No Connect | No Connect | No Connect |
| **18** | GND | GND | No Connect | GND | GND | No Connect |
| **19** | REFCLK_P | REFCLK_N | No Connect | No Connect | No Connect | No Connect |

**Notes:**

1. Asterisk (*) is used to indicate an active-low signal.
2. +3.3Vaux power is not used by the carrier. Contact Acromag to enable +3.3Vaux power to AcroPack modules and/or ID EEPROM. The carrier provides +3.3V power to the modules.
3. +12V_AUX and -12V_AUX are not used by the carrier. +12V and -12V are created from +3.3V to support XMC carriers that do not supply these voltages.

### JTAG Programming/Debug Connector

JTAG programming/debug is supported through the JTAG signals of the XMC P15 connector. An alternate header is supplied if JTAG is not available from the XMC carrier (See reference designator J3 located on bottom side of

board). JTAG is provided for developing applications that use Acromag's FPGA AcroPack modules. An adapter cable is available to connect to a Xilinx Platform USB II programming device (or equivalent). See Signal Interface Products for ordering information.

The pin assignment for J3 is shown below. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to bypass the TDI and TDO signals. A CPLD on the carrier is included in the JTAG chain. The Xilinx Vivado tools can detect the presence of the CPLD in the JTAG chain, and skip it when accessing the FPGAs on the AcroPack modules.

**Table 1 JTAG Programming/Debug Connector (J3) Pin Assignment**

| Signal | Pin |
|---|---|
| TDI | 1 |
| TDO | 2 |
| GND | 3 |
| TCK | 4 |
| TMS | 5 |
| VREF (3.3V) | 6 |

**Notes:**

TMS – **JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.

TCK – **JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.

TDO – **JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.

TDI – **JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

$V_{REF}$ – The target reference voltage $V_{REF}$ is 3.3 Volts

GND – Signal Return

# 3. PROGRAMMING INFORMATION

This XMCAP2022 carrier board has no end user programmable components. The PCIe switch on the carrier is transparent to the end user.

# 4. THEORY OF OPERATION

This section describes the functionality of the circuitry used on the carrier board. Refer to Figure 6 as you read this section.

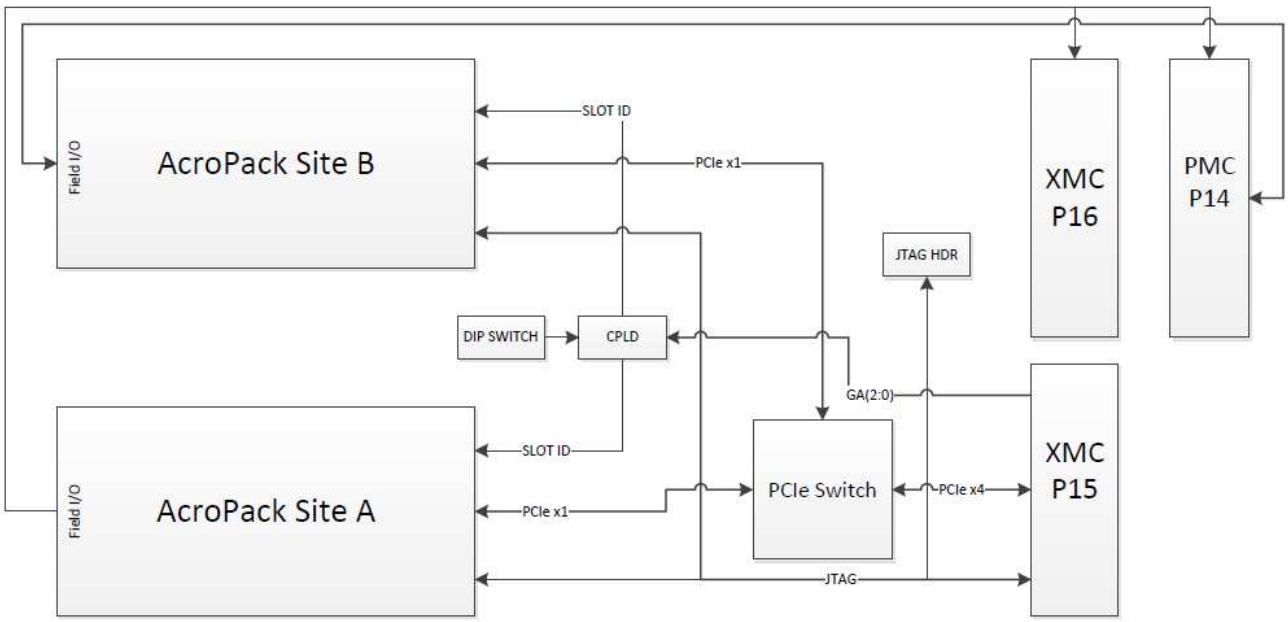



**Figure 6 XMCAP2022 AcroPack Carrier Block Diagram**

## PCIe SWITCH

The PCIe switch is a 6 port 8 lane PCIe Gen 2 switch. It expands the single host PCIe port to two ports, one for each AcroPack site. The host port consists of four PCIe lanes, each of the AcroPack sites have one lane each.

**Important Note:** The XMCAP2022 board is not hot-swappable.

## DC/DC CONVERTERS

The XMCAP2022 has four DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present at the host interface. The +1.5V supply is sourced from the VPWR host power. The +5 Volt, +12 Volt, and -12V supplies are sourced from +3.3 Volt host power.

## SLOT ADDRESSING

The XMCAP2022 carrier can be assigned by a combination of host supplied Geographical Addressing bits and/or by selecting the appropriate combination of SW1 switch settings. The slot address is 8 bits long and

consists of 3 bits to identify the site on the carrier where the AcroPack module is installed and 5 bits that are determined by host's Geographical Address bits (A0-A2) and the SW1 switch settings on the carrier (A3,A4). The CPLD will serialize the slot address and transmit the address to the AcroPack module as requested by the AcroPack module. The processes of reading the slot address is typically initiated by host software. See CARRIER ADDRESS ASSIGNMENT in section 2 for details regarding slot address selection.

## JTAG

A JTAG interface is provided for programming and debugging FPGAs on AcroPack modules. It is intended to be used with a Xilinx Platform USB II programming device. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to complete the JTAG chain. The slot address CPLD is included first in the JTAG chain for factory programming. When two AcroPack modules with Xilinx FPGAs are installed on the carrier the module in slot A appears next in the chain followed by the module in slot B.

## POWER SUPPLY FET SWITCHES

The +5V, +12V, and -12V power supplies to each AcroPack module are individually switched by onboard FETs. When the AcroPack PRESENT* signal, Pin 45 on the mini-PCIe connector, is seen to be grounded these supplies are turned on to supply voltage to the AcroPack module(s).

***WARNING: When installing a commercial mini-PCIe module onto the XMCAP2022 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.***

# 5. SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. .

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

## PRELIMINARY SERVICE PROCEDURE

**CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS**

Before beginning repair, be sure that all of the procedures in Section 2, PREPARATION FOR USE, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or AcroPack with one that is known to work correctly is a good technique to isolate a faulty board.

## WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag web site at www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab or your specific carrier model ordering page.

Acromag’s application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the “I/O Questions Answered” or directly from the “Contact Us” tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

# 6. SPECIFICATIONS

## PHYSICAL

### Physical Configuration (conforms to VITA 42 air-cooled XMC Specification)

Length.....5.866 inches (149 mm)
Width.....2.9134 inches (74 mm)
Board thickness .....0.066” +/-0.0066” (1.676 mm)
Max AcroPack module height .....0.083 inches (2.1 mm)*
Weight ..... XMC2022-LF: 2.26 oz (64 g)

### Connectors

P15 (XMC/PCIe Bus) .....114-pin plug (Samtec ASP-103614-5)
P16 Rear I/O (Carrier Field I/O) .....114-pin plug (Samtec ASP-103614-5),
P14 Rear I/O (Carrier Field I/O) .....64-pin plug (Molex 71436-2464),
P1, P2 (AcroPack Field I/O).....100-pin socket (Samtec SS5-50-3.00-L-D-K-TR)
J1, J2 (Mini-PCIe) .....52-pin socket (TE Connectivity 1759547-1)
J3 (JTAG) .....6-pin micro connector (Molex 78171-5006)

## POWER

Board power requirements are a function of the installed AcroPack modules.

The current specified below is for the XMCAP2022 carrier board only.

| | |
|---|---|
| +3.3 Volts (±5 %) | 140 mA Typical |
| VPWR = +5V (±5 %) | 200 mA Typical |
| VPWR = +12V (±8 %) | <100 mA Typical |

Add the current for each of the AcroPack modules to calculate the total current required from each supply.

The carrier is designed to provide the voltages and currents to the AcroPack modules as shown in Table 9. Note the rated current is *combined* for both AcroPack modules.

**Table 8 Module Isolation Specifications**

| Supply Voltage | Shared Current (Max) |
|---|---|
| +12V +/- 5% (max) | 1 A[1] |
| -12V +/- 5% (max) | 0.8 A[2] |
| +5V +/- 5% (max) | 2 A[3] |
| +3.3V +/- 5% (max) | 3 A[4] |
| +1.5V +/- 5% (max) | 2 A[5] |

**Notes:**

1. +12V is created from the host's +3.3V supply. This 1A current also supplies the -12V, so combined +12V and -12V current cannot exceed 1A.

2. -12V is created from the onboard +12V supply, which is fed from the host's +3.3V supply. Since the maximum output of the +12V supply is 1A, the combined +12V and -12V current cannot exceed 1A.
3. +5V is created from the host's +3.3V supply.
4. +3.3V is fed directly from the host's +3.3V supply.
5. +1.5V is created from the host's VPWR supply.

## PCIe BUS COMPLIANCE

Specification ..... This device meets or exceeds all written PCI Express specifications per revision 2.1. PCIe bus switch supports PCIe Gen 2 signals but rates exceed the rated bandwidth of the AcroPack connect.

## ENVIRONMENTAL

Operating Temperature .....-40 to +70°C (with 200 LFM airflow)
Relative Humidity .....5-95% non-condensing
Storage Temperature .....-55 to +125°C.

### EMC Compliance

The XMCAP2022 is designed to comply with EMC Directive 2004/108/EC.

| | |
|---|---|
| Immunity | per EN 61000-6-2<br>Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2<br>Radiated Field Immunity (RFI), per IEC 61000-4-3<br>Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4<br>Surge Immunity, per IEC 61000-4-5<br>Conducted RF Immunity (CRFI), per IEC 61000-4-6 |
| Emissions | per EN61000-6-4<br>Enclosure Port, per CISPR 16<br>Low Voltage AC Mains Port, per CISPR 16<br>Note: This is a Class A product |

### Vibration and Shock Standard

The XMCAP2022 is designed to pass the following Vibration and Shock standards.

**Vibration, Sinusoidal Operating**...Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

**Vibration, Random Operating**.....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

**Shock, Operating** .....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

### Reliability Prediction

**MTBF (Mean Time Between Failure):** MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, $G_BG_C$*

| Temperature | MTBF (Hours) | MTBF (Years) | Failure Rate (FIT[1]) |
|---|---|---|---|
| **25°C** | TBD | TBD | TBD |
| **40°C** | TBD | TBD | TBD |

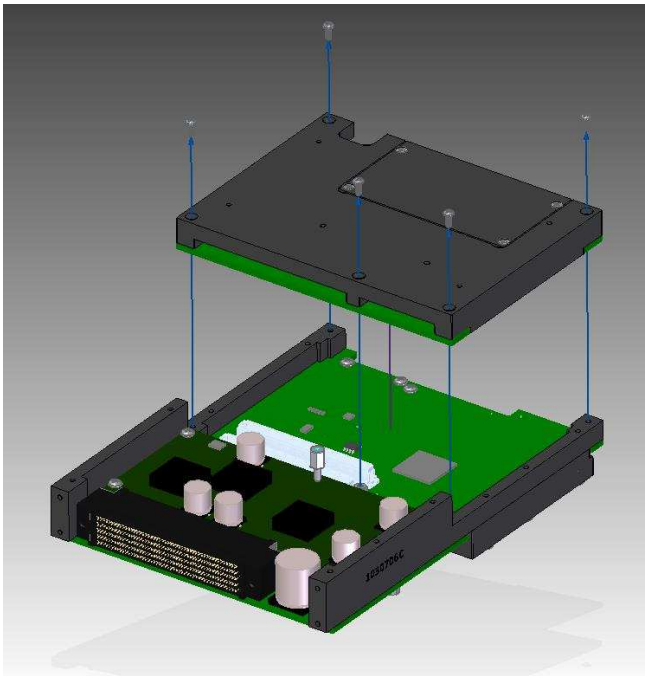
[1] FIT is Failures in $10^9$ hours.

# 7. APPENDIX A

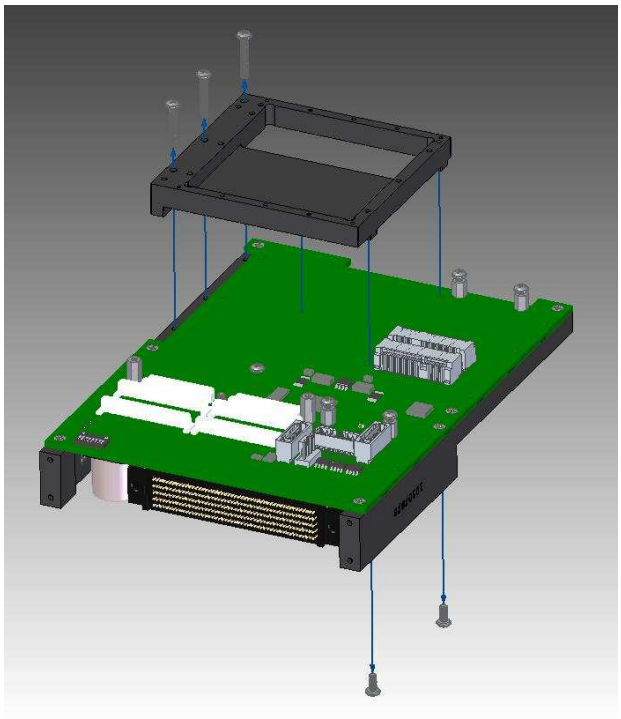
## Heatsink Installation

The following instructions describe how to remove the existing ARCX generic XMC heatsink and install a custom XMCAP202x heatsink.

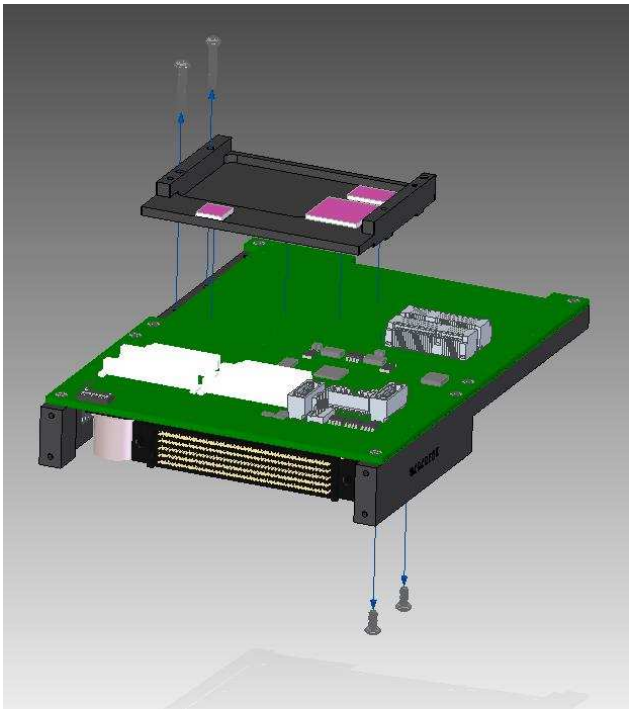
1. Refer to the ARCX box disassembly instructions found in the ARCX box manual to remove the assembly from its enclosure.
2. Remove the XCOM-6400 CPU module from the carrier by removing the 5 (M2.5 x 6mm) screws. Carefully lift the XCOM-6400 CPU module up and away from the carrier (ACEX-46xx) board.



3. Remove the 5 screws shown below to remove the generic XMC heatsink.



4. Install the custom heatsink as shown, using the 4 screws provided.

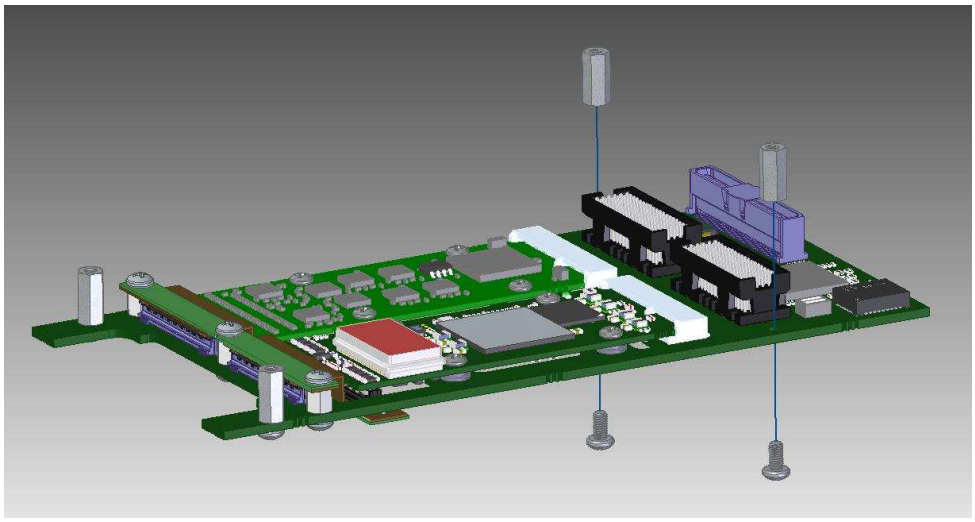


# 8. APPENDIX B

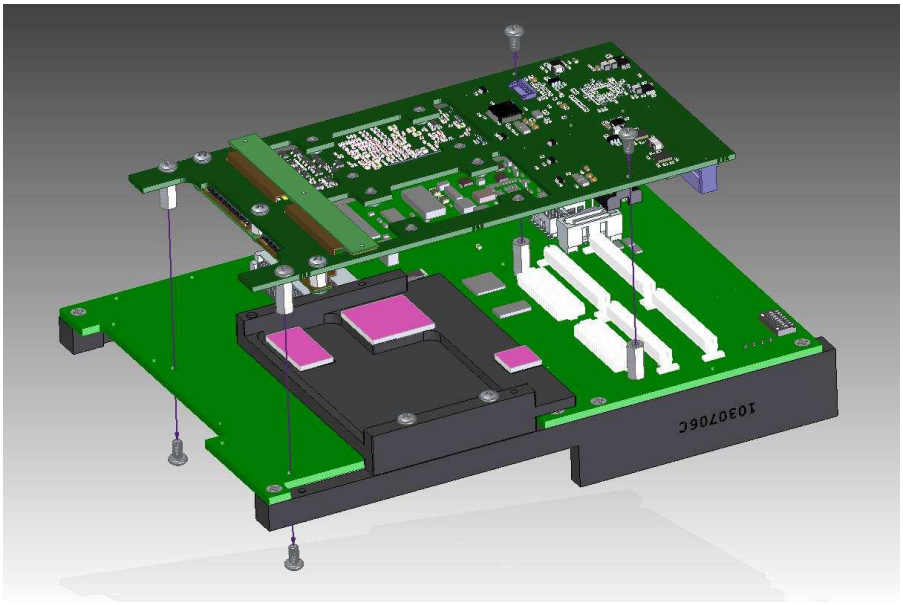
## XMCAP202x Module Installation

The following instructions describe how to install an XMCAP202x into an ARCX box. It is assumed that the ARCX has already been removed from its enclosure and the custom heatsink has been installed.

1. Remove the standard XMC standoffs shown below – these standoffs should already be installed on the ARCX carrier board.



2. Install the XMCAP202x on the carrier as shown below using the 4 screws provided.



3. Installation is complete. Refer to the ARCX box User Manual for instructions on reinstalling the XCOM-6400 CPU and reassembly.

# 9. CERTIFICATE OF VOLATILITY

| Certificate of Volatility | | | | |
|---|---|---|---|---|
| Acromag Model<br>XMCAP2022-LF | Manufacturer:<br>Acromag, Inc.<br>30765 Wixom Rd<br>Wixom, MI 48393 | | | |
| Volatile Memory | | | | |
| Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)<br>□ Yes ■ No | | | | |
| Non-Volatile Memory | | | | |
| Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)<br>■ Yes □ No | | | | |
| Type (EEPROM, FLASH etc.) | Size: | User Modifiable | Function: | Process to Sanitize: |
| EEPROM | 16K bytes | Yes | PCIe switch configuration | Overwrite EEPROM contents. |
| EEPROM | 256 bytes | Yes | FRU Data | Overwrite EEPROM contents. |

| Acromag Representative | | | | |
|---|---|---|---|---|
| Name:<br>Russ Nieves | Title:<br>Director of Sales and Marketing | Email:<br>rnieves@acromag.com | Office Phone:<br>248-295-0838 | Office Fax:<br>248-624-9234 |

## 10.REVISION HISTORY

| Release Date | Version | EGR/DOC | Description of Revision |
|---|---|---|---|
| 18 JUN 2018 | -- | CAB | Prelim |
| 19 JUN 2018 | -- | ENZ | Prelim – AcroPack A pinout revised |
| 31 JUL 2018 | -- | ENZ | Prelim – pinout to 38999 revised, board configuration drawing updated and block diagram added. |
| 3 JAN 2019 | A | ENZ/ARP | Added heatsink information and assembly instructions. Release. |
| 10 JAN 2019 | B | ENZ/ARP | Swap pictures between items 3 and 4 in APPENDIX A. |

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