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XVME-100

RAM/ROM MEMORY MODULE

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Chapter 1

MODULE DESCRIPTION

1.1 INTRODUCTION

The XVME-100 RAM/ROM Memory Module is a single-high, VMEbus compatible board, which can accommodate up to 1M byte of RAM, EPROM, or mask programmable ROM or 256K bytes of EEPROM. The module is designed with an on-board battery backup circuit to provide power to CMOS RAM devices in the event of a power failure.

The XVME-100 has eight 28/32-pin JEDEC sockets which are logically arranged as 2 banks of 4 sockets each. Each bank is designed to employ memory devices of the same type and speed, and each bank can be independently configured (via jumpers) in terms of:

- VME Address/Memory Chip Size
- Address Modifier Decode
- Memory Device Speed
- Memory Device Pinout
- Memory Backup Power

The XVME-100 RAM/ROM Memory Module has power down protection circuitry which prevents data from being written to memory when the voltage falls below 4.75 Volts. The module also has the option of asserting SYSRESET under this condition.

1.2 MANUAL STRUCTURE

The purpose of this first chapter is to introduce the user to the general specifications and functional capabilities of the XVME-100. Successive chapters will develop the various aspects of module installation and operation in the following progression:

Chapter One - A general description of the memory module, including complete functional and environmental specifications, VMEbus compliance information, and a block diagram.

Chapter Two - Module installation information covering the location of pertinent module components, jumper options, and standard board installation information.

The Appendices are designed to introduce and reinforce a variety of module-related topics including: Backplane signal/pin descriptions, a block diagram and schematics, a quick reference section, and power monitor calibration procedures.

1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows and operational block diagram of the memory module.

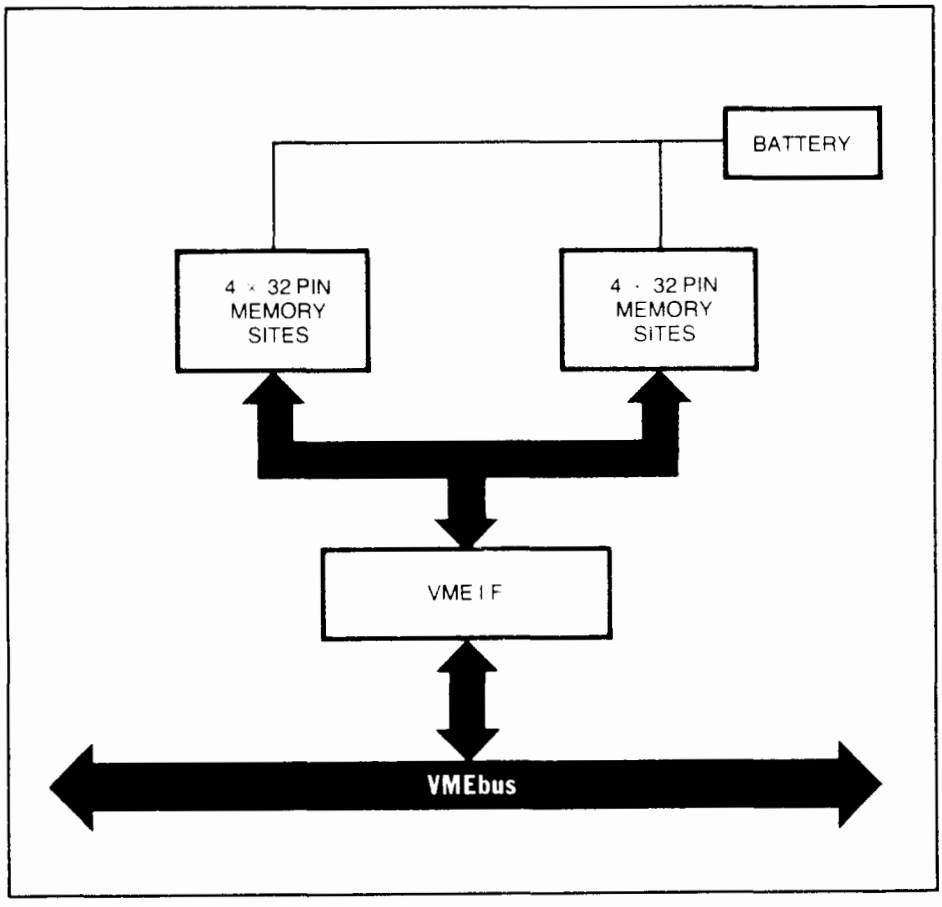


Figure 1-1. Operational Block Diagram

1.4 SPECIFICATIONS

Table 1-1 lists the XVME-100 Memory Module's characteristics and specifications.

Table 1-1. Memory Module Specifications

Characteristic	Specification
Maximum Memory Capacity:	2 banks of 4 sites
EPROM	1M byte
RAM	1M byte
Mask Programmable ROM	1M byte
EEPROM	256K bytes
Device Sizes Supported:	
EPROM	8K by 8 up to 128K by 8
RAM	8K by 8 up to 128K by 8
Mask Programmable ROM	8K by 8 up to 128K by 8
EEPROM	8K by 8 up to 32K by 8 (EEPROM must have quick write/polling technique and must employ TTL logic levels.)
Device Speeds Supported	100ns, 150ns, 200ns, & 250ns
Power Requirements	+5V @ 900mA typ., 1A max.
Battery Rating	1.4Amp hours
Battery Life	6 years typ. (using an 8-6264 Hitachi RAM or equivalent device)

VMEbus COMPLIANCE

Complies with VMEbus Specifications, Revision C.1

- A24:D16/D08(EO) DTB Slave
- 4 BUS GRANT INs are connected to their respective BUS GRANT OUTs
- IACKIN is connected to IACKOUT
- SINGLE - 3U Form Factor

Table 1-1. Memory Module Specifications (continued)

Characteristic	Specification
ENVIRONMENTAL	
Temperature	
Operating	0 to 65 C (32 to 149 F)
Non-operating	-40 to 85 C (-40 to 158 F)
Humidity	5 to 95% RH non-condensing (Extreme low humidity conditions may require special protection against static discharge)
Altitude	
Operating	Sea-level to 10,000 ft. (3048m)
Non-operating	Sea-level to 50,000 ft. (15240m)
Vibration	
Operating	5 to 2000Hz .015 inches peak-to-peak displacement 2.5 g peak (maximum) acceleration
Non-operating	5 to 2000Hz .030 inches peak-to-peak displacement 5.0 g peak (maximum) acceleration
Shock	
Operating	30 g peak acceleration, 11msec duration
Non-operating	50 g peak acceleration, 11msec duration

Chapter 2

XVME-100 INSTALLATION

2.1 INTRODUCTION

This chapter explains how to configure the memory module prior to installation in a VMEbus system. Included in this chapter is information on jumper options, jumper locations, and power monitor circuit calibration and installation procedures.

2.2 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers, memory sockets, and the VMEbus P1 connector on the XVME-100 Memory Module are illustrated in Figure 2-1. Figure 2-1A show an expanded left side of the board, and Figure 2-1B the right for clarification purposes.

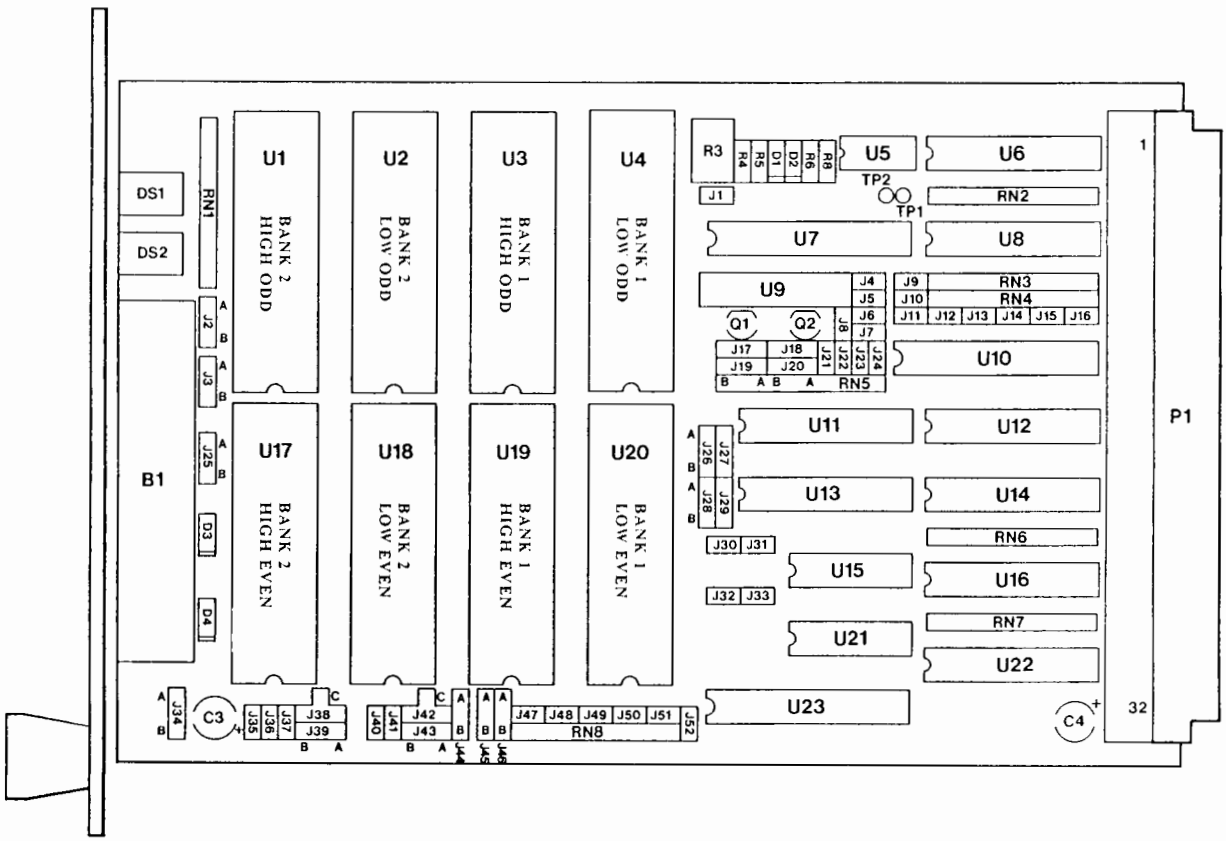


Figure 2-1. Location of Jumpers, Sockets, and Connector

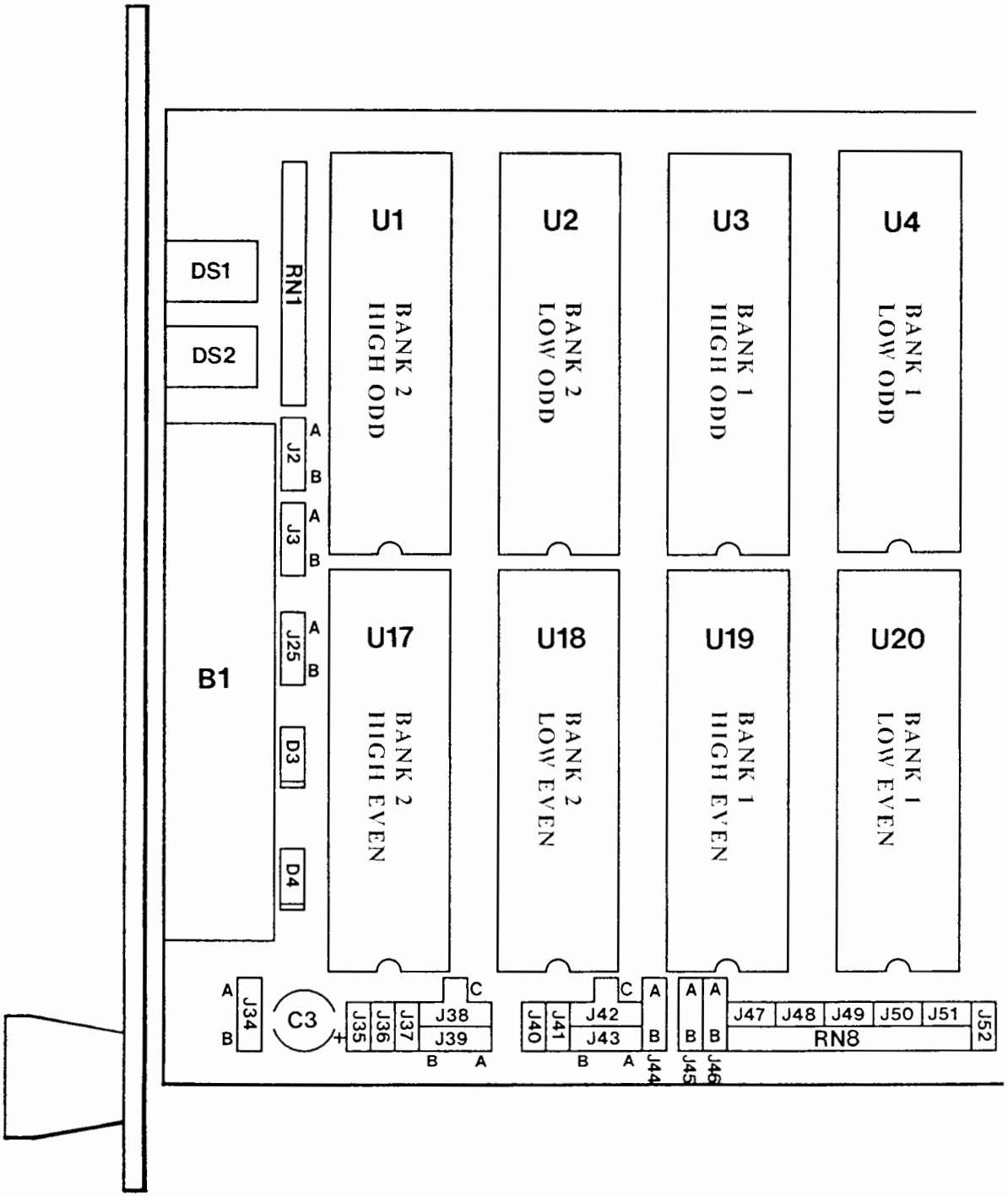


Figure 2-1A. Expanded Left Side of XVME-100

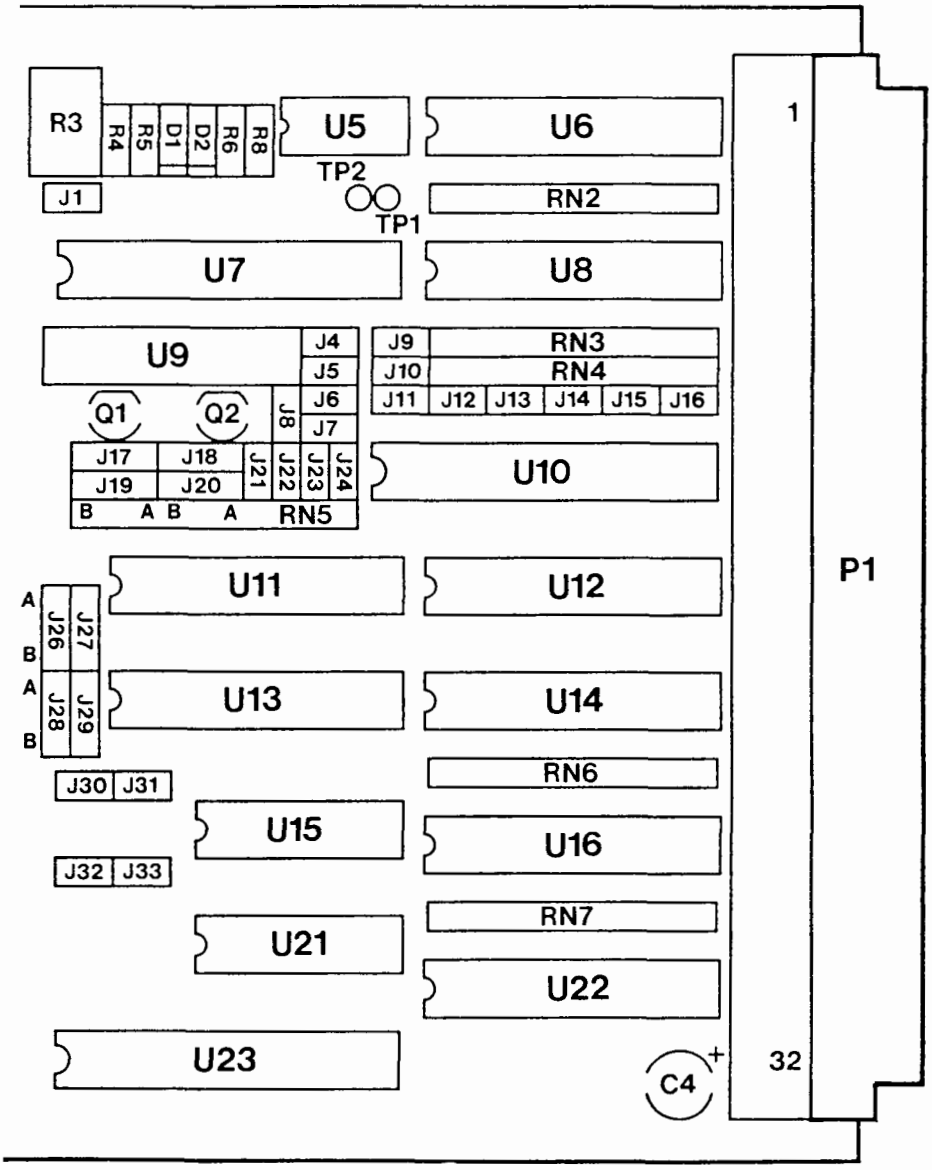


Figure 2-1B. Expanded Right Side of XVME-100

2.3 JUMPERS

Prior to installing the XVME-100 Memory Module, it will be necessary to configure several jumper options. The configuration is dependant upon which type of memory devices to be used. The following table shows a list of the jumpers and a brief description of their use.

Table 2-1. Jumper List

Jumper	Description	Section
J1	Power Monitor Calibration	2.4.6
J2	Memory Type - bank 2	2.4.4
J3	Memory Type - bank 2	2.4.4
J4	Speed Select - bank 2	2.4.3
J5	Speed Select - bank 2	2.4.3
J6	Speed Select - bank 1	2.4.3
J7	Speed Select - bank 1	2.4.3
J8	SYSRESET* Driver, enable	2.4.6
J9	Data Access - bank 2	2.4.2
J10	Program Access - bank 1	2.4.2
J11	Data Access - bank 1	2.4.2
J12	Program Access - bank 2	2.4.2
J13	Supervisor Only - bank 1	2.4.2
J14	VME Address - bank 1	2.4.1
J15	Supervisor Only - bank 2	2.4.2
J16	VME Address - bank 2	2.4.1
J17	VME Address - bank 1	2.4.1
J18	VME Address - bank 1	2.4.1
J19	VME Address - bank 1	2.4.1
J20	VME Address - bank 1	2.4.1
J21	VME Address - bank 1	2.4.1
J22	VME Address - bank 1	2.4.1
J23	VME Address - bank 1	2.4.1
J24	VME Address - bank 1	2.4.1
J25	Memory Type - bank 2	2.4.4
J26	VME Address - bank 2	2.4.1
J27	VME Address - bank 2	2.4.1
J28	VME Address - bank 2	2.4.1
J29	VME Address - bank 2	2.4.1
J30	VME Address - bank 2	2.4.1
J31	VME Address - bank 2	2.4.1
J32	VME Address - bank 2	2.4.1
J33	VME Address - bank 2	2.4.1
J34	Battery, alternate power source	2.4.5
J35	+5V STDBY, alternate power source	2.4.5
J36	Memory Type - bank 2	2.4.4
J37	Memory Type - bank 2	2.4.4
J38	Memory Type - bank 2	2.4.4
J39	Memory Type - bank 2	2.4.4

Table 2-1. Jumper List (continued)

Jumper	Description	Section
J40	Memory Type - bank 1	2.4.4
J41	Memory Type - bank 1	2.4.4
J42	Memory Type - bank 1	2.4.4
J43	Memory Type - bank 1	2.4.4
J44	Memory Type - bank 1	2.4.4
J45	Memory Type - bank 1	2.4.4
J46	Memory Type - bank 1	2.4.4
J47	Size Select - bank 2	2.4.1
J48	Size Select - bank 2	2.4.1
J49	Size Select - bank 2	2.4.1
J50	Size Select - bank 1	2.4.1
J51	Size Select - bank 1	2.4.1
J52	Size Select - bank 1	2.4.1

2.4 JUMPER DESCRIPTIONS

The two banks are independently configurable, via jumpers to define five different memory module parameters, these parameters are:

1. VME Address/Memory Chip Size
2. Address Modifier Decode
3. Memory Device Speed
4. Memory Device Pinout
5. Memory Backup Power

The following five subsections examines these jumper options in closer detail, showing specifically when and how jumpers should be configured.

2.4.1 VME Address/Memory Chip Size

12 jumpers exist for each bank (24 total) to define the VMEbus address and memory chip size. Table 2-2 lists the jumpers and their definitions. The bank will occupy a VMEbus address space of four times the memory chip size. The bank must be assigned to a boundary which is a multiple of four times the memory chip size.

Table 2-2. VME Base Address and Memory Chip Size Jumpers

BANK 1

BASE ADDRESS BIT	= 1	= 0
A23	J14 Out	J14 In*
A22	J23 Out	J23 In*
A21	J21 Out	J21 In*
A20	J22 Out	J22 In*
A19	J24 Out	J24 In*
A18	J20 Out	J20B*
A17	J18 Out	J18B*
A16	J19 Out	J19B*
A15	J17 Out	J17B*

* Factory shipped configuration

Device Size In Bits	J17	J19	J18	J20	J50	J51	J52	J14	J23	J21	J22	J24
8K x 8	X	X	X	X	In	In	In	X	X	X	X	X
16K x 8	A	X	X	X	In	In	Out	X	X	X	X	X
32K x 8	A	A	X	X	In	Out	In	X	X	X	X	X
64K x 8	A	A	A	X	In	Out	Out	X	X	X	X	X
128K x 8	A	A	A	A	Out	In	In	X	X	X	X	X

X = Use to define state of corresponding base address bit per above chart

BANK 2

BASE ADDRESS BIT	= 1	= 0
A23	J16 Out	J16 In*
A22	J31 Out	J31 In*
A21	J30 Out	J30 In*
A20	J33 Out	J33 In*
A19	J32 Out	J32 In*
A18	J28 Out	J28A*
A17	J26 Out	J26A*
A16	J29 Out	J29A*
A15	J27 Out	J27A*

* Factory shipped configuration

Device Size In Bits	J27	J29	J26	J28	J47	J48	J49	J16	J31	J30	J33	J32
8K x 8	X	X	X	X	In	In	In	X	X	X	X	X
16K x 8	B	X	X	X	In	In	Out	X	X	X	X	X
32K x 8	B	B	X	X	In	Out	In	X	X	X	X	X
64K x 8	B	B	B	X	In	Out	Out	X	X	X	X	X
128K x 8	B	B	B	B	Out	In	In	X	X	X	X	X

X = Use to define state of corresponding base address list per above chart

The following is an example of the jumpering required to install 32K x 8 EPROMs in bank 1.

EXAMPLE:

27256 32K x 8 EPROMs are to installed in bank 1 with a VMEbus base address of 8E0000 Hex.

J17	A
J19	A
J18	OUT
J20	OUT
J50	IN
J51	OUT
J52	IN
J14	OUT
J23	IN
J21	IN
J22	IN
J24	OUT

Bank 1 will reside in memory address:

8E0000 Hex. through 8FFFFF Hex.

Figure 2-2 shows the memory map for the XVME-100, and Figure 2-3 shows the bank addressing four times the memory chip size.

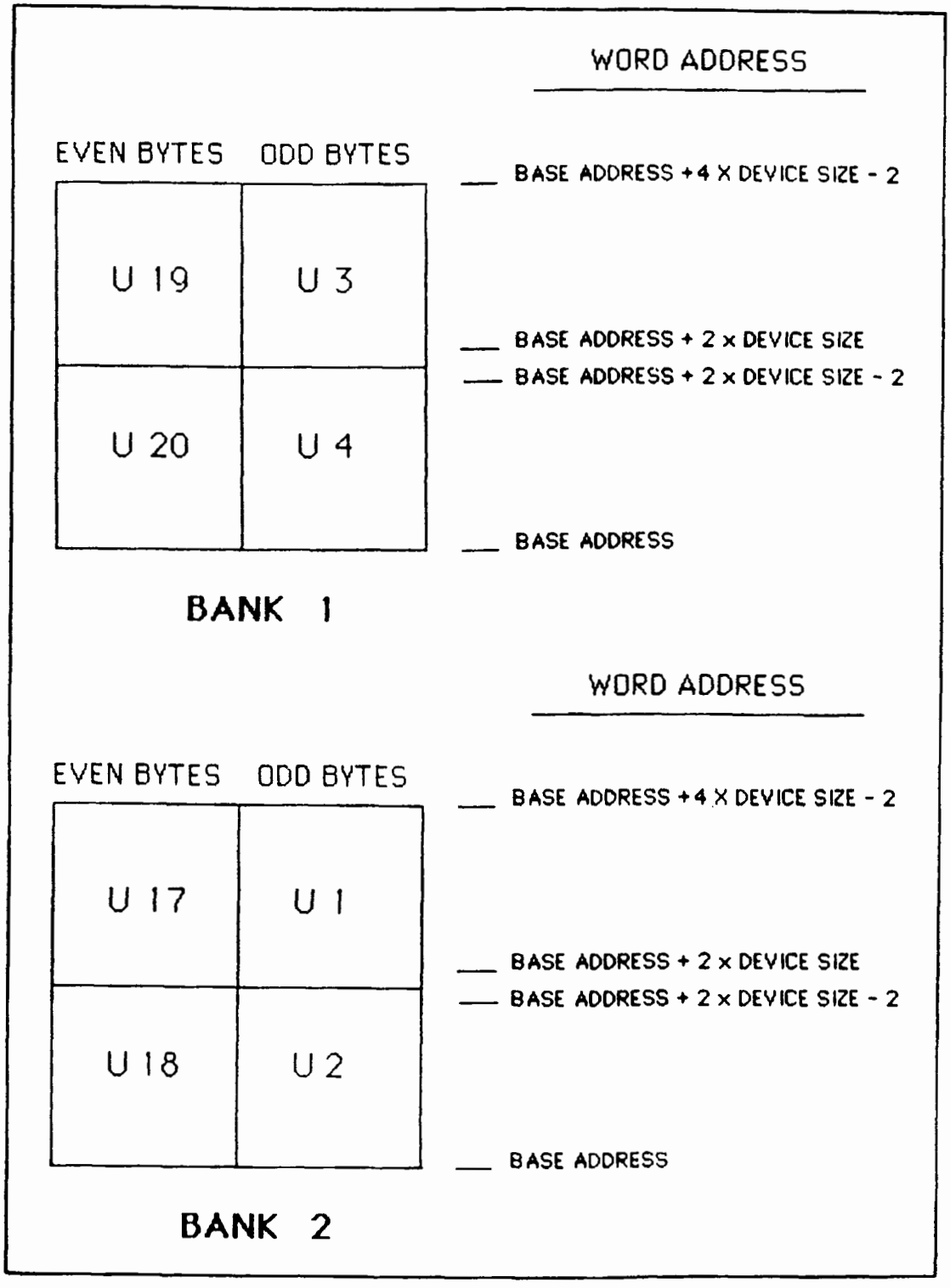


Figure 2-2. XVME-100 Memory Map

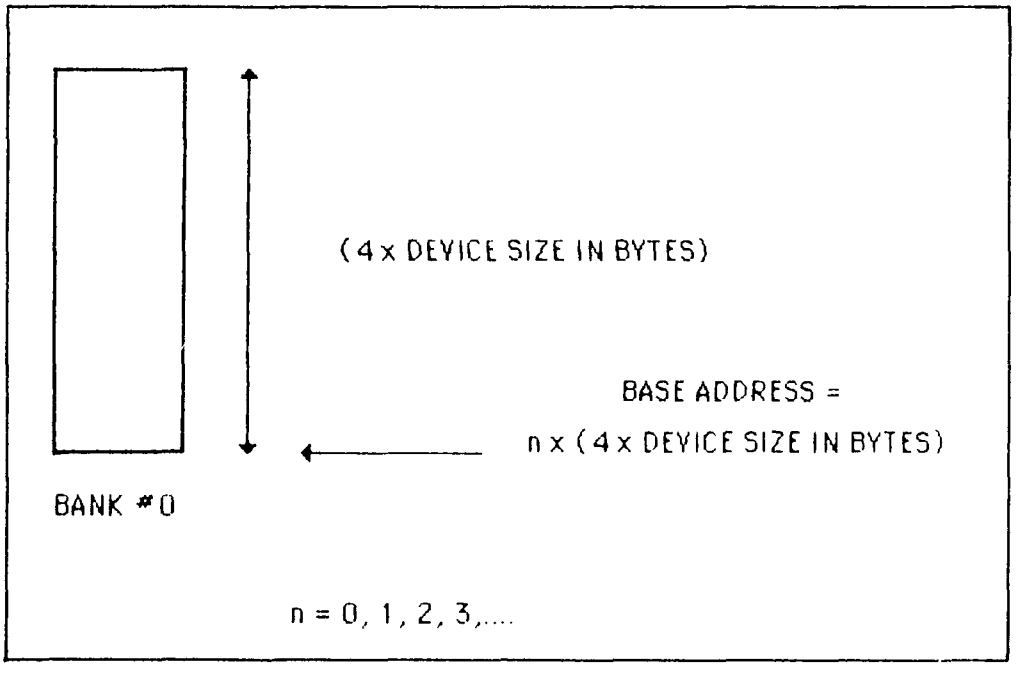


Figure 2-3. Addressing - 4 x Chip Size

2.4.2 Address Modifier Decode

The address modifier decode uses three jumpers for each bank (6 total). Both banks reside in the standard A24 address space. The first jumper is the supervisor select, when the jumper is in, the bank will respond only to supervisor accesses, when the jumper is out, the bank will respond to supervisor and non-privileged accesses. During each access of a bank, that bank's LED (green) on the front panel, will momentarily light.

The second jumper is the data space select, when this jumper is in, the bank will respond to data accesses, when out, the bank won't respond to data accesses.

The third jumper is the program space select, when the jumper is in, the module will respond to program accesses, when out, the module won't respond to program accesses.

Table 2-3 lists these three jumpers and their definitions.

Table 2-3. Address Modifier Jumpers

BANK 1

Jumpers	Description
J13 In* J13 Out	Supervisor Only AM2 = 1 Supervisor & Non-privileged AM2 = don't care
J11 In* J11 Out	Data Access Responds to Address Modifier codes No Data Access Won't respond to 3DH or 39H
J10 In* J10 Out	Program Access 3EH or 3AH No Program Access Won't respond to 3EH or 3AH

BANK 2

Jumpers	Description
J15 In* J15 Out	Supervisor Only AM2 = 1 Supervisor & Non-privileged AM2 = don't care
J9 In* J9 Out	Data Access Responds to Address Modifier codes No Data Access Won't respond to 3DH or 39H
J12 In* J12 Out	Program Access 3EH or 3AH No Program Access Won't respond to 3EH or 3AH

* = Factory shipped configuration

These three jumpers are independent of each other. When both the data space select and the program space select jumpers are out, the bank will be disabled from VMEbus accesses.

2.4.3 Memory Device Speed

Two jumpers exist for each bank (4 total) to define the speed of the memory devices. Selections are 100, 150, 200, and 250 ns devices. Table 2-4 lists the jumpers and speed definition for each device.

Table 2-4. Memory Device Speed Jumpers

BANK 1

Speed Select	Jumpers J6	Jumpers J7
100ns	Out	Out
150ns	Out	In
200ns	In	Out
250ns	In*	In*

BANK 2

Speed Select	Jumpers J4	Jumpers J5
100ns	Out	Out
150ns	Out	In
200ns	In	Out
250ns	In*	In*

* = Factory shipped configuration

VMEbus access timing is a function of the memory device speed of the bank being accessed. Data strobe asserted to DTACK* asserted will typically be 100 ns plus the chosen access time. Data strobe negated to DTACK* negated will be 50 ns typical.

2.4.4 Memory Device Pinout

There are seven jumpers for each of the banks (14 total) on the XVME-100 which define the memory device pinout. Table 2-5 lists the jumpers and memory type. Figure 2-4 and show chip pinouts.

Table 2-5. Memory Device Pinout Jumpers

BANK 1

Memory Type	Jumpers						
	J45	J43	J46	J41	J42	J40	J44
64k/128k EPROM	Out*	B*	Out*	In*	C*	In*	B*
256K EPROM	B	B	B	X	C	In	B
1 M ROM	B	A	B	X	B	In	B
64K RAM	A	B	A	X	X	Out	@
256K/1M RAM	A	B	A	In	A	In	@
512K/1 M EPROM 64K/128K/256K/512K ROM	B	B	B	Out	B	In	B

BANK 2

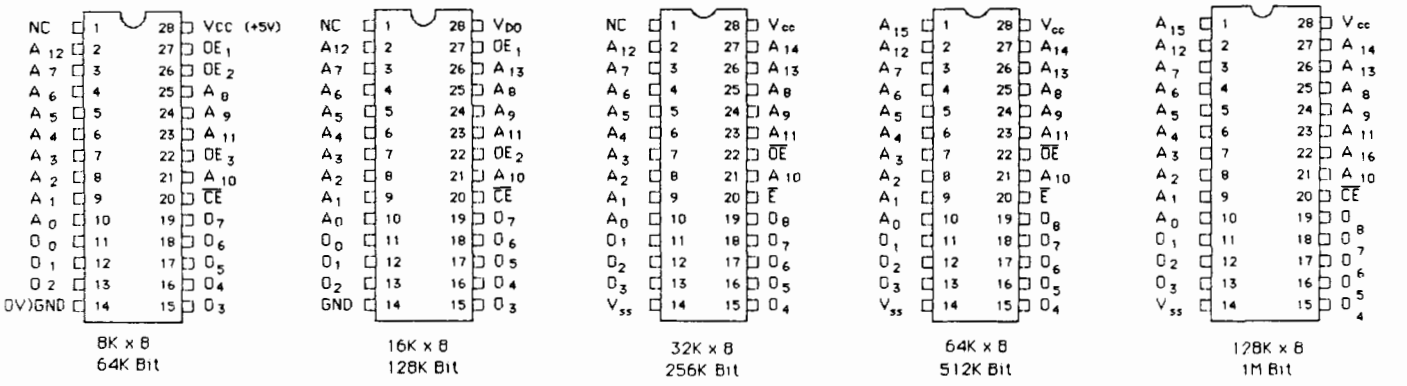
Memory Type	Jumpers						
	J25	J39	J2	J37	J38	J36	J3
64k/128k EPROM	Out*	B*	Out*	In*	C*	In*	B*
256K EPROM	B	B	B	X	C	In	B
1 M ROM	B	A	B	X	B	In	B
64K RAM	A	B	A	X	X	Out	@
256K/1M RAM	A	B	A	In	A	In	@
512K/1 M EPROM 64K/128K/256K/512K ROM	B	B	B	Out	B	In	B

X = Don't Care
@ = For alternate power source J3A (See section 2.4.5 (BANK 2))
= For alternate power source J44A (See section 2.4.5 (BANK 1))

For System Vcc J3B (BANK 2)
For System Vcc J44B (BANK 1)

* = Factory shipped configuration

MASK PROGRAMMABLE ROM



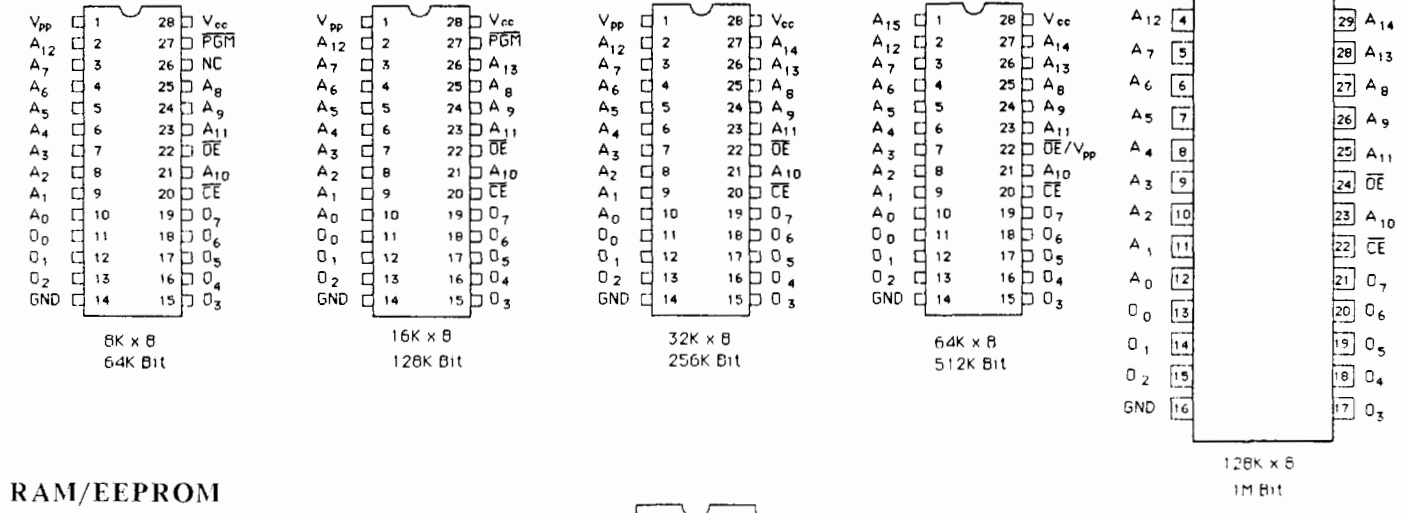
Pins 26 & 27 must be programmed as don't care

Pin 22 must be programmed active low

Pin 27 must be programmed as don't care

Pin 22 must be programmed active low

EPROM



RAM/EEPROM

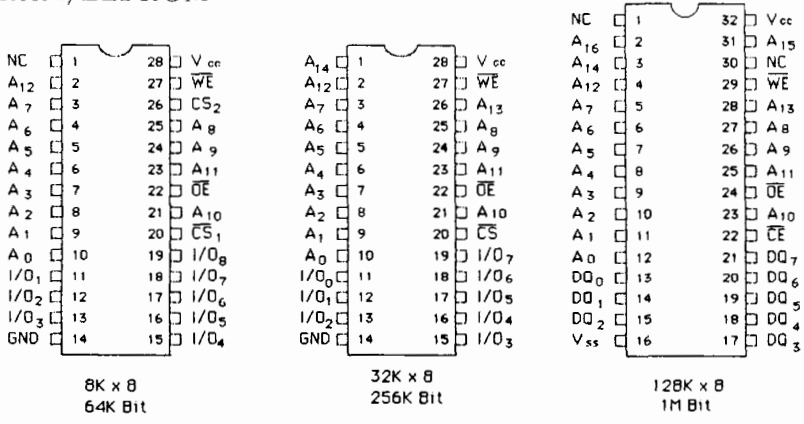


Figure 2-4. Memory Chip Pinouts

EXAMPLE:

Bank 1 8K x 8 RAM Memory device pinout jumpers

Memory Type	J45	J43	J46	J41	J42	J40	J44
64k Bits	A	B	A	X	X	OUT	@

Bank 2 Memory device pinout jumpers

Memory Type	J25	J39	J2	J37	J38	J36	J3
64K Bits	A	B	A	X	X	OUT	@

X = Don't care
@ = Alternate power source

2.4.5 Memory Backup Power

During power loss, the CMOS RAM chips may have an alternative power source connected to retain the data stored. Two alternative power sources are available: the on board battery and the +5V standby signal from the VMEbus. The following chart shows the jumper configuration for each option:

Alternative Power Source	J34	J35
None	A*	Out*
Battery	B	Out
+5V Standby	A	In

* Factory shipped configuration

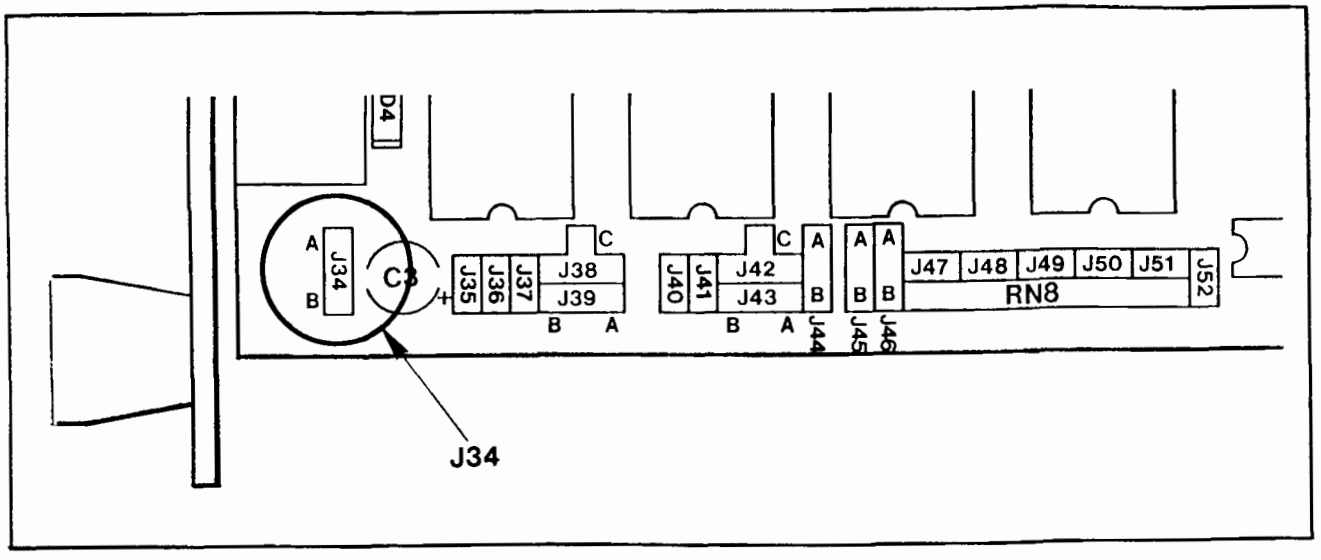


Figure 2-5. Location of Jumper J34

In order to achieve maximum battery life, RAM chips must have a small data retention current. Most static RAM suppliers have chips that guarantee very low data retention currents. These should be used to prolong battery life.

To calculate the typical battery life, use the following equation:

$$\text{Hours of battery life} = \frac{1{,}400{,}000}{((n \times I_SB) + 10)}$$

where: I_SB is the data retention current required by the particular RAM chips, in micro amperes

n = the # of RAM chips selected to be battery backed.

Example:

8 Hitachi 6264LP-15 are used, they have a typical I_SB of 2 uA.

$$\text{Battery Life} = \frac{1{,}400{,}000}{((8 \times 2) + 10)}$$

$$= 53850 \text{ hrs.}$$

$$= 6.1 \text{ years}$$

The shelf life of the battery is 10 years, so data retention cannot be guaranteed to be over 10 years regardless of the RAM chips used.

CAUTION

The following are some general precautions about batteries which should be adhered to:

- Do not short your battery
- Do not place module on a metal (conductive) surface
- Do not charge the battery
- Do not connect in wrong polarity (+, -) of the battery
- Do not directly solder onto the battery
- Do not use the battery at temperatures other than those specified
- Do not use with other types of batteries
- Do not heat the battery
- Do not incinerate the battery

The user has three different options available for choosing alternate power source of each bank. These options depend on the configurations of J34 and J35 and are as follows:

Alternate Power Source = Battery (J34B, J35 OUT)

Bank 1 Power	J44
Battery	A
Vcc*	B
Bank 2 Power	**J3**
Battery	A
Vcc*	B

Alternate Power Source = +5V Standby (J34A, J35 IN)

Bank 1 Power	J44
+5V Standby	A
Vcc*	B
Bank 2 Power	**J3**
+5V Standby	A
Vcc*	B

Alternate Power Source = None (J34A, J35 OUT factory shipped configuration)

Bank 1 Power	J44
Vcc*	B
Bank 2 Power	**J3**
Vcc*	B

* If EEPROM or EPROM are installed in any bank, the Vcc Jumper should be installed to prevent drawing current from the alternate power source.

2.4.6 Power Monitor

A power monitor is provided to disable the memory chips when Vcc falls below 4.75V. This monitor sometimes requires calibration. It is calibrated when it leaves the factory, however if the user has need to recalibrate, use the following procedure:

NOTE

Refer to Figure 2-6 for location of jumpers and test points.

1) Apply power to the module while on an extender board.

2) Remove J1.

3) Connect the negative side of a 4.75V power reference to TP2 (ground).

4) Connect the positive side of the 4.75V power reference to the left terminal of J1.

5) Connect a volt meter or a scope to TP1.

6) If the voltage of TP1 is high (> 4V) then turn POT R3 counter-clockwise, until the voltage of TP1 goes low (< 0.8V).

7) Slowly turn POT R3 clockwise until the point where the voltage of TP1 goes high. Stop turning POT R3 at this point.

8) Remove voltage reference, voltage meter and install J1.

9) The power monitor is now calibrated, apply glip to the POT's screw to prevent it from loosening.

A SYSRESET* driver is provided to assert SYSRESET* when the power monitor circuitry detects that Vcc is less than 4.75V. To enable the SYSRESET* driver, install J8, and to disable the SYSRESET* driver remove J8.

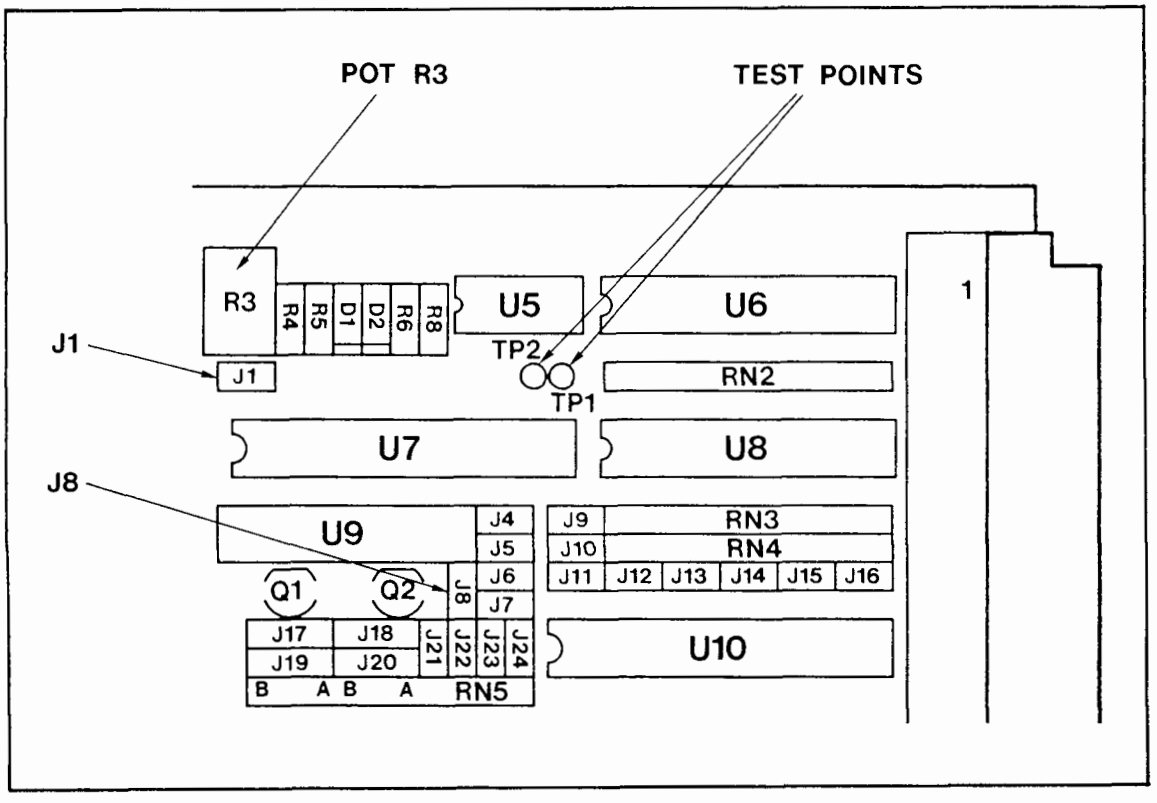


Figure 2-6. Location of Jumpers and Test Points

2.5 INSTALLING MEMORY CHIPS ON THE XVME-100

As was previously mentioned, there are a total of eight 32-pin sockets intended for use by RAM, EPROM, EEPROM, and Mask Programmable ROM devices on the XVME-100 Module.

Installing memory in any of the sockets is simply a matter of setting the proper jumpers and installing the memory devices.

The following is the procedure for installing memory devices in the sockets on the XVME-100 Memory Module.

1) With all power removed form the board, locate the proper socket (see Figure 2-1 for location of sockets and banks).

2) Reference the notched end of the memory chips as shown in Figure 2-7. When installing a 28 pin chip, the chip should be oriented towards the bottom of the board, leaving the bottom holes exposed as shown below.

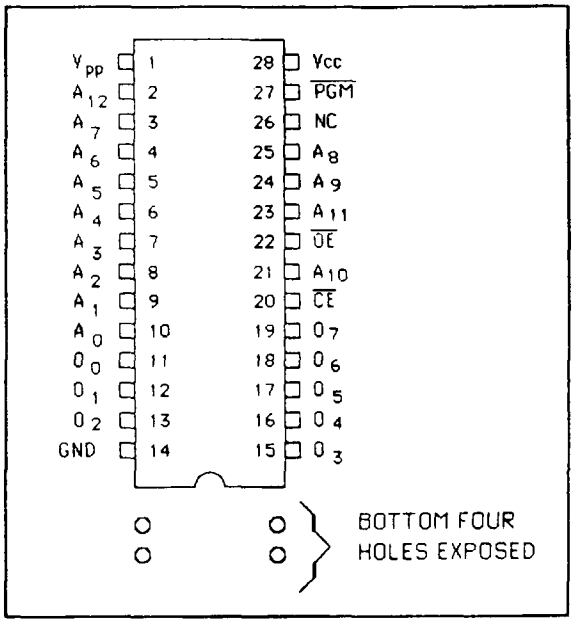


Figure 2-7. Notched End of the Memory Chip

3) Line up the pins on each chip with the socket holes found at the inside top of each socket location, and push each chip firmly, and evenly into place.

NOTE

Static precautions should be exercised when handling the memory chips, especially the CMOS RAM chips.

4) Check to make sure that the chips are fully seated in the bottom of the sockets, with no pins bent or out of alignment in the sockets.

2.6 CARDCAGE INSTALLATION PROCEDURE

CAUTION

Do not attempt to install or remove any boards without first turning off the power to the bus, and all related external power supplies.

Prior to installing a module, you should determine and verify all relevant jumper configurations. (Please check the jumper configuration with the diagram and lists in the manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2) Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage.

3) Push the card slowly toward the rear of the chassis until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excess pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

Once the board is properly seated, it should be secured by tightening the two machine screws at the extreme top and bottom of the front panel.

2.7 INSTALLING A 6U FRONT PANEL KIT (optional)

XYCOM Model Number XVME-945 is an optional 6U front panel kit designed to replace the existing 3U front panel on the XVME-100. The 6U front panel facilitates the secure installation of single-high modules in those chassis which are designed to accommodate double-high modules. The following is a step-by-step procedure for installing the 6U front panel on an XVME-100 Module (refer to figure 2-8 for a graphic depiction of the installation procedure).

1. Disconnect the module from the bus.

2. Remove the screw and plastic collar assemblies (labeled #6 and #7) from the extreme top and bottom of the existing 3U front panel (#11), and install the screw assemblies in their corresponding locations on the 6U front panel.

3. Slide the module identification plate (labeled #13) from the handle (#9) on the 3U front panel. By removing the screw/nut found inside the handle, the entire handle assembly will separate from the 3U front panel. Remove the counter-sunk screw (#8) to separate the 3U front panel from the printed circuit board (#12).

4. Line-up the plastic support brackets on the printed circuit board with the corresponding holes in the 6U front panel (i.e. the holes at the top and top-center of the panel). Install the counter-sunk screw (#8) in the hole near the top center of the 6U panel, securing it to the lower support bracket on the printed circuit board.

5. Install the handle assembly (which was taken from the 3U panel) at the top of the 6U panel, using the screw and nut previously attached inside the handle. After securing the top handle, slide the module identification plate in place.

6. Finally, install the bottom handle (i.e. the handle that accompanies the kit - labeled #2) using the screw and nut (#3 & #5) provided. Slide the XYCOM VMEbus I.D. plate (#4) in place on the bottom handle. The module is now ready to be re-installed in the backplane.

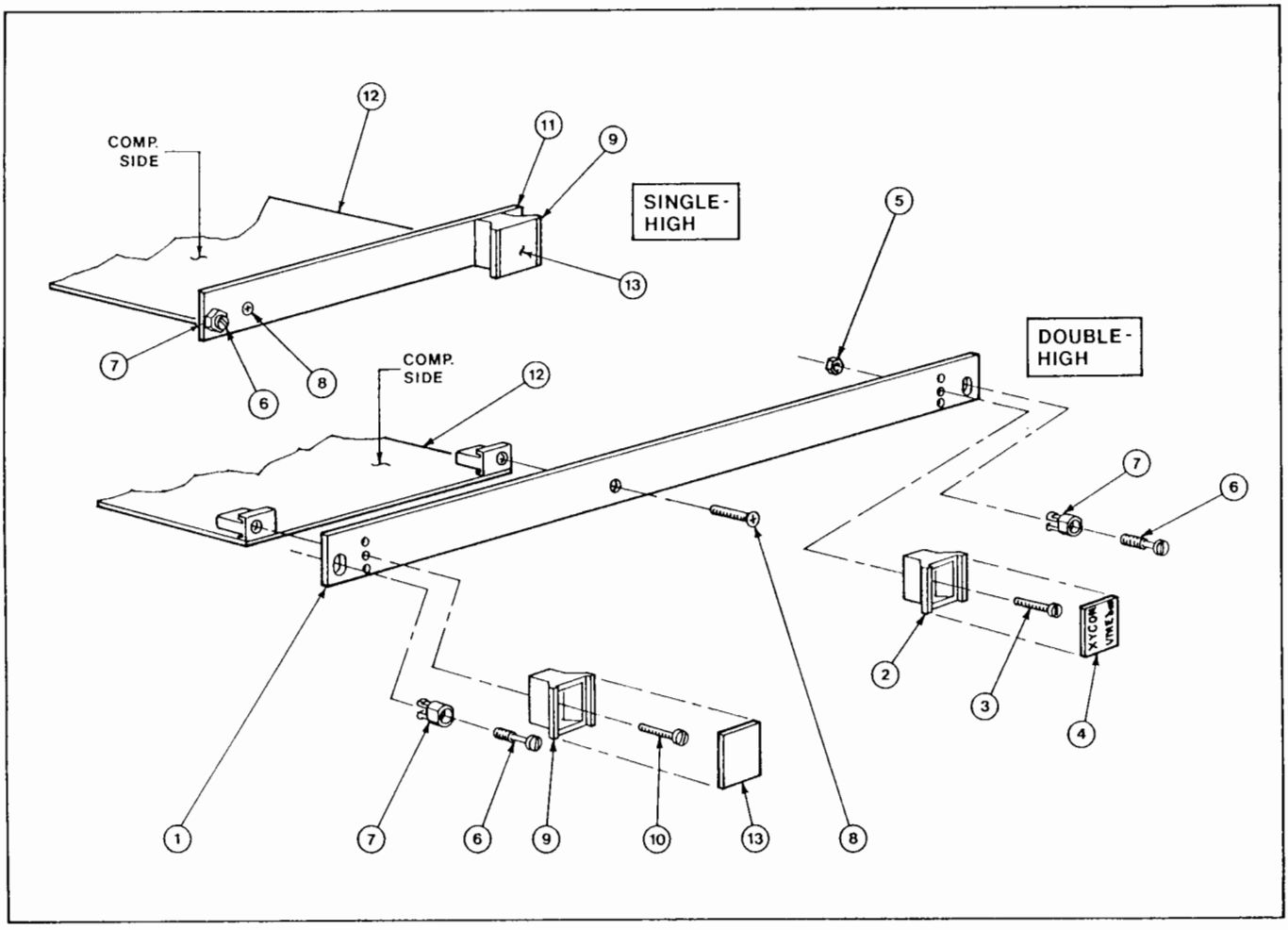


Figure 2-8. Installation of an XVME-945 6U Front Panel

Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

Table A-1. P1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	1A:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17, 18,19 1C:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	1A:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A01-A23	1A:24-30 1C:15-30	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:1	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,10	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	1B:5,7, 9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	1B:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DS1*	1A:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).
DTACK*	1A:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A:1-8 1C:1-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A:9,11, 15,17,19, 1B:20,23, 1C:9 2B:2,12, 22,31	GROUND

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQ1*-IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	1A:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:10	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	1C:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	1B:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5V	1A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12V	1A:31	-12 VDC POWER: Used by system logic circuits.

BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2. P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Appendix B

POWER MONITOR

A power monitor is provided to disable the memory chips when VCC falls below 4.75V. This monitor sometimes requires calibration. It is calibrated when it leaves the factory, however it may be necessary to recelebrate after an extended amount of time. To calibrate the power monitor perform the following steps:

NOTE

Refer to Figure B-1 for location of jumpers and test points.

1) Apply power to the module while on an extender board.

2) Remove J1.

3) Connect the negative side of a 4.75V power reference to TP2 (ground).

4) Connect the positive side of the 4.75V power reference to the left terminal of J1.

5) Connect a volt meter or a scope to TP1.

6) If the voltage of TP1 is high (> 4V) then turn POT R3 counter-clockwise, until the voltage of TP1 goes low (< 0.8V).

7) Slowly turn POT R3 clockwise until the point where the voltage of TP1 goes high. Stop turning POT R3 at this point.

8) Remove voltage reference, voltage meter and install J1.

9) The power monitor is now calibrated, apply glip to the POT's screw to prevent it from loosening.

A SYSRESET* driver is provided to assert SYSRESET* when the power monitor detects that VCC is less than 4.75V. To enable the SYSRESET* driver, install J8, and to disable the SYSRESET* driver remove J8.

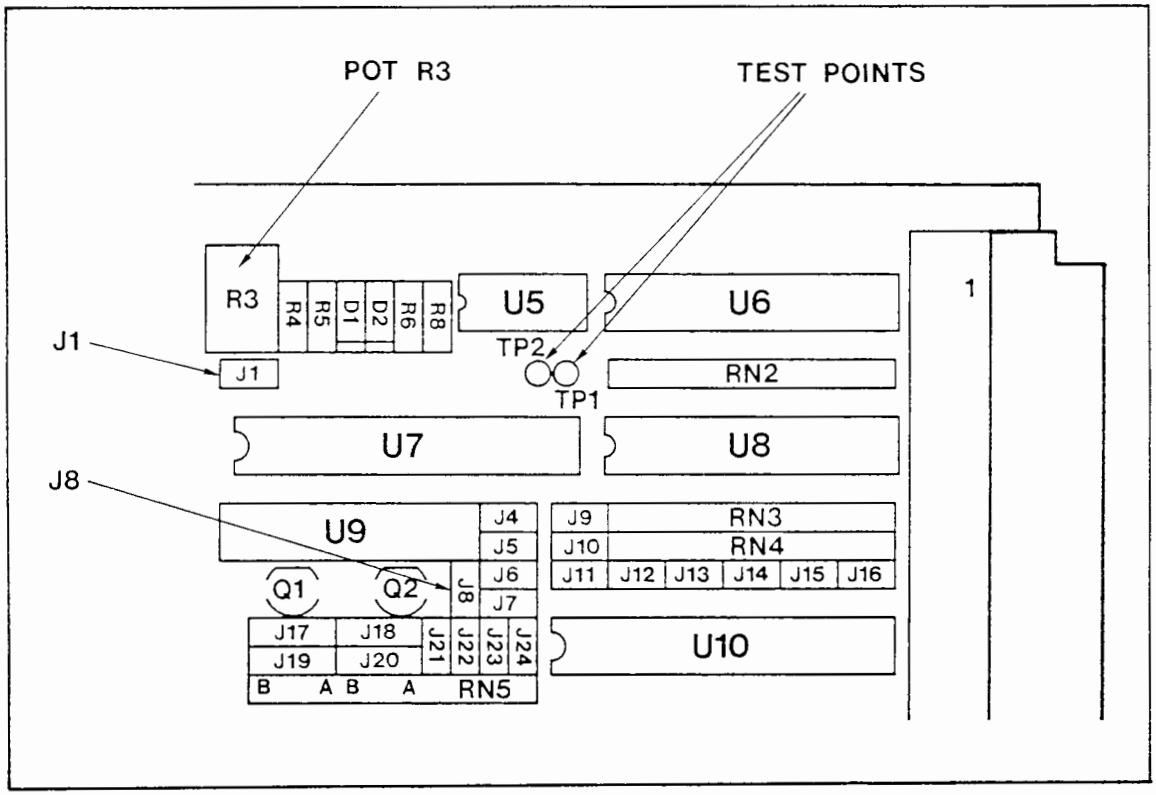
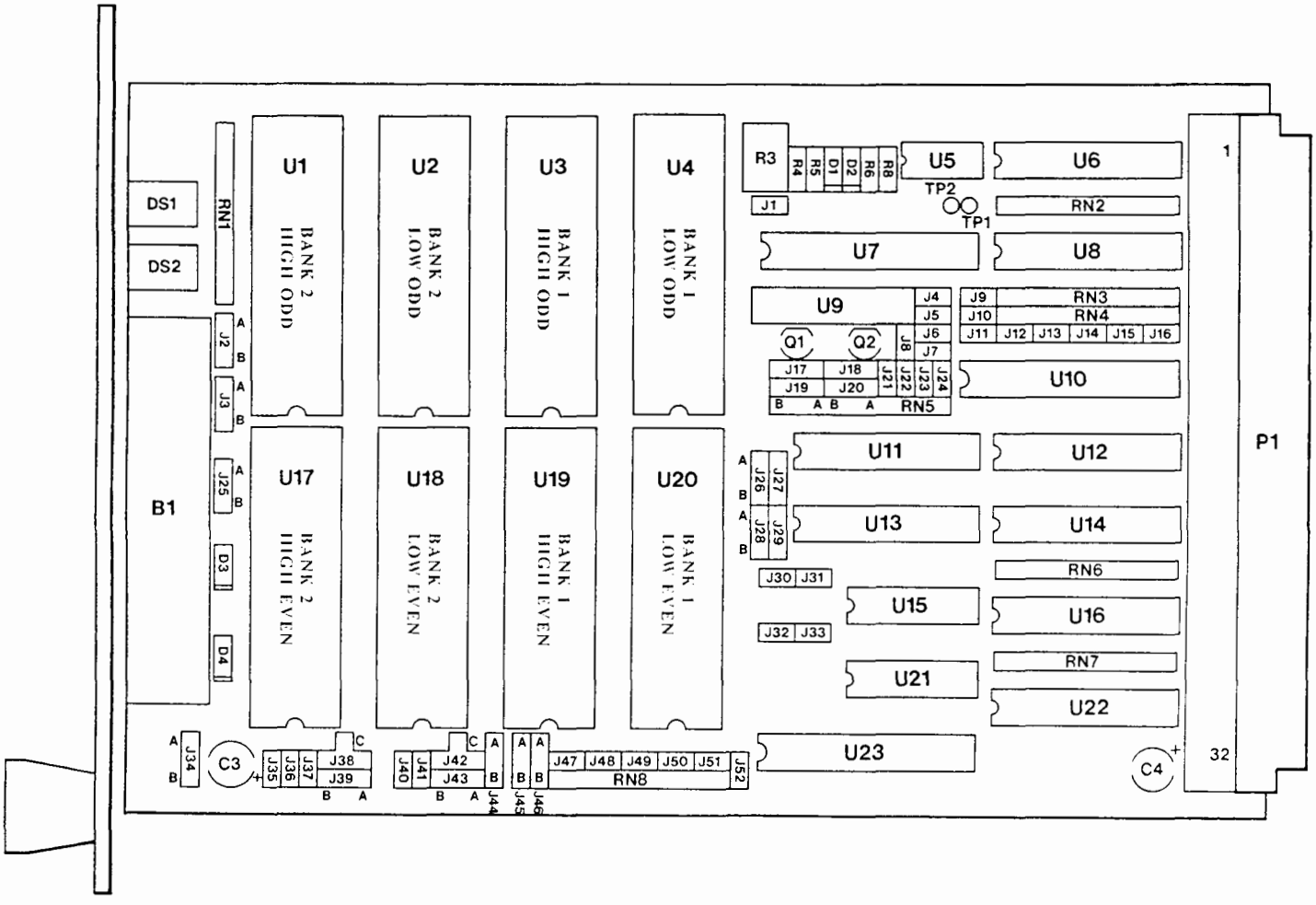
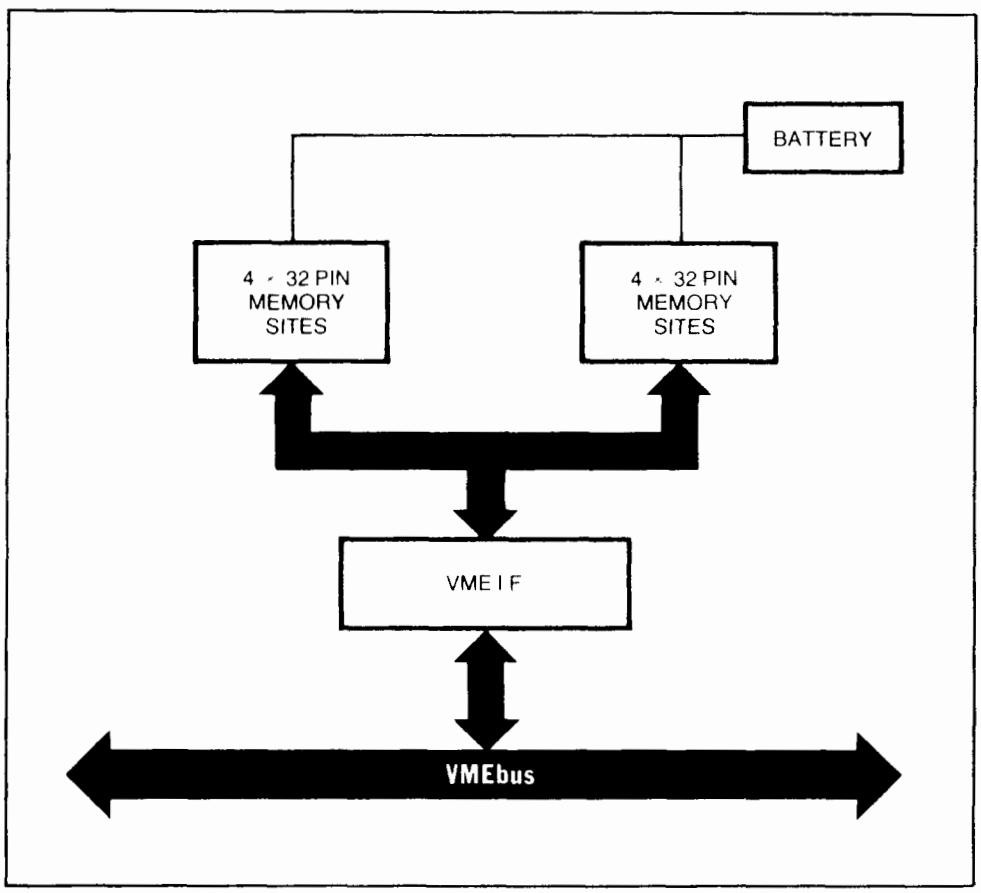


Figure B-1. Location of Jumpers and Test Points

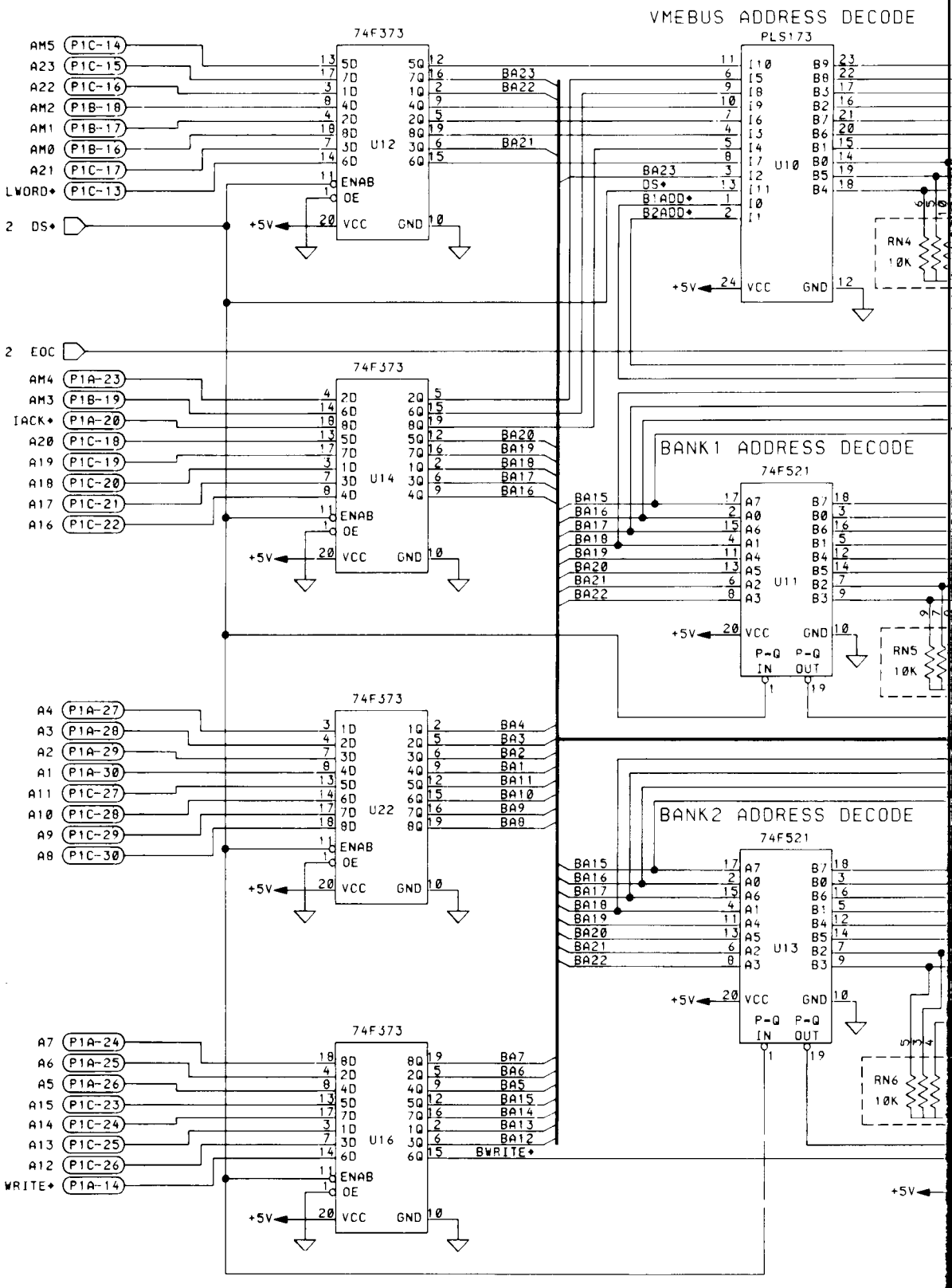
Appendix C

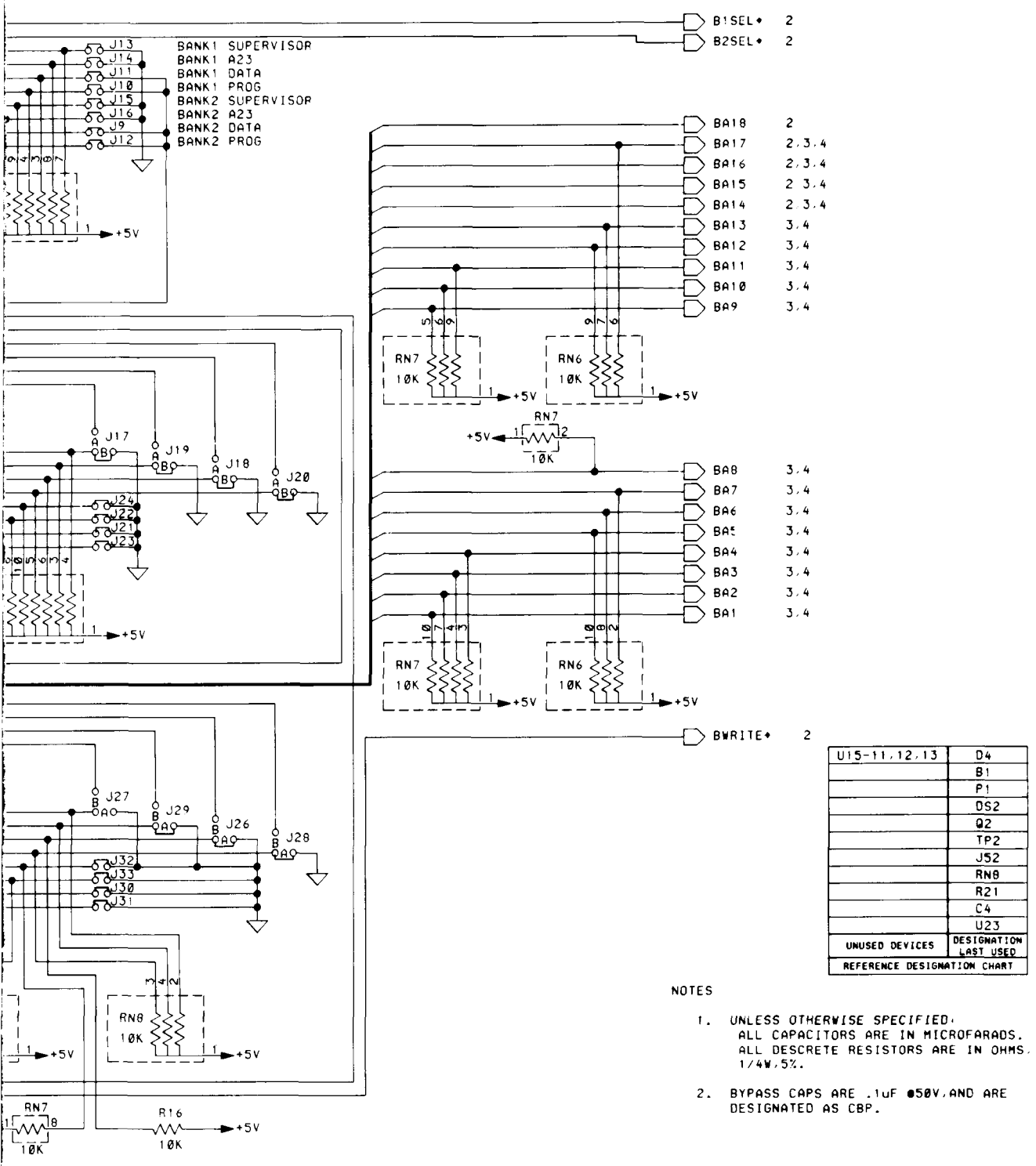
DIAGRAM AND SCHEMATICS





Operational Block Diagram


VMEBUS ADDRESS DECODE
74F373
U12
AM5 P1C-14
A23 P1C-15
A22 P1C-16
AM2 P1B-18
AM1 P1B-17
AM0 P1B-16
A21 P1C-17
LWORD* P1C-13
2 DS*
BA23
BA22
BA21
PLS173
U10
BA23
DS*
B1ADD*
B2ADD*
RN4
10K
+5V
2 EOC
74F373
U14
AM4 P1A-23
AM3 P1B-19
IACK* P1A-20
A20 P1C-18
A19 P1C-19
A18 P1C-20
A17 P1C-21
A16 P1C-22
BA20
BA19
BA18
BA17
BA16
BANK1 ADDRESS DECODE
74F521
U11
BA15
BA16
BA17
BA18
BA19
BA20
BA21
BA22
P-Q IN
P-Q OUT
RN5
10K
74F373
U22
A4 P1A-27
A3 P1A-28
A2 P1A-29
A1 P1A-30
A11 P1C-27
A10 P1C-28
A9 P1C-29
A8 P1C-30
BA4
BA3
BA2
BA1
BA11
BA10
BA9
BA8
BANK2 ADDRESS DECODE
74F521
U13
RN6
10K
74F373
U16
A7 P1A-24
A6 P1A-25
A5 P1A-26
A15 P1C-23
A14 P1C-24
A13 P1C-25
A12 P1C-26
WRITE* P1A-14
BA7
BA6
BA5
BA15
BA14
BA13
BA12
BWRITE*
ENAB
OE
VCC
GND



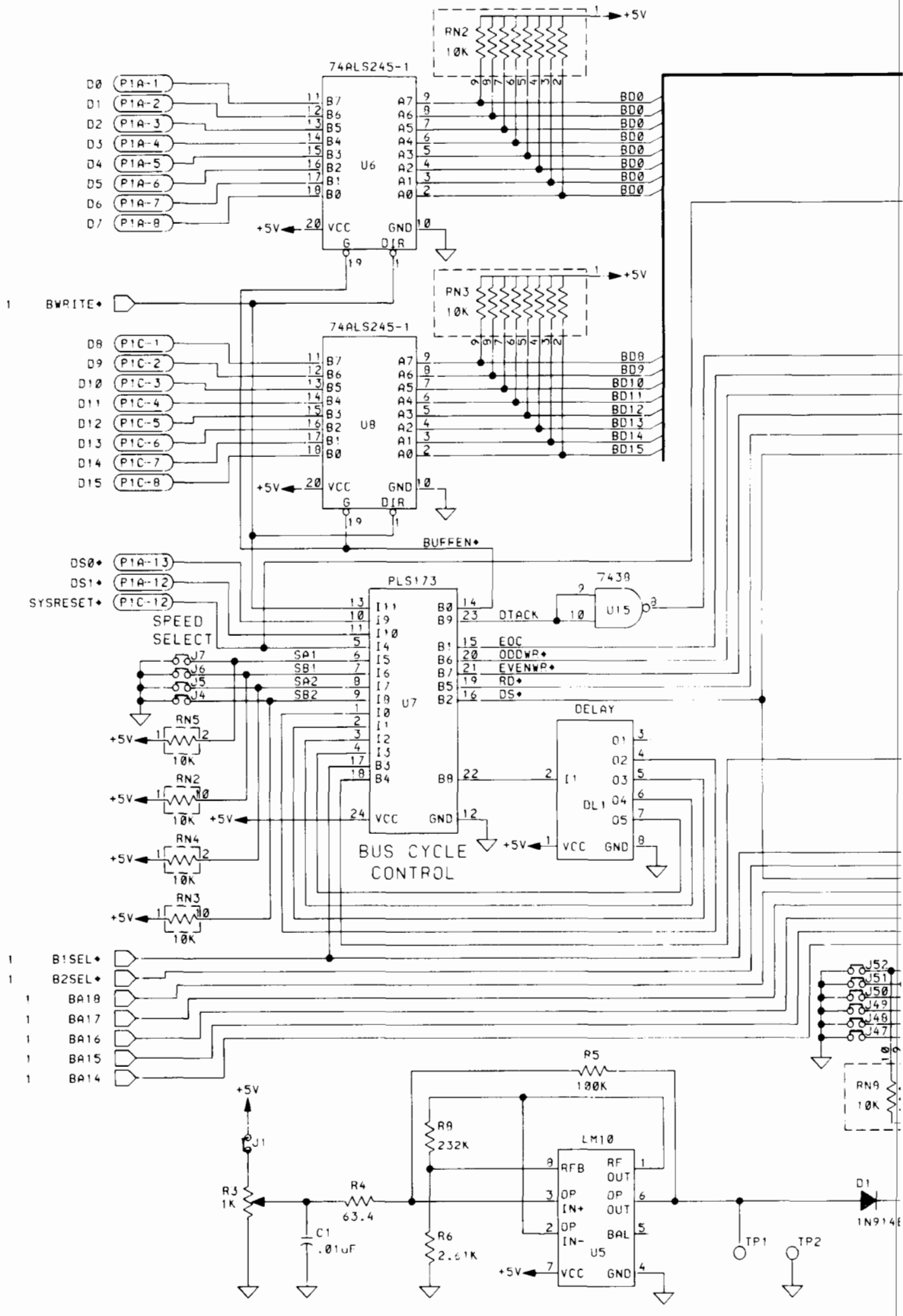
U15-11,12,13	D4
	B1
	P1
	DS2
	Q2
	TP2
	J52
	RN8
	R21
	C4
	U23
UNUSED DEVICES	DESIGNATION LAST USED
REFERENCE DESIGNATION CHART	

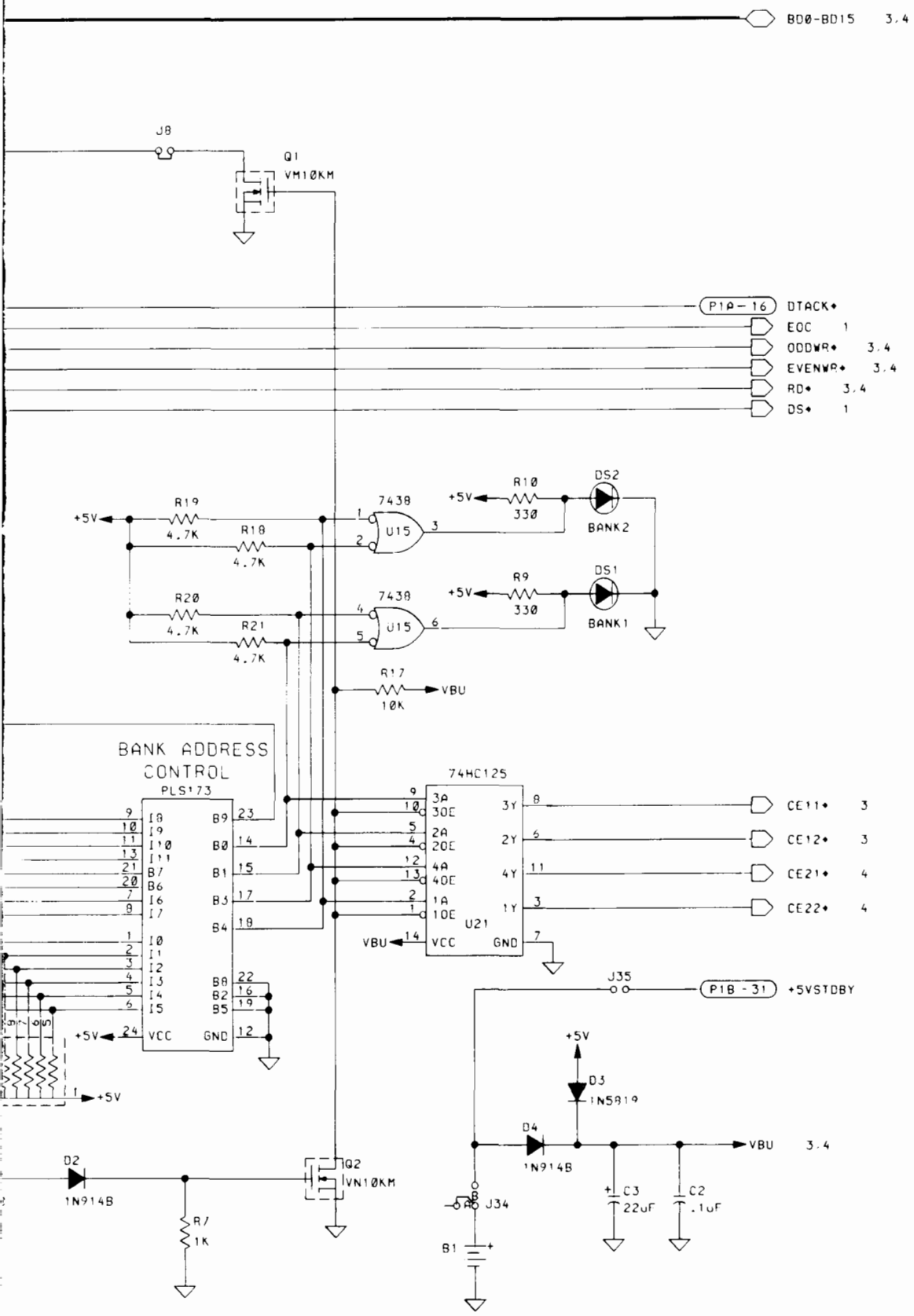
NOTES

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE IN MICROFARADS. ALL DESCRETE RESISTORS ARE IN OHMS, 1/4W,5%.

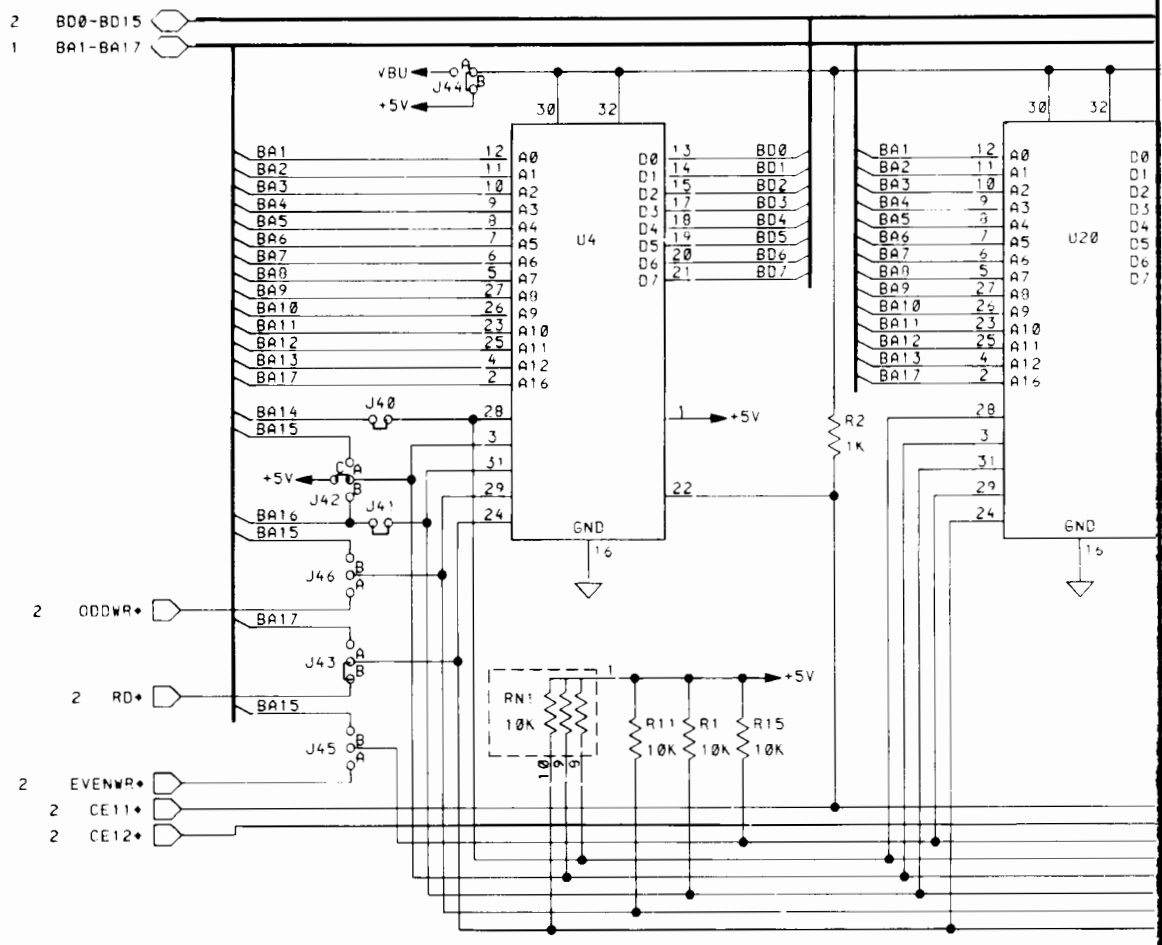
2. BYPASS CAPS ARE .1uF @50V,AND ARE DESIGNATED AS CBP.

XVME-100 Schematic Sheet 1 of 4

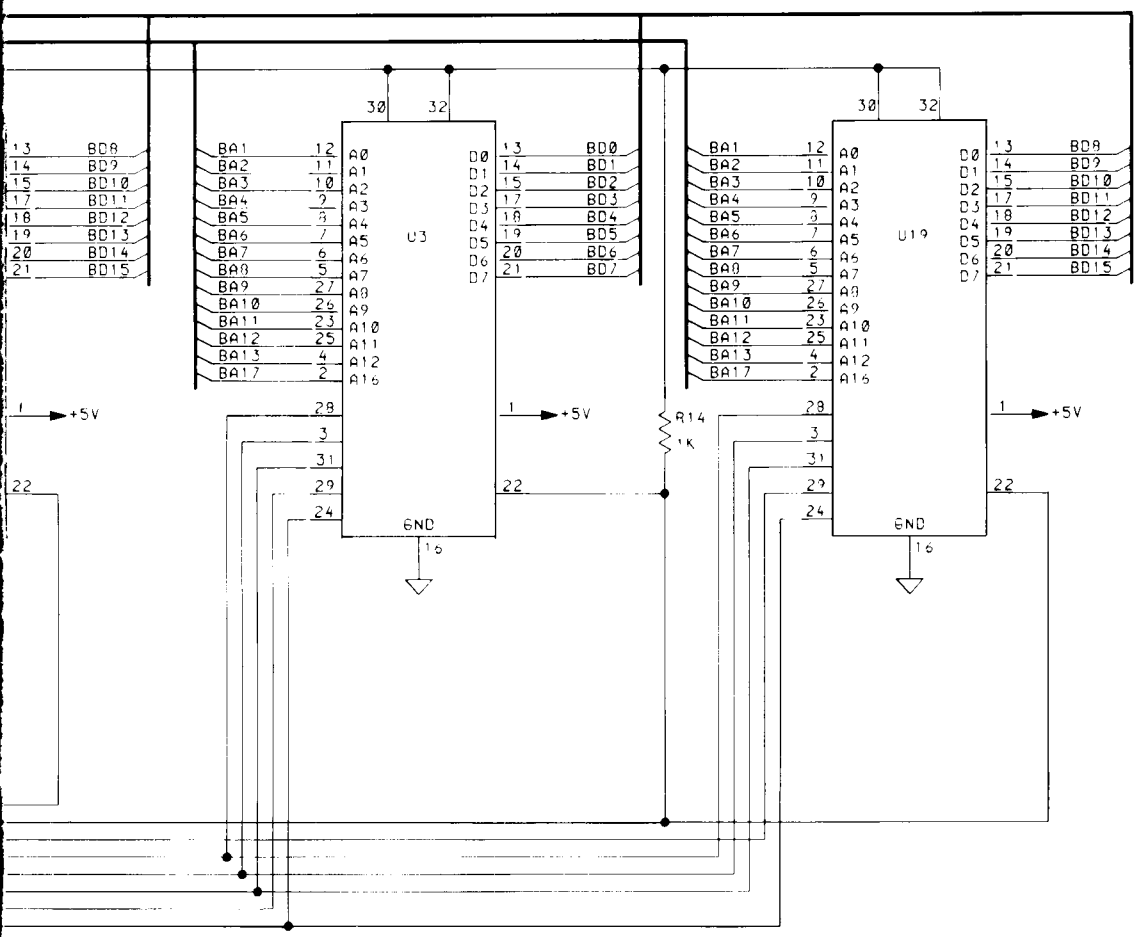

RN2
10K
+5V
74ALS245-1
U6
D0
D1
D2
D3
D4
D5
D6
D7
P1A-1
P1A-2
P1A-3
P1A-4
P1A-5
P1A-6
P1A-7
P1A-8
B7
B6
B5
B4
B3
B2
B1
B0
A7
A6
A5
A4
A3
A2
A1
A0
VCC
GND
G
DIR
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
RN3
10K
U8
D8
D9
D10
D11
D12
D13
D14
D15
P1C-1
P1C-2
P1C-3
P1C-4
P1C-5
P1C-6
P1C-7
P1C-8
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
BWRITE*
BUFFEN*
DS0*
DS1*
SYSRESET*
P1A-13
P1A-12
P1C-12
SPEED
SELECT
SA1
SB1
SA2
SB2
J7
J6
J5
J4
RN5
RN2
RN4
RN3
10K
PLS173
U7
DTACK
EOC
ODDWP*
EVENWP*
RD*
DS*
7438
U15
DELAY
DL1
BUS CYCLE
CONTROL
B1SEL*
B2SEL*
BA18
BA17
BA16
BA15
BA14
J52
J51
J50
J49
J48
J47
RN9
R5
100K
R9
232K
R6
2.61K
R4
63.4
R3
1K
C1
.01uF
J1
LM10
U5
RFB
OP IN+
OP IN-
RF OUT
OP OUT
BAL
D1
1N914
TP1
TP2

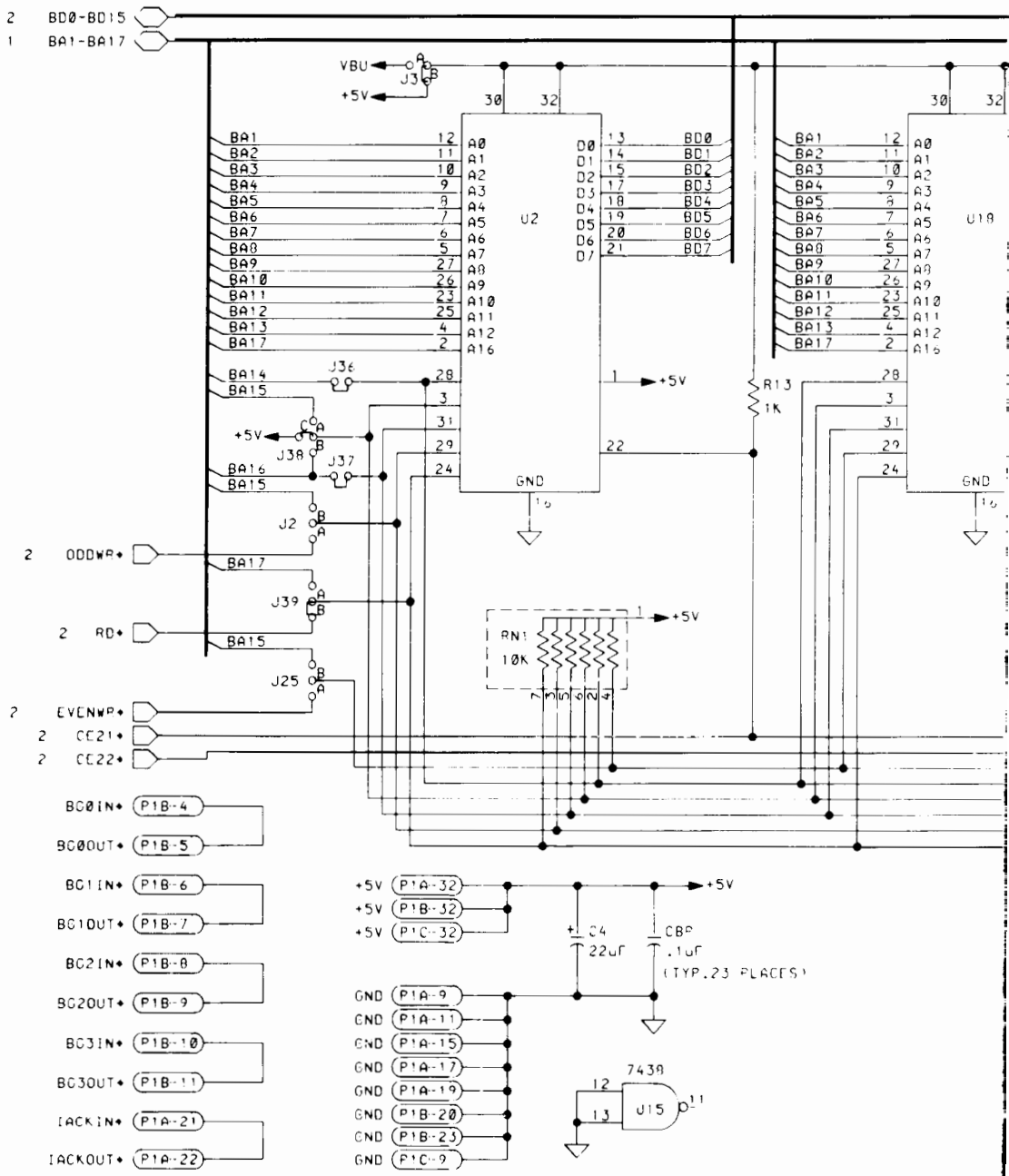


XVME-100 Schematic, Sheet 2 of 4

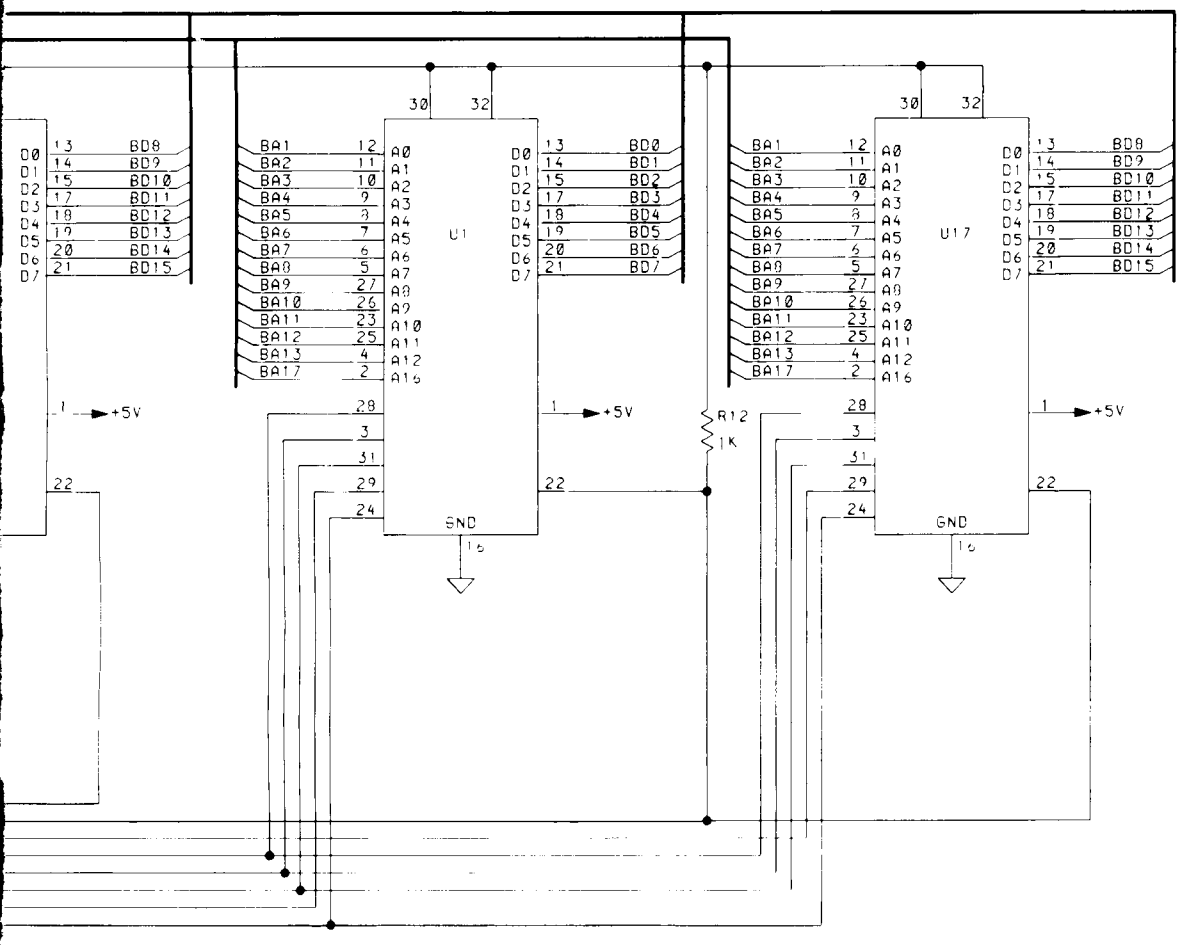

2 BD0-BD15
1 BA1-BA17
VBU
J44
+5V
30
32
U4
U20
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BA12
BA13
BA17
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A16
D0
D1
D2
D3
D4
D5
D6
D7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BA14
BA15
BA16
J40
J41
J42
J43
J45
J46
R2
1K
GND
RN1
10K
R11
R1
R15
2 ODDWR*
2 RD*
2 EVENWR*
2 CE11*
2 CE12*

MEMORY BANK 1




2 BD0-BD15
1 BA1-BA17
VBU
+5V
J35
U2
U19
R13
1K
RN1
10K
J36
J37
J38
J39
J2
J25
2 ODDWR*
2 RD*
2 EVENWR*
2 CE21*
2 CE22*
BG0IN* P1B-4
BG0OUT* P1B-5
BG1IN* P1B-6
BG1OUT* P1B-7
BG2IN* P1B-8
BG2OUT* P1B-9
BG3IN* P1B-10
BG3OUT* P1B-11
IACKIN* P1A-21
IACKOUT* P1A-22
+5V P1A-32
+5V P1B-32
+5V P1C-32
C4 22uF
CBP .1uF (TYP. 23 PLACES)
GND P1A-9
GND P1A-11
GND P1A-15
GND P1A-17
GND P1A-19
GND P1B-20
GND P1B-23
GND P1C-9
7438
U15

MEMORY BANK 2



Appendix D

QUICK REFERENCE GUIDE

Table D-1. Jumper List

Jumper	Description	Section
J1	Power Monitor Calibration	2.4.6
J2	Memory Type - bank 2	2.4.4
J3	Memory Type - bank 2	2.4.4
J4	Speed Select - bank 2	2.4.3
J5	Speed Select - bank 2	2.4.3
J6	Speed Select - bank 1	2.4.3
J7	Speed Select - bank 1	2.4.3
J8	SYSRESET* Driver, enable	2.4.6
J9	Data Access - bank 2	2.4.2
J10	Program Access - bank 1	2.4.2
J11	Data Access - bank 1	2.4.2
J12	Program Access - bank 2	2.4.2
J13	Supervisor Only - bank 1	2.4.2
J14	VME Address - bank 1	2.4.1
J15	Supervisor Only - bank 2	2.4.2
J16	VME Address - bank 2	2.4.1
J17	VME Address - bank 1	2.4.1
J18	VME Address - bank 1	2.4.1
J19	VME Address - bank 1	2.4.1
J20	VME Address - bank 1	2.4.1
J21	VME Address - bank 1	2.4.1
J22	VME Address - bank 1	2.4.1
J23	VME Address - bank 1	2.4.1
J24	VME Address - bank 1	2.4.1
J25	Memory Type - bank 2	2.4.4
J26	VME Address - bank 2	2.4.1
J27	VME Address - bank 2	2.4.1
J28	VME Address - bank 2	2.4.1
J29	VME Address - bank 2	2.4.1
J30	VME Address - bank 2	2.4.1
J31	VME Address - bank 2	2.4.1
J32	VME Address - bank 2	2.4.1
J33	VME Address - bank 2	2.4.1
J34	Battery, alternate power source	2.4.5
J35	+5V STDBY, alternate power source	2.4.5
J36	Memory Type - bank 2	2.4.4
J37	Memory Type - bank 2	2.4.4
J38	Memory Type - bank 2	2.4.4
J39	Memory Type - bank 2	2.4.4
J40	Memory Type - bank 1	2.4.4
J41	Memory Type - bank 1	2.4.4
J42	Memory Type - bank 1	2.4.4

Table D-1. Jumper List (continued)

Jumper	Description	Section
J43	Memory Type - bank 1	2.4.4
J44	Memory Type - bank 1	2.4.4
J45	Memory Type - bank 1	2.4.4
J46	Memory Type - bank 1	2.4.4
J47	Size Select - bank 2	2.4.1
J48	Size Select - bank 2	2.4.1
J49	Size Select - bank 2	2.4.1
J50	Size Select - bank 1	2.4.1
J51	Size Select - bank 1	2.4.1
J52	Size Select - bank 1	2.4.1

Table D-2. VME Base Address and Memory Chip Size Jumpers

BANK 1

BASE ADDRESS BIT	= 1	= 0
A23	J14 Out	J14 In*
A22	J23 Out	J23 In*
A21	J21 Out	J21 In*
A20	J22 Out	J22 In*
A19	J24 Out	J24 In*
A18	J20 Out	J20B*
A17	J18 Out	J18B*
A16	J19 Out	J19B*
A15	J17 Out	J17B*

* Factory shipped configuration

Device Size In Bits	J17	J19	J18	J20	J50	J51	J52	J14	J23	J21	J22	J24
8K x 8	X	X	X	X	In	In	In	X	X	X	X	X
16K x 8	A	X	X	X	In	In	Out	X	X	X	X	X
32K x 8	A	A	X	X	In	Out	In	X	X	X	X	X
64K x 8	A	A	A	X	In	Out	Out	X	X	X	X	X
128K x 8	A	A	A	A	Out	In	In	X	X	X	X	X

X = Use to define state of corresponding base address bit per above chart

BANK 2

BASE ADDRESS BIT	= 1	= 0
A23	J16 Out	J16 In*
A22	J31 Out	J31 In*
A21	J30 Out	J30 In*
A20	J33 Out	J33 In*
A19	J32 Out	J32 In*
A18	J28 Out	J28A*
A17	J26 Out	J26A*
A16	J29 Out	J29A*
A15	J27 Out	J27A*

* Factory shipped configuration

Device Size In Bits	J27	J29	J26	J28	J47	J48	J49	J16	J31	J30	J33	J32
8K x 8	X	X	X	X	In	In	In	X	X	X	X	X
16K x 8	B	X	X	X	In	In	Out	X	X	X	X	X
32K x 8	B	B	X	X	In	Out	In	X	X	X	X	X
64K x 8	B	B	B	X	In	Out	Out	X	X	X	X	X
128K x 8	B	B	B	B	Out	In	In	X	X	X	X	X

X = Use to define state of corresponding base address list per above chart

Table D-3. Address Modifier Jumpers

BANK 1

Jumpers	Description
J13 In*	Supervisor Only AM2 = 1
J13 Out	Supervisor & Non-privileged AM2 = don't care
J11 In*	Data Access Responds to Address Modifier codes 3DH or 39H
J11 Out	No Data Access Won't respond to 3DH or 39H
J10 In*	Program Access 3EH or 3AH
J10 Out	No Program Access Won't respond to 3EH or 3AH

BANK 2

Jumpers	Description
J15 In*	Supervisor Only AM2 = 1
J15 Out	Supervisor & Non-privileged AM2 = don't care
J9 In*	Data Access Responds to Address Modifier codes 3DH or 39H
J9 Out	No Data Access Won't respond to 3DH or 39H
J12 In*	Program Access 3EH or 3AH
J12 Out	No Program Access Won't respond to 3EH or 3AH

* = Factory shipped configuration

Table D-4. Memory Device Speed Jumpers

BANK 1

Speed Select	Jumpers J6	J7
100ns	Out	Out
150ns	Out	In
200ns	In	Out
250ns	In*	In*

BANK 2

Speed Select	Jumpers J4	J5
100ns	Out	Out
150ns	Out	In
200ns	In	Out
250ns	In*	In*

* = Factory shipped configuration

Alternative Power Source	J34	J35
None	A*	Out*
Battery	B	Out
+5V Standby	A	In

* Factory shipped configuration

The user has three different options available for choosing alternate power source of each bank. These options depend on the configurations of J34 and J35 and are as follows:

Alternate Power Source = Battery (J34B, J35 OUT)

Bank 1 Power	J44
Battery	A
Vcc*	B
Bank 2 Power	**J3**
Battery	A
Vcc*	B

Alternate Power Source = +5V Standby (J34A, J35 IN)

Bank 1 Power	J44
+5V Standby	A
Vcc*	B
Bank 2 Power	**J3**
+5V Standby	A
Vcc*	B

Alternate Power Source = None (J34A, J35 OUT factory shipped configuration)

Bank 1 Power	J44
Vcc*	B
Bank 2 Power	**J3**
Vcc*	Binstalled to prevent drawing current from the alternate power source.

* If EEPROM or EPROM are installed in any bank, the Vcc Jumper should be installed to prevent drawing current from the alternate power source.

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