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XVME-630

68EC030 Processor Module

74630-002 A

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1.1 PRODUCT OVERVIEW

The XVME-630 is a high-performance, low-cost VMEbus compatible processor module. This single-board, double-high processor contains a 68EC030 CPU running at 25 or 40 MHz. The module contains three memory banks, each of which has four sockets. Bank 1 is designed to accept high-speed SRAM and Bank 2 accepts EPROM. Bank 3 is dual-ported to the VMEbus and can accommodate SRAM, EPROM, or Flash memory. Maximum memory is 2 Mbytes of SRAM in Bank 1; 4 Mbytes of EPROM in Bank 2; and 4 Mbytes of EPROM, 2 Mbytes of SRAM, or 1 Mbyte of Flash memory in Bank 3.

The XVME-630 Processor Module also provides two asynchronous/synchronous serial channels and two 16-bit programmable timers via an on-board 68562 Dual Universal Serial Communications Controller (DUSCC). Serial channel A is a dedicated RS-232C port, whereas channel B can be jumper-configured to RS-232C or RS-485.

The XVME-630 Processor Module provides all the VMEbus utilities required for a complete system, including:

- SYSCLK
- SYSRESET
- A single level arbiter
- A bus timer
- IACK daisy chain driver

The XVME-630 processor is specified as an A32/A24/A16:D32/D16/D08(EO) VMEbus Master, and as an IH(1)-IH(7) interrupt handler.

The XVME-630 module is equipped with three front panel LEDs to indicate diagnostic PASS/FAIL status (diagnostics are available separately as a monitor/RAM kit or can be written by the user) as well as RUN status.

Optional features include a probe and debug monitor (XVME-991) and a 68882 math co-processor (XVME-693/40).

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1.2 MANUAL STRUCTURE

The chapters in this manual are organized as follows:

Chapter One	**Module Description.** A general description of the XVME-630 Processor Module, including complete functional and environmental specifications, VMEbus compliance information, and a detailed block diagram.
Chapter Two	**Installation.** Module installation information such as jumper settings; connector pinouts; and chip, board, and optional math co-processor installation procedures.
Chapter Three	**Programming.** Includes the module memory map, caching information, 68562 DUSCC, control/status registers, the interrupt structure, RMW capabilities of dual-ported memory, real time clock programming, and software notes.
Appendix A	**VMEbus Connector/Pin Description.** Provides the pinouts and descriptions of the standard VMEbus backplane connectors P1 and P2 and the XVME-630 JK1 connector pinouts.
Appendix B	**Quick Reference Guide.** Lists jumpers, connectors, tables, device parameters according to wait states, and other reference information.
Appendix C	**Block Diagram, Assembly Drawing, and Schematics.**

NOTE

Two additional manuals are shipped with the XVME-630 to fully document its peripheral devices:

- Motorola MC68HC68T1 information (reprinted with permission of Motorola, and referenced as Xycom part number 74630-003)
- Signetics 68562 DUSCC Controller Manual (reprinted with permission of Signetics, and referenced as Xycom part number 74630-004)

The XVME-630 Manual covers module hardware specifics, register access addresses, and operational programming constraints. The Motorola manual provides information on the real time clock. The Signetics manual describes DUSCC programming and all other features of the DUSCC.

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1.3 XVME-630 FEATURES

The XVME-630 offers the following features:

- Motorola 68EC030 running at CPU speeds of either 25 or 40 MHz
- Motorola 68882 floating-point co-processor site
- Four 0 wait-state (2 clock reads, 3 clock writes) local SRAM sites. The sites support SRAM sizes from 32Kx8 up to 512Kx8 in a standard 28- or 32-pin JEDEC pinout (.300, .400, and .600 widths)
- Four 1, 2, 3, and 4 wait-state (3, 4, 5, and 6 clocks) local EPROM sites. The sites support EPROM sizes from 27C010 (128Kx8) to 27C080 (1Mx8) in a standard 32-pin JEDEC pinout (.600 wide only)
- Four dual-ported SRAM/EPROM/Flash sockets (with battery backed option). The sites support SRAM sizes from 64Kx8 to 512Kx8, EPROM sizes 27C010 (128Kx8) to 27C080 (1Mx8), and Flash sizes from 64Kx8 to 256Kx8, in a standard 32-pin JEDEC pinout (.600 wide only)
- Two asynchronous/synchronous serial channels based on the Signetics SCN68562 DUSCC chip. Channel A is RS-232C only; channel B is RS-232C or RS-485
- Serial battery-backed real time clock based on the Motorola MC68HC68T1. Also contains 32 bytes of battery-backed RAM
- BERR* timer with a BTO of 40.96 uS @ 25 MHZ and 25.6 uS @ 40 MHz typical
- Software watchdog timer with an approximate timeout of 160 uS
- Programmable VMEbus interrupter
- Interrupt handler
- VMEbus system controller functions including
  - Single level arbiter
  - 16 MHZ SYSCLK generator
  - IACK daisy-chain driver
  - Power monitor/SYSRESET* generator
- 2 user-defined, software-readable jumpers

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1.4 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows an operational block diagram of the XVME-630 Processor Module.

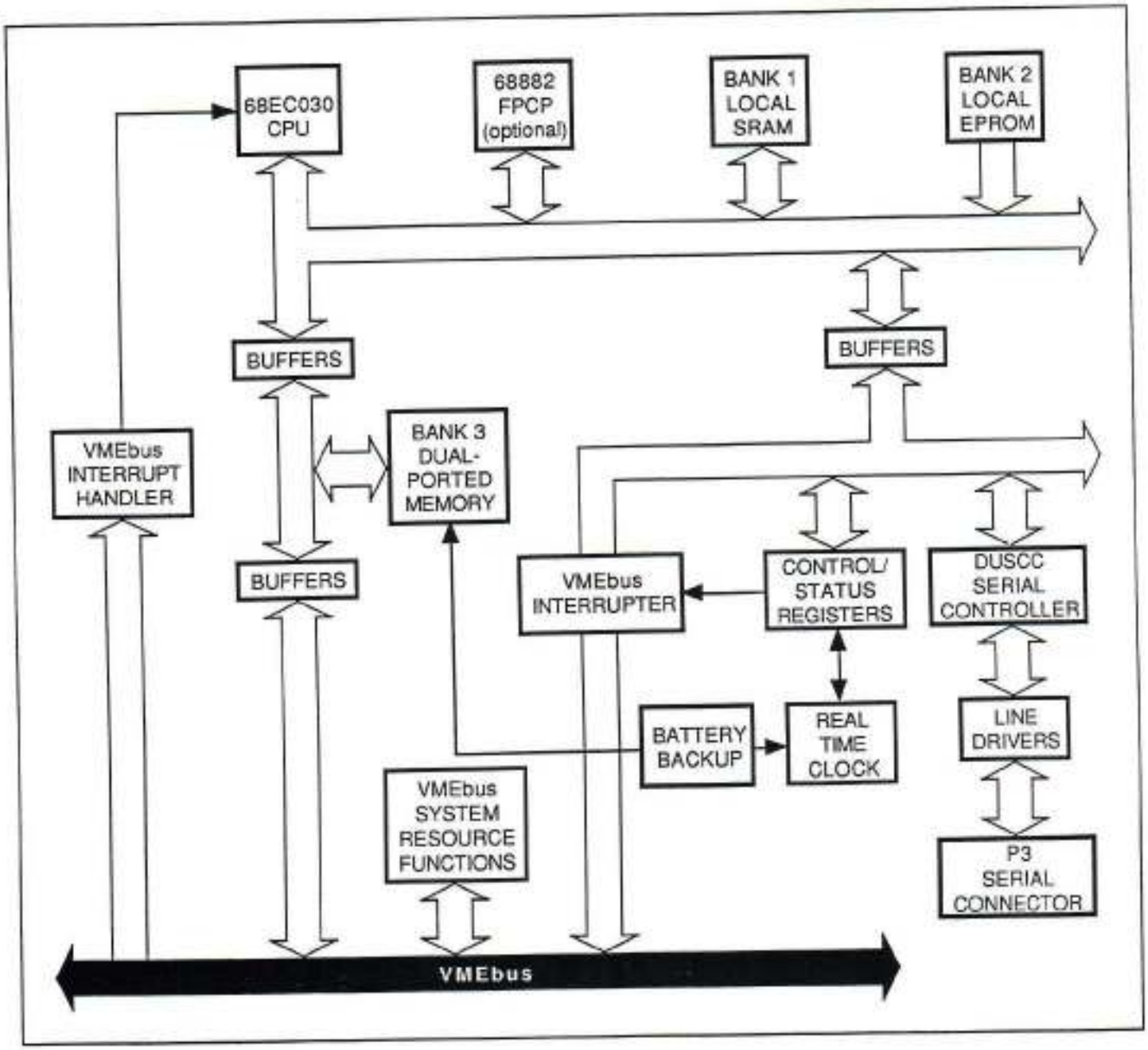


Figure 1-1. Module Operational Block Diagram

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1.4.1 68EC030 CPU

The XVME-630 Processor Module contains a Motorola MC68EC030 chip in a 128-pin PGA package, which runs at 25 or 40 MHz.

The CPU contains a 256 byte instruction cache, and a 256 byte data cache. These caches are each organized as 64 longword entries. Any time the CPU is allowed to cache a data fetch, the 68EC030 will fetch the additional data required to complete the cache entry. Along with the cache disable bits in the control/status registers, the caches may be ultimately disabled by control bits within the 68EC030 and by installing jumper J11.

For more information on control/status registers, see section 3.5.

For more information on caching, see section 3.3.

1.4.2 VMEbus Master Interface

The VME master interface on the XVME-630 Processor Module supports the following bus cycles:

- A32 (address modifier codes 09H, 0AH, 0DH, 0EH)
- A24 (address modifier codes 39H, 3AH, 3DH, 3EH)
- A16 (address modifier codes 29H, 2DH)
- D32
- D16
- D08(EO)
- Read-Modify-Write (RMW) cycles - D08(EO)
- Interrupt acknowledge cycles - D8(O)

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1.4.3 68562 Dual Universal Serial Communications Controller (DUSCC)

The Signetics SCN68562 serial controller is a dual asynchronous/synchronous receiver/transmitter in a 44-pin PLCC package. It provides two serial communication channels: channel A is configured for RS-232C operation, while channel B is jumper-configurable for either RS-232C or RS-485 operation.

The DUSCC also contains two programmable, 16-bit counter/timers associated with each serial channel. The counter/timers may be used as general purpose counter/timers when not required by that serial channel.

The DUSCC provides various inputs and outputs. These I/O points are used by the CPU to control and monitor a variety of module functions. The input lines are used to monitor the two user-configurable jumpers. The output lines are used to control serial channels A and B DTR output and the tri-stating of the RS-485 drivers.

1.4.4 Memory Banks

Three memory banks, consisting of four sockets each, provide a total of 12 32-pin memory sites to install RAM, EPROM, and Flash memory devices. Bank 1 is designed to accept high-speed SRAM devices and Bank 2 accepts EPROM devices. Bank 3 is dual-ported and can accept SRAM, EPROM, or Flash memory devices. See page 2-12 for the types of devices supported.

1.4.5 Interrupt Handler

The XVME-630 Processor Module can respond to all seven VMEbus interrupt levels. The VMEbus interrupt levels that the XVME-630 will handle are selected through seven jumpers, each corresponding to an interrupt request level. The interrupt handler prioritizes the interrupt sources, with on-board interrupts having a higher priority.

For more information on the interrupt handler, refer to section 3.6.1.

1.4.6 Interrupter

The 68EC030 processor can generate VMEbus interrupts on any of the seven VMEbus interrupt levels (D08(O)) through the interrupt vector register and control/status register 2. The interrupt vector register is a write-only register which contains the 8-bit vector which will be placed on the VME data bus during an interrupt acknowledge cycle. Control/status register 2 consists of six bits, which represent the binary value of the interrupt level to be generated. For information on setting these bits, refer to section 3.5.3.

For more information on the interrupter, refer to section 3.6.2.

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1.4.7 System Resource Functions

The XVME-630 Processor Module provides the following system resource functions:

- 16 MHz SYSCLK driver
- SYSRESET driver
- IACK daisy-chain driver
- Single-level arbiter
- Bus timeout

All system resource functions except the IACK daisy-chain driver can be enabled/disabled via jumpers (refer to section 2.2.9). (The IACK daisy chain driver is always operational and does not require jumpering.)

1.4.8 Real Time Clock

The XVME-630 contains a Motorola MC68HC68T1 time-of-day chip driven by a 32.768 KHz crystal. The crystal has an accuracy over the entire operating temperature range of +.003%, -.007% (+2.59 sec/day, -6.05 sec/day).

The MC68HC68T1 also contains 32 bytes of battery-backed CMOS SRAM and can interrupt the 68EC030.

1.4.9 Floating-Point Co-processor (Optional)

The XVME-630 has a 68-pin PGA socket which accepts a Motorola MC68882 floating point co-processor. This co-processor must run at the same speed as the 68EC030. The co-processor will respond to all floating-point instructions without regard to its co-processor ID.

> **NOTE**
> Floating point instructions executed without a floating point co-processor installed will result in a 68EC030 BERR* (LINE 1010 EMULATOR vector).

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1.4.10 Power Monitor Circuit

The XVME-630's power monitor circuit is based on the MAX690 chip from MAXIM. The chip performs two major functions:

- Monitors the system voltage and supplies a reset to the system if the voltage drops below a specified value.
- Provides a means of monitoring the battery voltage. Using bit 6 of control register 1 to load the battery, you can then determine whether the battery voltage is high enough to back up all the battery-backed devices by bit 6 in status register 0.

1.5 REFERENCE DOCUMENTS

The following documents are not included with the Xycom literature, but may be helpful for using the XVME-630. Contact Motorola for ordering information.

Publisher	Title	Part Number
Motorola	MC68EC030 User's Manual	MC68EC030UM/AD
Motorola	Programmer's Reference Manual	M68000PM/AD
Motorola	MC68881/882 User's Manual	MC68881UM/AD, Rev. 2

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1.6 SPECIFICATIONS

The tables below list the operational and environmental specifications for the XVME-630.

Table 1-1. Operational Specifications

CHARACTERISTIC	SPECIFICATIONS	
Processor	Motorola MC68EC030	
Speed	25 or 40 MHz	
Optional Math Co-processor		
Device	Motorola MC68882	
Speed Required	Same as CPU	
Serial Controller	Signetics SCN68562 (DUSCC), 2 async/sync channels, 2 16-bit counter/timers, multi-protocol operation	
Compatibility	One RS-232C only; one RS-232C or RS-485	
Maximum Data Rate	RS-232C	RS-485
Async Transmit	19.2 Kbps	38.4 Kbps
Async Receive	19.2 Kbps	38.4 Kbps
Sync Transmit	20 Kbps	4 Mbps
Sync Receive	20 Kbps	3.5 Mbps
Signals	TXD, RXD, RTS, CTS, DTR, DCD, TXC, RXC	
Real Time Clock	Motorola MC68HC68T1 driven by a 32.768 KHz crystal, time of day functions, periodic interrupts (488 uS to once-a-day), crystal accuracy range +.003%, -.007% (+2.59 sec/day, -6.05 sec/day), alarm function, 32 bytes of battery backed RAM	
Front Panel Indicators	FAIL (red), PASS (green), and RUN (green)	
Front Panel Switches	RESET and ABORT	
Power Requirements		
25 MHz	+5 V: 2.5 A typical, 3.5 A maximum +12 V: 32 mA typical, 50 mA maximum -12 V: 32 mA typical, 50 mA maximum	
40 MHz	+5 V: 3.5 A typical, 4.5 A maximum +12 V: 32 mA typical, 50 mA maximum -12 V: 32 mA typical, 50 mA maximum	

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Table 1-2. Environmental Specifications

CHARACTERISTIC	SPECIFICATIONS
Temperature	
Operating	0° to 65° C (32° to 149° F)
Non-operating	-40° to 85° C (-40° to 185° F)
Humidity	5 to 95% RH non-condensing (Extremely low humidity may require protection against static discharge.)
Altitude	
Operating	Sea-level to 10,000 ft. (3048 m)
Non-operating	Sea-level to 50,000 ft. (15240 m)
Vibration	
Operating	5 to 2000 Hz .015" peak to peak 2.5 g peak acceleration
Non-operating	5 to 2000 Hz .030" peak to peak 5.0 g peak acceleration
Shock	
Operating	30 g peak acceleration 11 msec duration
Non-operating	50 g peak acceleration 11 msec duration

Table 1-3. VMEbus Specifications

VMEbus Compliance

- A32/A24/A16:D32/D16/D08(EO) DTB master
- A32/A24:D32/D16/D08(EO) DTB slave
- RMW capability
- IH(1)-IH(7) D08(O) interrupt handler
- SGL arbiter
- R(0-3) bus requester
- RWD, ROR, or ROBC bus release
- ROACF (software controlled) bus release
- IDCD IACK daisy chain driver
- SYSCLK and SYSRESET driver
- Monitors SYSFAIL and ACFAIL
- Form factor: DOUBLE
  233.35 mm x 160 mm (9.2" x 6.3")

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2.1 INTRODUCTION

This chapter describes the XVME-630 jumpers and connectors, how to install memory chips and an optional math co-processor, and how to install the XVME-630 into a backplane.

2.2 CONFIGURING THE JUMPERS

Prior to installing the XVME-630 board, you must configure the jumpers to match your application. The jumper locations are shown on the following page. The jumper functions are listed in Table 2-1 and described fully in the following sections.

NOTE
The XVME-630 is shipped with all jumpers positioned on the stake posts. You must configure the board to your system needs. Refer to the jumper lists on the following pages for more information.

NOTE
The XVME-630 obtains power from both the VMEbus P1 and P2 backplanes. Both backplanes must be installed for proper operation.

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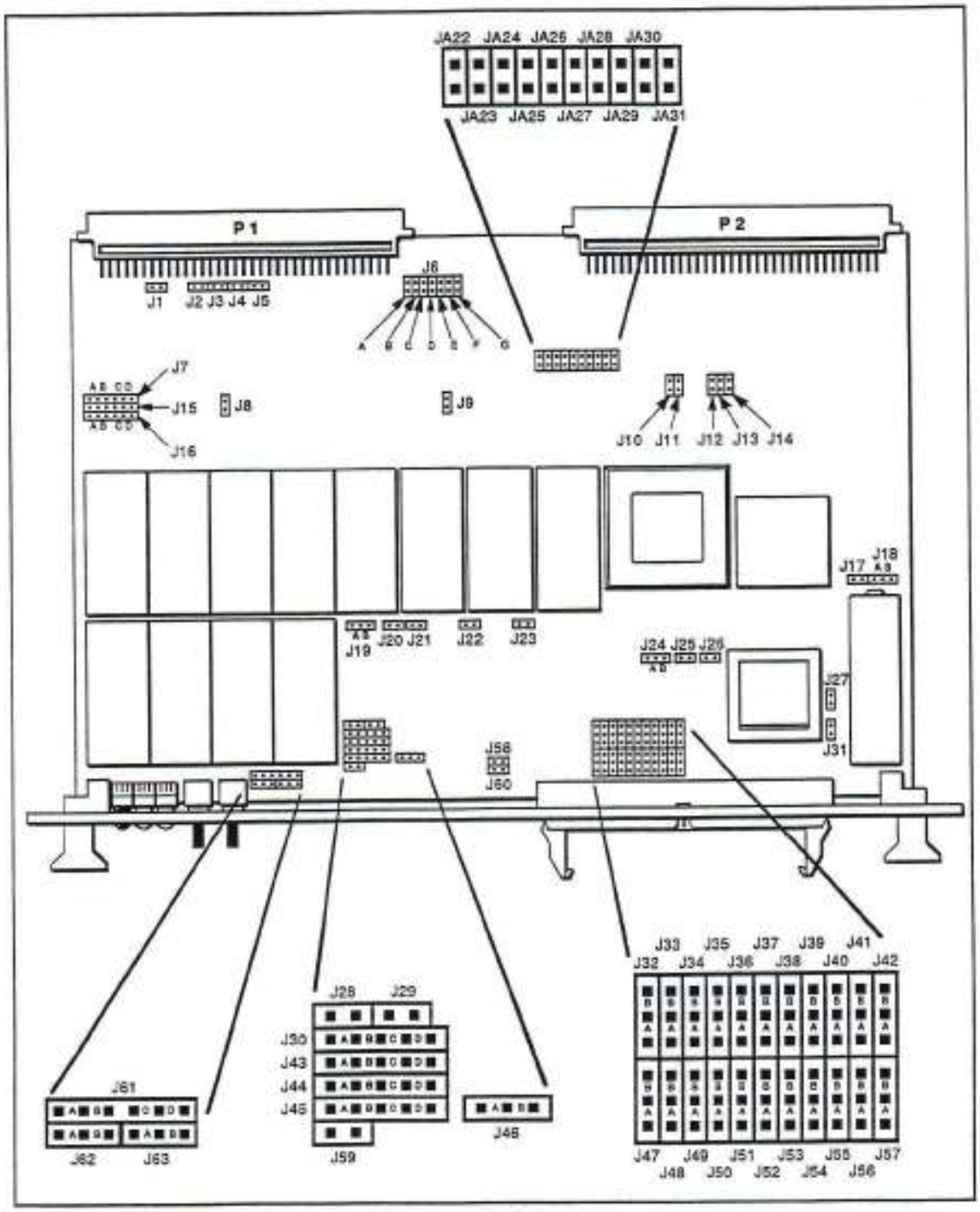


Figure 2-1. Jumper Locations

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Table 2-1. Jumper Settings

Jumper	Position	Function	Section Reference
J1	IN	VMEbus BERR* timer enabled	2.3.9
	OUT	VMEbus BERR* timer disabled	
J2	IN	VMEbus SYSCLK driver enabled	2.3.9
	OUT	VMEbus SYSCLK driver disabled	
J3	IN	VMEbus single level arbiter enabled	2.3.9
	OUT	VMEbus single level arbiter disabled	
J4	IN	VMEbus SYSFAIL* driver enabled	2.3.13
	OUT	VMEbus SYSFAIL* driver disabled	
J5	IN	Dual-ported memory responds to supervisory or non-privileged VMEbus slave accesses	2.3.4
	OUT	Dual-ported memory responds only to supervisory VMEbus slave accesses	
J6	IN	VMEbus interrupt handler, handles IRQ	2.3.11
	OUT	VMEbus interrupt handler, does not handle IRQ	
	A	VMEbus IRQ7*	
	B	VMEbus IRQ6*	
	C	VMEbus IRQ5*	
	D	VMEbus IRQ4*	
	E	VMEbus IRQ3*	
	F	VMEbus IRQ2*	
	G	VMEbus IRQ1*	
J7, J15,J16		**VMEbus Master Bus Requester Level** / **BGIN to BGOUT Jumpers (outside posts only)**	2.3.2
	A	0 — J7B-J15B, J7C-J15C, J7D-J15D	
	B	1 — J7A-J15A, J7C-J15C, J7D-J15D	
	C	2 — J7A-J15A, J7B-J15B, J7D-J15D	
	D	3 — J7A-J15A, J7B-J15B, J7C-J15C	
J8	IN	Dual-ported memory responds to VMEbus Standard address space slave accesses	2.3.4
	OUT	Dual-ported memory responds to VMEbus Extended address space slave accesses	

All jumpers are installed when shipped.

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Table 2-1. Jumper Settings (Continued)

Jumper	Position	Function	Section Reference
J9	IN OUT	Release on request VMEbus bus release mechanism Do not release on request	2.3.12
J10		NOT USER CONFIGURABLE	
J11	IN OUT	Cache disabled Cache enabled	2.3.3
J12 J13 J14 OUT OUT OUT OUT OUT IN OUT IN OUT OUT IN IN IN OUT OUT IN OUT IN IN IN OUT IN IN IN		Dual-ported memory 8 wait states 2 wait states 3 wait states 4 wait states 5 wait states 6 wait states 7 wait states 8 wait states	2.3.7.2
J15		Used with J7 and J16 (see J7 on previous page)	2.3.2
J16		Used with J7 and J15 (see J7 on previous page)	2.3.2
J17	IN OUT	Oscillator power applied (normal operation) Oscillator not powered (test mode)	2.3.5
J18	A B	Battery disconnected (shipping position) Battery connected (normal operation)	2.3.1
J19 J20 A OUT A OUT A IN B IN		Determines local EPROM device 27C010 27C020 27C040 27C080	2.3.7.1
J21,J23 J22 IN OUT OUT IN		Sets local SRAM device size 28-pin 32-pin	2.3.7.1
J24	A B	1 wait-state local SRAM reads/writes 0 wait-state local SRAM reads/1 wait-state writes	2.3.7.2

All jumpers are installed when shipped.

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Table 2-1. Jumper Settings (Continued)

Jumper	Position	Function	Section Reference
J25 IN IN OUT OUT	**J26** IN OUT IN OUT	Sets local EPROM wait state reads 1 wait-state reads 2 wait-state reads 3 wait-state reads 4 wait-state reads	2.3.7.2
J27		User definable, software readable jumper	2.3.10
J28	IN OUT	Reset push button will reset the XVME-630 Reset push button will not reset the XVME-630	2.3.8
J29	IN OUT	Reset push button will generate VMEbus SYSRESET* Reset push button will not generate VMEbus SYSRESET*	2.3.8
J30		Used to specify dual-ported memory device type with J43, J44, J45, J46, J59, J61, J62, and J63	2.3.7.1
J31		User definable jumper	2.3.10
J32-J42, J47-J57	A B	Serial channel B is RS-232C Serial channel B is RS-485	2.3.6
J43-J46		Used to specify dual-ported memory device type with J40, J59, J61, J62, and J63	2.3.7.1
J58	IN OUT	XVME-630 will be reset by a VMEbus SYSRESET* XVME-630 will not be reset by a VMEbus SYSRESET*	2.3.8
J59		Used to specify dual-ported memory device type with J30, J43, J44, J45, J46, J61, J62, and J63	2.3.7.1
J60		XVME-630 can generate a VMEbus SYSRESET* XVME-630 cannot generate a VMEbus SYSRESET*	2.3.8
J61-J63		Used to specify dual-ported memory device type with J30, J43, J44, J45, J46, and J59	2.3.7.1
JA22-JA23		Selects Standard or Extended VMEbus slave address (A23-A22) (in=0, out=1)	2.3.4
JA24-JA31		Selects Extended VMEbus slave address (A31-A24) (in=0, out=1)	2.3.4

All jumpers are installed when shipped.

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2.3 JUMPER DESCRIPTIONS

The following sections describe the jumper configurations for the XVME-630 module. Jumpers are grouped by functionality, and the functions appear in alphabetical order.

2.3.1 Battery (J18)

When jumper J18 is positioned to B, the back-up battery is enabled. When it is positioned to A, the battery is disabled. *The XVME-630 is shipped from the factory with J18 positioned to A.* However, J18 should be set to B to allow the real time clock to be updated and dual-ported SRAM data (if desired) to be retained upon power-down.

2.3.2 Bus Grant and Bus Request Level Selection Jumpers (J7,J15, J16)

Jumpers J7, J15, and J16 are used to select the bus request and bus grant levels as shown below:

Jumpers J7, J15, and J16	VMEbus Master Bus Request Level	BGIN to BGOUT Jumpers (Outside Posts Only)
A	0	J7B-J15B, J7C-J15C, J7D-J15D
B	1	J7A-J15A, J7C-J15C, J7D-J15D
C	2	J7A-J15A, J7B-J15B, J7D-J15D
D	3	J7A-J15A, J7B-J15B, J7C-J15C

For example, to select VMEbus master request level 3, you would set jumpers J7, J15 and J16 to D, and then connect J7A to J15A, J7B to J15B, and J7C to J15C. Refer to Figure 2-2 on the following page for an example of positioning the BGIN to BGOUT jumpers.

NOTE

J7, J15, and J16 **must** all be in the same position. Refer to the drawing on the next page for an example.

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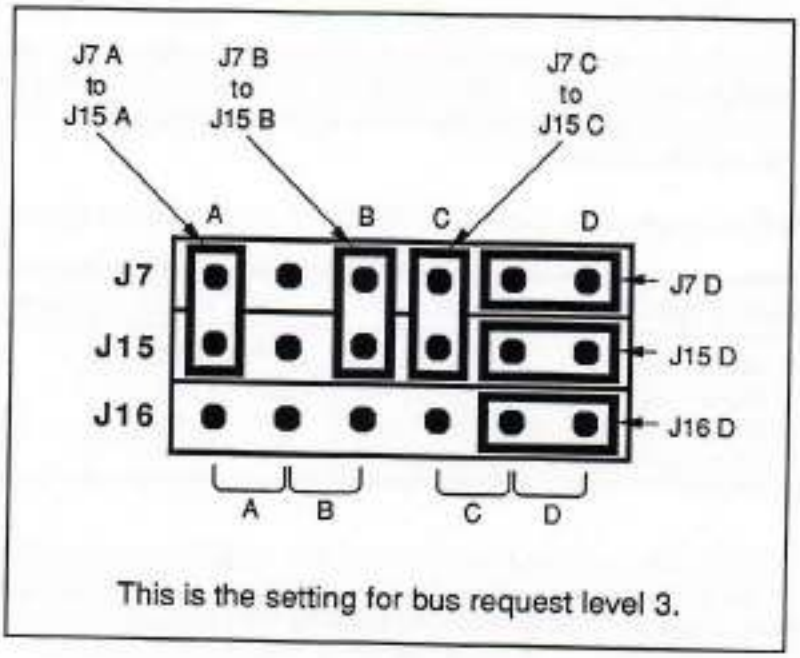


Figure 2-2. Positioning the BGIN to BGOUT Jumpers

2.3.3 Cache (J11)

When jumper J11 is IN, caching is disabled. When J11 is OUT, caching is enabled.

For more information on caching, see section 3.3.

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2.3.4 Dual Ported Memory (J5, J8, JA22-JA31)

Dual ported memory on the XVME-630 allows other bus masters in the system to access local memory on the XVME-630. The VMEbus slave interface on the XVME-630 controls access to its memory. Jumpers J5, J8, and JA21 to JA31 allow you to configure the slave interface to respond to various addresses and address modifier codes.

Jumper J5 indicates whether the slave will respond to non-privileged accesses. When J5 is installed, Bank 3 responds to both supervisory and non-privileged accesses; when J5 is removed, Bank 3 responds to supervisory accesses only.

Jumper J8 controls whether dual ported memory (Bank 3) is addressable through the VMEbus Standard or Extended address space. When J8 is IN, dual ported memory is addressable in the VMEbus Standard address space. When J8 is OUT, dual ported memory is addressable in the VMEbus Extended address space.

The address modifiers associated with the settings of J5 and J8 are shown below:

VMEbus Data Transfer Type	J5	J8	Address Modifier
Extended, Supervisory	OUT	OUT	0DH
Standard, Supervisory	OUT	IN	3DH
Extended, Non-privileged or Supervisory	IN	OUT	09H or 0D
Standard, Non-privileged or Supervisory	IN	IN	39H or 3D

Jumpers JA22 to JA31 select a Standard or Extended VMEbus slave address at which Bank 3 will reside (in=0, out=1). Jumpers JA31-JA22 correspond to VMEbus address lines A31-A22 respectively. When a jumper is installed, the address bit broadcast by the master is compared to a 0. If the jumper is removed, the address bit is compared to a 1.

The bits which are compared depend on the setting of jumper J8:

- When J8 is set to respond to VMEbus Extended address space, address lines A31-A22 are compared.
- When J8 is set to respond to VMEbus Standard address space, only address lines A23-A22 are compared (A31-A24 are ignored).

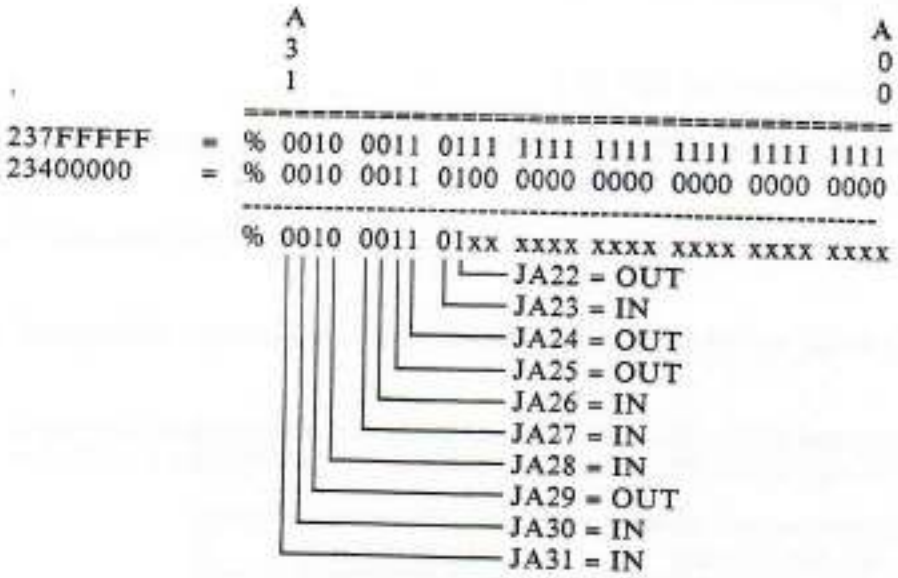
The examples on the following page show how to use the JA jumpers.

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Example 1

VMEbus supervisor at Extended address 23400000-237FFFFF

J8 = OUT (VMEbus Extended address space)

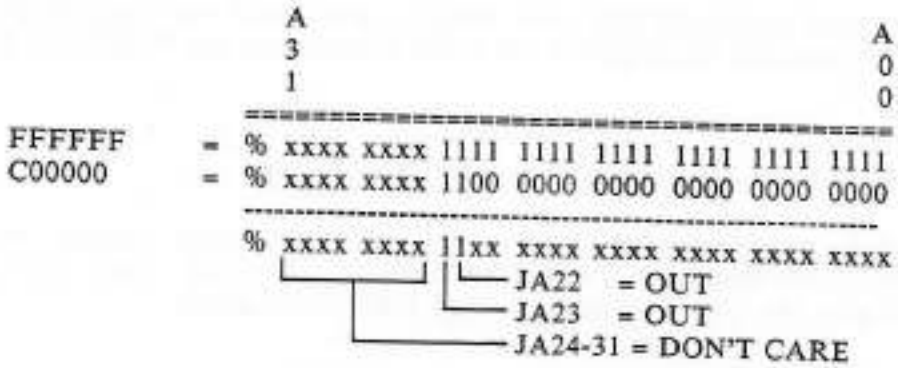


J5 = OUT ; Supervisory only

Example 2

VMEbus non-privileged at Standard address C00000-FFFFFF

J8 = IN (VMEbus Standard address space)



J5 = IN (Supervisory or non-privileged)

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2.3.5 Oscillator Power (J17)

Jumper J17 determines whether oscillator power is applied to the XVME-630. When J17 is IN, oscillator power is supplied. When J17 is removed, oscillator power is not supplied.

J17 should be IN for normal operation.

2.3.6 Serial Port Selection (J32-J42 and J47-J57)

Serial channel A is configured as RS-232C. Serial channel B can be jumper-configured to RS-232C or RS-485.

When jumpers J32 to J42 *and* J47 to J57 are positioned to A, serial channel B is configured as RS-232C.

When jumpers J32 to J42 *and* J47 to J57 are positioned to B, serial channel B is configured as RS-485.

When serial channel B is configured for RS-485 operation, the tri-stating of the RS-485 drivers is controlled by two DUSCC outputs, GPO2A (bit 2 in OMRA) and GPO2B (bit 2 in OMRB).

RS-485 Signals		Output Control	
TXD, RTS	Low impedance	OMRB bit 2	= 0
	High impedance		= 1
TRXC, DTR	Low impedance	OMRA bit 2	= 0
	High impedance		= 1

The GPO2A and GPO2B pins must first be configured as general purpose outputs by writing a 0 to bit 6 of PCRA and PCRB.

OMRA bit 2 controls the state of the pin GP02A on the DUSCC, and OMRB bit 2 controls the state of the pin GP02B. For example, when OMRA bit 2 is 0, GP02A sets the DUSCC TXD, RTS as low impedance.

2.3.7 SRAM/EPROM (J12-J14, J19-J23, J24, J30, J43-J46, J59, J62-63)

The XVME-630 contains three memory banks, consisting of four sockets each. Jumpers are used to configure the size of the devices and speed for each of the banks. Bank 3 uses additional jumpers to configure the type of devices: SRAM, EPROM, or Flash.

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2.3.7.1 SRAM/EPROM Type Selection (J19-J23, J30, J43-J46, J59, J62-63)

Bank 1 - SRAM
Bank 1 (which consists of sockets U74-U77) is dedicated for use with SRAM devices, and can accept up to 2 Mbytes. Jumpers J21, J22, and J23 must be set to specify whether 28-pin or 32-pin SRAMs are used. The SRAMs used must all be the same type.

If you are using a 28-pin SRAM, insert jumpers J21 and J23, and remove jumper J22. If you are using 32-pin SRAMs, insert J22 and remove J21 and J23.

	J21	J22	J23
28-pin SRAM	IN	OUT	IN
32-pin SRAM	OUT	IN	OUT

Bank 2 - EPROM
Bank 2 (sockets U70-U73) is dedicated for use with EPROM devices, and can accept 27C010, 27C020, 27C040, or 27C080 EPROMs. The EPROMs installed must all be the same type.

Jumpers J19 and J20 are used to select the type of EPROM installed in Bank 2. The table below shows the jumpers settings for the various EPROM possibilities.

J19	J20	Device Selected
A	OUT	27C010
A	OUT	27C020
A	IN	27C040
B	IN	27C080

Bank 3 - Dual Ported
Memory bank 3 (sockets U100-U103) can accept 27C010, 27C020, 27C040, or 27C080 EPROM devices, RAM devices, or Flash devices.

> **NOTE**
> Memory bank 3 (sockets U100 (byte 0) to U103 (byte 3)) must contain the same type of devices (i.e. all EPROM, all SRAM, or all Flash), with each chip identical in memory size.)

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The type and size of the devices located in memory bank 3 is selected via jumpers J30, J43-J46, J59, and J61-63. The table below lists the jumper settings for the various devices that can be installed in these locations.

DUAL-PORTED MEMORY DEVICE TYPE	J63	J61	J59	J46	J62	J45,J44 J43,J30
SRAM (Battery & Non-battery Backed)						
4x[64kx8]	B	A	OUT	A	B	A,C
4x[128kx8]	B	A	OUT	A	B	A,C
4x[256kx8]	B	A	IN	A	B	A,C
4x[512kx8]	B	A	IN	A	B	A,C
EPROM						
27C010 4x[128kx8]	A	C	OUT	B	OUT	A,D
27C020 4x[256kx8]	A	C	IN	B	OUT	A,D
27C040 4x[512kx8]	A	C	IN	B	A	A,D
27C080 4x[1mx8]	A	B	IN	B	A	A,D
Flash						
4x[32kx8]	A	D	OUT	B	OUT	B,D
4x[64kx8]	A	D	OUT	B	OUT	B,D
4x[128kx8]	A	D	OUT	B	OUT	B,D
4x[256kx8]	A	D	IN	B	OUT	B,D

Refer to section 2.5 for information on installing the chips.

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2.3.7.2 SRAM/EPROM Wait State Selection (J12-J14, J24-26)

> **NOTE**
> The timing parameters of the memory devices must be correlated with the number of wait states chosen. The tables and figures starting on page B-10 of the Quick Reference Guide show the timing parameter requirements for all three banks as a function of wait states. All parameters must be satisfied to guarantee proper operation.

Bank 1 - SRAM

Jumper J24 determines the number of wait states associated with SRAM chip reads and writes. When J24 is positioned to A, 1 wait state local SRAM reads and writes will be performed. When J24 is positioned to B, 0 wait state reads and 1 wait state writes will be performed.

J24	Number of Wait States
A	1 wait state reads/writes
B	0 wait state reads, 1 wait state writes

Bank 2 - EPROM

Jumpers J25 and J26 determine the number of wait states associated with local EPROM chip reads as shown in the table below:

J25	J26	Number of Wait State Reads
IN	IN	1
IN	OUT	2
OUT	IN	3
OUT	OUT	4

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Bank 3 - Dual Ported

Bank 3 can accommodate SRAM, EPROM, or Flash memory devices. Jumpers J12 through J14 determine the number of wait states associated with the dual ported memory as shown below:

J12	J13	J14	Number of Wait States
OUT	OUT	OUT	8
OUT	OUT	IN	2
OUT	IN	OUT	3
OUT	IN	IN	4
IN	OUT	OUT	5
IN	OUT	IN	6
IN	IN	OUT	7
IN	IN	IN	8

NOTE

The timing parameters of the memory devices must be correlated with the number of wait states chosen. The tables and figures starting on page B-10 of the Quick Reference Guide show the timing parameter requirements for all three banks as a function of wait states. All parameters must be satisfied to guarantee proper operation.

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2.3.8 SYSRESET (J28, J29, J58, J60)

A reset to the XVME-630 is always generated by the power monitor circuit, after a power outage.

J28 enables and disables the reset push button on the XVME-630 front panel. When J28 is IN, the reset button will reset the XVME-630 board. When J28 is out, the push button is disabled from resetting the XVME-630.

J29 enables or disables the push button from generating a VMEbus reset. When J29 is IN and the XVME-630 is set to generate a VMEbus SYSRESET* (see J60 below), the reset button will generate a VMEbus reset. When J29 is OUT, the reset button will not generate a VMEbus reset.

J58 determines whether other boards in the VMEbus backplane can reset the XVME-630. When J58 is IN, the XVME-630 is reset by a VMEbus SYSRESET*. When J58 is out, the XVME-630 is not reset by a VMEbus SYSRESET*.

J60 determines whether the XVME-630 circuitry can generate a VMEbus SYSRESET*. When J60 is IN, the XVME-630 can generate the SYSRESET*; when J60 is OUT, the XVME-630 cannot generate the SYSRESET*.

The table below shows how to position these four jumpers for the various options:

J28	J29	J58	J60	Reset button resets		On-board circuitry reset by	Power monitor resets		Reset instruc. generates SYSRESET*
				O-B Cir.	VMEbus		O-B Cir.	VMEbus	
OUT	OUT	OUT	OUT						
OUT	OUT	OUT	IN				✓		
OUT	OUT	IN	OUT				✓	✓	✓
OUT	OUT	IN	IN			✓	✓		
OUT	IN	OUT	OUT			✓	✓	✓	✓
OUT	IN	OUT	IN				✓		
OUT	IN	IN	OUT		✓	✓	✓	✓	✓
OUT	IN	IN	IN			✓	✓		
IN	OUT	OUT	OUT		✓		✓	✓	✓
IN	OUT	OUT	IN	✓		✓	✓		
IN	OUT	IN	OUT	✓		✓	✓	✓	✓
IN	OUT	IN	IN	✓			✓		
IN	IN	OUT	OUT	✓		✓	✓	✓	✓
IN	IN	OUT	IN	✓		✓	✓		
IN	IN	IN	OUT	✓	✓		✓	✓	✓
IN	IN	IN	IN	✓		✓	✓		
				✓	✓	✓	✓	✓	✓

✓ = yes, blank = no

O-B Cir. = On-Board Circuitry

For example, if you want the XVME-630 reset button to reset the XVME-630 and the VMEbus backplane, and the XVME-630 board to be able to generate SYSRESETs, but not be affected by them, position the following jumpers: J28 in, J29 in, J60 in, J58 out.

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2.3.9 System Resource Functions (J1, J2, J3)

The system resource functions provide the following, as defined in the VMEbus specification: SYSCLK driver, bus timer, SGL bus arbiter, and IACK daisy chain driver. The IACK daisy chain driver is always operational and therefore not jumperable. The other functions are described below.

Bus Timer (J1)
Installing jumper J1 enables the VMEbus timer on the XVME-630, and removing J1 disables the timer. When the bus timer is enabled, the XVME-630 drives the BERR* signal to the system whenever a bus cycle is not completed within the timeout period. This allows the current bus master to terminate its bus cycle and prevent a "locked" condition on the VMEbus. The timeout period depends on the XVME-630 board speed as shown below:

Board Speed	BERR* will not be asserted before	Typical Timeout	BERR* will be asserted after
25 MHz	40.32 uS	40.96 uS	41.60 uS
40 Mhz	25.20 uS	25.60 uS	26.00 uS

SYSCLK Driver (J2)
When J2 is IN, it enables the XVME-630 to drive the SYSCLK signal on the VMEbus backplane. When J2 is OUT, it disables the SYSCLK driver.

Single Level Arbiter (J3)
The single level arbiter (VMEbus bus request level 3) is enabled by installing jumper J3, and disabled by removing J3. With the XVME-630 arbiter enabled, no VMEbus master should be configured to request the VMEbus at VMEbus bus request levels 0, 1, or 2.

2.3.10 User-Configurable (J27, J31)

The DUSCC provides two user-definable, software-readable configuration jumpers, J27 and J31. These jumpers are connected to the GPI1A and GPI2A pins, whose state can be read at bits 0 and 1 of the DUSCC's ICTSRA register. These jumpers are independent of any hardware function and can be defined for any software configuration function.

DUSCC Register Bit Location	J31		J27	
	Out	In	Out	In
ICTSRA bit 0	1	0		
ICTSRA bit 1			1	0

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2.3.11 VMEbus Interrupt Level Selection Jumpers (J6A-J6G)

The XVME-630 module recognizes all seven VMEbus interrupts. When jumpers within J6 are installed, the interrupt handler handles the specified IRQs. When jumpers within J6 are removed, interrupts are not handled. The table below shows how the settings of jumper J6 correspond to the interrupt levels:

Jumper J6 Position	VMEbus Interrupt Level
A	IRQ7*
B	IRQ6*
C	IRQ5*
D	IRQ4*
E	IRQ3*
F	IRQ2*
G	IRQ1*
OUT	Disabled

Local sources can also interrupt the CPU (refer to section 3.6 of this manual for more information).

2.3.12 VMEbus Release on Request (J9)

If J9 is IN, the XVME-630 will release the VMEbus on any request (ROR). If J9 is OUT, the XVME-630 will not release on request.

2.3.13 VMEbus SYSFAIL Driver (J4)

When the FAIL LED is lit (as controlled by bit 0 of control register 1 (address 0800000H; see section 3.5.2), the XVME-630 will assert SYSFAIL* on the VMEbus if jumper J4 is IN. If J4 is OUT, the XVME-630 cannot assert the SYSFAIL* signal.

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2.4 CONNECTORS

The following sections list the signals passed by the ports and connectors on the XVME-630 module.

2.4.1 VMEbus P1 Connector

Table 2-2. P1 Pinouts

Pin #	Row A Signal	Row B Signal	Row C Signal
1	D0	BBSY*	D8
2	D01	BCLR*	D9
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

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2.4.2 VMEbus P2 Connector

Table 2-3. P2 Pinouts

Pin #	Rows A and C Signal	Row B Signal
1	User-defined	+5V
2	User-defined	GND
3	User-defined	N/C
4	User-defined	A24
5	User-defined	A25
6	User-defined	A26
7	User-defined	A27
8	User-defined	A28
9	User-defined	A29
10	User-defined	A30
11	User-defined	A31
12	User-defined	GND
13	User-defined	+5V
14	User-defined	D16
15	User-defined	D17
16	User-defined	D18
17	User-defined	D19
18	User-defined	D20
19	User-defined	D21
20	User-defined	D22
21	User-defined	D23
22	User-defined	GND
23	User-defined	D24
24	User-defined	D25
25	User-defined	D26
26	User-defined	D27
27	User-defined	D28
28	User-defined	D29
29	User-defined	D30
30	User-defined	D31
31	User-defined	GND
32	User-defined	+5V

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2.4.3 JK1 Connector

The XVME-630 Processor Module provides two asynchronous serial channels (A and B). Both channels are configured as "DCE" equipment. Channel A is configured for RS-232C, while channel B can be jumper-configured as RS-232C or RS-485 (see section 2.3.6 for jumper settings).

Both channels have transmit (TxD) and receive (RxD) lines, as well as modem control inputs (RTS and DTR) and modem control outputs (CTS and DCD). Both RS-232C and RS-485 signals are accessible via a 50-pin connector (JK1) located on the module front panel. Figure 2-3 shows the module front panel and how the pins are situated in the connector.



Figure 2-3. Connector JK1

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Table 2-4 shows the pin designations for channel A of the JK1 connector, while Table 2-5 on the following page shows the pin designations for channel B of JK1.

Table 2-4. JK1 Channel A Pinouts

PIN	RS-232C SIGNAL	Mass Terminated 25-Pin Connector
1	N/C	Pin 1
2	N/C	Pin 14
3	RXDA	Pin 2
4	N/C	Pin 15
5	TXDA	Pin 3
6	N/C	Pin 16
7	CTSA	Pin 4
8	TRXCA	Pin 17
9	RTSA	Pin 5
10	N/C	Pin 18
11	N/C	Pin 6
12	N/C	Pin 19
13	GND	Pin 7
14	DCDA	Pin 20
15	DTRA(GPO1A)	Pin 8
16	N/C	Pin 21
17	N/C	Pin 9
18	N/C	Pin 22
19	N/C	Pin 10
20	N/C	Pin 23
21	N/C	Pin 11
22	RTXCA	Pin 24
23	N/C	Pin 12
24	N/C	Pin 25
25	N/C	Pin 13

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Table 2-5. JK1 Channel B Signals

PIN	RS-232C SIGNAL	Mass Terminated 25-Pin Connector	RS-485 SIGNAL
26	N/C	Pin 1	+5V
27	N/C	Pin 14	TXDB+
28	RXDB	Pin 2	RTSB-
29	N/C	Pin 15	RTSB+
30	TXDB	Pin 3	TXDB-
31	N/C	Pin 16	TRXCB+
32	CTSB	Pin 4	DTRB-(GPO1B)
33	TRXCB	Pin 17	CTSB+
34	RTSB	Pin 5	TRXCB-
35	N/C	Pin 18	GND
36	N/C	Pin 6	DCDB-
37	N/C	Pin 19	DCDB+
38	GND	Pin 7	GND
39	DCDB	Pin 20	RXDB+
40	DTRB(GPO1B)	Pin 8	RXDB-
41	N/C	Pin 21	RTXCB-
42	N/C	Pin 9	N/C
43	N/C	Pin 22	RTXCB+
44	N/C	Pin 10	CTSB-
45	N/C	Pin 23	N/C
46	N/C	Pin 11	N/C
47	RTXCB	Pin 24	DTRB+(GPO1B)
48	N/C	Pin 12	N/C
49	N/C	Pin 25	N/C
50	N/C	Pin 13	N/C

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2.5 INSTALLING MEMORY CHIPS ON THE XVME-630 PROCESSOR MODULE

The XVME-630 has 12 32-pin sockets intended for use by SRAM, EPROM, or Flash devices. The table below shows which banks are used for which kinds of memory, which sockets comprise each bank, and other memory information.

Table 2-6. Memory Capacity

	BANK 1 Local SRAM	BANK 2 Local EPROM	BANK 3 Dual-Ported
Memory Type	SRAM	EPROM	SRAM, EPROM, or Flash
Sockets Used	U74 (byte 0) to U77 (byte 3)	U70 (byte 0) to U73 (byte 3)	U100 (byte 0) to U103 (byte 3)
Maximum Memory	2 Mbytes	4 Mbytes	SRAM: 2 Mbytes EPROM: 4 Mbytes Flash: 1 Mbyte
Memory Chip Sizes	32Kx8 to 512Kx8	128Kx8 to 1Mx8	SRAM: 64Kx8 to 512Kx8 EPROM: 128Kx8 to 1Mx8 Flash: 32Kx8 to 245Kx8
Wait State Options	0, 1	1 to 4	2 to 8
Timing Parameters	See Appendix B	See Appendix B	See Appendix B
DIP Part Width (JEDEC Pinout Compatible)	.3", .4", .6"	.6"	.6"

NOTE

All memory will be shadowed throughout the 64 Mbyte address space for banks 1 through 3. For example, if four 128Kx8 EPROMs are installed in Bank 2, they only occupy 512 Kbytes of the 64 Mbyte space mapped out for them. Thus, the 512 Kbytes are shadowed 128 times throughout the 64 Mbyte EPROM map.

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Installing memory chips involves the following steps:

1. Set the jumpers to match the devices you selected according to the tables in section 2.3.7.1 and Table 2-6 on the previous page.

2. Set the appropriate jumpers to select the desired wait states as described in section 2.3.7.2.

2. Install the appropriate devices into the appropriate sockets (see Table 2-6), referencing the notched ends of the chips as shown in Figure 2-4.

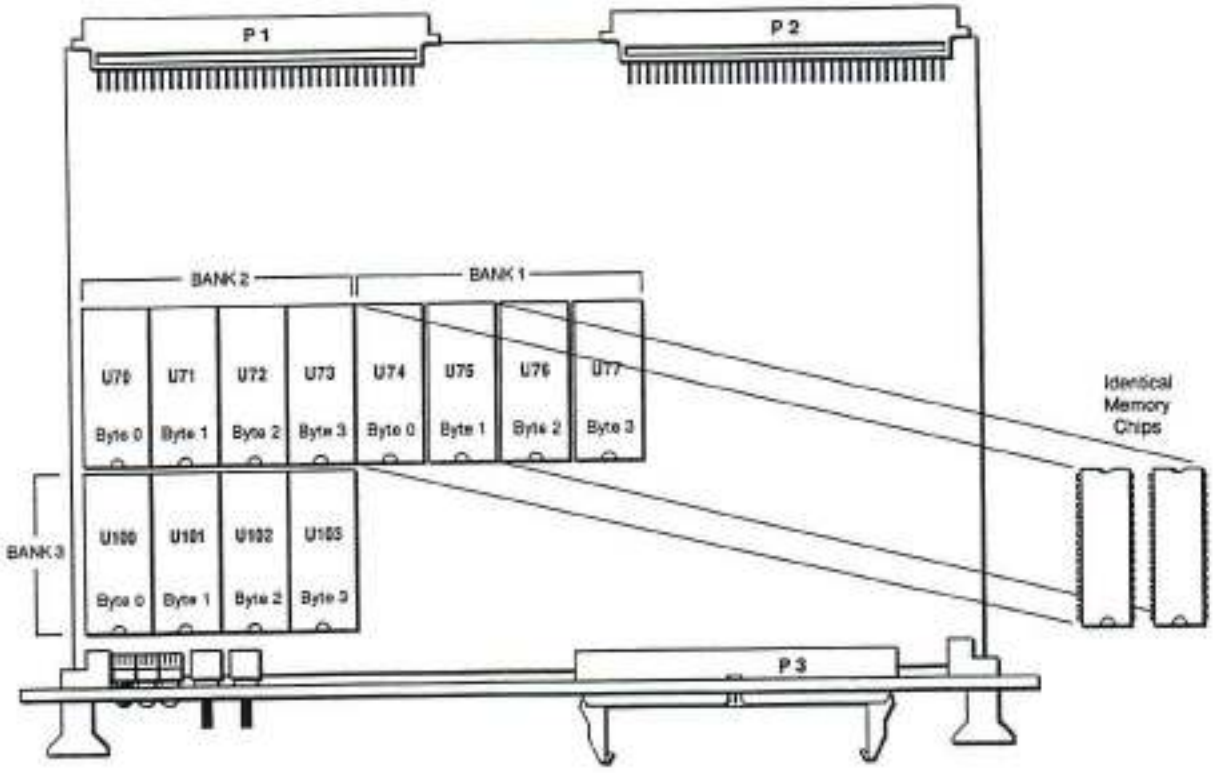


Figure 2-4. Installing Memory Chips

CAUTION

Use an extraction tool to remove any memory chips. Using a screwdriver could damage the board.

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2.6 INSTALLING THE XVME-630

All Xycom XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-630 Processor Module is a double-high VMEbus module, and as such requires both P1 and P2 backplanes.

> **WARNING**
> Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.
>
> **CAUTION**
> Before installing a module, determine and verify all jumper settings and all connections to external devices or power supplies. (Check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the cardcage, perform the following steps:

1. Make sure that the cardcage slot you want to use is clear and accessible.
2. Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage.
3. Slowly push the card toward the rear of the chassis until the connectors engage (the card should slide freely in the plastic guides).
4. Apply straight-forward pressure to the handle located on the front panel of the module until the connector is fully engaged and properly seated.

> **NOTE**
> It should not be necessary to use excessive pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5. Once the board is properly seated, secure it to the chassis by tightening the two machine screws at the top and bottom of the board.

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2.7 INSTALLING AN OPTIONAL MATH CO-PROCESSOR

U66 on the XVME-630 board is a 68-pin PGA socket which accepts a Motorola MC68882 math co-processor chip. This co-processor must be rated at the same speed as the 68EC030. The co-processor will respond to all floating-point instructions without regard to its co-processor ID.

To install the co-processor, simply:

1. Locate socket U66 on the XVME-630.

2. Make sure pins 1 line up and insert the co-processor chip into the socket U66 as shown below.

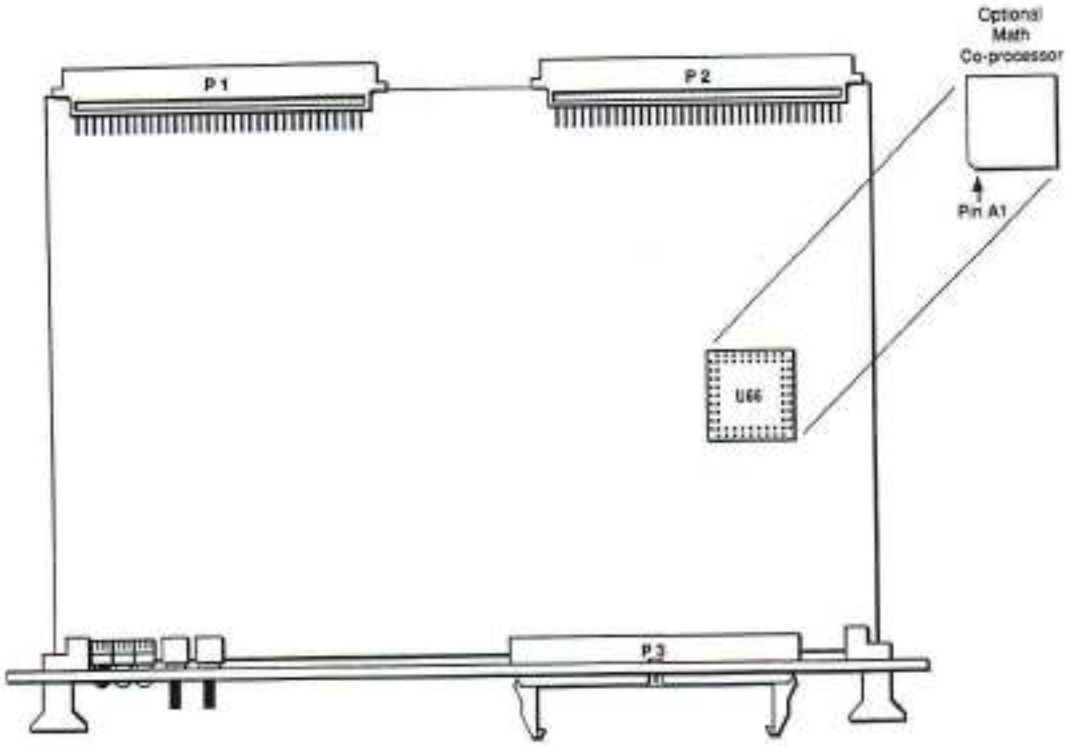


Figure 2-5. Installing an Optional Math Co-Processor

CAUTION

Use an extraction tool to remove the math co-processor chip. Using a screwdriver could damage the board.

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3.1 INTRODUCTION

This chapter provides information needed to program the XVME-630 module. This information is presented as follows:

- Module memory map
- Caching
- DUSCC software accesses
- I/O port addresses, registers, and descriptions
- Interrupts
- Read/modify/write capabilities of dual-ported memory
- Real time clock
- Software notes

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3.2 THE XVME-630 PROCESSOR MODULE MEMORY MAP

Figure 3-1 shows the XVME-630 Module memory map as seen by the 68EC030.

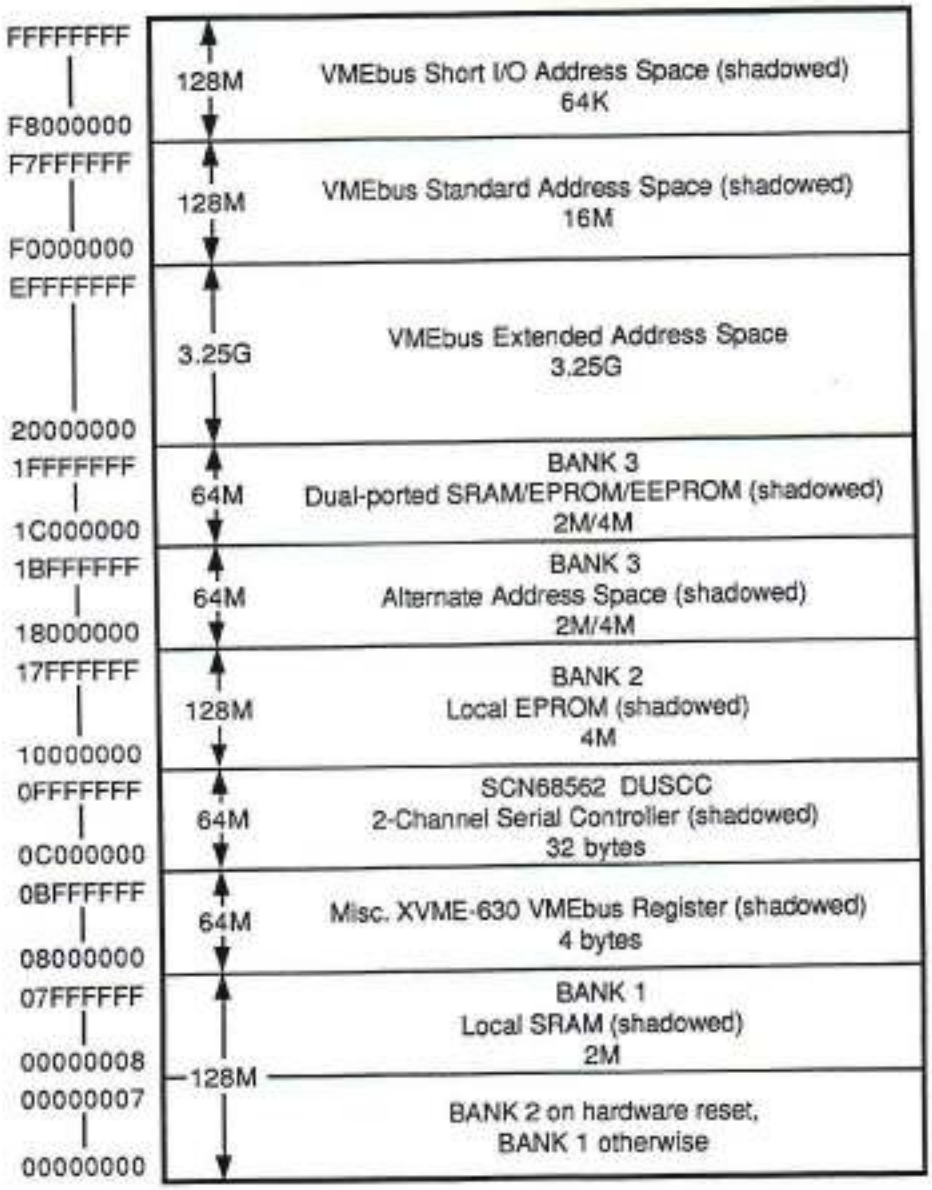


Figure 3-1. XVME-630 Processor Module Memory Map

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3.2.1 Bank 1 Local SRAM

Bank 1 is accessed through synchronous 68EC030 cycles (asserting STERM*), and is not battery-backed. Byte, word, and longword data accesses and instruction fetches to this memory space are accessed as longwords.

Bank 1 sits directly on the 68EC030's address and data bus to minimize memory access time. This allows the 68EC030 to read these SRAMs in two clocks (0 wait states) and write them in three clocks (1 wait state).

Bank 1 accepts four SRAMs in sizes of 32Kx8 to 512Kx8. A custom pin arrangement (four rows of pins) is used in this bank to allow interchanging fast monolithic SRAMs with .300, .400, and .600 centers. Refer to section 2.3.7 for more information.

3.2.2 Bank 2 Local EPROM

Bank 2 is accessed through synchronous 68EC030 cycles (asserting STERM*). This bank is mapped into low memory (over Bank 1) upon the 68EC030's reset to allow the EPROM to supply the initial program counter (PC) and stack pointer (SP). The vector in this EPROM containing the initial PC must jump to an address where address bit A28=1 (i.e. Bank 2, EPROM). (This is necessary to enable Bank 1.) Bank 2 is taken out of the initial overlay of Bank 1 when A28 goes high after reset.

Byte, word, and longword data accesses, and instruction accesses to this memory space are accessed as longwords. This bank of memory sits directly on the 68EC030's address bus, but is buffered from the CPU's data bus to allow faster EPROM accesses and slower EPROM device turnoff times.

Bank 2 can accept four EPROMs in sizes of 128Kx8 (27C010) to 1Mx8 (27C080). See section 2.3.7 for information on setting the jumpers to correspond to the type of EPROM and the number of wait states (1 to 4).

3.2.3 Bank 3 Dual Ported

Bank 3 is accessed through synchronous 68EC030 cycles (asserting STERM*). Bank 3 may **not** be accessed by the 68EC030 through the VMEbus (using both the master and slave interfaces), but through the specific dual-ported block in the local memory map.

This bank is accessible as a 4 Mbyte block of 32 bit-wide memory as a slave in the VMEbus. The address of this memory is selectable on 4 Mbyte boundaries in the VMEbus Extended or Standard address space.

Bank 3 is buffered from the local 68EC030 bus to allow the 68EC030 to operate on the local bus while another master on the VMEbus does a slave access to Bank 3. Accesses to this bank are slower than accesses to the other banks because of the dual-ported arbitration and support of slower memory types.

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This bank can accept four SRAMs (64Kx8 to 512Kx8), four EPROMs (128Kx8 (27C010) to 1Mx8 (27C080)), or four Flash devices (64Kx8 to 256Kx8). (Refer to section 2.3.7.1 to set the jumpers to select the memory speed of the device.) If SRAM is installed in Bank 3, it may be made non-volatile by the on-board battery or VMEbus +5VSTANDBY.

3.2.4 VMEbus Standard Address Space

Any 68EC030 memory references to bytes in the range F0000000H-F7FFFFFFH will map into the VMEbus Standard address space. The 68EC030's lower 24-bit address bus is mapped directly onto the lower 24-bit VMEbus address bus.

3.2.5 VMEbus Extended Address Space

Any 68EC030 memory references to bytes in the range 20000000H-EFFFFFFFH will map into the VMEbus Extended address space. The 68EC030's entire 32-bit address bus is mapped directly onto the 32-bit VMEbus address bus.

> **NOTE**
> VMEbus Extended memory addresses 00000000H-1FFFFFFH and F0000000-FFFFFFFF are not accessible.

3.2.6 VMEbus Short I/O Address Space

Any 68EC030 references to bytes in address space F8000000H-FFFFFFFFH will reference the VMEbus Short I/O address space. The lower 16 bits of the 68EC030's address bus will be used to select a byte in the 64 Kbyte Short I/O space.

3.2.7 DUSCC Serial Controller

Any 68EC030 memory references to bytes in the range 0C000000H-0FFFFFFFH will reference the SCN68562 Dual Universal Serial Communications Controller (DUSCC).

Section 3.4 provides more information about the DUSCC.

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3.3 CACHING

The 68EC030 processor contains a 256 byte instruction cache and a 256 byte data cache. These caches are each organized as 64 longword entries. Any time the CPU is allowed to cache a data fetch, the 68EC030 will fetch the additional data required to complete the cache entry. Along with the cache disable bits in the control/status registers, the caches may be ultimately disabled by control bits within the 68EC030 and by installing jumper J11.

For more information on the control and status registers, refer to section 3.5.

3.3.1 Instruction Cache

The 68EC030 can cache instruction fetches from any location in local SRAM (Bank 1), local EPROM (Bank 2), dual-ported memory (Bank 3), and VMEbus Standard and Extended address spaces. Unaligned instruction fetches and cache filling may cause the 68EC030 to execute additional memory cycles.

Local SRAM, Local EPROM, and Dual-ported SRAM/EPROM (Banks 1, 2, & 3): Instruction fetches from these banks are always performed in 32-bit longwords and are cached.

VMEbus Extended Memory: Instruction fetches from this area are performed according to bit 5 of control register 3 and the specified address. Instructions with the aforementioned bit set to 0 yield word accesses, while setting this bit to 1 results in longword accesses. Bit 4 of control register 1 determines whether the instruction fetch is cached. If this bit is set to 1, the instruction is cached; if the bit is 0, the instruction is not cached.

VMEbus Standard Memory: Instruction fetches from this area are performed according to bit 5 of control register 3 and the specified address. Instructions with bit 5 set to 0 yield word accesses, while setting this bit to 1 results in longword accesses. Bit 3 of control register 1 controls whether the instruction fetch is cached. If this bit is set to 1, the instruction is cached; if this bit is 0, the instruction is not cached.

VMEbus Short I/O: Instruction fetches from this area are not allowed and will result in VMEbus cycles with illegal address modifiers.

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3.3.2 Data Cache

The 68EC030 can cache data from local SRAM (Bank 1), local EPROM (Bank 2), dual-ported memory (Bank 3), and the VMEbus Standard and Extended address spaces. Unaligned data accesses and cache filling may cause the 68EC030 to execute additional memory cycles. Some unaligned accesses cannot be cached.

Local SRAM and Local EPROM (Banks 1 & 2): Data fetches from these banks consist of 32-bit longwords and are cached.

Dual-ported SRAM/EPROM/EEPROM (Bank 3): Data fetches from this bank consist of 32-bit longwords. Bit 2 of control register 1 determines whether the data fetch is cached. If this bit is 1, the data is cached; if this bit is 0, the data is not cached.

VMEbus Extended Memory: Data is fetched from this area according to the data width specified by the programmer (i.e. MOVE.L, MOVE.W, MOVE.B). Bit 4 of control register 1 determines whether the data fetch is cached. If this bit is 1, the data is cached; if this bit is 0, the data is cached. Byte reads from this area are never cached.

VMEbus Standard Memory: Data is fetched from this area according to the data width specified by the programmer (i.e. MOVE.L, MOVE.W, MOVE.B). Bit 3 of control/status register 1 determines whether the data fetch is cached. If this bit is 1, the data is cached; if this bit is 0, the data is not cached. Byte reads from this area are never cached.

VMEbus Short I/O: Data is fetched from this area according to the data width specified by the programmer (i.e. MOVE.L, MOVE.W, MOVE.B). Data accesses to this area are never cached.

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3.4 SOFTWARE ACCESSES TO THE DUSCC

Software must ensure that accesses to the DUSCC are at least 160 nS apart (CS* high). This delay requirement can be satisfied worst case (40 MHz, instruction cache enabled) by executing the following empty subroutine before each DUSCC access:

MAIN PROGRAM

```
RD_DUSCC
   BSR      DUSCC_DELAY
   MOVE.B   DUSCC,D1
   BSR      DUSCC_DELAY
   MOVE.B   DUSCC+1,D2
```

DELAY ROUTINE

```
DUSCC_DELAY
   RTS
```

Two user-definable, software-readable jumpers (J31 and J27) are accessible through the DUSCC. These jumpers are connected to the GPI1A and GPI2A pins, whose state can be read at bit 0 and bit 1 of the DUSCC's ICTSRA. These jumpers are independent of any hardware function and can be defined for any software configuration function.

DUSCC Register Bit Location	J31		J27	
	Out	In	Out	In
ICTSRA bit 0	1	0		
ICTSRA bit 1			1	0

The DUSCC addresses and the associated registers are shown on the following pages for reference. For more information on the DUSCC, refer to the Signetics 68562 DUSCC Controller User Manual.

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ADDRESS(HEX)	DUSCC REGISTER	
0C000000	CMR1A	- Channel mode register 1, channel A
0C000001	CMR2A	- Channel mode register 2, channel A
0C000002	S1RA	- Syn 1/secondary address 1 register, channel A
0C000003	S2RA	- Syn 2/secondary address 2 register, channel A
0C000004	TPRA	- Transmitter parameter register, channel A
0C000005	TTRA	- Transmitter timing register, channel A
0C000006	RPRA	- Receiver parameter register, channel A
0C000007	RTRA	- Receiver timing register, channel A
0C000008	CTPRHA	- Counter/timer preset register high, channel A
0C000009	CTPRLA	- Counter/timer preset register low, channel A
0C00000A	CTCRA	- Counter/timer control register, channel A
0C00000B	OMRA	- Output and miscellaneous register, channel A
0C00000C	CTHA	- Counter/timer high, channel A
0C00000D	CTLA	- Counter/timer low, channel A
0C00000E	PCRA	- Pin configuration register, channel A
0C00000F	CCRA	- Channel command register, channel A
0C000010	TXFIFOA	- Transmitter FIFO, channel A
0C000011	TXFIFOA	- Transmitter FIFO, channel A (alternate address)
0C000012	TXFIFOA	- Transmitter FIFO, channel A (alternate address)
0C000013	TXFIFOA	- Transmitter FIFO, channel A (alternate address)
0C000014	RXFIFOA	- Receiver FIFO, channel A
0C000015	RXFIFOA	- Receiver FIFO, channel A (alternate address)
0C000016	RXFIFOA	- Receiver FIFO, channel A (alternate address)
0C000017	RXFIFOA	- Receiver FIFO, channel A (alternate address)
0C000018	RSRA	- Receiver status register, channel A
0C000019	TRSRA	- Transmitter and receiver status register, channel A
0C00001A	ICTSRA	- Input and counter/timer status register, channel A
0C00001B	GSR	- General status register
0C00001C	IERA	- Interrupt enable register, channel A
0C00001E	IVR	- Interrupt vector register, unmodified
0C00001F	ICR	- Interrupt control register

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ADDRESS(HEX)	DUSCC REGISTER	
0C000020	CMR1B	- Channel mode register 1, channel B
0C000021	CMR1B	- Channel mode register 2, channel B
0C000022	S1RB	- Syn 1/secondary address 1 register, channel B
0C000023	S2RB	- Syn 2/secondary address 2 register, channel B
0C000024	TPRB	- Transmitter parameter register, channel B
0C000025	TTRB	- Transmitter timing register, channel B
0C000026	RPRB	- Receiver parameter register, channel B
0C000027	RTRB	- Receiver timing register, channel B
0C000028	CTPRHB	- Counter/timer preset register high, channel B
0C000029	CTPRLB	- Counter/timer preset register low, channel B
0C00002A	CTCRB	- Counter/timer control register, channel B
0C00002B	OMRB	- Output and miscellaneous register, channel B
0C00002C	CTHB	- Counter/timer high, channel B
0C00002D	CTLB	- Counter/timer low, channel B
0C00002E	PCRB	- Pin configuration register, channel B
0C00002F	CCRB	- Channel command register, channel B
0C000030	TXFIFOB	- Transmitter FIFO, channel B
0C000031	TXFIFOB	- Transmitter FIFO, channel B (alternate address)
0C000032	TXFIFOB	- Transmitter FIFO, channel B (alternate address)
0C000033	TXFIFOB	- Transmitter FIFO, channel B (alternate address)
0C000034	RXFIFOB	- Receiver FIFO, channel B
0C000035	RXFIFOB	- Receiver FIFO, channel B (alternate address)
0C000036	RXFIFOB	- Receiver FIFO, channel B (alternate address)
0C000037	RXFIFOB	- Receiver FIFO, channel B (alternate address)
0C000038	RSRB	- Receiver status register, channel B
0C000039	TRSRB	- Transmitter and receiver status register, channel B
0C00003A	ICTSRB	- Input and counter/timer status register, channel B
0C00003B	GSR	- General status register (alternate address)
0C00003C	IERB	- Interrupt enable register, channel B
0C00003E	IVRM	- Interrupt vector register, modified
0C00003F	MRR	- Master reset register

3.5 CONTROL/STATUS REGISTERS

The XVME-630 contains four byte-wide control/status registers. These register should be accessed by byte instructions for proper operation.

Table 3-1. XVME-630 Registers

Address (Hex)	Register Name
08000003	Control Register 3
08000002	Control Register 2
08000001	Control Register 1
08000000	Interrupter Vector/Status Register 0

The following subsections describe the bit functions of the four registers.

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3.5.1 Status Register 0 (Address 08000000H)

This read-only register provides status information for various conditions. The bits of this register are described below.

Bit 7 is the state of the MISO (Master In Slave Out) signal from the MC68HC68T1 real time clock. This bit will reflect the state of the data bit read from the real time clock when SS and SCK are active. (Refer to section 3.8 in this manual or to the Motorola manual for more information on programming the real time clock.)

1 = Serial data bit read is a 1
0 = Serial data bit read is a 0

Bit 6 gives the state of the MAX690's PFO* signal, used to check the battery voltage.

1 = Battery voltage is OK
0 = Battery voltage is low

Bit 5 shows whether the XVME-630 is asserting the VMEbus BBSY* signal.

1 = The XVME-630 is asserting the VMEbus BBSY* signal
0 = The XVME-630 is not asserting the VMEbus BBSY* signal

Bit 4 shows whether the XVME-630's interrupter VMEbus IRQ* has been acknowledged.

1 = The VMEbus interrupt has not been acknowledged
0 = The VMEbus interrupt has been acknowledged

Bit 3 gives the state of the ACFAIL* interrupt (logical OR of the ACFAIL* flip-flop and the actual ACFAIL* signal).

1 = A negative going transition of the VMEbus ACFAIL* signal has not occurred since the ACFAIL* flip-flop has been cleared, and ACFAIL* is not currently being asserted
0 = Either a VMEbus ACFAIL* has occurred or ACFAIL* is currently being asserted

Bit 2 gives the state of the abort push button interrupt.

1 = Abort push button interrupt is currently negated
0 = Abort push button interrupt is currently being asserted

Bit 1 gives the state of the software watchdog timer interrupt.

1 = The software watchdog timer interrupt is currently negated
0 = The software watchdog timer interrupt is currently being asserted

Bit 0 gives the inverted state of the VMEbus SYSFAIL* signal.

1 = The VMEbus SYSFAIL* signal is currently being asserted
0 = The VMEbus SYSFAIL* signal is currently negated

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3.5.2 Control Register 1 (Address 08000001H)

This read/write register controls many module functions. The bits of this register are described below. All bits of this port are set to zero when the module is reset or powered-up.

Bit 7 is unused.

Bit 6 controls the battery test load.
- 1 = Battery is loaded
- 0 = Battery is unloaded

Bit 5 allows the XVME-630 to acquire and retain mastership of the VMEbus.
- 1 = The XVME-630 wishes to acquire mastership of the VMEbus and retain it as long as this bit is a 1
- 0 = The XVME-630 does not want extended mastership of the VMEbus or wishes to release current mastership

Bit 4 controls whether VMEbus Extended memory accesses are cached (assuming cache is enabled on CPU).
- 1 = Cached
- 0 = Not cached

Bit 3 controls whether VMEbus Standard memory accesses are cached (assuming cache is enabled on CPU).
- 1 = Cached
- 0 = Not cached

Bit 2 controls whether dual-ported memory is cached (assuming cache is enabled on CPU).
- 1 = Cached
- 0 = Not cached

Bit 1 controls the green pass LED.
- 1 = Pass LED is on
- 0 = Pass LED is off

Bit 0 controls the red fail LED. Also may assert the VMEbus SYSFAIL* signal (jumper selectable).
- 1 = Fail LED is off; SYSFAIL* is negated (with jumper in)
- 0 = Fail LED is on; SYSFAIL* is asserted (with jumper in)

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3.5.3 **Control Register 2** (Address 08000002H)

This read/write register controls the functions shown below. All bits of this port are set to zero when the module is reset or powered-up.

Bit 7 is the MOSI (Master **O**ut Slave **I**n) signal of the MC68HC68T1 real time clock. This bit is latched into the real time clock by bit 6 (SCK).

1 = Data bit written to the RTC is a 1
0 = Data bit written to the RTC is a 0

Bit 6 is connected to the SCK (Serial Cloc**K**) pin of the real time clock and is used to latch the data being read from or written to real time clock's serial interface. The edge used to latch the data is determined by the state of this bit when the bit 5 (SS) signal is asserted. If this bit is 0 when SS is asserted, data will be latched on the rising edge of SCK. If this bit is 1 when SS is asserted, data will be latched on the falling edge of SCK. (Refer to the section 3.8 of this manual or to the Motorola manual for more information on programming the real time clock.)

1 = Drive the RTC's SCK line HI
0 = Drive the RTC's SCK line LO

Bit 5 is connected to the SS (Slave Select) pin of the real time clock which enables the real time clock serial interface when 1. Bit 5 (along with bit 6) also determines which edge of SCK will latch the data being transferred to or from the real time clock.

1 = RTC interface active (asserted)
0 = RTC interface inactive (negated)

Bit 4 enables the Interrupter Acknowledged Interrupt.

1 = Enables the Interrupter Acknowledged Interrupt
0 = Disables the Interrupter Acknowledged interrupt

Bit 3 generates a VMEbus interrupt when a 0 then a 1 is written to this bit.

1 = A positive going transition of this bit generates a VMEbus interrupt
0 = VMEbus interrupt generator disabled

Bits 2-0 indicates the IRQ level on which the VMEbus Interrupter will generate an interrupt. Powers up in the 000 state (illegal).

111 = Generates VMEbus IRQ7*
110 = Generates VMEbus IRQ6*
101 = Generates VMEbus IRQ5*
100 = Generates VMEbus IRQ4*
011 = Generates VMEbus IRQ3*
010 = Generates VMEbus IRQ2*
001 = Generates VMEbus IRQ1*
000 = Illegal

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3.5.4 **Control Register 3** (Address 08000003H)

This read/write register controls the functions shown below. All bits of this port are set to zero when the module is reset or powered-up.

Bit 7 enables or disables the dual-ported memory from VMEbus accesses.
- 1 = Disables slave accesses
- 0 = Enables slave accesses

Bit 6 selects the VMEbus master release mechanism Release When Done (RWD)
- 1 = After a VMEbus access, the XVME-630 retains bus mastership until another VMEbus master requests the VMEbus
- 0 = The XVME-630 releases VMEbus mastership after each VMEbus access (RWD) This requires that for each VMEbus access, the XVME-630 will go through a VMEbus bus request/arbitration sequence

Bit 5 controls the width of VMEbus instruction fetches at address 80000000 and above (A31=1).
- 1 = VMEbus instruction fetches at 80000000H-FFFFFFFFH will be accessed in longwords
- 0 = VMEbus instruction fetches at 80000000H-FFFFFFFFH will be accessed in words

Bit 4 re-arms the SoftWare WatchDog Timer (SWWDT) when written from a 0 to a 1 (rising edge).

Bit 3 enables and clears the VMEbus ACFAIL* interrupt.
- 1 = Enables the ACFAIL* interrupt
- 0 = Disables or clears the ACFAIL* interrupt

Bit 2 enables and clears the abort push button interrupt.
- 1 = Enables the abort push button interrupt
- 0 = Disables or clears the abort push button interrupt

Bit 1 enables and clears the software watchdog timer. It should only be cleared in the interrupt service routine.
- 1 = Enables the software watchdog timer
- 0 = Disables or clears the software watchdog timer interrupt

Bit 0 enables the VMEbus SYSFAIL* interrupt.
- 1 = Enables SYSFAIL* interrupt
- 0 = Disables SYSFAIL* interrupt

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3.6 INTERRUPTS

The XVME-630 is capable of both handling and generating interrupts on the VMEbus. The following sections describe how these interrupts are handled and generated.

3.6.1 VMEbus Interrupt Handler

The seven VMEbus interrupts can directly interrupt the 68EC030. The VMEbus interrupt levels for the XVME-630 are selectable through seven jumpers, one corresponding to each interrupt request level (see section 2.3.11). In addition, the XVME-630 can also handle interrupts generated by the abort button, watchdog timer, ACFAIL, SYSFAIL, real time clock, and DUSCC.

The interrupt handler prioritizes all the interrupt sources such that on-board interrupts have a higher priority. The interrupt sources and their priorities are shown below:

Table 3-2. Interrupt Levels

Interrupt Level	Local Interrupt	Acknowledge Type
7	VMEbus ACFAIL*	Autovector
7	Software Watchdog Timer	Autovector
7	Abort Push Button	Autovector
7	VMEbus IRQ7*	VMEbus IACK
6	VMEbus SYSFAIL*	Autovector
6	VMEbus IRQ6*	VMEbus IACK
5	DUSCC Serial Controller	Autovector
5	VMEbus IRQ5*	VMEbus IACK
4	Interrupter IACK	Autovector
4	VMEbus IRQ4*	VMEbus IACK
3	Real Time Clock	Autovector
3	VMEbus IRQ3*	VMEbus IACK
2	VMEbus IRQ2*	VMEbus IACK
1	VMEbus IRQ1*	VMEbus IACK

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NOTE
The VMEbus interrupt handler will request mastership of the VMEbus on the same bus request level as the 68EC030 uses for its master cycles.

3.6.2 VMEbus Interrupter

The 68EC030 can generate D08(O) VMEbus interrupts. These interrupts are generated through the interrupt vector register and control/status register 2.

The interrupt vector register is a write-only register which contains the 8-bit vector which is to be placed on the VME data bus during an interrupt acknowledge cycle.

The interrupter is set by six bits in control register 2 and status register 0, as shown below:

Bits 0-2 (control register 2)
: These read/write bits represent the binary value of the interrupt level to be generated (0=illegal, 1-7=IRQ* 1-7).

Bit 3 (control register 2)
: This read/write bit is used to generate the interrupt. Writing a 0 and then a 1 to this bit generates an interrupt at the programmed interrupt level. During the interrupt acknowledge cycle, the vector contained in the interrupt vector register will be placed on the data bus, and the IRQ* will be negated (ROAK).

Bit 4 (status register 0)
: This read-only bit allows the 68EC030 to read the status of the interrupter, to determine if the VMEbus interrupt has been acknowledged.
1 = interrupt has not been acknowledged
0 = interrupt has been acknowledged

Bit 4 (control register 2)
: If this bit is 1, the 68EC030 will be interrupted on level 4 when the VMEbus interrupt has been acknowledged. This interrupt is an autovector.

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3.6.3 Generating VMEbus Interrupts

The VMEbus interrupter is comprised of three circuits:

- Vector register (0800000H)
- IACKIN/IACKOUT logic
- Control/status bits for generating interrupts

There are two ways to generate a VMEbus interrupt: polling and interrupting.

To poll, follow the steps below:

1. Preload the vector register. The vector is used to determine the source of the interrupt.
2. Load bits 0-2 of control register 2 (08000002H) with the VME interrupt level at which you wish to generate the interrupt.
3. Toggle bit 3 of control register 2 from 0 to 1.
4. Poll bit 4 of status register 1 (08000000H) to determine when the interrupt has been acknowledged (1 = interrupt pending; 0 = interrupt acknowledged).

To generate an interrupt, follow the steps below:

1. Preload the vector register. The vector is used to determine the source of the interrupt.
2. Load bits 0-2 of control register 2 (08000002H) with the VME interrupt level at which you wish to generate the interrupt.
3. If you would like the interrupter to interrupt the 68EC030 upon the VMEbus acknowledge, set bit 4 of control register 2 to 1.
4. Toggle bit 3 of control register 2 from 0 to 1.
5. Wait for the interrupt to occur. If in interrupt mode, the interrupt tells the 68EC030 that the VMEbus interrupt has been acknowledged.

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3.6.4 SYSFAIL, ACFAIL, and Abort Button

SYSFAIL, ACFAIL, and the abort button are all enabled by bits of control register 3.

Bit 3 controls the ACFAIL interrupt, bit 2 controls the ABORT button interrupt, and bit 0 controls the SYSFAIL interrupt. For all three bits, a value of 1 enables the interrupt and a value of 0 disables the interrupt.

3.6.5 Watchdog Timer

The software watchdog timer (SWWDT) allows the processor to regain control of a program that has gone astray. Using the SWWDT, the user program must clear the SWWDT at regular intervals to prevent the SWWDT timeout from expiring. If the user program goes astray, it is likely that the SWWDT will not be serviced regularly, the SWWDT timeout will expire, and a non-maskable interrupt will be generated to the 68EC030. This allows the user program to gain control.

To enable the SWWDT, bit 3 of control register 3 needs to be set to 1. When enabled, the SWWDT must be re-armed at a rate of 12-120 ms to avoid a SWWDT timeout. To re-arm, toggle bit 4 of control register 3 from 0 to 1 (a rising edge will re-arm).

> **NOTE**
> Do not re-arm the SWWDT at increments faster than 12 ms.

After 155 ±35 mS without the SWWDT being re-armed, the interrupt is generated. Re-arming the SWWDT at increments between 120 mS and 195 mS is **not** recommended as the results cannot be guaranteed. The SWWDT should be armed just before enabling it to prevent any false interrupts from occurring. Once the SWWDT has expired, the interrupt may be cleared (and disabled) by writing a 0 to the enable bit (control register 3, bit 1).

3.6.6 Real Time Clock

For the real time clock, an alarm may be set to interrupt the XVME-630 at a particular time (based on an hour/minute/second comparison) or periodically from every 488 uS to once-per-day (programmable).

See the Motorola manual for more information on generating interrupts.

3.6.7 DUSCC

The DUSCC can be programmed to interrupt the XVME-630. For information on programming, refer to the Signetics manual.

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3.7 DUAL PORTED READ/MODIFY/WRITES

This section describes how the XVME-630 handles read/modify/write (RMW) cycles in dual-ported memory.

To increase performance, the XVME-630's dual-ported memory is switched to a state favoring the local 68EC030 after each slave access. A local 68EC030 bus cycle to the dual-ported memory can then be started before the previous slave cycle has been completed on the VMEbus. The priority between master and slave accesses to the dual-ported memory is as follows:

1) If any dual-ported slave cycle is in progress while the local 68EC030 requests a RMW cycle, the dual-ported control circuitry forces the VMEbus access to be completed (waiting for VMEAS* to be negated)

2) In all other situations, the local 68EC030 has immediate access to the dual-ported memory after the current bus cycle has been completed

> **NOTE**
> Situation 2) can effectively divide a VMEbus slave RMW cycle in the dual-ported memory. This could cause a problem if a location in dual-ported memory is being used to hold an ownership flag or semaphore.

Assume we have a VMEbus system with two XVME-630s (XVME-630[A] and XVME-630[B]), and a semaphore is defined to control the ownership of XVME-630[A]'s dual-ported memory. This semaphore is located in the first byte of XVME-630[A]'s dual-ported memory (assume an Extended memory slave address of 80000000).

The following code could not be used to correctly set and clear the semaphore:

XVME-630[A]

```
DPORT_A   EQU     $1C000000
SPHORE_A  EQU     DPORT_A+$00

;00 = MEMORY NOT IN USE
;80 = MEMORY IS IN USE

GET_MEM_A
          TAS     SPHORE_A
          BNE     GET_MEM_A
          RTS

RELEASE_MEM_A
          MOVE.B  #$00,SPHORE_A
          RTS
```

XVME-630[B]

```
DPORT_B   EQU     $80000000
SPHORE_B  EQU     DPORT_B+$00

;00 = MEMORY NOT IN USE
;80 = MEMORY IS IN USE

GET_MEM_B
          TAS     SPHORE_B
          BNE     GET_MEM_B
          RTS

RELEASE_MEM_A
MOVE.B    #$00,SPHORE_B
RTS
```


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If the previous code were to be used while XVME-630[A] has ownership of the memory, XVME-630[B] would try to obtain ownership using the GET_MEM_B routine, and XVME-630[A] would release the memory using the RELEASE_MEM_A routine. This would cause the following sequence of events:

XVME-630[A]	Semaphore	XVME-630[B]
	80	TAS SPHORE_B read = 80, "z" = FALSE
MOVE.B #00,SPHORE_A write SPHORE_A = $00	00	
	80	write SPHORE_B = $80

XVME-630[A] has released ownership of the memory, yet the semaphore is still set (it is incorrectly set by XVME-630[B]). A deadlock exists because both XVME-630[A] and XVME-630[B] think the other owns the memory, and neither will release it.

However, there are two ways around this problem:

Solution #1: Change the RELEASE_MEM_A code to the following:

```
RELEASE_MEM_A
        MOVEM.L     D0/D1,-(A7)
        MOVE.B      SPHORE_A,D0
        MOVE.B      #$00,D1
        CAS.B       D0,D1,SPHORE_A
        MOVEM.L     (A7)+,D0/D1
        RTS
```

The new sequence of events would be as follows:

XVME-630[A]	Semaphore	XVME-630[B]
	80	TAS SPHORE_B read = $80, "z" = FALSE
	80	write SPHORE_B = $80
CAS.B D0,D1,SPHORE_A write SPHORE_A = $00	00	

By clearing the semaphore with a local 68EC030 RMW cycle, any current VMEbus cycle (in this case a RMW) is completed before the local 68EC030 cycle is initiated. This method of clearing the semaphore allows both fast access of dual-ported memory by XVME-630[A] and the correct operation of the semaphores.

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Solution #2: Use the dual-ported memory alternate address space.

The dual-ported memory is shadowed at address 18000000-1BFFFFFF. Accesses to this address space force the completion of the current VMEbus cycle (waiting for VMEAS* to be negated) before initiating the local 68EC030 cycle. Using the replacement line below for the alternate address space allows the original code from program #1 to work correctly.

```
ALT_DPORT EQU          $18000000          ; DUAL-PORTED ALTERNATE ADDRESS SPACE
SPHORE_A  EQU          ALT_DPORT+$00
```

> **NOTE**
>
> All accesses to the dual-ported memory alternate address space will be inherently slower. For best performance, use this alternate memory space only for RMW considerations.

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3.8 REAL TIME CLOCK

The real time clock (RTC) is accessed serially using bits in the control and status registers. See the Motorola MC68HC68T1 data sheet for information on the transfer of data to the RTC. The following code will work at 40 MHz execution out of local SRAM with the instruction cache enabled (the fastest possible combination), and can be used to access the RTC.

Sample routines to access the RTC are shown below, and a typical single byte read or write sequence is shown on page 3-23.

```
CONTROL_STATUS          EQU   $08000000
VECTOR_REG              EQU   CONTROL_STATUS+0
ST_REG_0                EQU   CONTROL_STATUS+0
CS_REG_1                EQU   CONTROL_STATUS+1
CS_REG_2                EQU   CONTROL_STATUS+2
CS_REG_3                EQU   CONTROL_STATUS+3

RD_RTC_RAM              EQU   $00
RD_RTC_SECS             EQU   $20
RD_RTC_MINS             EQU   $21
RD_RTC_HOURS            EQU   $22
RD_RTC_DAY_OF_WK        EQU   $23
RD_RTC_DAY_OF_MT        EQU   $24
RD_RTC_MONTH            EQU   $25
RD_RTC_YEAR             EQU   $26
RD_RTC_STATUS_REG       EQU   $30
RD_RTC_CLK_CTRL_REG     EQU   $31
RD_RTC_INT_CTRL_REG     EQU   $32

WR_RTC_RAM              EQU   $80
WR_RTC_SECS             EQU   $A0
WR_RTC_SECS_ALARM       EQU   $A8
WR_RTC_MINS             EQU   $A1
WR_RTC_MINS_ALARM       EQU   $A9
WR_RTC_HOURS            EQU   $A2
WR_RTC_HOURS_ALARM      EQU   $AA
WR_RTC_DAY_OF_WK        EQU   $A3
WR_RTC_DAY_OF_MT        EQU   $A4
WR_RTC_MONTH            EQU   $A5
WR_RTC_YEAR             EQU   $A6
WR_RTC_CLK_CTRL_REG     EQU   $B1
WR_RTC_INT_CTRL_REG     EQU   $B2

RTC_MISO                EQU   7
RTC_MOSI                EQU   7
RTC_SCK                 EQU   6
RTC_SS                  EQU   5
```


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```
*************************************************************
*                                                           *
*            RTC_ADDR                                       *
*************************************************************
* ENTRY CONDITIONS    : D1 = ADDR TO WRITE TO RTC           *
* EXIT CONDITIONS     : NONE                                *
* REGISTERS AFFECTED  : NONE                                *
*************************************************************

RTC_ADDR
   BTST    #RTC_SS,CS_REG_2        ; TEST SS BIT
   BNE     RTC_ADDR                ; LOOP UNTIL SS IS NEGATED

   BSET    #RTC_SS,CS_REG_2        ; ASSERT SS
   BSR     RTC_WR                  ; WRITE ADDRESS

   RTS

*************************************************************
*                                                           *
*            RTC_RD                                         *
*************************************************************
* ENTRY CONDITIONS    :  NONE                               *
* EXIT CONDITIONS     :  D1 = BYTE READ FROM RTC            *
* REGISTERS AFFECTED  :  D1 ONLY                            *
*************************************************************

RTC_RD
   MOVEM.L D0,-(A7)                ; PUSH REGISTER

   MOVE.B  #1,D1                   ; INITIALIZE "1" IN LSB

RD_LOOP
   BSET    #RTC_SCK,CS_REG_2       ; CLOCK SCK HI
   BCLR    #RTC_SCK,CS_REG_2       ; CLOCK SCK LO
   MOVE.B  ST_REG_0,D0             ; READ RAW "MISO" DATA
   LSL.B   #1,D0                   ; SHIFT MSB INTO "X" BIT
   ROXL.B  #1,D1                   ; ROTATE "X" BIT INTO LSB, MSB INTO "C"
   BCC     RD_LOOP                 ; HAS THE "1" BEEN SHIFTED OUT ???

   MOVEM.L (A7)+,D0                ; RESTORE REGISTER
   RTS

*************************************************************
*                                                           *
*            RTC_WR                                         *
*************************************************************
* ENTRY CONDITIONS    :  D1 = BYTE TO WRITE TO RTC          *
* EXIT CONDITIONS     :  NONE                               *
* REGISTERS AFFECTED  :  NONE                               *
*************************************************************
```


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```
RTC_WR
   MOVEM.L D0,-(A7)                    ; PUSH REGISTER

   MOVE.B  #8,D0                       ; LOOP THROUGH 8 BITS
WR_LOOP
   ROL.B   #1,D1                       ; ROTATE MSB INTO "C"
   BCC     MSB_LO                      ; NEXT BIT IS "0"
   BSET    #RTC_MOSI,CS_REG_2          ; SET MOSI = "1"
   BRA     MOSI_SET                    ; SKIP AHEAD
MSB_LO
   BCLR    #RTC_MOSI,CS_REG_2          ; SET MOSI = "0"
MOSI_SET
   BSET    #RTC_SCK,CS_REG_2           ; CLOCK SCK HI
   BCLR    #RTC_SCK,CS_REG_2           ; CLOCK SCK LO

   SUB.B   #1,D0                       ; DECREMENT LOOP COUNTER
   BNE     WR_LOOP                     ; ARE WE DONE ???

   MOVEM.L (A7)+,D0                    ; RESTORE REGISTER
   RTS

*************************************************************
*           RTC_DONE                                        *
*************************************************************
* ENTRY CONDITIONS    :  NONE                               *
* EXIT CONDITIONS     :  RTC DATA TRANS. COMPLETED          *
* REGISTERS AFFECTED  :  NONE                               *
*************************************************************

RTC_DONE
   BCLR    #RTC_SS,CS_REG_2            ; NEGATE SS

   RTS
```

A TYPICAL SINGLE BYTE READ OR WRITE SEQUENCE IS SHOWN BELOW:

```
************************
* SINGLE BYTE READ     *
************************

   MOVE.B  #RD_RTC_RAM,D1              ; RTC ADDRESS $00
   BSR     RTC_ADDR                    ; PRESENT ADDRESS TO RTC
   BSR     RTC_RD                      ; READ DATA FROM RTC ADDRESS $00
           ; (DATA IS IN D1)
   BSR     RTC_DONE                    ; COMPLETE CYCLE

************************
* SINGLE BYTE WRITE    *
************************

   MOVE.B  #WR_RTC_RAM,D1              ; RTC ADDRESS $00
   BSR     RTC_ADDR                    ; PRESENT ADDRESS TO RTC
   MOVE.B  #$AA,D1                     ; LOAD DATA TO WRITE
   BSR     RTC_WR                      ; WRITE DATA TO RTC ADDRESS $00
   BSR     RTC_DONE                    ; COMPLETE CYCLE
```


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As long as the RTC cycle is not completed, additional locations may be accessed (block reads or block writes, but not mixed) without re-presenting the address to the RTC. The address register in the RTC is automatically incremented after each byte transfer.

> **NOTE**
>
> Only the lowest 5 address bits in the RTC increment; e.g. if you are sequentially accessing RAM, after location 1F, the next location will be 00. Conversely, after an access to location 3F, the next location will be 20.

Typical multiple byte read and write sequences are shown below:

```
*************************
* MULTIPLE BYTE READ *
*************************

   MOVE.B   #RD_RTC_RAM,D1        ; RTC ADDRESS $00
   BSR      RTC_ADDR              ; PRESENT ADDRESS TO RTC
   BSR      RTC_RD                ; READ DATA FROM RTC ADDRESS $00
            ; (DATA IS IN D1)
   MOVE.B   D1,BUFFER
   BSR      RTC_RD                ; READ DATA FROM RTC ADDRESS $01
            ; (DATA IS IN D1)
   MOVE.B   D1,BUFFER+1
   BSR      RTC_DONE              ; COMPLETE CYCLE

**************************
* MULTIPLE BYTE WRITE *
**************************

   MOVE.B   #WR_RTC_RAM,D1        ; RTC ADDRESS $00
   BSR      RTC_ADDR              ; PRESENT ADDRESS TO RTC
   MOVE.B   #$AA,D1               ; LOAD DATA TO WRITE
   BSR      RTC_WR                ; WRITE DATA TO RTC ADDRESS $00
   MOVE.B   #$55,D1               ; LOAD DATA TO WRITE
   BSR      RTC_WR                ; WRITE DATA TO RTC ADDRESS $01
   BSR      RTC_DONE              ; COMPLETE CYCLE
```


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3.9 ALIGNING DATA REFERENCES IN CAS INSTRUCTIONS

Data references to the VMEbus in CAS and CAS2 instructions must be aligned. The XVME-630 cannot indivisibly execute unaligned read/modify/write (RMW) instructions (CAS and CAS2) across the VMEbus. (When unaligned, these instructions require multiple read and write cycles due to an address change.)

The TAS instruction always generates RMW cycles. The CAS instruction generates RMW cycles only when referencing a byte operand. CAS2 never generates RMW cycles.

3.10 LOCKING ACCESS TO THE VMEBUS

The XVME-630 provides a mechanism to allow it to obtain and lock the VMEbus from use by other VMEbus masters. This mechanism is software-controlled via bit 5 of control register 1 (GETBUS). Additionally, bit 5 of status register 0 (BBSY) indicates whether the XVME-630 has possession of the VMEbus.

Locking access to the VMEbus requires adhering to the following rules and protocol to avoid a potential deadlock condition:

- Do not assert GETBUS unless BBSY is negated.
- Once GETBUS is asserted, do not negate GETBUS unless BBSY is asserted.

The proper protocol to use the GETBUS bit is shown below:

- Make sure the XVME-630 does not have control of the VMEbus. If the BBSY bit is 0, the bus is released. If the BBSY bit is 1, the XVME-630 still owns the bus from a previous access (since it is not currently accessing the VMEbus). This only happens if the RWD bit is negated (1), so assert RWD (0) and wait for the BBSY bit to be 0. This guarantees that the XVME-630 does not own the VMEbus.
- Since the XVME-630 does not own the bus, GETBUS can now be asserted (1). When the BSY bit is 1, the XVME-630 owns the VMEbus for as long as GETBUS is asserted.
- To release control of the VMEbus, negate GETBUS (0).

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3.11 SOFTWARE NOTES

Some programming hints and tips are shown below for reference.

- The XVME-630 can execute the **STOP** instruction.
- The XVME-630 can execute the **RESET** instruction. This will result in the generation of a VMEbus SYSRST*, but not an XVME-630 on-board reset.
- Executing a **BKPT** instruction (breakpoint) results in a BERR*, which causes the 68EC030 to take the illegal instruction vector.
- Executing a floating-point instruction with no floating point co-processor installed results in a BERR*, which forces the 68EC030 to take the line 1010 emulator vector.
- Software must ensure that accesses to the DUSCC are at least 160 nS apart (CS* high time).
- Software must ensure that the XVME-630's dual-ported memory is not disabled (bit 7, control register 3) while another VMEbus master is accessing the XVME-630's dual-ported memory. This can be guaranteed by acquiring the VMEbus through the GETBUS bit (bit 5, control register 1), disabling the slave memory, and releasing the VMEbus.
- During slave accesses, dual-ported Bank 3 will **not** respond to VMEbus program accesses (address modifiers 3A, 3E, 0A, 0E).

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The XVME-630 Processor Module is a double-high VMEbus compatible module. On the rear edge of the board is a 96-pin bus connector labeled P1. The signals carried by connector P1 are the standard address, data, and control signals required for a P1 backplane interface, as defined by the VMEbus specification. Table A-1 identifies and defines the signals carried by the P1 connector.

Table A-1. P1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B:3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	1A:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17 18,19 1C:1	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	1A:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A:24-30 1C:15-30	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.

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Table A-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BBSY*	1B:1	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,10	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	1B:5,7, 9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
BR0*-BR3*	1B:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DS1*	1A:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).

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Table A-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
DTACK*	1A:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A:1-8 1C:1-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A:9,11, 15,17,19, 1B:20,23, 1C:9 2B:2,12, 22,31	GROUND
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQ1*-	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector IRQ7 driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERVED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.

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Table A-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSCLK	1A:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.
SYSFAIL*	1C:10	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	1C:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	1B:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5V	1A:32 1B:32 1C:32 2B:1,13,32	+5VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12V	1A:31	-12 VDC POWER: Used by system logic circuits.

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BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2. P1 Pin Assignments

Pin #	Row A Signal	Row B Signal	Row C Signal
1	D0	BBSY*	D8
2	D01	BCLR*	D9
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

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BACKPLANE CONNECTOR P2

The following table lists the P2 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-3. P2 Pin Assignments

Pin #	Rows A and C Signal	Row B Signal
1	IOCHCK*	+5V
2	SD7	GND
3	SD6	N/C
4	SD5	A24
5	SD4	A25
6	SD3	A26
7	SD2	A27
8	SD1	A28
9	SD0	A29
10	IOCHRDY	A30
11	AEN	A31
12	SA19	GND
13	SA18	+5V
14	SA17	D16
15	SA16	D17
16	SA15	D18
17	SA14	D19
18	SA13	D20
19	SA12	D21
20	SA11	D22
21	SA10	D23
22	SA9	GND
23	SA8	D24
24	SA7	D25
25	SA6	D26
26	SA5	D27
27	SA4	D28
28	SA3	D29
29	SA2	D30
30	SA1	D31
31	SA0	GND
32	GND	+5V

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Table A-4. JK1 Channel A Pinouts

PIN	RS-232C SIGNAL	Mass Terminated 25-Pin Connector
1	N/C	Pin 1
2	N/C	Pin 14
3	RXDA	Pin 2
4	N/C	Pin 15
5	TXDA	Pin 3
6	N/C	Pin 16
7	CTSA	Pin 4
8	TRXCA	Pin 17
9	RTSA	Pin 5
10	N/C	Pin 18
11	N/C	Pin 6
12	N/C	Pin 19
13	GND	Pin 7
14	DCDA	Pin 20
15	DTRA(GPO1A)	Pin 8
16	N/C	Pin 21
17	N/C	Pin 9
18	N/C	Pin 22
19	N/C	Pin 10
20	N/C	Pin 23
21	N/C	Pin 11
22	RTXCA	Pin 24
23	N/C	Pin 12
24	N/C	Pin 25
25	N/C	Pin 13

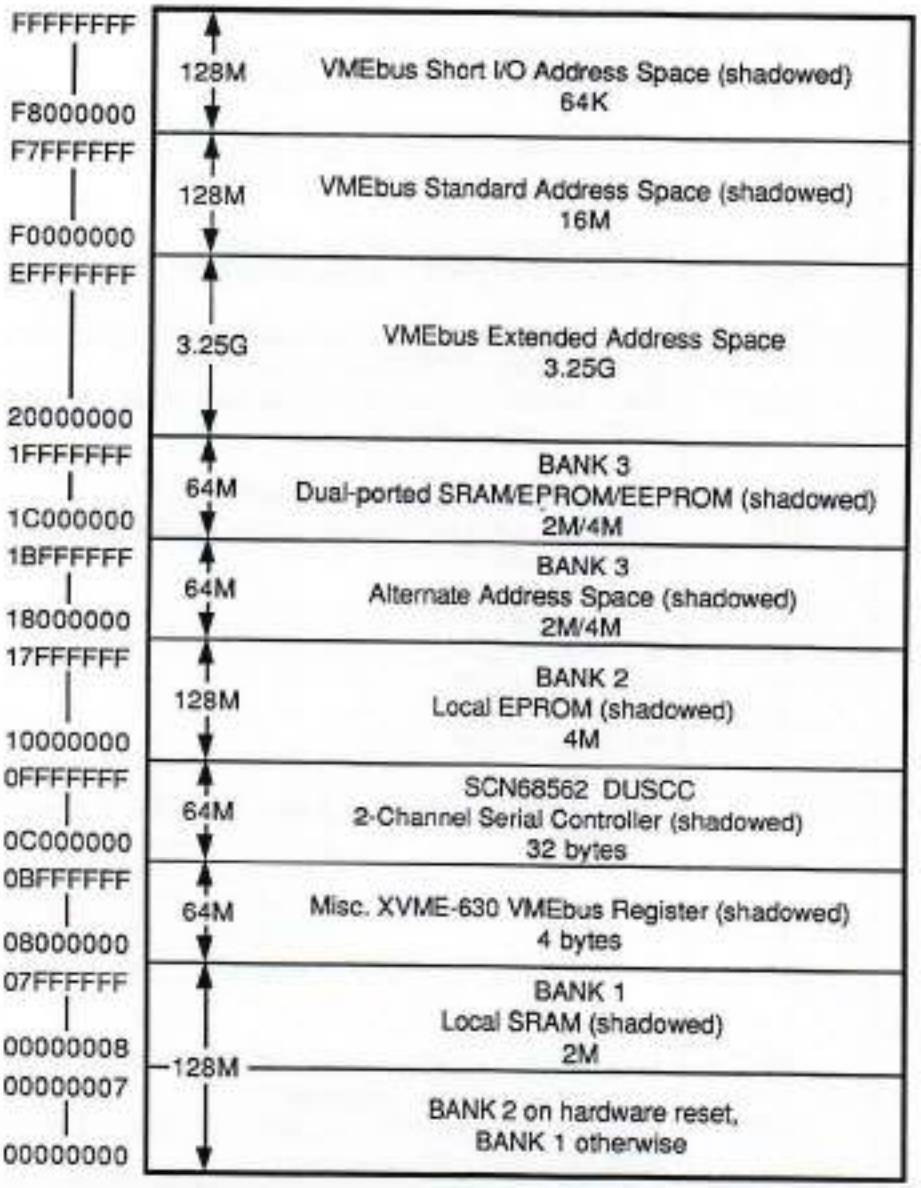
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Table A-5. JK1 Channel B Signals

PIN	RS-232C SIGNAL	Mass Terminated 25-Pin Connector	RS-485 SIGNAL
26	N/C	Pin 1	+5V
27	N/C	Pin 14	TXDB+
28	RXDB	Pin 2	RTSB-
29	N/C	Pin 15	RTSB+
30	TXDB	Pin 3	TXDB-
31	N/C	Pin 16	TRXCB+
32	CTSB	Pin 4	DTRB-(GPO1B)
33	TRXCB	Pin 17	CTSB+
34	RTSB	Pin 5	TRXCB-
35	N/C	Pin 18	GND
36	N/C	Pin 6	DCDB-
37	N/C	Pin 19	DCDB+
38	GND	Pin 7	GND
39	DCDB	Pin 20	RXDB+
40	DTRB(GPO1B)	Pin 8	RXDB-
41	N/C	Pin 21	RTXCB-
42	N/C	Pin 9	N/C
43	N/C	Pin 22	RTXCB+
44	N/C	Pin 10	CTSB-
45	N/C	Pin 23	N/C
46	N/C	Pin 11	N/C
47	RTXCB	Pin 24	DTRB+(GPO1B)
48	N/C	Pin 12	N/C
49	N/C	Pin 25	N/C
50	N/C	Pin 13	N/C

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Memory Map (Factory Shipped Configuration)



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Table B-1. Jumper Settings

Jumper	Position	Function	Section Reference
J1	IN	VMEbus BERR* timer enabled	2.3.9
	OUT	VMEbus BERR* timer disabled	
J2	IN	VMEbus SYSCLK driver enabled	2.3.9
	OUT	VMEbus SYSCLK driver disabled	
J3	IN	VMEbus single level arbiter enabled	2.3.9
	OUT	VMEbus single level arbiter disabled	
J4	IN	VMEbus SYSFAIL* driver enabled	2.3.13
	OUT	VMEbus SYSFAIL* driver disabled	
J5	IN	Dual-ported memory responds to supervisory or non-privileged VMEbus slave accesses	2.3.4
	OUT	Dual-ported memory responds only to supervisory VMEbus slave accesses	
J6	IN	VMEbus interrupt handler, handles IRQ	2.3.11
	OUT	VMEbus interrupt handler, does not handle IRQ	
	A	VMEbus IRQ7*	
	B	VMEbus IRQ6*	
	C	VMEbus IRQ5*	
	D	VMEbus IRQ4*	
	E	VMEbus IRQ3*	
	F	VMEbus IRQ2*	
	G	VMEbus IRQ1*	
J7, J15,J16	**VMEbus Master Bus Requester Level**	**BGIN to BGOUT Jumpers (outside posts only)**	2.3.2
	A	0 — J7B-J15B, J7C-J15C, J7D-J15D	
	B	1 — J7A-J15A, J7C-J15C, J7D-J15D	
	C	2 — J7A-J15A, J7B-J15B, J7D-J15D	
	D	3 — J7A-J15A, J7B-J15B, J7C-J15C	
J8	IN	Dual-ported memory responds to VMEbus Standard address space slave accesses	2.3.4
	OUT	Dual-ported memory responds to VMEbus Extended address space slave accesses	

All jumpers are installed when shipped.

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Table B-1. Jumper Settings (Continued)

Jumper	Position	Function	Section Reference
J9	IN OUT	Release on request VMEbus bus release mechanism Do not release on request	2.3.12
J10		NOT USER CONFIGURABLE	
J11	IN OUT	Cache disabled Cache enabled	2.3.3
J12 J13 J14 OUT OUT OUT OUT OUT IN OUT IN OUT OUT IN IN IN OUT OUT IN OUT IN IN IN OUT IN IN IN		Dual-ported memory 8 wait states 2 wait states 3 wait states 4 wait states 5 wait states 6 wait states 7 wait states 8 wait states	2.3.7.2
J15		Used with J7 and J16 (see J7 on previous page)	2.3.2
J16		Used with J7 and J15 (see J7 on previous page)	2.3.2
J17	IN OUT	Oscillator power applied (normal operation) Oscillator not powered (test mode)	2.3.5
J18	A B	Battery disconnected (shipping position) Battery connected (normal operation)	2.3.1
J19 J20 A OUT A OUT A IN B IN		Determines local EPROM device 27C010 27C020 27C040 27C080	2.3.7.1
J21,J23 J22 IN OUT OUT IN		Sets local SRAM device size 28-pin 32-pin	2.3.7.1
J24	A B	1 wait-state local SRAM reads/writes 0 wait-state local SRAM reads/1 wait-state writes	2.3.7.2

All jumpers are installed when shipped.

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Table B-1. Jumper Settings (Continued)

Jumper	Position	Function	Section Reference
J25 IN IN OUT OUT	**J26** IN OUT IN OUT	Sets local EPROM wait state reads 1 wait-state reads 2 wait-state reads 3 wait-state reads 4 wait-state reads	2.3.7.2
J27		User definable, software readable jumper	2.3.10
J28	IN OUT	Reset push button will reset the XVME-630 Reset push button will not reset the XVME-630	2.3.8
J29	IN OUT	Reset push button will generate VMEbus SYSRESET* Reset push button will not generate VMEbus SYSRESET*	2.3.8
J30		Used to specify dual-ported memory device type with J43, J44, J45, J46, J59, J61, J62, and J63	2.3.7.1
J31		User definable jumper	2.3.10
J32-J42, J47-J57	A B	Serial channel B is RS-232C Serial channel B is RS-485	2.3.6
J43-J46		Used to specify dual-ported memory device type with J40, J59, J61, J62, and J63	2.3.7.1
J58	IN OUT	XVME-630 will be reset by a VMEbus SYSRESET* XVME-630 will not be reset by a VMEbus SYSRESET*	2.3.8
J59		Used to specify dual-ported memory device type with J30, J43, J44, J45, J46, J61, J62, and J63	2.3.7.1
J60		XVME-630 can generate a VMEbus SYSRESET* XVME-630 cannot generate a VMEbus SYSRESET*	2.3.8
J61-J63		Used to specify dual-ported memory device type with J30, J43, J44, J45, J46, and J59	2.3.7.1
JA22-JA23		Selects Standard or Extended VMEbus slave address (A23-A22) (in=0, out=1)	2.3.4
JA24-JA31		Selects Extended VMEbus slave address 9A31-A24) (in=0, out=1)	2.3.4

All jumpers are installed when shipped.

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Table B-2. Bank 1 SRAM Selection Jumpers

	J21	J22	J23
28-pin SRAM	IN	OUT	IN
32-pin SRAM	OUT	IN	OUT

Table B-3. Bank 1 Wait State Selection Jumper

J24	Number of Wait States
A	1 wait state reads/writes
B	0 wait state reads, 1 wait state writes

Table B-4. Bank 2 EPROM Selection Jumpers

J19	J20	Device Selected
A	OUT	27C010
A	OUT	27C020
A	IN	27C040
B	IN	27C080

Table B-5. Bank 2 EPROM Wait State Selection Jumpers

J25	J26	Number of Wait State Reads
IN	IN	1
IN	OUT	2
OUT	IN	3
OUT	OUT	4

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Table B-6. Bank 2 Wait States Vs. Access Times

Bank 2 Specifications			
Wait States	**J25, J26**	**tADDR-DV 25 MHz (max)**	**tADDR-DV 40 MHz (max)**
1	IN, IN	70.5 nS	40.0 nS
2	IN, OUT	110.5 nS	65.0 nS
3	OUT, IN	150.5 nS	90.0 nS
4	OUT, OUT	190.5 nS	115.0 nS

Table B-7. Bank 3 Memory Selection Jumpers

DUAL-PORTED MEMORY DEVICE TYPE	J63	J61	J59	J46	J62	J45,J44 J43,J30
SRAM (Battery & Non-battery Backed)						
4x[64kx8]	B	A	OUT	A	B	A,C
4x[128kx8]	B	A	OUT	A	B	A,C
4x[256kx8]	B	A	IN	A	B	A,C
4x[512kx8]	B	A	IN	A	B	A,C
Non-Battery Backed SRAM						
4x[64kx8]	B	A	OUT	A	B	A,C
4x[128kx8]	B	A	OUT	A	B	A,C
4x[256kx8]	B	A	IN	A	B	A,C
4x[512kx8]	B	A	IN	A	B	A,C
EPROM						
27C010 4x[128kx8]	A	C	OUT	B	OUT	A,D
27C020 4x[256kx8]	A	C	IN	B	OUT	A,D
27C040 4x[512kx8]	A	C	IN	B	A	A,D
27C080 4x[1mx8]	A	B	IN	B	A	A,D
Flash						
4x[32kx8]	A	D	OUT	B	OUT	B,D
4x[64kx8]	A	D	OUT	B	OUT	B,D
4x[128kx8]	A	D	OUT	B	OUT	B,D
4x[256kx8]	A	D	IN	B	OUT	B,D

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Table B-8. Bank 3 Wait State Selection Jumpers

J12	J13	J14	Number of Wait States
IN	IN	IN	8
IN	IN	OUT	2
IN	OUT	IN	3
IN	OUT	OUT	4
OUT	IN	IN	5
OUT	IN	OUT	6
OUT	OUT	IN	7
OUT	OUT	OUT	8

Table B-9. Bus Grant Jumpers

Jumpers J7, J15, and J16	VMEbus Master Bus Request Level	BGIN to BGOUT Jumpers (Outside Posts Only)
A	0	J7B-J15B, J7C-J15C, J7D-J15D
B	1	J7A-J15A, J7C-J15C, J7D-J15D
C	2	J7A-J15A, J7B-J15B, J7D-J15D
D	3	J7A-J15A, J7B-J15B, J7C-J15C

Table B-10. Interrupt Selection Jumpers

Jumper J6 Position	VMEbus Interrupt Level
A	IRQ7*
B	IRQ6*
C	IRQ5*
D	IRQ4*
E	IRQ3*
F	IRQ2*
G	IRQ1*
OUT	Disabled

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Table B-11. SYSRESET Jumper Options

J28	J29	J58	J60	Reset button resets		On-board circuitry reset by	Power monitor resets		Reset instruc. generates SYSRESET*
				O-B Cir.	VMEbus		O-B Cir.	VMEbus	
OUT	OUT	OUT	OUT				✓		
OUT	OUT	OUT	IN				✓	✓	✓
OUT	OUT	IN	OUT			✓	✓		
OUT	OUT	IN	IN			✓	✓	✓	✓
OUT	IN	OUT	OUT				✓		
OUT	IN	OUT	IN		✓	✓	✓	✓	✓
OUT	IN	IN	OUT			✓	✓		
OUT	IN	IN	IN		✓		✓	✓	✓
IN	OUT	OUT	OUT	✓		✓	✓		
IN	OUT	OUT	IN	✓		✓	✓	✓	✓
IN	OUT	IN	OUT	✓			✓		
IN	OUT	IN	IN	✓		✓	✓	✓	✓
IN	IN	OUT	OUT	✓		✓	✓		
IN	IN	OUT	IN	✓	✓		✓	✓	✓
IN	IN	IN	OUT	✓		✓	✓		
IN	IN	IN	IN	✓	✓	✓	✓	✓	✓

✓ = yes, blank = noO-B Cir. = On-Board Circuitry

Table B-12. User-Configurable Jumpers

DUSCC Register Bit Location	J31		J27	
	Out	In	Out	In
ICTSRA bit 0	1	0		
ICTSRA bit 1			1	0

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Table B-13. VMEbus Data Transfer Jumpers

VMEbus Data Transfer Type	J5	J8	Address Modifier
Extended, Supervisory	OUT	OUT	0DH
Standard, Supervisory	OUT	IN	3DH
Extended, Non-privileged or Supervisory	IN	OUT	09H or 0DH
Standard, Non-privileged or Supervisory	IN	IN	39H or 3DH

Table B-14. Bus Timeouts

Board Speed	BERR* will not be asserted before	Typical Timeout	BERR* will be asserted after
25 MHz	40.32 uS	40.96 uS	41.60 uS
40 Mhz	25.20 uS	25.60 uS	26.00 uS

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Table B-15. Devices Parameters According to Wait States, Banks 1 and 2, 25 MHz

RAM Device Parameter	Must be	Bank 1 SRAM Wait States		Bank 2 EPROM Wait States			
		1	2	1	2	3	4
t_{CO}	≤	30	70	N/A	N/A	N/A	N/A
t_{AA}	≤	38	78	70	110	150	190
t_{OE}	≤	13	53	N/A	N/A	N/A	N/A
t_{OLZ}	≥	0	0	N/A	N/A	N/A	N/A
t_{OHZ}	≤	33	33	N/A	N/A	N/A	N/A
t_{RC}	≤	80	120	120	160	200	240
t_{AS}	≤	42	42	N/A	N/A	N/A	N/A
t_{AW}	≤	83	83	N/A	N/A	N/A	N/A
t_{CW}	≤	76	76	N/A	N/A	N/A	N/A
t_{WP}	≤	40	40	N/A	N/A	N/A	N/A
t_{WR}	≤	8	8	N/A	N/A	N/A	N/A
t_{DH}	≤	11	11	N/A	N/A	N/A	N/A
t_{DW}	≤	42	42	N/A	N/A	N/A	N/A
t_{WC}	≤	120	120	N/A	N/A	N/A	N/A

For a definition of the parameters, see Figures B-1 and B-2 on pages B-14 and B-15.

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Table B-16. Devices Parameters According to Wait States, Banks 1 and 2, 40 MHz

RAM Device Parameter		Bank 1 SRAM Wait States		Bank 2 EPROM Wait States			
Must be		1	2	1	2	3	4
t_{CO}	≤	15	40	N/A	N/A	N/A	N/A
t_{AA}	≤	22	47	40	65	90	115
t_{OE}	≤	7	32	N/A	N/A	N/A	N/A
t_{OLZ}	≥	0	0	N/A	N/A	N/A	N/A
t_{OHZ}	≤	18	18	N/A	N/A	N/A	N/A
t_{RC}	≤	50	75	75	100	125	150
t_{AS}	≤	25	25	N/A	N/A	N/A	N/A
t_{AW}	≤	50	50	N/A	N/A	N/A	N/A
t_{CW}	≤	43	43	N/A	N/A	N/A	N/A
t_{WP}	≤	25	25	N/A	N/A	N/A	N/A
t_{WR}	≤	5	5	N/A	N/A	N/A	N/A
t_{DH}	≤	7	7	N/A	N/A	N/A	N/A
t_{DW}	≤	25	25	N/A	N/A	N/A	N/A
t_{WC}	≤	75	75	N/A	N/A	N/A	N/A

For a definition of the parameters, see Figures B-1 and B-2 on pages B-14 and B-15.

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Table B-17. Devices Parameters According to Wait States, Bank 3, 25 MHz

RAM Device Parameter Must be		Wait States						
		2	3	4	5	6	7	8
t_{CO}	≤	N/A	N/A	N/A	N/A	N/A	N/A	N/A
t_{AA}	≤	104	144	184	224	264	305	344
t_{OE}	≤	65	105	145	185	225	265	305
t_{OLZ}	≥	0	0	0	0	0	0	0
t_{OHZ}	≤	50	50	50	50	50	50	50
t_{RC}	≤	160	200	240	280	320	360	400
t_{AS}	≤	27	27	27	27	27	27	27
t_{AW}	≤	113	153	193	233	273	313	353
t_{CW}	≤	N/A	N/A	N/A	N/A	N/A	N/A	N/A
t_{WP}	≤	80	120	160	200	240	280	320
t_{WR}	≤	15	15	15	15	15	15	15
t_{DH}	≤	17	17	17	17	17	17	17
t_{DW}	≤	44	84	124	164	204	244	284
t_{WC}	≤	160	200	240	280	320	360	400

For a definition of the parameters, see Figures B-1 and B-2 on pages B-14 and B-15.

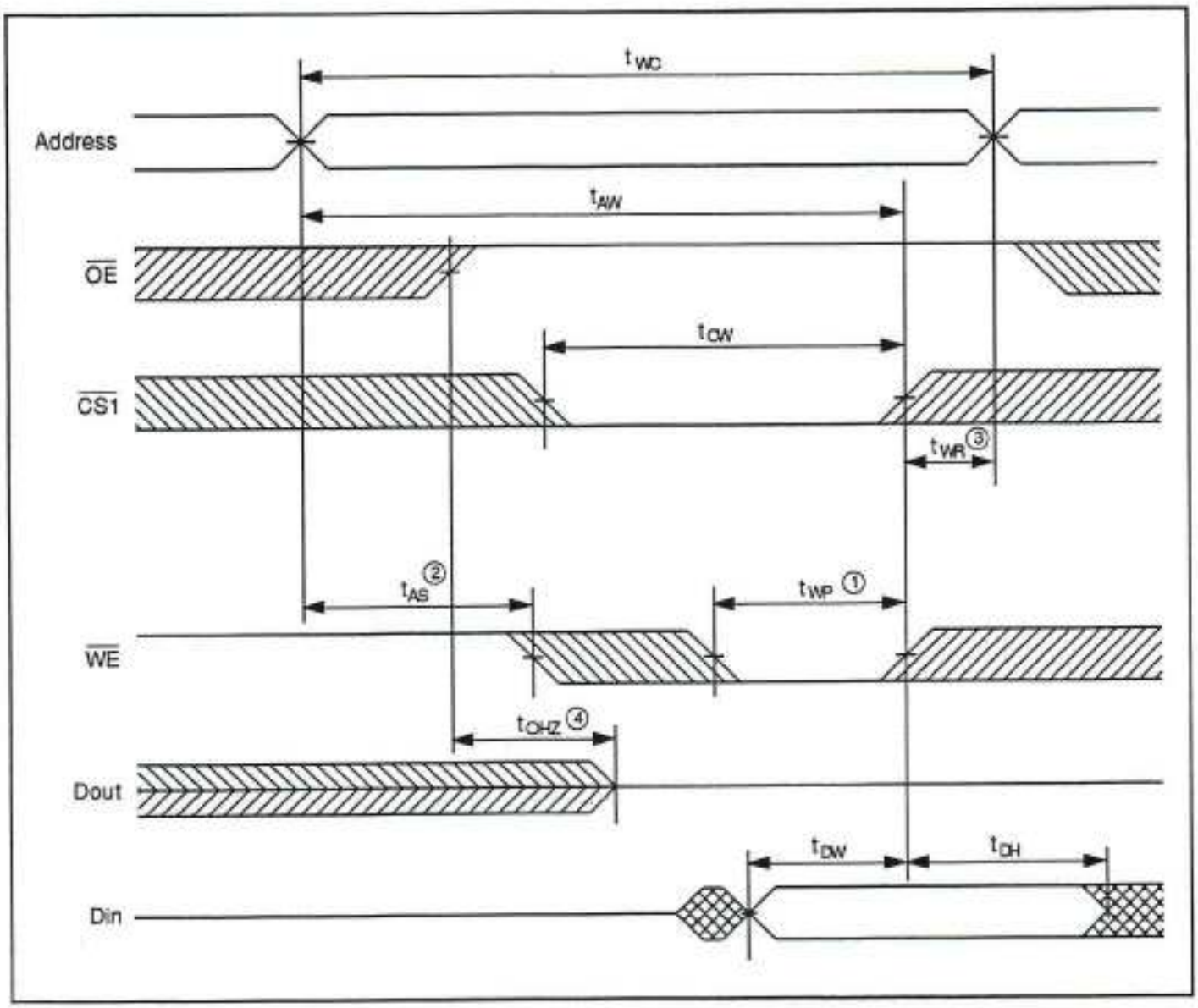
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Table B-18. Devices Parameters According to Wait States, Bank 3, 40 MHz

RAM Device Parameter Must be		Wait States						
		2	3	4	5	6	7	8
t_{CO}	≤	N/A	N/A	N/A	N/A	N/A	N/A	N/A
t_{AA}	≤	58	83	108	133	158	183	208
t_{OE}	≤	36	61	86	111	136	161	186
t_{OLZ}	≥	0	0	0	0	0	0	0
t_{OHZ}	≤	50	50	50	50	50	50	50
t_{RC}	≤	100	125	150	175	200	225	250
t_{AS}	≤	12	12	12	12	12	12	12
t_{AW}	≤	66	91	116	141	166	191	216
t_{CW}	≤	N/A	N/A	N/A	N/A	N/A	N/A	N/A
t_{WP}	≤	50	75	100	125	150	175	200
t_{WR}	≤	7	7	7	7	7	7	7
t_{DH}	≤	9	9	9	9	9	9	9
t_{DW}	≤	22	47	72	97	122	147	172
t_{WC}	≤	100	125	150	175	200	225	250

For a definition of the parameters, see Figures B-1 and B-2 on pages B-14 and B-15.

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① A write occurs during the overlap of a low $\overline{CS1}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

② t_{AS} is measured from the address valid to the beginning of write.

③ t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high to the end of the write cycle.

④ During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

Figure B-1. Write Timing Waveform

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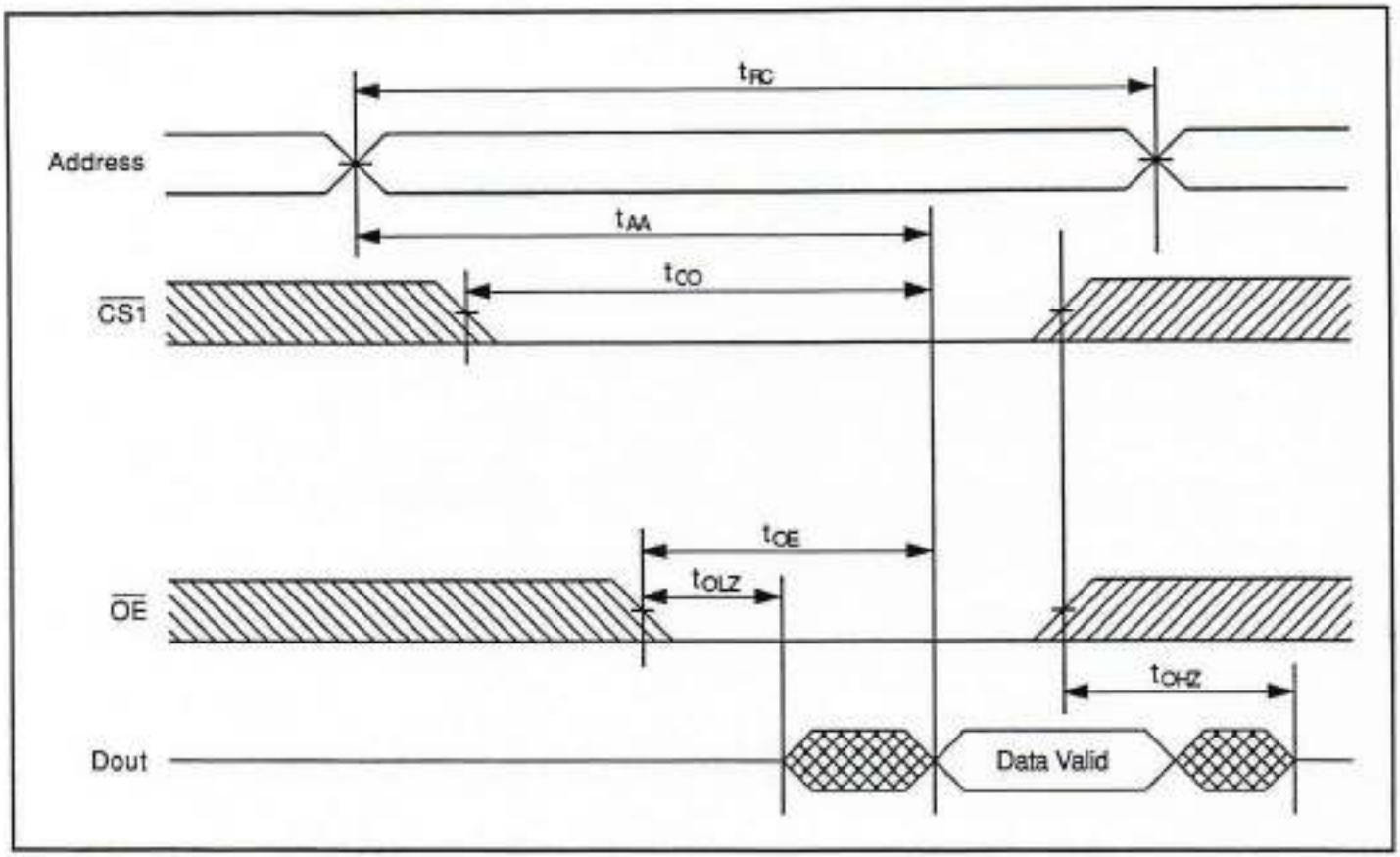
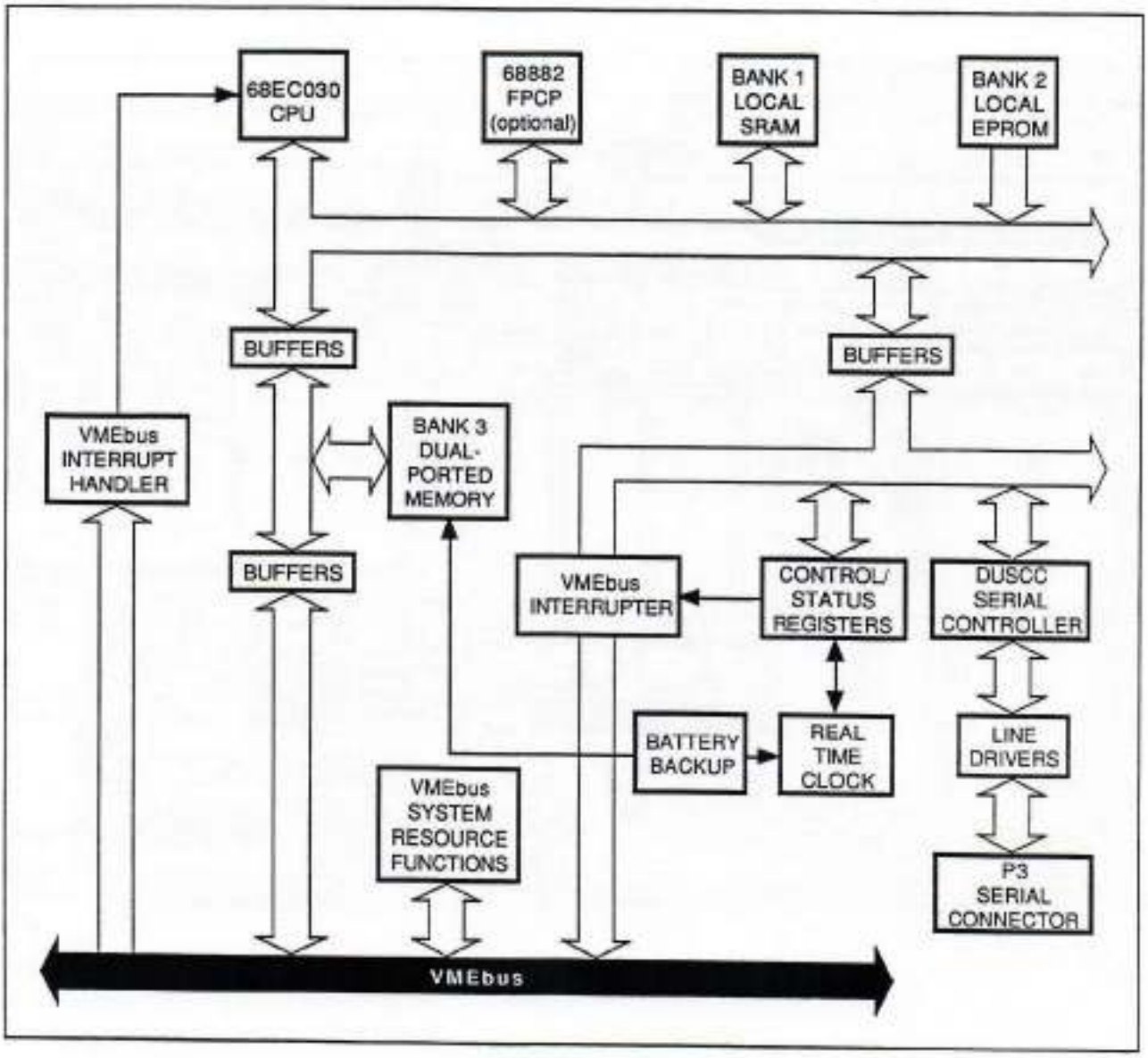


Figure B-2. Read Timing Waveform

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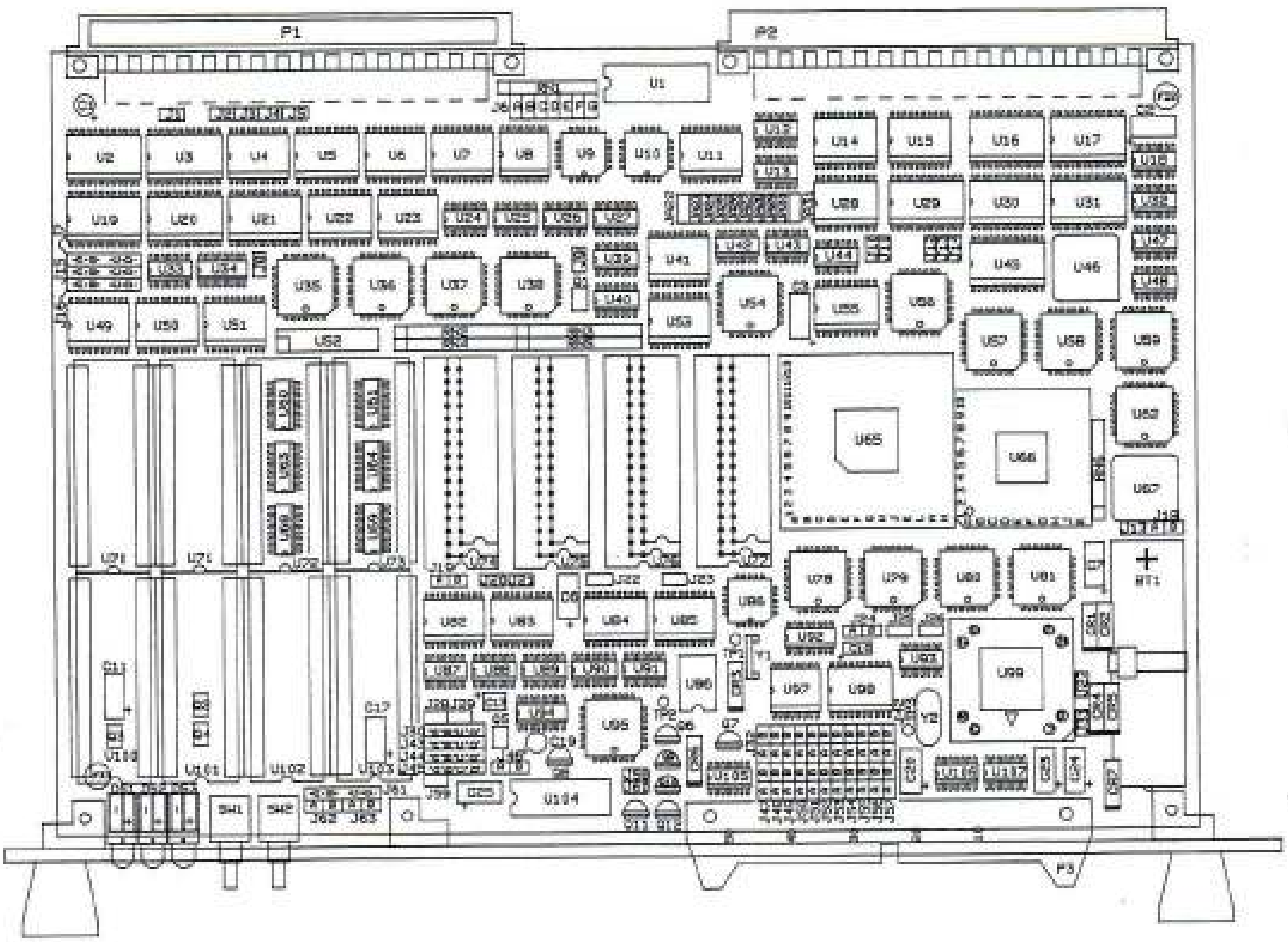
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Block Diagram



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Assembly Drawing



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Numeric

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