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XMC-6260-CC

Terminator 4 ASIC Based

XMC Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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RELATED PUBLICATIONS

The following manuals and part specifications provide the necessary information for in depth understanding of the XMC-6260-CC board.

Chelsio T4/T5 Unified Wire for Linux Installation and User's Guide	**http://service.chelsio.com**
Chelsio T4/T5 Unified Wire for Windows Installation and User Guide	**http://service.chelsio.com**

1.0 GENERAL INFORMATION

The XMC-6260-CC is a dual port XAUI 10 Gigabit Ethernet Unified Wire adapter XMC module. This conduction cooled module is optimized for cloud computing, HPC, virtualization, storage and other data center applications.

The heart of the XMC-6260-CC is Chelsio's Terminator 4 (T4) ASIC. The T4 ASIC provides the highest 10GbE performance available and dramatically lowers host-system CPU communications overhead with on-board hardware that off-loads TCP/IP, iSCSI, FCoE and iWARP RDMA processing from its host system. The XMC-6260-CC frees up host CPU cycles for useful applications. As a result, the system achieves increased bandwidth, lower latency, and lower power.

The XMC-6260-CC is an XMC module with eight high speed serial lanes allocated to the XMC P15 connector. These lanes are used as an 8-lane PCIe 2.0 interface.

Two high speed XAUI Ethernet interfaces are routed from the ASIC to a secondary XMC P16 connector. Each XAUI port is comprised of four lanes, each operating at 3.125Gbps for a total of 10Gb/s of data throughput in each direction.

The XMC-6260-CC has a 256kb EEPROM, 32Mb of serial flash memory, and 5Gb DDR3 SDRAM. The serial flash memory contains the ASIC's internal microprocessor firmware code. The EEPROM contains hardware and PCIe configuration information. On power up, the ASIC will copy the firmware from the flash into DRAM. The 5Gb of DDR3 will contain the data buffers and connection information to support up to 32K offloaded connections.

Ordering Information

The following table lists the orderable model and its description. XMC-6260-CC-LF is conduction-cooled with an operating temperature of -40°C to +85°C.

Table 1.1: *The XMC-6260-CC board is only available in a lead free version.*

MODEL	Description
XMC-6260-CC-LF	Lead Free, RoHS compliant

Key Features

An XMC-6260 block diagram, found at the end of this manual, illustrates the key features listed below.

- **Terminator 4 ASIC –** A high performance purpose-built protocol processor with a single processor data-flow pipelined architecture that delivers up to one million connections and simultaneously supports wire-speed, fully offloaded TCP/IP, UDP, FCoE, iSCSI and iWARP RDMA on a single unified wire.
- **DDR3 SDRAM –** Provides 64 Meg x 72-bit DDR3 SDRAM. The SDRAM is linked to the ASIC device for the storage of the ASIC's internal microprocessor firmware, data buffers and connection information to support up to 32k offloaded connections.
- **P15 High Speed Interface –** Eight high speed serial lanes are allocated to the XMC P15 connector. These lanes are used as an 8 lane PCIe Gen 2 interface to the T4 ASIC.
- **P16 High Speed Interface –** Eight high speed serial lanes are allocated to the XMC P16 connector. These lanes are used as a dual port XAUI interface to the T4 ASIC providing a full-duplex 10GbE interface.

Applications

- **Data-Center Networking**
  - Scale up servers and network-attached storage (NAS) systems
  - Link servers in multiple facilities to synchronize data centers
  - Consolidate local area networks (LAN), storage area networks (SAN) and cluster networks

- **Cloud Computing**
  - Virtualization features to maximize cloud scaling and utilization
  - Runs InfiniBand, Fibre Channel apps unmodified on internet
  - Cloud ready functional and management features
  - Quality of Service (QoS) and Traffic management
- **Networked Storage**
  - Enable high performance NAS systems and Ethernet-based IP SANs
  - Develop shared-storage systems providing both file- and block-level services
- **High Performance Computing**
  - Very low latency Ethernet
  - Increase cluster fabric bandwidth
  - Deploy Ethernet-only networking for cluster fabric, LAN and SAN

Hardware Requirements

The XMC-6260-CC supports architectures with PCIE (x4, x8, x16) gen 2 slots. Note that running a 10Gb adapter on a PCI x4 slot is not recommended as performance will be significantly reduced by the limitations of PCI. PCIe Gen 2 is also backwards compatible with Gen 1; however, the use of Gen 1 will also result in significantly reduced performance.

Software Requirements

The XMC-6260-CC has been developed to run on 64-bit Linux based platforms as well as 64-bit Windows systems and therefore it is a base requirement for running the driver. To know more about the complete list of operating systems supported by each driver, please refer to the driver's README information available from Chelsio's website at http://service.chelsio.com.

MAC Addresses

A MAC ID has been assigned to each of the two XAUI ports on the XMC-6260-CC. The base address has been listed on a label on the bottom side of the board. The following MAC address will be the next increment of 8. For example, if the base MAC ID is 00:01:C3:00:7F:5A, the other MAC ID is 00:01:C3:00:7F:62.

2.0 PREPARATION FOR USE

Unpacking and Inspecting



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

Card Cage Considerations

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermo conduction must be provided to prevent a temperature rise above the maximum operating temperature.

Board Installation

Remove power from the system before installing board, cables, termination panels, and field wiring.

P15 Primary XMC Connector

The P15 primary XMC connector connects directly to the T4 ASIC via eight lanes of Gen 2 PCI Express. The connector pin out, complies with the ANSI/VITA 42.3-2006 pin definitions. Note that the XMC-6280 does not support wakeup functionality and does not have a 3.3V aux line.

This XMC connector is a 114-pin Samtec ASP-103614-05 connector. The connector complies with the ANSI/VITA 42.3-2006.

P16 Secondary XMC Connector

Table 2.4: *P16 XMC Connector pin definitions.*

	A	B	C	D	E	F
01	X2_TD0p	X2_TD0n	NC	X2_TD1p	X2_TD1n	NC
02	GND	GND	NC	GND	GND	NC
03	X2_TD2p	X2_TD2n	NC	X2_TD3p	X2_TD3n	NC
04	GND	GND	NC	GND	GND	NC
05	X3_TD0p	X3_TD0n	NC	X3_TD1p	X3_TD1n	NC
06	GND	GND	NC	GND	GND	NC
07	X3_TD2p	X3_TD2n	NC	X3_TD3p	X3_TD3n	NC
08	GND	GND	NC	GND	GND	NC
09	RFU*	RFU*	NC	RFU*	RFU*	NC
10	GND	GND	NC	GND	GND	NC
11	X2_RD0p	X2_RD0n	NC	X2_RD1p	X2_RD1n	NC
12	GND	GND	NC	GND	GND	NC
13	X2_RD2p	X2_RD2n	NC	X2_RD3p	X2_RD3n	NC
14	GND	GND	NC	GND	GND	NC
15	X3_RD0p	X3_RD0n	NC	X3_RD1p	X3_RD1n	NC
16	GND	GND	NC	GND	GND	NC
17	X3_RD2p	X3_RD2n	NC	X3_RD3p	X3_RD3n	NC
18	GND	GND	NC	GND	GND	NC
19	RFU*	RFU*	NC	RFU*	RFU*	NC

*These pins are reserved for future use by the VITA 42.6 XMC 10 Gigabit Ethernet 4-lane Protocol Layer Standard.

X(2:3)_RD[0:3]. Link 2 and 3 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data from the carrier over Link 2 and 3. These signals tolerate EIA-644 signal levels.

X(2:3)_TD[0:3]. Link 2 and 3 Differential Transmit. These signals are used by the XMC to transmit high-speed protocol-specific data from the carrier over Link 2 and 3. These signals tolerate EIA-644 signal levels.

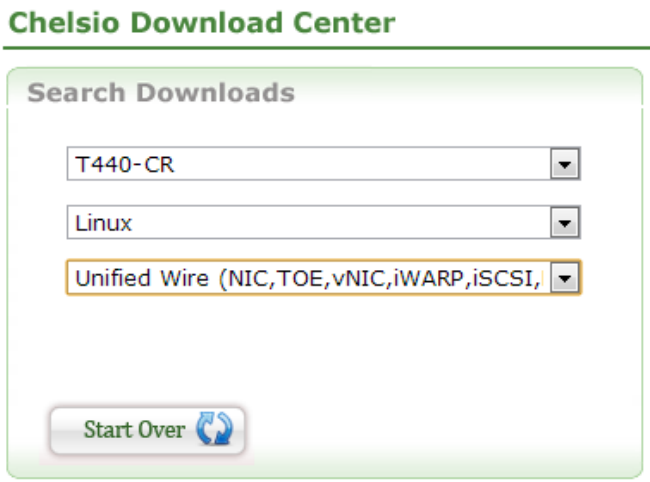
Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

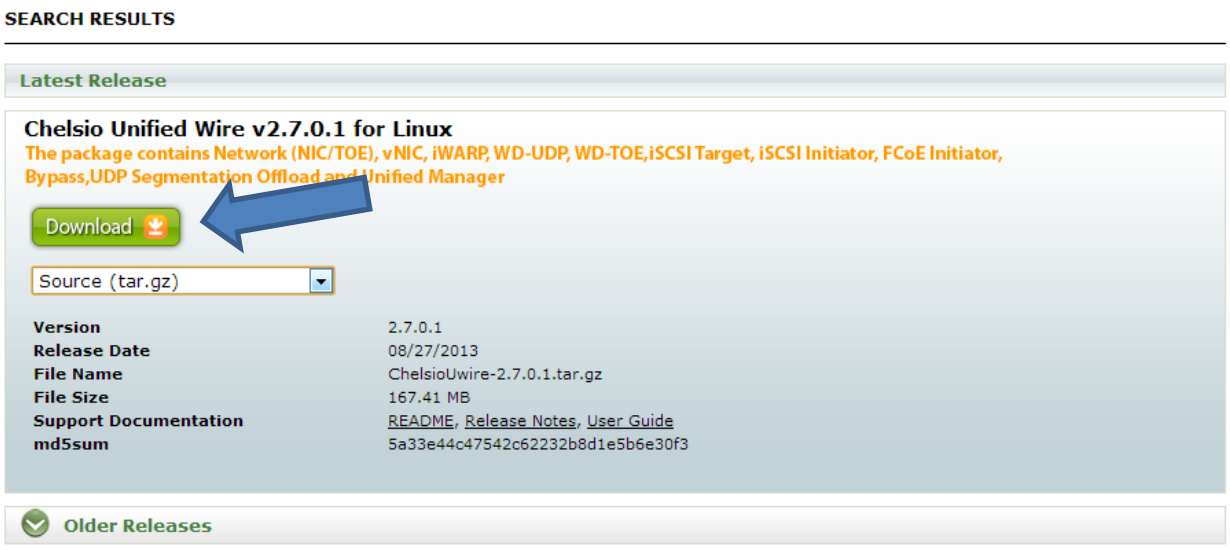
3.0 SOFTWARE/DRIVER INFORMATION

Software/Driver Download from Linux Source Tarball

1. Go to service.chelsio.com and search the downloads as shown below.



2. In the **SEARCH RESULTS** choose the source tarball.



3. Read and accept the Chelsio End User License Agreement.



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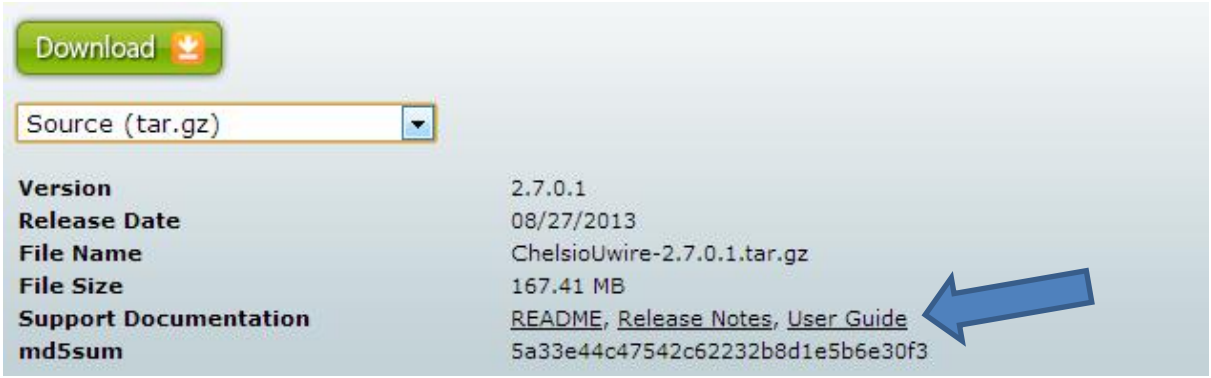
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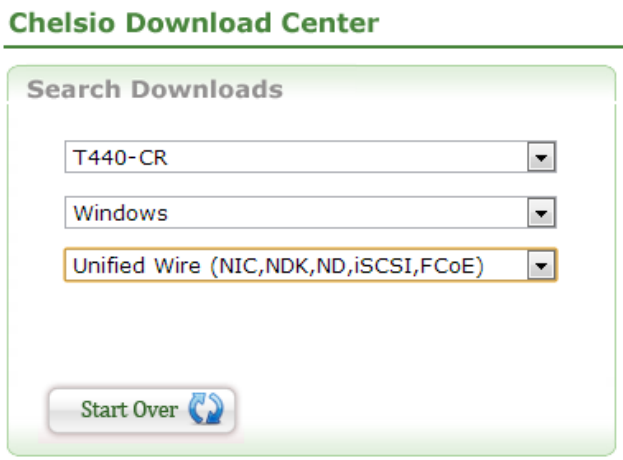
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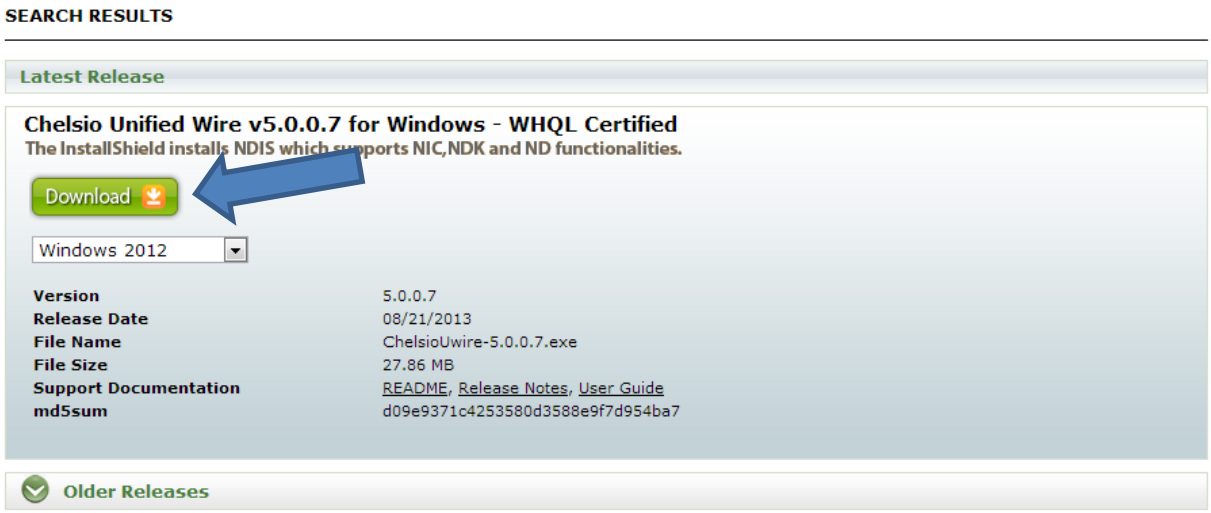


Software/Driver Download for Windows Operating Systems

1. Go to http://service.chelsio.com and search the downloads as shown below.



2. In the **SEARCH RESULTS** select the desired release based on operating system and functionality. For example, this release is for Windows Server 2012 and supports NIC, NDK and ND functionalities. Click on **Older Releases** to view older releases. Click **Download** to download the driver.



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4.0 THEORY OF OPERATION

This section contains information regarding the design of the board. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the XMC-6260-CC Block Diagram, shown below, as you review this material.

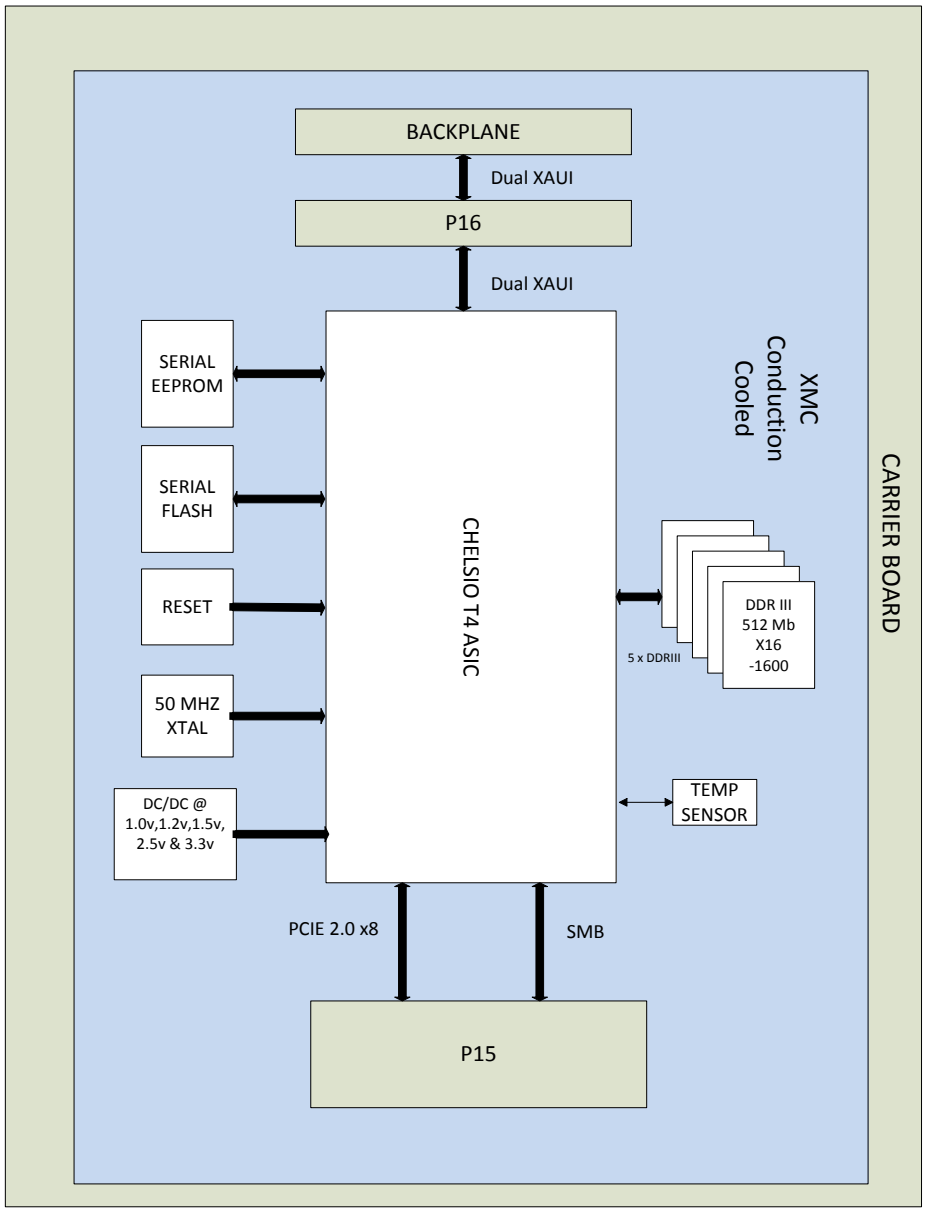


Figure 4.1: XMC-6260-CC Block Diagram

PCIE INTERFACE LOGIC

The XMC-6260-CC host interface is through PCI Express 2.0 which provides a 5Gbps interface to the carrier/CPU board. The PCIe interface supports 8 physical functions (PF). SR-IOV is supported on 4 PF with 128 virtual functions (VF). It supports x1, x2, x4 and x8 link widths. Maximum payload sizes and memory read request sizes of 128B to 2KB are supported, with up to 128 outstanding PCIe reads.

Dual XAUI Interface

The board contains two XAUI ports routed from the T4 ASIC's integrated full-duplex Ethernet MACs directly to the P16 XMC connector. Each XAUI port is comprised of 4 lanes, each operating at a speed of 3.125Gbps. With 8b/10b encoding, each XAUI port provides 10Gbps throughput in each direction. These XAUI links correlate with links 2 and 3 of the VITA 42.6 specification.

DDR3

There is a 64 Meg x 72-bit of DDR3 memory onboard for the purpose of storing connection states and buffers for up to 32K offloaded connections. Five DDR3 memory devices are used to form a 72-bit data bus. Each of the devices are 64 Meg x 16 bit (1Gb) in size.

Clock Generation

There is one onboard 50MHz XTAL providing the core clock to the T4 ASIC. This XTAL is all that is needed in order for the ASIC to internally produce the necessary clocks needed for operation.

Serial EEPROM

There is a 256Kb Atmel SPI Serial EEPROM which contains all the hardware configuration including things like pll multipliers and PCIe information. It also contains information on how to configure the firmware for the T4 ASIC including things like how to set up the DDR3 and the number of ports available on the card.

This Serial EEPROM is not intended to be reprogrammed by the customer, and doing so could cause a device failure.

Serial Flash

The 32 Mb serial flash contains all the ASIC's internal microprocessor firmware code. Once the ASIC and microprocessor boots itself, the EEPROM is read first to get configuration information. Then the ASIC copies the firmware from the flash to DDR3 memory and runs everything from there.

This Serial EEPROM is not intended to be reprogrammed by the customer, and doing so could cause a failure in the device. The driver will auto-load the firmware if an update is required. The kernel must be configured to enable userspace firmware loading support:

Device Drivers → Generic Driver Options → Userspace firmware loading support

Temperature Sensor

A Texas Instruments TMP421 temperature sensor is connected to the thermal pins of the Terminator 4 ASIC to monitor the junction temperature of the ASIC and also the local temperature of the temperature senor. The ASIC has been designed to shut down at junction temperatures above 115 degrees Celsius. This is in an attempt to save the chip from being damaged and is not a guarantee that it will not be damaged.

Power System Devices

The power to the XMC-6260-CC is taken from the XMC P15 connector VPWR_5/12 pins. The VPWR_5/12 power is the V in voltage to the three LTM4602 devices U16, U17 and U18 and also to the LTM4601 devices U19 and U21. The LTM4602 devices output +2.5V, +1.5V and +1.2V while the LTM4601 devices output +1.0V. The +1.5V supply is input to the TPS51200 device U15 to output +0.75V for DDR3 termination.

Figure 4.2: Power Distribution

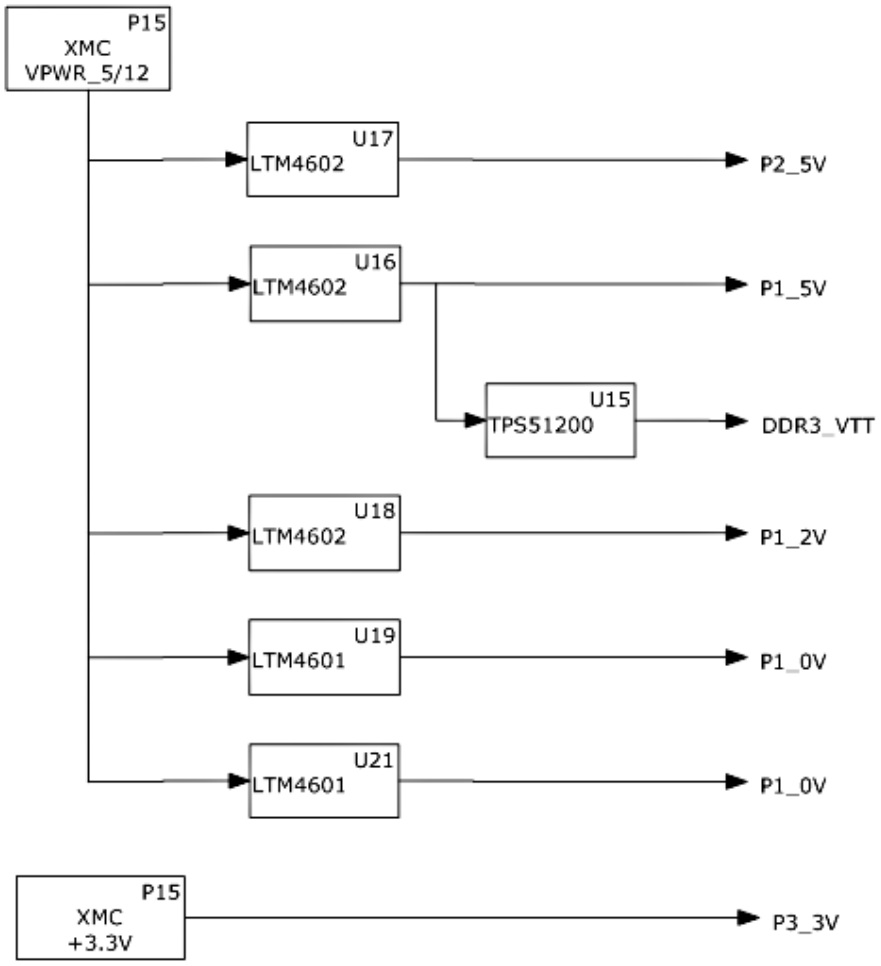


Figure 4.3: Power System

Device	Reference Designator	Description	Power Rail Name	Power Rail Current
LTM4602	U17	ASIC, PCIe, Ethernet	P2_5V	6.0A
LTM4602	U16	ASIC, DDR3, PCIe, Ethernet	P1_5V	6.0A
TPS51200	U15	DDR3 Termination	DDR3_VTT	+/-2A
LTM4602	U18	ASIC, Ethernet	P1_2V	6.0A
LTM4601	U19	ASIC, PCIe,	P1_0V	12A
LTM4601	U21	ASIC, PCIe	P1_0V	12A

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested before shipment.

Service and Repair Assistance

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

Preliminary Service Procedure

CAUTION: **POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS**

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Height	13.5 mm (0.531 in)
Stacking Height	10.0 mm (0.394 in)
Depth	143.75 mm (5.866 in)
Width	74.0 mm (2.913 in)
Board Thickness	1.57 mm (0.062 in)
Unit Weight:	3.9316oz (111.46g)

POWER REQUIREMENTS

Power will vary dependent on the application.

3.3 VDC (±5%)	Typical 50 mA	Max. 100 mA
+12/5 VDC (±5%)	Typical 1 A	Max. 1.5 A
-12 VDC (±5%)	0mA	

On Board 1.0V Power to T4 ASIC	Current Rating (available for the T4 ASIC)
1.0V (±5%)	12A typical 24A maximum

ENVIRONMENTAL

Operating Temperature

Model	*Operating Temperature*
XMC-6260-CC-LF	***-40℃ to 85℃***

Relative Humidity: 5-95% Non-Condensing.

Storage Temperature: -55°C to 100°C.

Non-Isolated: PCIe bus and field commons have a direct electrical connection.

Radiated Field Immunity (RFI): Complies with IEC 61000-4-3 with no register upsets.

Conducted R F Immunity (CRFI): Complies with IEC 61000-4-6 with no register upsets.

Surge Immunity: Not required for signal I/O per IEC 61000-4-5.

Electric Fast Transient (EFT) Immunity: Complies with IEC 61000-4-4 Level 3 (1.0KV at field I/O terminals).

Electrostatic Discharge (ESD) Immunity: Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) Level 2 (4KV enclosure port contact discharge).

Radiated Emissions: Meets or exceeds European Norm 61000-6-3:2007 for class A equipment. Shielded cable with I/O connections in shielded enclosure is required to meet compliance.

Terminator 4 ASIC (U1)

The Chelsio fourth generation Terminator 4 ASIC is a 27x27mm 675-pin FCBGA package with a 8-lane PCIe gen2 interface to the server and two XAUI link MAC interfaces on the network side.

P15 XMC Connector

114 pin Samtec ASP-103614-05 connector complies with ANSI/VITA 42.3-2006

P15 is the primary XMC connector

8 Gigabit differential pairs are provided for use as 8 lane PCIe Gen 2.0.

System Management (XMC provides hardware definition information read by the external controller using IPMI commands and I2C serial bus transactions.)

3.3V power (4 pins at 1A/pin)

Variable power (5V or 12V) (8 pins at 1A/pin)

P16 XMC Connector

114 pin Samtec ASP-103614-05 connector complies with ANSI/VITA 42.6-2009 XMC 10 Gigabit Ethernet 4-Lane Protocol Layer standards.

P16 is the secondary XMC connector

Dual XAUI links are provided, each link comprised of 4 lanes running at 3.125Gb/s each for a combined data throughput of 10Gb/s per link.

Board Crystal

Board Crystal: 50MHz (U22)

Frequency Stability: ± 0.00500% or 50ppm

DDR3 Memory

64 Meg x 16-bit Micron Device MT41J64M16JT-125:G uses a double data rate architecture.

Five MT41J64M16JT-125:G memory devices (U8, U9, U10, U11 and U14) are used to form a 72-bit data bus to the T4 ASIC.

The DDR3 is used to store the T4 microprocessor firmware and also for data buffers and connection information when offload is enabled.

256Kb EEPROM

256Kb (32,768 x 8) Atmel SPI Serial EEPROM contains hardware configuration and PCIe configuration information. It also contains the T4 ASIC firmware configuration data.

32Mb Flash

32Mb (4Mb x 8) Micron M25P32 Serial Flash contains the T4's internal microprocessor firmware code.

Temperature Sensor

A Texas Instruments **TMP421** is supplied as a way to monitor the temperature of the ASIC and is connected to the thermal pins of the Chelsio T4 ASIC.

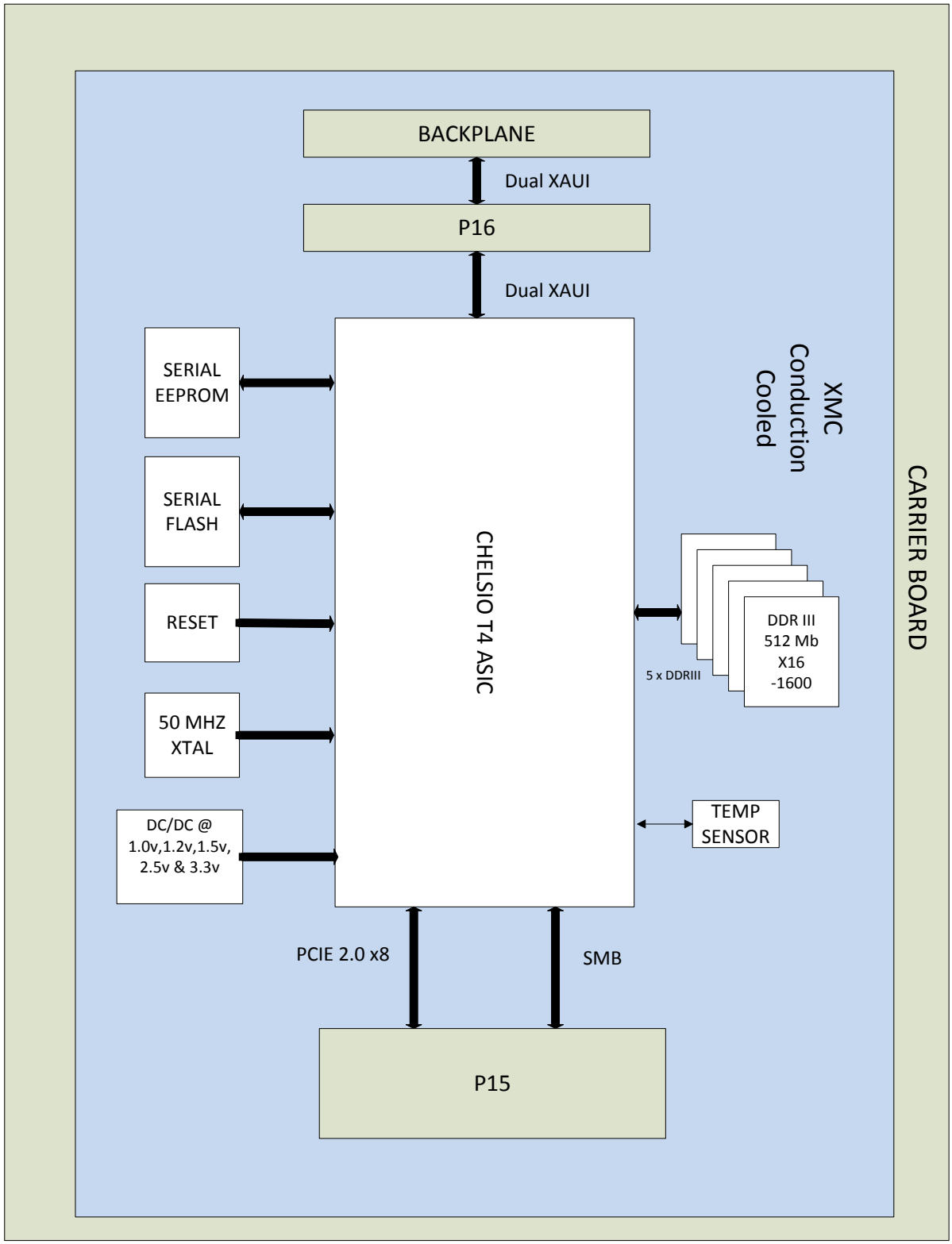
PCIe Bus Interface

XMC Compatibility: Conforms to PCI Express Base Specification v2.0, and XMC Specification, P1386.1

ANSI/VITA 42.0: Complies with XMC module mechanicals and connectors

ANSI/VITA 42.3: XMC module with PCI Express Interface

XMC-6260-CC Block Diagram



Certificate of Volatility

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
XMC-6260-LF</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)
SDRAM</td><td>Size:
64 Meg x
72-bit</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Data storage for ASIC</td><td colspan="2">Process to Sanitize:
Power Down</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)
Flash</td><td>Size:
32Mbit</td><td>User Modifiable
□ Yes
■ No</td><td>Function:
Storage of ASIC Firmware</td><td colspan="2">Process to Sanitize:
Not Applicable</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)
EEPROM</td><td>Size:
246Kbit</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Storage of PCIe, hardware and ASIC configuration data</td><td colspan="2">Process to Sanitize:
Clear EEPROM memory by writing zeros to all sectors of the EERPOM</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Joseph Primeau</td><td>Title:
Dir. of Sales and Marketing</td><td>Email:
jprimeau@acromag.com</td><td>Office Phone:
248-295-0823</td><td colspan="2">Office Fax:
248-624-9234</td></tr>
</table>

Revision History

Release Date	Version	EGR/DOC	Description of Revision
1-MAY-14	A	EZ/EZ	Initial Acromag release.
2 Oct 15	B	CAB/MJO	Remove Leaded Option for RoHS Compliance.

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