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XVME-6500

Intel® 4th Generation Core

Single-Slot VMEbus CPU Module



USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This user manual was written for technically qualified personnel who will be working with systems incorporating the XVME-6500 CPU. It is not intended for a general, non-technical audience that is unfamiliar with VMEbus devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

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1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 Product Summary

The XVME-6500 is a CPU module that uses an Intel® 4th Generation Core Processor (Haswell) 6U VME64x VMEbus form factor. It is available in an air-cooled model only. An extended temperature air-cooled model is also available for operating in a -40°C to +75°C range.

The standard module has two DDR3L ECC SODIMMs, for a total of 16GB of DDR3 memory. The standard model The SODIMMs are firmly attached to the module with screws and surrounded by heat sink material to provide a mechanically and thermally robust mechanism.

A large amount of I/O is available, as summarized in the "Key Features and Benefits" section below.

There are two PMC/XMC sites available on the module. These can be used as 2 XMC, 2 PMC, or one of each type. All 64 pins of rear I/O from the PMC/XMC module's P4 connector are routed to the XVME-6500's P0 and P2 connectors. Note the P0 connector is optional and also carries 2 Gigabit Ethernet connections.

Two special build options are offered for the P0 and P2 I/O. Instead of the 64 pins of rear I/O from the lower site XMC module's P4 connector, the P0 connector can instead carry I/O from the XMC module's P6 connector. An option is also available to have the P2 connector's I/O compatible with the XVME-6300 by giving up some of the PMC/XMC I/O normally available on the P2 connector. Please consult the factory for these options.

In lieu of one PMC/XMC module, the optional XBRD-9060 I/O Expander module may be installed to give more I/O on the front panel, as well as 2 SSD mSATA drives.

The module uses a FPGA-based VME bridge on a dedicated PCIe bus to minimize VMEbus transfer times. The module will function in either a 3-row (with reduced I/O) or 5-row VMEbus backplane, with or without a 3.3V backplane power supply (reduced 5V & 3.3V power is available to the PMC/XMC sites when a 5V-only power supply is available from the backplane).

The optional XVME-9640 Rear-Transition Module is available to give easy access to all of the P2 connector's I/O signals.

A two digit LED display is available for Power ON Self-Test (POST) codes, should a problem arise during the boot operation. This display is available for application software user codes after POST to aid in software debugging.

A 26-pin XDP debug connector is also available for connecting compatible emulator tools directly to the CPU. *For more information see Intel publication 479493, Shark Bay and Denlow Platforms Debug Port Design Guide*.

1.4 Related Material

The following manuals and part specifications provide the necessary information for in-depth understanding of the XVME-6500 module.

- ANSI/VITA 1.1-1991 (R2003), *VME64 Extensions.* http://vita.com
- ANSI/VITA 1.5-2003 (R2009), *2eSST.* http://vita.com
- ANSI/VITA 39-2003, *PCI-X Auxiliary Standard for PMCs and Processor PMCs.* http://vita.com
- ANSI/VITA 42, *XMC.* http://vita.com
- *The APTIO Haswell Core BIOS Manual For Acromag Products (8501026).*
- Intel® document No. 328901, *Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2,* Rev: 002, September, 2013. http://www.intel.com/content/www/us/en/processors/core/CoreTechnicalResources.html
- *ALTHEA 7910 Application Programming Interface* Software API for PCI Express to VME Interface.

1.5 Ordering Information

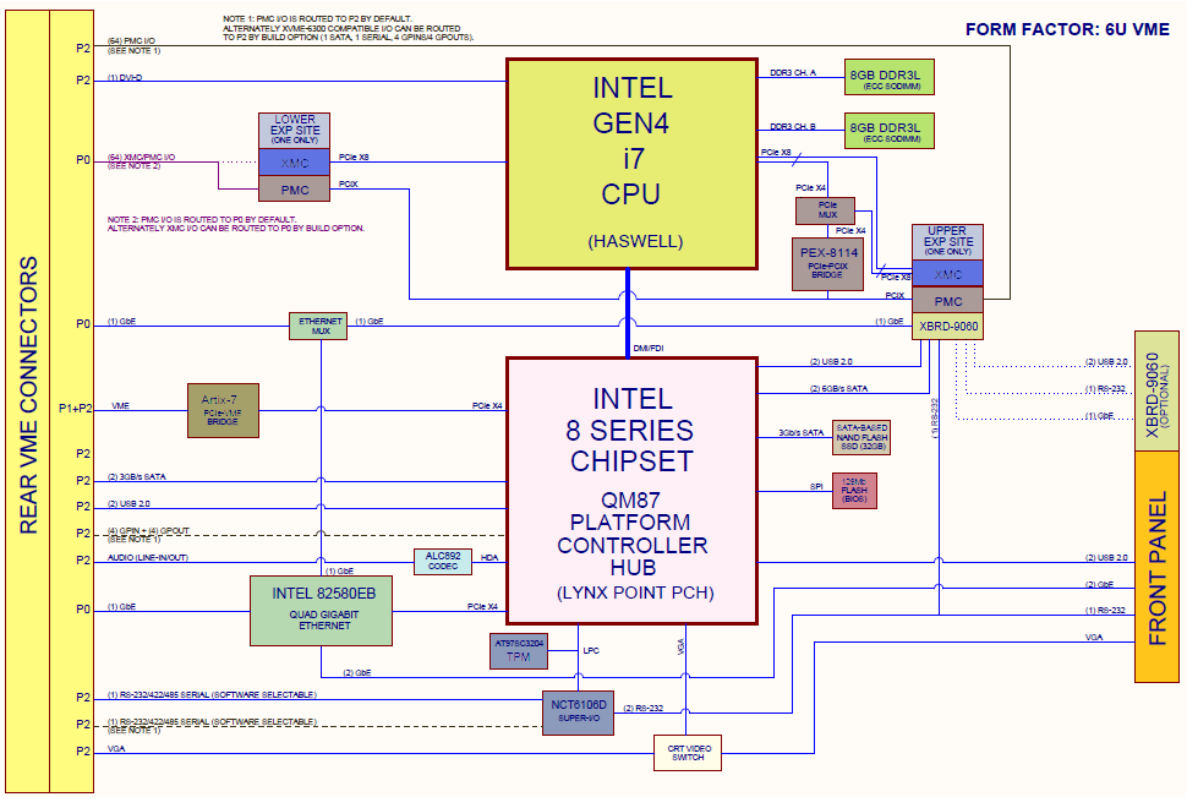
When ordering the XVME-651X-116YZ-LF VMEbus CPU module, please select from and specify the available options (X, Y and Z) as defined below (such as XVME-6510-1160-LF, XVME-6510-1161E-LF, XVME-6511-1160-LF, XVME-6511-1162E-LF, etc.):

- Select the rear I/O to P0 option (X):
  - ✓ 0: PMC P4 rear I/O
  - ✓ 1: XMC P6 rear I/O
- Select the Connector Option (Y);
  - ✓ 0: with P0
  - ✓ 1: without P0
  - ✓ 2: with P0, battery-less option
  - ✓ 3: without P0. Battery-less option
- Select the operating environment (temperature) option (Z):
  - ✓ Blank: Standard temperature operation
    0°C to 70°C
  - ✓ E: Extended temperature operation
    -40°C to 75°C

1.6 Key Features and Benefits

The XVME-6500 block diagram shown in Fig. 1.6.a illustrates the key components and features that are summarized on the following pages.

Fig. 1.6.a: XVME-6500 Block Diagram



1.6.1 Intel® 4th Gen (Haswell) Core CPU

This 2.4GHz quad-core i7, 64-bit, 22-nanometer (Haswell) CPU with integrated GT2 graphics contains direct interfaces for DDR3L, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the QM87 Platform Control Hub (PCH).

- **DDR3L SDRAM –** Two SODIMM sockets support up to 16GB of DDR3L ECC at 1600MHz. Dual-channel mode is used with the two SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe x8 (2) –** Traditionally used for external graphics, but on the XVME-6500 supports any PMC/XMC devices. One of the connections is muxed with a PEX8114 PCIe > PCI-X bridge for PMC vs. direct XMC connection. This bridge drives both PMC sites when enabled, but the lower site may still contain an XMC module even if the PMC bridge is enabled.
- **DVI-D –** This digital display interface supports connection of both, DVI-D, or HDMI display devices.
- **Programmable CPU power limits –** By simply programming a lower power

limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

1.6.2 Intel QM87 Chipset (Lynx Point) PCH

The Intel 8 Series QM87 (Lynx Point) PCH provides extensive I/O support, as listed below:

- **PCIe x4 (2)** – There are two PCIe ports of x4 width. The first is connected to the FPGA-based VME Bridge. The other is connected to the Intel 82580EB Quad Gigabit Ethernet controller.
- **SATA II (2)** – There are two SATA ports that operate up to 3Gb/sec connected to the VME P2 connector.
- **SATA III (2)** – There are two SATA ports that operate up to 6Gb/sec connected to the Expansion Site connector for the optional XBRD-9060
- **Bootable on-board SSD Flash** – 32GB of soldered-down on-board SSD Flash is standard on all units. The device can be write protected with an option in the BIOS.
- **USB 2.0 (6)** – There are two ports connected to the VME P2 connector and two ports connected to the front panel's 26-pin connector that function at USB 2.0 or USB 1.1 speeds. There are an additional two ports available on the Expansion Site connector for the optional XBRD-9060.
- **VGA** – An analog VGA port is available, including DDC clock and data, at either the VME P2 connector or the front panel's 26-pin connector. Only one connection may be used at a time and should auto switch when a monitor is plugged in to either port. Override switches are available on SW2.
- **LPC –** The Low Pin-count Bus is connected to both the NCT6106D Super-I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **SPI –** The Serial Peripheral Interface is used for the onboard boot flash.
- **HDA Audio** – The HDA audio port is connected to an ALC892 high definition audio codec. Analog stereo line-in and line-out ports are available on the VME P2 connector.
- **SMBUS** – This I2C-compatible System Management Bus has connections to the memory DIMMs, the XMC connectors, and also to an onboard EEPROM for module identification.

1.6.3 Intel 82580EB Quad Ethernet Controller

The Intel 82580EB Gigabit Ethernet Controller contains both the MAC and the physical layer. It provides 4 ports that auto-sense 10-Base-T, 100Base-T, and 1000Base-TX connections. Two of these are available on the front panel's RJ Point 5 connector. Two are available on the optional VME P0 connector, for use on a VITA 31.1 Switch-Fabric compliant backplane, or via the optional XVME-9640 RTM module. One of these P0 ports may instead be switched to the Expansion Site connector, making it available on the front panel via the XBRD-9060 I/O Expander module.

1.6.4 Nuvoton NCT6106D Super-I/O

The Nuvoton NCT6106D is an LPC device that provides temperature and voltage monitoring, Port 80 debug via 2 digit 7-segment display, and the following serial ports:

- One RS-232 only, including RTS, CTS, DTR, and DSR control lines. Available on the front panel's 26-pin connector.
- One RS-232/RS-422/RS-485 (software selectable). TX/RX signals only. Available on the VME P2 connector.
- One RS-232 only. TX/RX signals only. Routed to the Expansion Site connector to make the port available on the front panel via the optional XBRD-9060.

1.6.5 Atmel AT97SC3204 TPM

The Atmel AT97SC3204 is a fully integrated security module that implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

1.6.6 FPGA-based VME to PCI Express Bridge

The FPGA-based VME to PCIe bridge is a full VME64x Master/Slave interface with slot-1 functions and interrupt management. All VME64x data transactions (SBT, BLT, MBLT, 2eVME and 2eSST) on all common addressing space modes (A16, A24 and A32) along with a fully programmable hardware byte swapper function are supported. It has been successfully implemented and validated in VME SBCs since 2009 under Linux and VxWorks allowing the solution to meet high maturity and reliability levels required by the industry.

1.6.7 Expansion Sites

There are two expansion sites available on the XVME-6500, referred in this manual as the Upper Site and the Lower Site. The Upper Site is at the top of the XVME-6500 when installed vertically in a VME chassis. The Lower Site is in the middle of the board, adjacent to the CPU heatsink.

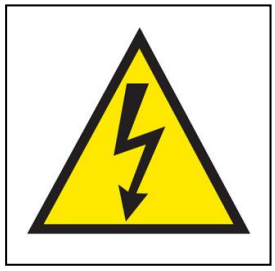
The Upper Site can be used for a PMC or XMC module, with the I/O from the J24 connector routed to the VME P2 connector. The Upper Site can instead be used with the optional XBRD-9060 I/O Expander module.

The Lower Site can be used for a PMC or XMC module, with the I/O from the J14 connector routed to the VME P0 connector, if installed. Alternatively, I/O from the J16 connector can be routed to the P0 connector.

Note: If one PMC and one XMC module are installed in the Expansion Sites, the PMC module must be installed in the Upper Site.

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installing into a Backplane

The XVME-6500 is a 6U, single-slot module. For proper cooling, the air-cooled models must only be installed into an air-cooled chassis.

The XVME-6500 modules are designed to comply with all physical and electrical VMEbus backplane specifications of VME64x.

The XVME-6500 is available both with and without a P0 connector. Without P0 would normally be required for a legacy system that contains a stiffener bar in that location.

In order to have access to some of the listed P2 I/O and to supply enough power for the i7-4700EQCPUit is recommended that a backplane with 5-row, 160-pin P1 and P2 connectors be used.

Note: *When used in a legacy system with 3-row, 96-pin P1 and P2 connectors, power available to the expansion sites will be severely limited and the programmable power limits on the CPU should be used.*

WARNING: ***Never install or remove any boards before turning off power to the bus and all related external power supplies.***

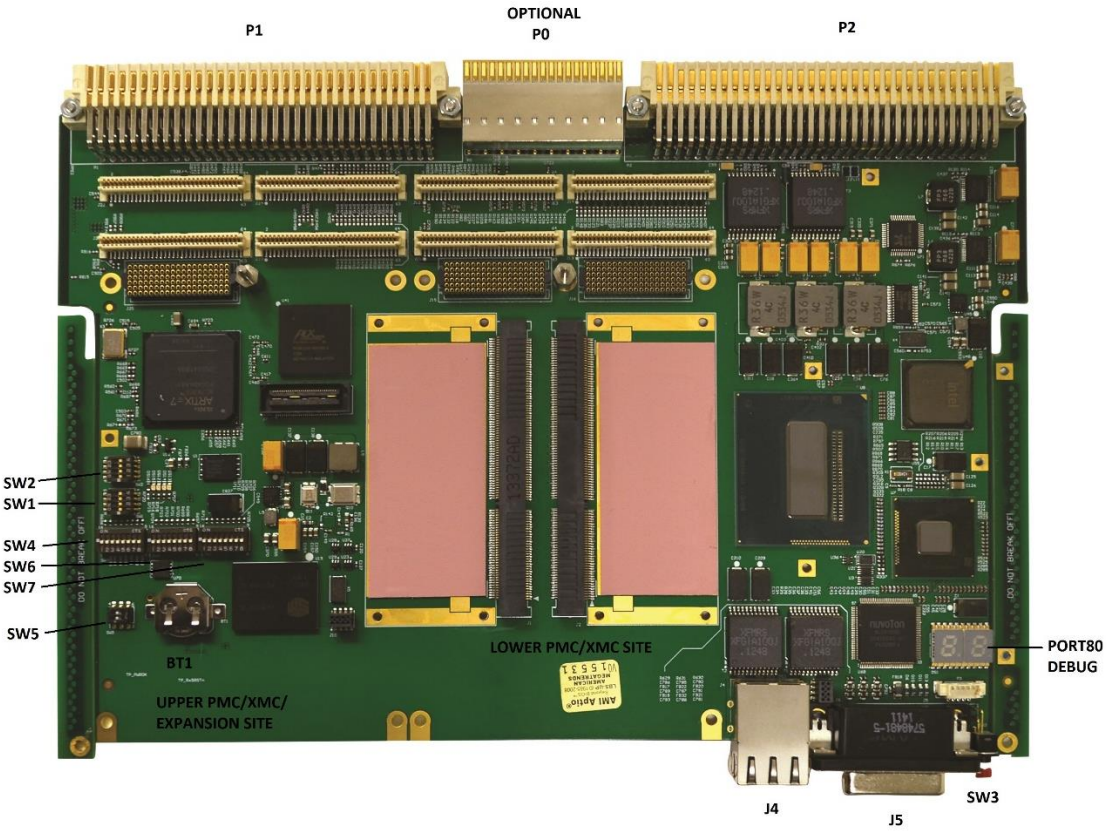
1. Disconnect all power supplies to the backplane and the card cage. Disconnect the power cable.
2. Make sure backplane connectors P1 and P2 are available.
3. Verify that all DIP switch settings are correct.
4. Verify that the card cage slot is clear and accessible.
5. Install the XVME-6500 in the card cage by centering the unit on the plastic guides in the slots (P1 connector facing up). Push the board slowly toward the rear of the chassis until the P1 and P2 connectors engage. The board should slide freely in the plastic guides.

WARNING: ***Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for damage or obstructions.***

6. Secure the module to the chassis by tightening the machine screws at the top and bottom of the board.
7. Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the XVME-6500 board, or on the XVME-9640 Rear Transition Module.

3.0 HARDWARE INFORMATION AND CONFIGURATION

Fig. 3.1.a: XVME-6500 Top View



3.1 Module Hardware Switch Configuration

3.1.1 Core Configuration Switch SW1

Table 3.1.a: Core Configuration Switch SW1

Table 3.1.a summarizes the functions, settings, and descriptions for dip switches SW1-1 thru SW1-4.

Core Configuration Switch SW1			
Position	**Function**	**Switch Setting**	**Description**
1	Front Panel Reset Button	OFF	No Pushbutton Reset
		ON (default)	Front Panel Reset Button Causes Local Reset
2	ORB GND	OFF (default)	ORB GND Isolated
		ON	ORB GND tied to digital GND
3	BIOS Recovery	OFF (default)	Normal Operation
		ON	Restore BIOS Defaults
4	Onboard 3.3V Regulator	OFF	Auto Enable Onboard 3.3V Regulator if Not on Backplane
		ON (default)	Force Onboard 3.3V Regulator On

SW1-1 is used to configure whether the front panel reset switch can be used to reset the XVME-6500 (and subsequently the whole VME chassis depending on SW4-6).

SW1-2 is used to isolate ORB GND (the front panel's chassis connection) from digital ground, if necessary to isolate ground loops.

SW1-3 is reserved and should be left in the OFF position for normal operation.

SW1-4 is used to configure the operation of the onboard 3.3V regulator. When the switch is OFF the onboard 3.3V regulator is automatically enabled whenever 3.3V is not detected on the backplane. Setting this switch to ON forces the onboard 3.3V regulator to be enabled always.

3.1.2 Core Configuration Switch SW2

Table 3.1.b summarizes the functions, settings, and descriptions for dip switches SW2-1 thru SW2-4.

Table 3.1.b: Core Configuration Switch SW2

Core Configuration Switch SW2			
Position	**Function**	**Switch Setting**	**Description**
1	PMC Bus Speed Override	OFF	100/50/25MHz
		ON (default)	133/66/33MHz
2	XMC Select Override	OFF (default)	Upper Site XMC/PMC Auto-Detect
		ON	Upper Site Force XMC
3:4	Monitor Auto-Detect Override	OFF:OFF	Force Rear VGA Port Enable
		OFF:ON	Force Front VGA Port Enable
		ON:OFF (default)	VGA Port Auto-Detect
		ON:ON	Force Front VGA port Enable

SW2-1 is used to override the automatic selection of the PMC bus speed. When the switch is on the bus speed is automatically selected at 133/66/33MHz. When the switch is off the speed is overridden as follows:

133MHz normal bus speed will slow down to 100MHz

66MHz normal bus speed will slow down to 50MHz

33MHz normal bus speed will slow down to 25MHz

Note that with two 133MHz PMC modules installed there may be instability unless the bus speed is slowed down to 100MHz, as recommended by VITA 39.

SW2-2 is used to override the automatic detection of PMC/XMC modules in the upper PMC/XMC site. If an installed XMC module is not automatically recognized, closing this switch will turn off the PMC bridge and force the connection to the XMC card instead of the bridge.

SW2-3 and 2-4 are used to override the automatic VGA monitor detection on the VGA ports. If a monitor connected to a port is not automatically recognized, setting the switches as shown will force a particular VGA port to be active.

3.1.3 VME Configuration Switch SW4

Table 3.1.c summarizes the functions, settings, and descriptions for dip switch SW4.

Table 3.1.c: VME Configuration Switch SW4

VME Configuration Switch SW4		
Position	**Function**	**Function Description**
1-2	VME_ SYSCON	*Sw.1 – Sw.2* OFF – OFF : Disable VME System Controller OFF – ON : Enable VME system Controller (default) ON – OFF : Enable in VME64x mode while GA = "00001" ON – ON : Enable Auto-ID mode by BGIN#3 detected low
3	SYSRESET_in _ENA	VME SYSRESETn assertion on VME backplane will cause a local reset (OFF by default)
4	VME64x_ AUTOID_ENA	Enable VME Auto Slot Identification Logic (ON by default)
5	PON_FSM_ DIS	Disable PON_FSM micro-sequencer (ON by default)
6	SYSRESET_ou t_ENA	A local reset will generate a VME SYSRESETn assertion on VME backplane (ON by default)
7	SPI_WR_ PROT	Enable Write Protect for SPI Flash EEPROM configuration (ON by default)
8	SPI_CFG_ ENA	Enable SPI Flash EEPROM configuration (ON by default)

SW4 is used to configure the VME system controller properties, as well as the reset behavior, start-up behavior and properties of the EEPROM which holds the FPGA firmware.

SW4-1 and SW4-2 are used to manually enable or disable the system controller functionality of the bridge. System controller can also be automatically enabled in 64x mode when the geographic address of the board is "00001," or slot 1. If both switches are on, Auto-ID mode is selected and system controller will be enabled if the BGIN#3 signal from the backplane is detected low at power-up.

If SW4-3 is on, a VME SYSRESETn assertion on the backplane will cause a local reset. Otherwise, the signal will be isolated from the backplane.

If a VME64x backplane is being used, SW4-4 can be used to enable Auto Slot Identification.

SW4-5 will disable the PON_FSM micro-sequencer. The micro-sequencer allows the power-up value of the CR/CSR registers to be automatically set-up by the PON_FSM controller without intervention of local intelligence. Please refer to Technical User Guide for more information.

SW4-6 will enable the propagation of a local reset (restarting the OS or pushing the front panel reset button) to the VME SYSRESETn signal on the VME backplane.

SW4-7 and SW4-8 are for the SPI flash write protest and SPI programming enable signals. The SPI flash contains the firmware for the FPGA; therefore, these two signals should always be kept enabled unless stated otherwise in Acromag documentation.

3.1.4 JTAG VREF Configuration Switch SW5

Table 3.1.d summarizes the functions, settings, and descriptions for dip switch SW5.

Table 3.1.d: JTAG VREF Configuration Switch SW5

JTAG VREF Configuration Switch SW5			
Position	**Function**	**Switch Setting**	**Description**
1-3	Lower Site (J8) JTAG VREF Configuration	1-2 (default)	Lower Site VREF = 3.3V
		2-3	Lower Site VREF = 2.5V
4-6	Upper Site (J9) JTAG VREF Configuration	4-5 (default)	Upper Site VREF = 3.3V
		5-6	Upper Site VREF = 2.5V

SW5 is used to select the VREF voltage for the XMC/PMC JTAG connections on J8 and J9.

3.1.5 VME PCIe Configuration Switch SW6

Table 3.1.e summarizes the functions, settings, and descriptions for dip switches SW6-1 thru SW6-8.

Table 3.1.e: VME Configuration Switch SW6

VMEbus PCIe Configuration Switch SW6		
Position	**Function**	**Function Description**
1	PCIe_EPMEM_PF_A64	Enable PCIe End-point Prefetchable Memory in A64 addressing (OFF by default)
2-4	PCIe_EPMEM_PF_SIZ	PCIe End-point Prefetchable Memory BAR Size, *Sw.2-Sw.3-Sw.4* OFF-OFF-OFF : Not Enabled ON-OFF-OFF : 64 Mbytes (default) OFF-ON-OFF : 128 MBytes ON-ON-OFF : 256 Mbytes OFF-OFF-ON : 512 Mbytes ON-OFF-ON : 1024 Mbytes OFF-ON-ON : 2048 Mbytes ON-ON-ON : 4096 MBytes
5-7	PCIe_EPMEM_NoPF_SIZ	PCIe End-point Non-Prefetchable Memory BAR Size, *Sw.5-Sw.6-Sw.7* OFF-OFF-OFF : Not Enabled ON-OFF-OFF : 4 Mbytes (default) OFF-ON-OFF : 8 MBytes ON-ON-OFF : 16 Mbytes OFF-OFF-ON : 32 Mbytes ON-OFF-ON : 64 Mbytes OFF-ON-ON : 128 Mbytes ON-ON-ON : 256 MBytes
8	PCIe_EPMEM_IO_4K	PCIe End-point IO Space OFF : IO Space 256 Bytes ON : IO Space 4 Kbytes (default)

SW6 is for the PCIe memory configuration of the VME bridge. Do not use a prefetchable memory BAR size greater than 1024 Mbytes while in A32 addressing mode (SW6-1 off).

3.1.6 VME Configuration Switch SW7

Table 3.1.f summarizes the functions, settings, and descriptions for dip switch SW7.

Table 3.1.f: VME Configuration Switch SW7

Table 3.1.f summarizes the functions, settings, and descriptions for dip switch SW7.

VME Configuration Switch SW7		
Position	**Function**	**Function Description**
1-8	AD[16:23]	VME CSR address: when the switch is closed, the corresponding address is set to '1'. (all OFF by default)

SW7 is used to configure the 64K CR/CSR window offset mapping when VME64x mode is not used. When VME64x mode is used, the value of SW7 is not used, and the CR/CSR register is mapped using the geographic address provided by the backplane.

3.2 Power Supply and Management

3.2.1 Power Options

The XVME-6500 can be used in any of the following VMEbus systems, with the associated caveats:

- 3-row, 5V-only legacy system. This system will limit the P2 I/O and the incoming power to the XVME-6500 to 60W. The DVI-D port and the lower 15 diff pair of PMC I/O will not be accessible. Because of the reduced power input, the use of the i7 CPU requires that the programmable power limits be employed.

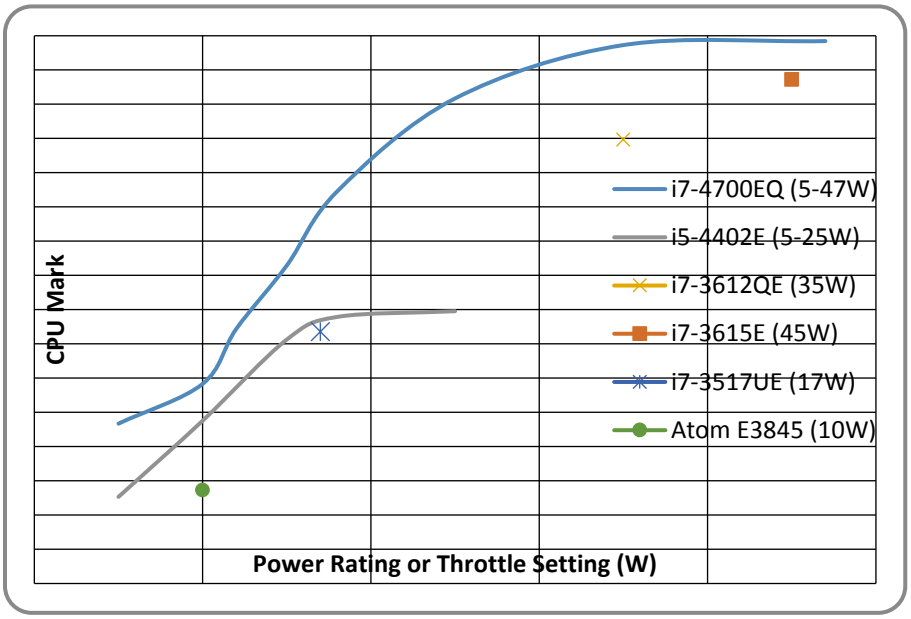
  See Section 3.16.5 for guidance on what limits should be used in conjunction with the installed PMC/XMC modules.

- 5-row, 5V-only legacy system. This system permits all available P2 I/O to be accessible to the XVME-6500, but the lack of a 3.3V power supply means that the available 90W of 5V power also feeds the 3.3V needs of the XVME-6500, as well as those of any attached PMC/XMC modules.

- 5-row, 5V + 3.3V VME64x system. This system permits all available P2 I/O to be accessible to the XVME-6500, as well as allows for the maximum available power from the backplane (90W from 5V and 66W from 3.3V). This is the recommended system for the XVME-6500.

3.2.2 Programmable CPU Power Limits

The XVME-6500 features programmable power limits, allowing the user to 'dial-down' the maximum power consumption of the CPU in systems where power is a concern. The graph below shows that the i7-4700EQ CPU outperforms other available embedded Intel CPU's at every power point from 5W - 47W, even the i5-4402E, which can also use the programmable power limits.



By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

Note: Once the minimum frequency of 800MHz is reached the programmed limit could be exceeded. Extremely large workloads have a realistic minimum power of around 20W. However light to medium workloads can effectively maintain a power limit as low as 5-10W.

There are two programmable CPU limits. These are the long-term average Power Limit 1 (PL1) and the short-term Power Limit 2 (PL2). Depending on a windowed Power Limit 1 Time 'constant', the CPU can spend a short time above power level PL1 up to a maximum of PL2, allowing a significant performance boost for short workloads. If the CPU power remains above PL1 at the end of this time the power is then limited back to PL1. The power must drop below the PL1 limit before it allowed to increase back to PL2 again. For time spent above PL1 an equivalent amount of time must be spent below PL1 in order for it to rise again to PL2. The maximum time could be as much 2.5x the value of PL1 Time.

The default values for the I7-4700EQ CPU are as follows:

PL1	PL2	Tau
47W	59W	28 seconds

PL1 and PL2 can be programmed, in watts, to any value below the default. Entering a value above the default will result in the default value being used. Entering 0 also results in the default value being used.

PL1 Time can be programmed to any number of seconds up to 256, however it is recommended by Intel to always use the default value of 28. This value maximizes the effectiveness of the short-term performance boost while ensuring that the life of the part is not jeopardized by spending too much time above PL1.

See Section 3.16.5 for guidance on what limits should be used in conjunction with the installed PMC/XMC modules.

More details about programming these power limits using the BIOS setup utility are provided in *The Acromag Core BIOS Manual*.

3.2.3 Power Management

The XVME-6500 module uses the Advanced Configuration and Power Interface (ACPI) 3.0 standard to provide user-managed power via the operating system.

3.2.3.1 ACPI System States

There are only two ACPI "Module States" supported by the XVME-6500:

- G0/S0: Fully operational; the main memory is being used for all work.
- G3: Unpowered. Power has been mechanically removed from the system. Wake-up is not possible in this state.

Note that S3 (Standby or Sleep), S4 (Hibernate) and S5 (Soft Off) are not supported by the XVME-6500, even if the VME system supports a standby power supply.

3.2.3.2 ACPI Processor States

The Advanced Configuration and Power Interface (ACPI) provides an open standard for device configuration and power management by the operating system. More details about this feature are provided in *The APTIO Haswell Core BIOS Manual For Acromag Products*.

3.3 CPU

The Intel® Gen 4 (Haswell) CPU available on the XVME-6500 is a 2.4GHz quad-core i7. This 64-bit, 22-nanometer CPU with integrated GT2 graphics contains direct interfaces for DDR3L, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the QM87 Platform Control Hub (PCH).

- **DDR3L SDRAM –** 2 SODIMM sockets support up to 16GB of DDR3L ECC at 1600MHz. Dual-channel mode is used with 2 SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe x8 (2) –** Traditionally used for external graphics, but on the XVME-6500 supports any PMC/XMC devices. One of the connections is muxed with a PEX8114 PCIe > PCI-X bridge for PMC vs. direct XMC connection. This bridge drives both PMC sites when enabled, but the lower site may still contain an XMC module even if the PMC bridge is enabled.
- **DVI-D –** This digital display interface supports connection of both, DVI-D or HDMI display devices.
- **Programmable CPU power limits –** By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

3.3.1 Active Processor Core Selection

All of the CPU cores should be kept active in high-performance systems requiring all available computing power. Conversely, applications having reduced power requirements can save power by disabling one or more of the CPU cores. The number of active CPU cores can be specified in the CPU configuration menu. More details about this feature are provided in *The APTIO Haswell Core BIOS Manual For Acromag Products*.

3.3.2 Turbo Boost Configuration

By default Turbo Mode is enabled in the BIOS setup screen. Turbo Mode allows the CPU to go beyond the rated nominal clock frequency when there is headroom from the maximum Thermal Design Power of the CPU. This results in the highest available performance, but with a larger, more dynamic power draw during peak operations. More details about this feature are provided in *The APTIO Haswell Core BIOS Manual For Acromag Products*.

3.3.3 PCI Express Graphics (PEG)

The x16 PEG interface is bifurcated into 2 x8 general PCIe ports that connect the Intel®4th Gen (Haswell) processor to the PMC/XMC Expansion Sites.

Lanes [0:7] connect directly to the Lower XMC Site's J15 connector.

Lanes [8:12] are muxed between the lower 4 lanes of the Upper Site's J25

connector and the PEX8114 PCIe to PCI-X Bridge that is used to drive the PMC bus. This mux should switch automatically to XMC when an XMC module is installed into the Upper Site. If it does not this can be overridden with DIP Switch SW2-2.

Lanes [13:16] connect to the upper 4 lanes of the Upper Site's J25 connector.

The PEG interface meets the *PCI Express Base Specification, Revision 3.0* and supports:

- Low Swing (low-power/low-voltage) and Full Swing operating modes
- Static lane numbering reversal
- The Gen3 (8 GT/s) PCI Express frequency (not supported by XMC connectors)

3.4 Platform Controller Hub (PCH)

The Intel 8 Series QM87 (Lynx Point) PCH provides extensive I/O support, as listed below:

- **PCIe x4 (2)** – There are two PCIe ports of x4 width. The first is connected to the FPGA-based VME Bridge. The other is connected to the Intel 82580EB Quad Gigabit Ethernet controller.
- **SATA II (2)** – There are two SATA ports that operate up to 3Gb/sec connected to the VME P2 connector.
- **SATA III (2)** – There are two SATA ports that operate up to 6Gb/sec connected to the Expansion Site connector for the optional XBRD-9060.
- **Bootable on-board SSD Flash** – 32GB of soldered-down on-board SSD Flash is standard on all units.
- **USB 2.0 (4)** – There are two ports connected to the VME P2 connector and two ports connected to the front panel's 26-pin connector that function at USB 2.0 or USB 1.1 speeds. There are an additional two ports available on the Expansion Site connector for the optional XBRD-9060
- **VGA** – An analog VGA port is available, including DDC clock and data, at either the VME P2 connector or the front panel's 26-pin connector. Only one connection may be used at a time and should auto switch when a monitor is plugged in to either port. Override switches are available on SW2.
- **LPC –** The Low Pin-count Bus is connected to both the NCT6106D Super-I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **SPI –** The Serial Peripheral Interface is used for the onboard boot flash.
- **HDA Audio** – The HDA audio port is connected to an ALC892 high definition audio codec. Analog stereo line-in and line-out ports are available on the VME P2 connector.
- **SMBUS** – This I2C-compatible System Management Bus has

connections to the memory DIMMs, the XMC connectors, and also to an onboard EEPROM for module identification.

3.5 System Memory

The XVME-6500 has two 204-pin, right-angle SO-DIMM sockets (J1, J2) to accept DDR3L ECC SDRAM modules. At least one SDRAM module is required to make the system operational. Note that ECC (x72) SODIMM modules are required. Non-ECC modules (x64) are not supported. Two 8GB DDR3 SDRAM modules are included on the standard model.

Support for the following features is provided by the system memory interface:

- DDR3 SDRAM with transfer rates of 1600 MT/s
- 1 GB, 2 GB, 4 GB, and 8 GB DDR3 SDRAM densities
- 72-bit wide channels (64-bits plus 8 bits of ECC)

3.6 Video

3.6.1 VGA

The XVME-6500 uses the Intel® Lynx Point controller to support the analog VGA interface.

The VGA interface features include:

- Integrated 180 Mhz 24-bit RAMDAC
- Support for analog monitor resolutions up to 1920x2000 @60 Hz

The VGA port is available on either the front panel's 26-pin connector, or via the rear VME P2 connector. Only one port may be used at a time. It should auto-switch when a monitor is plugged in, but if it does not it can be configured with DIP switches SW2-3 & SW2-4.

3.6.2 Digital Display Interfaces

The DVI-D port, available on the rear VME P2 connector, will support the connection of either an HDMI or DVI display device. It can support 2.97 GT/s, with resolution up to 4096x2304 at 24 Hz or 2560x1600 at 60Hz using single-link HDMI, and up to 1920x1200 at 60Hz using single-link DVI.

The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.

The processor also integrates a dedicated Mini HD audio controller to drive audio on an HDMI connection. The HD audio controller on the PCH would continue to support down CODECs, and so on.

3.6.2.1 DVI

A Digital Visual Interface (DVI) transmits uncompressed digital audio and video signals from AV sources to video display devices. The DVI interface originates from the CPU, and supports DVI-D (digital only),

The DVI interface utilizes transition minimized differential signaling (TMDS) to transmit audio, video and auxiliary (control/status) data information through the DVI cable.

The BIOS will automatically detect installed devices that are using DVI interfaces, and will automatically configure the installed devices according to the video BIOS settings. For further information regarding BIOS device configuration BIOS, refer to Section 4.0, "BIOS Information and Configuration.

3.6.2.2 HDMI

(The information below is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audiovisual sources to television sets, projectors, and other video displays. It can carry high quality multi-channel audio data, and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. The HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface with 3D, 4K, Deep Color, and x.v. Color.

3.6.2.3 Integrated Audio

(The information below is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

HDMI and display port interfaces carry audio along with video.

- The processor supports two DMA controllers to output two high definition audio streams on two digital ports simultaneously.
- The processor supports only the internal HDMI and DP CODECs.

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

3.6.3 Configuring the Primary Display

To select a specific primary display, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.6.4 Configuring the Video Memory

To configure the video memory, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.6.5 Video Display Options

The XVME-6500 supports simultaneous, independent displays on the VGA and DVI-D ports.

Display mode choices when using multiple monitors include:

- Single display, in which one port is activated to display the output on one device.
- Clone mode, in which the same content, resolution, and color depth are sent to up to three display devices. Different refresh rates may be used on each display.
- Extended desktop, in which a larger Windows desktop spans up to three display devices. The displays can support different refresh rates, resolutions, and color depth.

3.7 Intel® High Definition Audio

The XVME-6500 uses Intel High Definition Audio thru an ALC892 Audio CODEC to provide both stereo line-in and stereo line-out connections.Enabling and configuring the HDA is discussed in *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.8 SATA

SATA (Serial Advance Technology Attachment) is the interface that connects the PCH to the supported mass storage devices (see below). Independent operation is achieved with the two integrated SATA host controllers on the PCH using the four SATA 3.0 ports.

The SATA features support:

- The SATA hard disk drives, solid state drives (SSD), and CD-ROM/DVD-ROM drives
- IDE, AHCI, and RAID (0, 1, 5, and 10) modes
- Data transfer rates of up to 6.0Gbps (ports on the XBRD-9060)
- Data transfer rates of up to 3.0Gbps (ports on the rear VME P2)

To configure SATA operation, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.9 General I/O

3.9.1 SMBus and I2C

The SMBus is connected directly to the PCH, and contains several devices accessible at the addresses shown below to Table 3.9.1.a, SMBus Address Table.

Table 3.9.1.a: SMBus Address Table

SMBus Address	Function
0x32	DIMMA Temp
0x34	DIMMB Temp
0xA0	ID EEPROM
0xA2	DIMMA SPD
0xA4	DIMMB SPD
0xA8	Lower XMC Site
0xAA	Upper XMC Site

3.9.2 Low Pin Count (LPC)

The LPC interface contains the onboard NCT6776D Super I/O device, which supplies the serial ports and also outputs the Port80 Power On Self Test (POST) codes to the dual 7-segment display.

For further information regarding the system BIOS and LPC interfaces, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.9.3 Serial Ports

Four 16550-compatible serial ports are supplied by the NCT6776 Super I/O chip:

- One RS-232 only, including RTS, CTS, DTR, and DSR control lines, is available on the front panel's 26-pin connector.
- One RS-232/RS-422/RS-485 (software selectable), with TX/RX signals only is available on the VME P2 connector.
- One RS-232 only, with TX/RX signals only is routed to the Expansion Site connector to make the port available on the front panel via the optional XBRD-9060.

- One RS-232/RS-422/RS-485, including RTS, CTS, DTR, and DSR control lines, is available when the board is built for optional XVME-6300 I/O compatibility mode (consult factory for more info).

For further information regarding BIOS serial port configuration, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.9.4 USB

The Intel® Lynx Point PCH has up to two Enhanced Host Controller Interface (EHCI) host controllers to support USB high-speed signaling on all eight USB 2.0 high-speed ports (USB 2.0 allows data transfers up to 480 Mbps.).

These USB features support:

- USB hard disk drives, flash drives, floppy disk drives, and CD-ROM/DVD-ROM drives
- High-speed, full-speed, and low-speed USB
- High-speed USB 2.0 debug port on USB port 1
- Console redirection on USB port 1 with a debug cable

PCH USB 2.0 ports 0 and 1 are routed to the front panel's 26-pin connector. Both ports share 1A of available power.

PCH USB 2.0 Ports 2 and 3 are routed to the optional XBRD-9060.

PCH USB 2.0 Ports 8 & 9 are routed to the VME P2 connector. Both ports share 1A of available power.

For information on configuring specific USB ports see *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.10 Gigabit Ethernet

The XVME-6500 uses the Intel 82580EB Gigabit Ethernet Controller, which contains both the MAC and the physical layer.

It provides 4 ports that auto-sense 10-Base-T, 100Base-T, and 1000Base-TX connections. Any port may be used to PXE boot from a PXE server on the network. Link and Activity LEDs are available for each port.

- Two ports are available on the front panel's RJ Point 5 connector. One adapter cable is included with the XVME-6500 to connect from the front panel's RJ Point 5 connector to a standard RJ45 connector.
- Two ports are available on the optional VME P0 connector, for use on a VITA 31.1 Switch-Fabric compliant backplane, or via the optional XVME-9640 RTM module.
- One of the P0 ports may instead be switched to the Expansion Site connector, making it available on the front panel via the XBRD-9060 I/O Expander module.

For information regarding how to boot from the network, refer to *The APTIO*

Haswell Core BIOS Manual For Acromag Products.

3.11 Battery Powered Real Time Clock (RTC)

A Motorola® MS146818B-compatible real-time clock (RTC) is included in the Intel® Lynx Point PCH. The RTC has 256 bytes of battery-backed RAM and runs on a 32.768 KHz crystal with a 3V battery. The RTC performs two key functions:

- It keeps track of the time of day, and
- It stores system data, even after powering down the system.

To clear the RTC and CMOS RAM settings, remove battery BT1 from the socket for 10 seconds and reinstall.

The battery can be replaced with a standard CR1225 battery.

Note: If the battery has been removed, the RTC voltage drops below 2.5V, or when a BIOS update has been done, the first time the system is powered on it may partially boot and then restart up to two times. This behavior is normal.

3.12 Security

3.12.1 Trusted Platform Support

The XVME-6500 uses the Atmel AT97SC3204 fully integrated security module, which implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

3.12.2 Password Control

You are able to specify:

- An Administrator password with full control, and
- A User password with limited access to the BIOS settings.

For further information on setting the password, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13 System Management

3.13.1 Intel® Hyper-Threading Technology

(Note: The following information is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

The Intel® HT Technology is enabled by default; no action by the operator is required.

For further information on disabling support for this technology, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13.2 Enhanced Intel® SpeedStep Technology (EIST)

The Enhanced Intel® SpeedStep Technology (EIST) used by this processor enables very high performance while also meeting power-conservation needs. When EIST is enabled, the clock frequency of the CPU is dynamically changed in response to the CPU load

The Intel® SpeedStep feature is enabled by default. For further information on disabling support for this technology, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13.3 Intel® Virtualization Technology (Intel VT-x and VT-d)

Intel® Virtualization Technology (Intel VT) makes a single system appear as multiple independent systems to software. This allows for multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. The first revision of this technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel VT-d) adds chipset hardware implementation to improve I/O performance and robustness.

The Intel® VT-x and VT-d features are enabled by default. For further information on disabling support for this technology, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13.4 Intel® Trusted Execution Technology (TXT)

The featured Intel® Trusted Execution Technology attests to the authenticity of a platform and its operating system and assures that an authentic OS starts in a trusted environment and can be considered a trusted OS.

Intel® TXT works in conjunction with the TPM so that the system software may make trust decisions.

The Intel TXT feature is enabled by default. For further information on disabling support for this technology, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13.5 Intel® Turbo Boost Technology

The number of active cores determines the maximum processor core operating frequency. See Section 3.3.1, "Active Processor Core Selection" for information and instructions.

(Note: The following information is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

The Intel® Turbo Boost Technology allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads.

The processor supports a Turbo mode in which the processor can use the thermal capacity associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, surging usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. See the appropriate processor family BIOS writer's guide for enabling details. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time. Refer to *The APTIO Haswell Core BIOS Manual For Acromag Products* and the

appropriate processor Turbo Implementation Guide for more information.

3.13.6 Intel® Active Management Technology

(Note: The following information is from Intel® publication "External Design Specifications – April 2013, Revision 2.1" for the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub [PCH]).

Intel® Active Management Technology (Intel® AMT) is a set of advanced manageability features developed to extend the manageability capability for IT through Out Of Band (OOB). This allows asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low power, or "off" state, or in situations when the operating system is hung.

For further information on configuring this technology, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.13.7 Intel® Matrix Storage Technology

Intel® Matrix Storage Technology is supported by Intel's 8 Series QM87 Lynx Point PCH, which provides:

- AHCI functionality,
- RAID 0/1/5/10 Support, and
- Intel® Smart Response Technology.

3.13.8 Intel® Configurable TDP Technology

Intel® Configurable TDP Technology (cTDP) allows users to reconfigure the 47W thermal design power (TDP) level of the i7-4700EQ CPU down to 37W in systems where a lower amount of power is available or a smaller thermal solution is required.

For further information on configuring the TDP levels, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.14 Thermal Management

The Intel® Haswell processor contains a digital thermal sensor for each execution core and a thermal monitor to measure the processor's temperature. A thermal sensor connected to the NCT6776 Super-I/O is used to measure the module's temperature.

The integrated graphics and memory controller (GMC) monitors its temperature and initiates thermal management with an internal digital thermal sensor. Memory loading or high GMC temperatures will result in bandwidth throttling.

The temperature of the Intel® Lynx Point PCH is monitored by two thermal sensors located on the PCH. The system will be shut down by the PCH when its thermal limit is reached.

3.14.1 Thermal Monitoring

The BIOS setup utility displays the processor and board temperatures. For further information on how to check these temperatures, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.14.2 Thermal Throttling

3.14.2.1 CPU Throttling (Hardware Controlled)

The processor must not exceed the 100°C maximum junction temperature (Tj).

When the integrated thermal monitor on the processor determines that the maximum processor temperature has been reached, the CPU clock speed will be throttled back in 100MHz increments to keep Tj from exceeding the maximum junction temperature of 100°C.

If throttling is not enough to keep the processor's Tj below the catastrophic temperature limit of 105°C, the voltage supply to the processor will be turned off within 500ms to prevent permanent silicon damage.

3.14.2.2 Thermal Management (OSPM Controlled)

In addition to the hardware throttling described above, software controlled passive trip points may be configured using the system BIOS setup.

For information on how to configure these trip points, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.14.3 Memory Throttling

The memory bandwidth can be throttled back automatically if a thermal sensor is on the DIMM. The NCT6776D will alert the memory controller via PECI when the system memory exceeds its normal operating temperature.

For further information on configuring the memory bandwidth throttling based on temperature readings from the DIMM's thermal sensor, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.14.4 Thermal Management Hardware

The XVME-6500 is available in air-cooled and extended air-cooled models only. A larger double-slot heatsink is also available as an accessory. Please consult the factory for more information.

Air-cooled assemblies must be installed into an air-cooled VME chassis with proper airflow across the board. At least 300LFM of airflow is required to ensure proper operation across entire specified temperature range.

In addition to the air-cooled heatsink assemblies, special SODIMM heat spreaders are used to remove heat from the SODIMM modules, as well as

hold them tightly secured to the board.

To remove the SODIMM modules, simply remove the 4 screws per SODIMM from the back side of the PCB.

3.15 Watchdog

The XVME-6500 features a software-triggered multi-stage watchdog solution. When the watchdog timer expires the module by default causes a system reset.

For further information on the Watchdog feature, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

3.16 Expansion Sites

The XVME-6500 features two expansion sites that allow the board to be customized for a wide array of customer applications.

The Lower Site accepts either PMC or XMC modules, with the module's P4 user I/O routed as 100ohm differential pairs to the optional P0 connector on the XVME-6500. A build option is available to instead route the I/O from the module's P6 connector to the XVME-6500's P0 connector.

The Upper Site accepts PMC or XMC modules, with the module's P4 user I/O routed as 100ohm differential pairs to the P2 connector on the XVME-6500. A build option is available to instead add a second serial port, 4 General Purpose Digital Inputs, and 4 General Purpose Digital Outputs to the XVME-6500's P2 connector, making the XVME-6500 compatible with the P2 I/O of the XVME-6300. Please consult factory regarding this option.

3.16.1 XMC Modules

XMC modules can be used in either or both Upper and Lower Expansion Sites on the XVME-6500, however if one XMC module is used in conjunction with one PMC module the XMC module must be in the Lower Site.

Each Expansion Site connects to the XMC module with a x8 PCIe interface. While the connection itself supports Gen2 speeds, please note that the XMC connectors are only rated for Gen1 speeds, limiting the supported speed of the XMC modules to Gen1. A build option is available for the XMC connectors to instead be VITA 61 connectors, which do support Gen2 speeds, however this limits the site(s) to having only VITA 61 modules supported. Please consult factory regarding this option.

When an XMC module is installed in the Upper Site, the PEX8114 PXIe to PCI-X Bridge is automatically disabled and all 8 lanes of the PCIe interface for the Upper site are connected to the XMC module. If this automatic mechanism does not work with a particular XMC module, SW2-2 may be used to force the site to work in XMC mode.

Note: Processor XMC modules are not supported on the XVME-6500.

3.16.2 PMC Modules

PMC modules can be used in either or both Upper and Lower Expansion Sites on the XVME-6500, however if one PMC module is used in conjunction with one XMC module the PMC module must be in the Upper Site.

When a PMC module is installed in the Upper Site, the PEX8114 PXIe to PCI-X Bridge is enabled and connected using lanes of the PCIe interface for the Upper Site. If PMC modules are not recognized, check SW2-2 to be sure it is not forcing the sites to work in XMC mode.

The PMC interface uses PCI-X and can function at 133MHz, 100MHz, 66MHz or 50MHz bus speeds. SW2-1 may be used to select a maximum bus speed, or allow it to be automatic based on the PMC card(s) installed.

Note: The VITA 39 Specification, "*PCIX Auxiliary Standard for PMCs*" states that "Dual PMC site carriers shall under-clock the bus at 100MHz when 133MHz capable PMC(s) are installed and the 133MHz mode is enabled." Instability may result with some 133MHz capable PMC modules with the bus speed set at 133MHz. Under-clocking to 100MHz using SW2-1 is recommended when 133MHz module(s) are installed.

Note: Processor PMC modules are not supported on the XVME-6500.

3.16.3 PMC/XMC JTAG Interfaces

Some PMC/XMC modules may utilize JTAG connections for FPGA programming or other module debug activities. Individual JTAG connections are available for each site through the use of a Molex 78171-5006 6-pin micro connector. J8 is used for connection to the Lower Site, while J9 is used for connection to the Upper Site.

Adapter cables to connect between J8/J9 and a Xilinx USB programmer are available. Please consult factory for more information.

VREF voltage on the connector can be selected as either 2.5V or 3.3V using switch SW5.

3.16.4 XBRD-9060 I/O Expander Module

The optional XBRD-9060 module may be installed in the Upper Site of an air-cooled XVME-6500 to bring more I/O to the front panel, as well as allow mSATA SSD modules to be added for storage.

The following I/O is available on the front panel of the XBRD-9060:

- One Gigabit Ethernet port via a standard RJ-45 connector. When this port is enabled on the XBRD-9060 module, one of the Ethernet ports on the P0 connector is disabled.
- One RS-232 serial port. This port only contains TX/RX signals. It is brought out on a mini USB-B connector, but an adapter cable is included with the module for connection using a standard DB-9 connector.
- Two USB 2.0 ports. These ports use standard USB-A connectors and can operate as either USB 2.0 or USB 1.1 connections.

The XBRD-9060 contains 2 mSATA sockets that allow 2 SSD drives to be added to the XVME-6500 while still remaining within a single VME slot. Using the software RAID functionality of the QM87 PCH, these drives can even be setup as a RAID0/1 array if redundancy or extra speed is desired.

3.16.5 Power Available to Expansion Modules

The power requirements given in Section 6.4 do not include attached expansion modules. The amount of power available to the expansion sites depends on which CPU is used on the XVME-6500, the programmable PL1 power limit used for that CPU, and what type of backplane/power supply combination is powering it. In order to maintain the stability and long life of the XVME-6500, the programmed CPU PL1 power limit should be set according to the following equation:

PL1 = Total Available 5V Power - Expected Combined Expansion Card 5V Power - Rest of Board 5V Power.

The Total Available 5V Power is determined by the backplane type:

Backplane Type	Total Available 5V Power
5-row with 5V & 3.3V supplied	90W
5-row with 5V only supplied	87.5W (2.5W of 3.3V made from 5V)
3-row with 5V only supplied	57.5W (2.5W of 3.3V made from 5V)

Expected Combined Expansion Card 5V Power is the amount of 5V power the installed PMC/XMC expansion modules are expected to consume.

The Rest of Board 5V Power is ~23.5W (typical).

Example 1:
An XVME-6500 is used in a 5-row backplane with 5V only power. The expected expansion card power is 40W. To determine the value to use for PL1:

PL1= 90W - 40W – 23.5W = 26.5W. *A value no larger than 26.5 should be programmed into the BIOS setup utility for PL1 in this situation.*

Example 2:
An XVME-6500 is used in a 3-row backplane with 5V only power. The expected expansion card power is 40W. To determine the value to use for

PL1: PL1= 57.5W - 40W – 23.5W = -6.0W. *The expected expansion card power is too large for this scenario.*

Example 3:
An XVME-6500 is used in a 3-row backplane with 5V only power. The expected expansion card power is 30W. To determine the value to use for PL1:

PL1= 57.5W - 30W – 23.5W = 4.0W.

Care must be taken in this situation. Since this value is much less than 20W, only very small workloads on the CPU will keep the power at this limit. The expected expansion card power is still likely too large to maintain a long life of the XVME-6500.

See Section 3.2.2 for more details regarding Programmable CPU Power Limits.

If PL1 is not lowered using the Programmable CPU Power Limits, the following tables describe the available power for installed expansion modules.

For i7-4700EQ CPU:

Backplane Type	Combined Expansion Module Power	
5-row with 5V & 3.3V supplied	5V: 20W	3.3V: 63.5W
5-row with 5V only supplied	5V: 17.5W	3.3V: included in 5V
3-row with 5V only supplied	ONLY SUPPORTED WITH PL1 lowered	

3.17 VME Interface

The XVME-6500 connects to the VMEbus through the high-performance FPGA-based VME Bridge that is fully compliant with all VME64x data transactions (SBT, BLT, MBLT, 2eVME, and 2eSST) on all common addressing space modes (A16, A24 and A32). This allows the XVME-6500 to take advantage of the higher performance VME protocols, but sill co-exist with VME boards utilizing legacy protocols.

The VME Bridge connects to the QM87 PCH directly via a x4 PCIe Gen 2 connection, allowing maximum throughput to/from the VMEbus. The FPGA-based VME bridge also features a fully programmable hardware byte swapper function.

For VMEbus configuration options, see Sections 3.1.3, 3.1.5, and 3.1.6.

Five VME Bridge LEDs are provided for visual indication of the bus status for quick debugging. The LEDs are described below in Table 3.17.a.

Table 3.17.a: VME Bridge Status LEDs

VME Bridge Status LEDs		
LED Marking	**Function**	**Function Description**
DS12	VME SLOT1	Provides VME System Controller Status. ON – System Controller Enabled OFF – System Controller Disabled
DS13	VME SLAVE	Activated on VME slave transactions.
DS14	VME MASTER	Activated on VME master transactions.
DS15	FPGA OK	Provides VME operational status. OFF – not operational TOGGLE – FPGA VME bridge is operational
DS16	PCIE ERROR	Provides PCIe status.* OFF – LTSSM L0 state (normal working state) TOGGLE Slow – LTSSM Configuration states TOGGLE Fast – LTSSM L1 states ON – any other state

*Refer to PCI Express specification.

For driver information on the FPGA VME Bridge please refer to *ALTHEA 7910 Application Programming Interface* manual.

3.18 Front Panel Layout

- **PASS/FAIL LEDs:** The green PASS and red FAIL LEDs are used as an indication of board health during the BIOS boot up. As the BIOS starts the POST, the red FAIL LED will be turned off. When the BIOS completes the POST, the green PASS LED is turned on.
- **USER LEDs:** The USER LEDs are accessible by user software. See Section 4 for more information.
- **ETHERNET LINK/ACTIVITY LEDs:** For each Ethernet port, the top LED shows the port is LINKed, while the bottom LED indicates ACTIVITY.
- **RESET Switch:** The front panel switch can be configured to cause a local reset and also may reset the VME backplane, depending on the configuration of SW1-1 and SW4-6.

4.0 FIRMWARE/BIOS INFORMATION AND CONFIGURATION

4.1 XVME-6500 Special BIOS Features

This section contains information on configuring features specific to the XVME-6500. For other, more generic BIOS setup information, refer to *The APTIO Haswell Core BIOS Manual For Acromag Products.*

To access the XVME-6500 specific items in the BIOS setup, select the Acromag menu item.

Fig. 4.1.a: Acromag BIOS Setup Menu



- The GPO0-3 default output levels can be configured. Note that these outputs are only available with the 'XVME-6300 Compatible I/O' build option.
- The default output levels of the front panel User LEDs can be configured. The LED is on when the output level is high.
- The serial protocol used by COM4 and COM2 can be either RS-232 or RS-422/485. Note that COM4 is only available with the 'XVME-6300 Compatible I/O' build option.
- The ID EEPROM on the SMBus can be configured as Read/Write or Read-Only.
- The soldered-down SSD can be configured as Read/Write or Read-Only.
- The XMC mezzanine modules can configured as Read/Write or Read-Only. XMC Slot A is the lower slot. XMC Slot B is the upper slot. Note the mezzanine must support use of the MVMRO signal.
- The rear DVI-D port can be enabled/disabled.

4.2 Drivers and Utilities

Drivers and Utilities for the XVME-6500 can be downloaded from Acromag's website at https://www.acromag.com/.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Single Board Computer (SBC) products like the XVME-6500 are generally difficult to repair. The module can be easily damaged unless special SBC repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. For these and other reasons, it is strongly recommended that a non-functioning SBC be returned to Acromag for repair.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation for the module to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

5.3 Where to Get Help

If the problem persists, the next step should be to visit the Acromag website at https://www.acromag.com. Our web site contains the most up-to-date product and software information.

Acromag's application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6.0 SPECIFICATIONS

6.1 Physical

The XVME-6500 conforms to the 6U Eurocard form-factor.

Height	233.35 mm (9.187 in)
Depth	160.0 mm (6.3 in)
Minimum Backplane Pitch	20.32 mm (0.8 in)

Unit Weight

with P0 connector:	17.8 oz (0.507 kg)
without P0 connector:	17.4 oz (0.494 kg)

6.2 Connector Information

6.2.1 J3 CPU XDP Debug Connector

This connector is a 26-pin Molex 52435-2671 and complies with Intel Shark Bay Debug Port Design Guide. It can be used for debug of the CPU using tools and guides available from authorized Intel representatives.

6.2.2 J6 SPI BIOS Programming Header

This header is used to program the 128Mb SPI Flash EPROM containing the BIOS and ME Firmware and is for factory use only.

6.2.3 J17 FPGA-based VME Bridge Programming Header

This header is used to program the 128Mb SPI Flash EPROM containing the FPGA firmware and is for factory use only.

PIN	SIGNAL
1	JTAG_TDI
2	JTAG_TDO
3	GND
4	JTAG_TCK
5	JTAG_TMS
6	JTAG_VREF

6.2.4 VME Interface

6.2.4.1 P0 VME Connector (Optional)

This optional connector is a standard 6-row, 2mm Type B, 95-pin Harting 17-25-095-2102. It contains 2 Ethernet and the Lower Site's PMC I/O (XMC instead with build option)

ROW/PIN	A	B	C	D	E	F
1	GND	GND	GND	GND	GND	GND
2	ENET0_MX0_P	ENET0_MX0_N	GND	ENET0_MX2_P	ENET0_MX2_N	
3	ENET0_MX1_P	ENET0_MX1_N	GND	ENET0_MX3_P	ENET0_MX3_N	GND
4	ENET1_MX0_P[1]	ENET1_MX0_N[1]	GND	ENET1_MX2_P[1]	ENET1_MX2_N[1]	
5	ENET1_MX1_P[1]	ENET1_MX1_N[1]	GND	ENET1_MX3_P[1]	ENET1_MX3_N[1]	GND
6	ENET1_LINK#	ENET0_LINK#	+3.3V_TO_RTM	ENET1_ACT#	ENET0_ACT#	
7	LWR_IO0_P	LWR_IO2_P	LWR_IO2_N	LWR_IO3_P	LWR_IO3_N	GND
8	LWR_IO0_N	LWR_IO4_P	LWR_IO4_N	LWR_IO5_P	LWR_IO5_N	
9	LWR_IO8_P	LWR_IO6_P	LWR_IO6_N	LWR_IO7_P	LWR_IO7_N	GND
10	LWR_IO8_N	LWR_IO1_P	LWR_IO1_N	LWR_IO9_P	LWR_IO9_N	
11	LWR_IO12_P	LWR_IO10_P	LWR_IO10_N	LWR_IO11_P	LWR_IO11_N	GND
12	LWR_IO12_N	LWR_IO25_N	LWR_IO25_P	LWR_IO13_P	LWR_IO13_N	
13	LWR_IO16_P	LWR_IO14_P	LWR_IO14_N	LWR_IO15_P	LWR_IO15_N	GND
14	LWR_IO16_N	LWR_IO31_N	LWR_IO31_P	LWR_IO17_P	LWR_IO17_N	
15	LWR_IO20_P	LWR_IO18_P	LWR_IO18_N	LWR_IO19_P	LWR_IO19_N	GND
16	LWR_IO20_N	LWR_IO29_N	LWR_IO29_P	LWR_IO21_P	LWR_IO21_N	
17	LWR_IO24_P	LWR_IO22_P	LWR_IO22_N	LWR_IO23_P	LWR_IO23_N	GND
18	LWR_IO24_N	LWR_IO26_N	LWR_IO26_P	LWR_IO27_N	LWR_IO27_P	
19	NC	LWR_IO30_N	LWR_IO30_P	LWR_IO28_N	LWR_IO28_P	GND

NC = NO CONNECT

[1] ENET1 signals may instead be switched to XBRD-9060 I/O Expander module, if installed.

6.2.4.2 P1 VME Connector

This standard VME 5-row, 160-pin Harting 02-01-160-2101 connector brings in power and VMEbus signals:

ROW/PIN	Z	A	B	C	D
1	NC	DO0	BBSY#	D08	+5V
2	GND	DO1	BCLR#	D09	GND
3	NC	DO2	ACFAIL#	D10	NC
4	GND	DO3	BG0IN#	D11	NC
5	NC	DO4	BG0OUT#	D12	NC
6	GND	DO5	BG1IN#	D13	NC
7	NC	DO6	BG1OUT#	D14	NC
8	GND	DO7	BG2IN#	D15	NC
9	NC	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	NC	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	+3.3V[1]
13	NC	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	+3.3V[1]
15	NC	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	+3.3V[1]
17	NC	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	+3.3V[1]
19	NC	GND	AM3	A19	NC
20	GND	IACK#	GND	A18	+3.3V[1]
21	NC	IACKIN#	NC	A17	NC
22	GND	IACKOUT#	NC	A16	+3.3V[1]
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7#	A14	+3.3V[1]
25	NC	A06	IRQ6#	A13	NC
26	GND	A05	IRQ5#	A12	+3.3V[1]
27	NC	A04	IRQ4#	A11	NC
28	GND	A03	IRQ3#	A10	+3.3V[1]
29	NC	A02	IRQ2#	A09	NC
30	GND	A01	IRQ1#	A08	+3.3V[1]
31	NC	-12V	NC	+12V	GND
32	GND	+5V	+5V	+5V	+5V

NC = NO CONNECT

[1] The XVME-6500 will use +3.3V from the backplane, if present, but it is not required.

6.2.4.3 P2 VME Connector (Standard I/O)

This standard VME 5-row, 160-pin Harting 02-01-160-2101 connector brings in standard PC I/O, as well as the Upper Site's PMC I/O.

Note: The signals on the 'A' and 'Z' rows is not available when installed in a legacy, 3-row backplane.

ROW/PIN	Z	A	B	C	D
1	UPR_IO0_P	SATA_TX2_P	+5V	AUD_OUT_R	DVI_P0_P
2	GND	SATA_TX2_N	GND	AUD_OUT_L	DVI_P0_N
3	UPR_IO0_N	GND	VME_RETRY#	AUD_GND	GND
4	GND	SATA_RX2_P	VME_A24	AUD_IN_L	DVI_P1_P
5	UPR_IO1_P	SATA_RX2_N	VME_A25	AUD_IN_R	DVI_P1_N
6	GND	UPR_IO16_N	VME_A26	UPR_IO16_P	GND
7	UPR_IO1_N	SATA_TX3_P	VME_A27	UPR_IO17_N	DVI_P2_P
8	GND	SATA_TX3_N	VME_A28	UPR_IO17_P	DVI_P2_N
9	UPR_IO2_P	UPR_IO24_P	VME_A29	VGA_RED	GND
10	GND	SATA_RX3_P	VME_A30	VGA_GRN	DVI_CLK_P
11	UPR_IO2_N	SATA_RX3_N	VME_A31	VGA_BLUE	DVI_CLK_N
12	GND	UPR_IO24_N	GND	VGA_VSYNC	GND
13	UPR_IO3_P	USB_P4_P	+5V	VGA_HSYNC	DVI_HPD
14	GND	USB_P4_N	VME_D16	UPR_IO18_N	DVI_SDA
15	UPR_IO3_N	UPR_IO25_P	VME_D17	VGA_I2C_DAT	DVI_SCL
16	GND	USB_P5_P	VME_D18	VGA_I2C_CLK	UPR_IO8_P
17	UPR_IO4_P	USB_P5_N	VME_D19	UPR_IO18_P	UPR_IO8_N
18	GND	UPR_IO25_N	VME_D20	COM2_TX	UPR_IO9_P
19	UPR_IO4_N	USB_+5V	VME_D21	COM2_TX-[1]	UPR_IO9_N
20	GND	USB_+5V	VME_D22	UPR_IO19_N	UPR_IO10_P
21	UPR_IO5_P	UPR_IO26_P	VME_D23	COM2_RX	UPR_IO1R_N
22	GND	UPR_IO26_N	GND	COM2_RX-[1]	UPR_IO11_P
23	UPR_IO5_N	UPR_IO27_P	VME_D24	UPR_IO19_P	UPR_IO11_N
24	GND	UPR_IO27_N	VME_D25	UPR_IO20_N	UPR_IO12_P
25	UPR_IO6_P	UPR_IO28_P	VME_D26	UPR_IO20_P	UPR_IO12_N
26	GND	UPR_IO28_N	VME_D27	UPR_IO21_N	UPR_IO13_P
27	UPR_IO6_N	UPR_IO29_P	VME_D28	UPR_IO21_P	UPR_IO13_N
28	GND	UPR_IO29_N	VME_D29	UPR_IO22_N	UPR_IO14_P
29	UPR_IO7_P	UPR_IO30_P	VME_D30	UPR_IO22_P	UPR_IO14_N
30	GND	UPR_IO30_N	VME_D31	UPR_IO15_N	UPR_IO15_P
31	UPR_IO7_N	UPR_IO31_P	GND	UPR_IO23_P	GND
32	GND	UPR_IO31_N	+5V	UPR_IO23_N	+5V

[1] TX- and RX- only used when serial port is in RS-422/RS-485 mode

6.2.4.4 P2 VME Connector (XVME-6300 Compatible I/O - Consult Factory for this Option)

A factory build option makes the P2 I/O compatible with the XVME-6300 pinout, although some PMC I/O signal differences remain from those on the XVME-6300. The highlighted pins below show the pin differences from the standard XVME-6500 I/O.

ROW/PIN	A	C	D
6	GND	NC	
7		NC	
8		GND	
9	GND		
12	GND		
14		GND	
15	GND		
16			GND
17		GND	NC
18	GND		NC
19			NC
20		GND	NC
21	GND		GND
22	COM4_TX		
23	COM4_RTS#_TX-[1]	GND	
24	GND	GPIN0	
25	COM4_RX	GPIN1	
26	COM4_DSR#_RX-[1]	GPIN2	
27	GND	GPIN3	
28	COM4_CTS#	GPOUT0	
29	COM4_DTR#	GPOUT1	
30		GPOUT2	
31		GPOUT3	
32		NC	

NC = NO CONNECT

[1] TX- and RX- only used when serial ports is in RS-422/RS-485 mode. RTS# and DSR# are available in RS-232 mode.

6.2.5 Lower PMC/XMC Site

6.2.5.1 J11 Lower PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	JTAG_TCK	-12V	2
3	GND	INTB#	4
5	INTC#	INTD#	6
7	NC	+5V	8
9	INTA#	NC	10
11	GND	NC	12
13	CLK_PCI	GND	14
15	GND	GNT1#	16
17	REQ#	+5V	18
19	+3.3V	AD(31)	20
21	AD(28)	AD(27)	22
23	AD(25)	GND	24
25	GND	C/BE(3)#	26
27	AD(22)	AD(21)	28
29	AD(19)	+5V	30
31	+3.3V	AD(17)	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	PCIXCAP	PU to 3.3V	40
41	NC	NC	42
43	PAR	GND	44
45	+3.3V	AD(15)	46
47	AD(12)	AD(11)	48
49	AD(9)	+5V	50
51	GND	C/BE(0)#	52
53	AD(6)	AD(5)	54
55	AD(4)	GND	56
57	+3.3V	AD(3)	58
59	AD(2)	AD(1)	60
61	AD(0)	+5V	62
63	GND	REQ64#	64

NC = NO CONNECT

PU = PULLUP

6.2.5.2 J12 Lower PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	+12V	NC	2
3	JTAG_TMS	JTAG_TDO	4
5	JTAG_TDI	GND	6
7	GND	NC	8
9	NC	NC	10
11	PU to 3.3V	+3.3V	12
13	RST#	GND	14
15	+3.3V	GND	16
17	NC	GND	18
19	AD(30)	AD(29)	20
21	GND	AD(26)	22
23	AD(24)	+3.3V	24
25	AD(22) (IDSEL#)	AD(23)	26
27	+3.3V	AD(20)	28
29	AD(18)	GND	30
31	AD(16)	C/BE(2)#	32
33	GND	NC	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE(1)#	GND	44
45	AD(14)	AD(13)	46
47	M66EN	AD(10)	48
49	AD(8)	+3.3V	50
51	AD(7)	NC	52
53	+3.3V	NC	54
55	NC	GND	56
57	NC	NC	58
59	GND	NC	60
61	ACK64#	+3.3V	62
63	GND	NC	64

NC = NO CONNECT

PU = PULLUP

6.2.5.3 J13 Lower PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	NC	GND	2
3	GND	C/BE(7)#	4
5	C/BE(6)#	C/BE(5)#	6
7	C/BE(4)#	GND	8
9	+3.3V	PAR64	10
11	AD(63)	AD(62)	12
13	AD(61)	GND	14
15	GND	AD(60)	16
17	AD(59)	AD(58)	18
19	AD(57)	GND	20
21	+3.3V	AD(56)	22
23	AD(55)	AD(54)	24
25	AD(53)	GND	26
27	GND	AD(52)	28
29	AD(51)	AD(50)	30
31	AD(49)	GND	32
33	GND	AD(48)	34
35	AD(47)	AD(46)	36
37	AD(45)	GND	38
39	+3.3V	AD(44)	40
41	AD(43)	AD(42)	42
43	AD(41)	GND	44
45	GND	AD(40)	46
47	AD(39)	AD(38)	48
49	AD(37)	GND	50
51	GND	AD(36)	52
53	AD(35)	AD(34)	54
55	AD(33)	GND	56
57	+3.3V	AD(32)	58
59	NC	NC	60
61	NC	GND	62
63	GND	NC	64

NC = NO CONNECT

6.2.5.4 J14 Lower PMC Site Rear-I/O Connector

This standard 64-pin Molex 71439-0164 connector interfaces the Rear I/O from the Lower PMC/XMC module's P4 connector. The corresponding signals can be found on the VME P0 connector. The signals are routed as 100ohm differential pairs.

PIN	SIGNAL	SIGNAL	PIN
1	LWR_IO0_P	LWR_IO1_P	2
3	LWR_IO0_N	LWR_IO1_N	4
5	LWR_IO2_P	LWR_IO3_P	6
7	LWR_IO2_N	LWR_IO3_N	8
9	LWR_IO4_P	LWR_IO5_P	10
11	LWR_IO4_N	LWR_IO5_N	12
13	LWR_IO6_P	LWR_IO7_P	14
15	LWR_IO6_N	LWR_IO7_N	16
17	LWR_IO8_P	LWR_IO9_P	18
19	LWR_IO8_N	LWR_IO9_N	20
21	LWR_IO10_P	LWR_IO11_P	22
23	LWR_IO10_N	LWR_IO11_N	24
25	LWR_IO12_P	LWR_IO13_P	26
27	LWR_IO12_N	LWR_IO13_N	28
29	LWR_IO14_P	LWR_IO15_P	30
31	LWR_IO14_N	LWR_IO15_N	32
33	LWR_IO16_P	LWR_IO17_P	34
35	LWR_IO16_N	LWR_IO17_N	36
37	LWR_IO18_P	LWR_IO19_P	38
39	LWR_IO18_N	LWR_IO19_N	40
41	LWR_IO20_P	LWR_IO21_P	42
43	LWR_IO20_N	LWR_IO21_N	44
45	LWR_IO22_P	LWR_IO23_P	46
47	LWR_IO22_N	LWR_IO23_N	48
49	LWR_IO24_P	LWR_IO25_P	50
51	LWR_IO24_N	LWR_IO25_N	52
53	LWR_IO26_P	LWR_IO27_P	54
55	LWR_IO26_N	LWR_IO27_N	56
57	LWR_IO28_P	LWR_IO29_P	58
39	LWR_IO28_N	LWR_IO29_N	60
61	LWR_IO30_P	LWR_IO31_P	62
63	LWR_IO30_N	LWR_IO31_N	64

6.2.5.5 J15 Lower XMC Site PCIe Connector

This standard 114-pin Samtec ASP-103612-04 connector connects the PEG (PCIe) interface from the CPU to the Lower XMC module.

ROW/PIN	A	B	C	D	E	F
1	PEG0_RX_P	PEG0_RX_N	+3.3V	PEG1_RX_P	PEG1_RX_N	+5V
2	GND	GND	NC	GND	GND	PLT_RST#
3	PEG2_RX_P	PEG2_RX_N	+3.3V	PEG3_RX_P	PEG3_RX_N	+5V
4	GND	GND	JTAG_TCK	GND	GND	NC
5	PEG4_RX_P	PEG4_RX_N	+3.3V	PEG5_RX_P	PEG5_RX_N	+5V
6	GND	GND	JTAG_TMS	GND	GND	+12V
7	PEG6_RX_P	PEG6_RX_N	+3.3V	PEG7_RX_P	PEG7_RX_N	+5V
8	GND	GND	JTAG_TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	JTAG_TDO	GND	GND	GND (GA0#)
11	PEG0_TX_P	PEG0_TX_N	NC	PEG1_TX_P	PEG1_TX_N	+5V
12	GND	GND	GND (GA1#)	GND	GND	NC
13	PEG2_TX_P	PEG2_TX_N	NC	PEG3_TX_P	PEG3_TX_N	+5V
14	GND	GND	GND (GA2#)	GND	GND	SMB_DATA
15	PEG4_TX_P	PEG4_TX_N	NC	PEG5_TX_P	PEG5_TX_N	+5V
16	GND	GND	XMCA_WP	GND	GND	SMB_CLK
17	PEG6_TX_P	PEG6_TX_N	NC	PEG7_TX_P	PEG7_TX_N	NC
18	GND	GND	NC	GND	GND	NC
19	PEG_CLK_P	PEG_CLK_N	NC	NC	NC	NC

NC = NO CONNECT

6.2.5.6 J8 Lower PMC/XMC Site JTAG Connector

This 6-pin Molex 78171-5006 connector carries the Lower PMC or XMC module's JTAG interface. The VREF voltage can be selected between 2.5V, or 3.3V with SW5.

PIN	SIGNAL
1	JTAG_TDI
2	JTAG_TDO
3	GND
4	JTAG_TCK
5	JTAG_TMS
6	JTAG_VREF

6.2.5.7 J16 Lower XMC Site Rear I/O Connector

This standard 114-pin Samtec ASP-103612-04 connector can, with a build option bring the Lower XMC module's P6 I/O to the XVME-6500's P0 connector instead of the XMC/PMC module's P4 connector. The signals are routed as 100ohm differential pairs.

ROW/PIN	A	B	C	D	E	F
1	LWR_IO0_P	LWR_IO0_N	NC	LWR_IO1_P	LWR_IO1_N	NC
2	GND	GND	NC	GND	GND	NC
3	LWR_IO2_P	LWR_IO2_N	NC	LWR_IO3_P	LWR_IO3_N	NC
4	GND	GND	NC	GND	GND	NC
5	LWR_IO4_P	LWR_IO4_N	NC	LWR_IO5_P	LWR_IO5_N	NC
6	GND	GND	NC	GND	GND	NC
7	LWR_IO6_P	LWR_IO6_N	NC	LWR_IO7_P	LWR_IO7_N	NC
8	GND	GND	LWR_IO30_N	GND	GND	LWR_IO31_N
9	LWR_IO8_P	LWR_IO8_N	LWR_IO30_P	LWR_IO9_P	LWR_IO9_N	LWR_IO31_P
10	GND	GND	LWR_IO28_N	GND	GND	LWR_IO29_N
11	LWR_IO10_P	LWR_IO10_N	LWR_IO28_P	LWR_IO11_P	LWR_IO11_N	LWR_IO29_P
12	GND	GND	LWR_IO26_N	GND	GND	LWR_IO27_N
13	LWR_IO12_P	LWR_IO12_N	LWR_IO26_P	LWR_IO13_P	LWR_IO13_N	LWR_IO27_P
14	GND	GND	LWR_IO24_N	GND	GND	LWR_IO25_N
15	LWR_IO14_P	LWR_IO14_N	LWR_IO24_P	LWR_IO15_P	LWR_IO15_N	LWR_IO25_P
16	GND	GND	LWR_IO22_N	GND	GND	LWR_IO23_N
17	LWR_IO16_P	LWR_IO16_N	LWR_IO22_P	LWR_IO17_P	LWR_IO17_N	LWR_IO23_P
18	GND	GND	LWR_IO20_N	GND	GND	LWR_IO21_N
19	LWR_IO18_P	LWR_IO18_N	LWR_IO20_P	LWR_IO19_P	LWR_IO19_N	LWR_IO21_P

NC = NO CONNECT

6.2.6 Upper PMC/XMC Site

6.2.6.1 J21 Upper PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	JTAG_TCK	-12V	2
3	GND	INTD#	4
5	INTA#	INTB#	6
7	NC	+5V	8
9	INTC#	NC	10
11	GND	NC	12
13	CLK_PCI	GND	14
15	GND	GNT1#	16
17	REQ#	+5V	18
19	+3.3V	AD(31)	20
21	AD(28)	AD(27)	22
23	AD(25)	GND	24
25	GND	C/BE(3)#	26
27	AD(22)	AD(21)	28
29	AD(19)	+5V	30
31	+3.3V	AD(17)	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	PCIXCAP	PU to 3.3V	40
41	NC	NC	42
43	PAR	GND	44
45	+3.3V	AD(15)	46
47	AD(12)	AD(11)	48
49	AD(9)	+5V	50
51	GND	C/BE(0)#	52
53	AD(6)	AD(5)	54
55	AD(4)	GND	56
57	+3.3V	AD(3)	58
59	AD(2)	AD(1)	60
61	AD(0)	+5V	62
63	GND	REQ64#	64

NC = NO CONNECT

PU = PULLUP

6.2.6.2 J22 Upper PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	+12V	NC	2
3	JTAG_TMS	JTAG_TDO	4
5	JTAG_TDI	GND	6
7	GND	NC	8
9	NC	NC	10
11	PU to 3.3V	+3.3V	12
13	RST#	GND	14
15	+3.3V	GND	16
17	NC	GND	18
19	AD(30)	AD(29)	20
21	GND	AD(26)	22
23	AD(24)	+3.3V	24
25	AD(23) (IDSEL#)	AD(23)	26
27	+3.3V	AD(20)	28
29	AD(18)	GND	30
31	AD(16)	C/BE(2)#	32
33	GND	NC	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE(1)#	GND	44
45	AD(14)	AD(13)	46
47	M66EN	AD(10)	48
49	AD(8)	+3.3V	50
51	AD(7)	NC	52
53	+3.3V	NC	54
55	NC	GND	56
57	NC	NC	58
59	GND	NC	60
61	ACK64#	+3.3V	62
63	GND	NC	64

NC = NO CONNECT

PU = PULLUP

6.2.6.3 J23 Upper PMC Site PCI-X Connector

This standard 64-pin Molex 71439-0164 connector interfaces the PCI-X bus to the Lower PMC module.

PIN	SIGNAL	SIGNAL	PIN
1	NC	GND	2
3	GND	C/BE(7)#	4
5	C/BE(6)#	C/BE(5)#	6
7	C/BE(4)#	GND	8
9	+3.3V	PAR64	10
11	AD(63)	AD(62)	12
13	AD(61)	GND	14
15	GND	AD(60)	16
17	AD(59)	AD(58)	18
19	AD(57)	GND	20
21	+3.3V	AD(56)	22
23	AD(55)	AD(54)	24
25	AD(53)	GND	26
27	GND	AD(52)	28
29	AD(51)	AD(50)	30
31	AD(49)	GND	32
33	GND	AD(48)	34
35	AD(47)	AD(46)	36
37	AD(45)	GND	38
39	+3.3V	AD(44)	40
41	AD(43)	AD(42)	42
43	AD(41)	GND	44
45	GND	AD(40)	46
47	AD(39)	AD(38)	48
49	AD(37)	GND	50
51	GND	AD(36)	52
53	AD(35)	AD(34)	54
55	AD(33)	GND	56
57	+3.3V	AD(32)	58
59	NC	NC	60
61	NC	GND	62
63	GND	NC	64

NC = NO CONNECT

6.2.6.4 J24 Upper PMC Site Rear I/O Connector

This standard 64-pin Molex 71439-0164 connector brings the Rear I/O from the PMC/XMC module's P4 connector. The corresponding signals can be found on the VME P2 connector. The signals are routed as 100ohm differential pairs.

PIN	SIGNAL	SIGNAL	PIN
1	UPR_IO0_P	UPR_IO1_P	2
3	UPR_IO0_N	UPR_IO1_N	4
5	UPR_IO2_P	UPR_IO3_P	6
7	UPR_IO2_N	UPR_IO3_N	8
9	UPR_IO4_P	UPR_IO5_P	10
11	UPR_IO4_N	UPR_IO5_N	12
13	UPR_IO6_P	UPR_IO7_P	14
15	UPR_IO6_N	UPR_IO7_N	16
17	UPR_IO8_P	UPR_IO9_P	18
19	UPR_IO8_N	UPR_IO9_N	20
21	UPR_IO10_P	UPR_IO11_P	22
23	UPR_IO10_N	UPR_IO11_N	24
25	UPR_IO12_P	UPR_IO13_P	26
27	UPR_IO12_N	UPR_IO13_N	28
29	UPR_IO14_P	UPR_IO15_P	30
31	UPR_IO14_N	UPR_IO15_N	32
33	UPR_IO16_P	UPR_IO17_P	34
35	UPR_IO16_N	UPR_IO17_N	36
37	UPR_IO18_P	UPR_IO19_P	38
39	UPR_IO18_N	UPR_IO19_N	40
41	UPR_IO20_P	UPR_IO21_P	42
43	UPR_IO20_N	UPR_IO21_N	44
45	UPR_IO22_P	UPR_IO23_P	46
47	UPR_IO22_N	UPR_IO23_N	48
49	UPR_IO24_P	UPR_IO25_P	50
51	UPR_IO24_N	UPR_IO25_N	52
53	UPR_IO26_P	UPR_IO27_P	54
55	UPR_IO26_N	UPR_IO27_N	56
57	UPR_IO28_P	UPR_IO29_P	58
59	UPR_IO28_N	UPR_IO29_N	60
61	UPR_IO30_P	UPR_IO31_P	62
63	UPR_IO30_N	UPR_IO31_N	64

6.2.6.5 J25 Upper XMC Site PCIe Connector

This standard 114-pin Samtec ASP-103612-04 connector connects the PEG (PCIe) interface from the CPU to the Upper XMC module.

ROW/PIN	A	B	C	D	E	F
1	PEG8_RX_P	PEG8_RX_N	+3.3V	PEG9_RX_P	PEG9_RX_N	+5V
2	GND	GND	NC	GND	GND	PLT_RST#
3	PEG10_RX_P	PEG10_RX_N	+3.3V	PEG11_RX_P	PEG11_RX_N	+5V
4	GND	GND	JTAG_TCK	GND	GND	NC
5	PEG12_RX_P	PEG12_RX_N	+3.3V	PEG13_RX_P	PEG13_RX_N	+5V
6	GND	GND	JTAG_TMS	GND	GND	+12V
7	PEG14_RX_P	PEG14_RX_N	+3.3V	PEG15_RX_P	PEG15_RX_N	+5V
8	GND	GND	JTAG_TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	JTAG_TDO	GND	GND	GND (GA0#)
11	PEG0_TX_P	PEG0_TX_N	NC	PEG1_TX_P	PEG1_TX_N	+5V
12	GND	GND	GND (GA1#)	GND	GND	XMC_SEL#
13	PEG2_TX_P	PEG2_TX_N	NC	PEG3_TX_P	PEG3_TX_N	+5V
14	GND	GND	GND (GA2#)	GND	GND	SMB_DATA
15	PEG4_TX_P	PEG4_TX_N	NC	PEG5_TX_P	PEG5_TX_N	+5V
16	GND	GND	XMCA_WP	GND	GND	SMB_CLK
17	PEG6_TX_P	PEG6_TX_N	NC	PEG7_TX_P	PEG7_TX_N	NC
18	GND	GND	NC	GND	GND	NC
19	PEG_CLK_P	PEG_CLK_N	NC	NC	NC	NC

NC = NO CONNECT

XMC_SEL# = Auto-switches mux to route PEG lines to XMC instead of PMC bridge when XMC module is installed

6.2.6.6 J9 Upper PMC/XMC Site JTAG Connector

This 6-pin Molex 78171-5006 connector carries the Lower PMC or XMC module's JTAG interface. The VREF voltage can be selected between 2.5V, or 3.3V with SW5.

PIN	SIGNAL
1	JTAG_TDI
2	JTAG_TDO
3	GND
4	JTAG_TCK
5	JTAG_TMS
6	JTAG_VREF

6.2.6.7 J7 Upper PMC/XMC Site Expansion Connector

This 60-pin Samtec QSH-030-01-L-D-A-K connector is used for I/O connection to the optional XBRD-9060 I/O Expander module.

PIN	SIGNAL	SIGNAL	PIN
1	ENET1_MDI2_N[1]	ENET1_MDI0_N[1]	2
3	ENET1_MDI2_P[1]	ENET1_MDI0_P[1]	4
5	GND	GND	6
7	ENET1_MDI3_N[1]	ENET1_MDI1_N[1]	8
9	ENET1_MDI3_P[1]	ENET1_MDI1_P[1]	10
11	GND	GND	12
13	SATA1_TX_N	SATA0_TX_N	14
15	SATA1_TX_P	SATA0_TX_P	16
17	GND	GND	18
19	SATA1_RX_N	SATA0_RX_N	20
21	SATA1_RX_P	SATA0_RX_P	22
23	GND	GND	24
25	Reserved	Reserved	26
27	Reserved	Reserved	28
29	GND	GND	30
31	Reserved	Reserved	32
33	Reserved	Reserved	34
35	GND	GND	36
37	USB2_N	USB3_N	38
39	USB2_P	USB3_P	40
41	SMB_CLK	SMB_DATA	42
43	+5V	+5V	44
45	USB_OC#	ENET1_ACT#	46
47	+5V	ENET1_LINK#	48
49	PLT_RST#	COM3_TXD	50
51	+3.3V	+3.3V	52
53	NC	COM3_RXD	54
55	+3.3V	GND	56
57	ENET1_SEL#	+3.3V	58
59	+3.3V	+1.5V	60

NC = NO CONNECT

[1] ENET1 signals may instead be switched to XBRD-9060 I/O Expander module, if installed.

[2] ENET1_SEL# Auto-switches ENET1 signals to XBRD-9060 when low.

6.2.7 Front Panel Connectors

6.2.7.1 J5 COM/USB/VGA Connector

This standard 26-pin D-SUB, TE 5748481-5 connector brings 2 USB, 1 VGA, and 1 RS-232 Serial Ports out the front panel. These can be accessed through standard connectors by using the supplied shielded dongle cable (P/N 4001128).

Note: The DB-9 serial connector on this dongle cable is wired as a DTE port.

PIN	SIGNAL
1	GND
2	USB0_P
3	USB0_N
4	GND
5	+5V USB
6	VGA_I2C_DAT
7	VGA_RED
8	VGA_GRN
9	VGA_BLUE
10	GND
11	USB1_P
12	USB1_N
13	GND
14	+5V VGA
15	VGA_I2C_CLK
16	GND_RED
17	GND_GREEN
18	GND_BLUE
19	COM1_CTS#
20	COM1_RTS#
21	COM1_DSR#
22	COM1_DTR#
23	COM1_TXD
24	COM1_RXD
25	VGA_VSYNC
26	VGA_HSYNC

6.2.7.2 J4 Dual Ethernet RJ Point 5 Connector

This 16-pin RJ-Point-Five Connector, TE 2170129-1, brings 2 Gigabit Ethernet ports out the front panel. These can be accessed through standard RJ-45 connectors by using the supplied adapter cables.

Note: Patch cables of various lengths with RJ Point 5 connectors on one end and standard RJ-45 connectors on the other are available from TE and Stewart Connector.

PIN	SIGNAL
1A	ENET2_MX0_P
2A	ENET2_MX0_N
3A	ENET2_MX1_P
4A	ENET2_MX1_N
5A	ENET2_MX2_P
6A	ENET2_MX2_N
7A	ENET2_MX3_P
8A	ENET2_MX3_N
1B	ENET3_MX0_P
2B	ENET3_MX0_N
3B	ENET3_MX1_P
4B	ENET3_MX1_N
5B	ENET3_MX2_P
6B	ENET3_MX2_N
7B	ENET3_MX3_P
8B	ENET3_MX3_N

6.2.8 P3 CPU Fan Connector

This 5-pin connector, Molex 53398-0571, can be used to power a 5V fan in situations where more cooling is necessary.

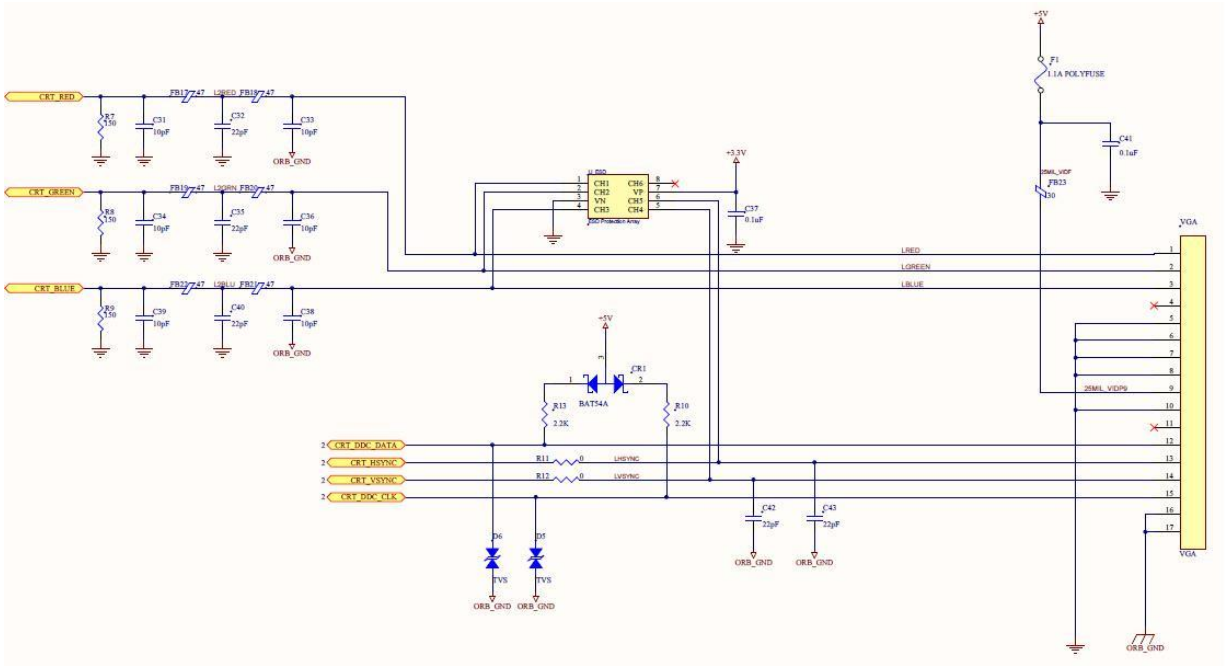
PIN	SIGNAL
1	NO CONNECT
2	FAN TACH
3	GND
4	FAN PWM
5	+5V

6.3 P2 I/O Signal Requirements

This section provides the information necessary to interface with the P2 I/O signals, without using a XVME-9640 RTM module.

6.3.1 VGA

For proper operation of the VGA display, 150ohm termination to GND is required on the CRT_REAR_RED, CRT_REAR_GREEN and CRT_REAR_BLUE signals. Failure to apply this termination may result in poor display quality and improper operation of Intel® HD Graphics control panel in Windows®. Also for proper monitor detection, the REAR_DDC_CLK and REAR_DDC_DATA lines should be level shifted to +5V. See the following for suggested interface schematic:



6.3.2 ESD

It is strongly suggested that ESD protection be included in interface circuitry on the VGA and USB ports. Failure to do so may cause damage the XVME-6500 in the event of an ESD discharge into the I/O pins.

6.4 Power Requirements

The power required to properly operate the XVME-6500 module will vary depending on many variables, including the operating system, application software, and the components that the module is integrated with. See notes below for defined variables used to measure the following power values:

+5VDC (+5/-3%) when the backplane supplies +3.3V

All configurations	S0 Idle[1]:	27.8W	
i7-4700EQ CPU			
	S0 Max[2]:	73.5W/86.1W	S0 Typ[3]: 50W
i7-4700EQ CPU (cTDP = 37W)			
	S0 Max[2]:	63W/73.5W	S0 Typ[3]: 50W

For systems with backplanes that do not supply 3.3V, add ~2.5W to the above 5V values.

+3.3VDC (+5/-2%) when the backplane supplies +3.3V

All configurations	S0 Idle[1]:	2.5W
	S0 Max[2]:	2.6W
	S0 Typ[3]:	2.5W

[1] S0 Idle was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System, idle at desktop with no active applications running. 16GB RAM. One connected SATA device, one USB keyboard, one USB mouse, VGA monitor. No PMC/XMC cards installed.

[2] S0 Max was measured with module operating at 40°C ambient with 300LFM airflow, using Windows 8.1 Operating System. Prime95 Large FFT torture test stressing all CPU cores at max. 16GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, VGA monitor, DVI monitor. No PMC/XMC cards installed. At temperatures above this, the CPU throttling during heavy CPU usage reduces the maximum power consumed more than it is raised from the increase in temperature.
With Turbo on, power is shown as PL1/PL2, where PL1 is the long-term power used, and PL2 is a short-term (typically <30 sec) power draw during turbo bursts. If Turbo is not used the board should not exceed the PL1 power, but performance may be impacted.

[3] S0 Typ was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System. Passmark Burn-In test running the following tests: CPU, Memory, 2D Graphics, 3D Graphics, Disk, and Network. 16GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, VGA monitor, DVI monitor. No PMC/XMC cards installed.

6.5 Environmental Considerations

Operating Temperature:
0°C to 70°C (Standard Air-Cooled models)[1]
-40°C to 75°C (Extended Air-Cooled models)[1]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification. Tested under Windows 8.1 with Passmark BurnInTest V7.1, running CPU, Memory, and 3D Graphics tests simultaneously. During application testing CPU temp should be closely monitored for max junction temp of 100°C using a program such as Argus Monitor or Open Hardware Monitor.

Note: CPU frequency throttling will occur if the CPU Tj temperature reaches 100°C. This is an effective mechanism to keep the unit from overheating. A small amount of intermittent throttling at higher ambient temperatures is to be expected and does not greatly affect system performance. For systems that need maximum performance at higher ambient temperatures and can handle the XVME-6500 consuming an extra slot, a larger heatsink is available as an accessory. Consult factory for more information.

WARNING: ***If airflow is not adequate, throttling can reach maximum and Tj temperature could exceed 100℃ resulting in system instability. This temperature should be monitored in end user system with user application software running to determine if final thermal solution is adequate.***

Relative Humidity: 5% to 95% Non-condensing (designed to comply)

Storage Temperature: -55°C to 105°C (designed to comply)

Shock, Operating: 30g peak acceleration, 11ms duration half-sine shock in all three axes in accordance with MIL-STD-810, Method 516, Procedure I

Vibration, Operating: Class V2 plug-in unit in accordance with MIL-STD-810, Method 514, Procedure I, one hour per axis

- 5Hz to 100Hz, PSD increasing at 3 dB/octave
- 100Hz to 1000Hz, PSD = 0.04 g2/Hz
- 1000Hz to 2000Hz, PSD decreasing at 6 dB/octave

EMC Directives: The XVME-6510 complies with EMC Directive 2014/30/EU.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2, Level 2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3, Class A.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4. Class A.
  Surge Immunity, per IEC 61000-4-5, Class A.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6, Class A.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16-2-3 Class A.
  Low Voltage AC Mains Port, per CISPR 16-2-3 Class A.

6.6 Reliability Prediction

Table 6.6.a: MTBF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	201,131	23.0	4,971.9
40°C	147,044	16.8	6,800.7

[1] FIT is Failures in 10^9 hours.

6.7 XVME-6500 Certificate of Volatility

Certificate of Volatility				
Acromag Model XVME-65XX-XXXXX-XX	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) SDRAM	Size: Up to 16GB (depends on SODIMM modules installed)	User Modifiable ■ Yes □ No	Function: Storage of code/data for CPU	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.) PCH internal CMOS SRAM	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Data storage for system/BIOS	Process to Sanitize: Remove Battery BT1 from socket.
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash (Qty: 2)	Size: 16Mbyte	User Modifiable ■ Yes □ No	Function: U6: Storage of Code and Data for System/BIOS U1: FPGA firmware	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash
Type(EEPROM, Flash, etc.) EEPROM (Qty: 2)	Size: 16Kbytes each	User Modifiable ■ Yes □ No	Function: U47: Ethernet Firmware/MAC ID U14: PEX8114 Bridge Config	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type(EEPROM, Flash, etc.) EEPROM	Size: 256bytes	User Modifiable ■ Yes □ No	Function: U20: Module ID and/or User Data	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type (EEPROM, Flash, etc.) NAND Flash memory	Size: 32GB	User Modifiable ■ Yes □ No	Function: U19: User data storage	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash

Acromag Representative				
Name: Russ Nieves	Title: Dir. of Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-624-0310	Office Fax: 248-624-9234

7.0 XBRD-9060 I/O Expander Accessory Module

The optional XBRD-9060 module may be installed in the Upper Site of an air-cooled XVME-6500 to bring more I/O to the front panel, as well as allow mSATA SSD modules to be added for storage.

The following I/O is available on the front panel of the XBRD-9060:

- One Gigabit Ethernet port via a standard RJ-45 connector. When this port is enabled on the XBRD-9060 module, one of the Ethernet ports on the P0 connector is disabled.
- One RS-232 serial port. This port only contains TX/RX signals. It is brought out on a mini USB-B connector, but an adapter cable is included with the module for connection using a standard DB-9 connector.
- Two USB 2.0 ports. These ports use standard USB-A connectors.

The XBRD-9060 also contains 2 mSATA sockets that allow 2 SSD drives to be added to the XVME-6500 while still remaining within a single VME slot. Using the software RAID functionality of the QM87 PCH, these drives can even be setup as a RAID0/1 array if redundancy or extra speed is desired.

7.1 Ordering Information

The XBRD-9060 is only available in a lead-free solder model. The full model number is XBRD-9060-LF.

7.2 Hardware Information and Configuration

7.2.1 Switch SW1 Configuration

Table 7.2.1.a summarizes the functions, settings, and descriptions for dip switch SW1.

Table 7.2.a: XBRD-9060 Configuration Switch SW1

Configuration Switch SW1			
Position	**Function**	**Switch Setting**	**Description**
1-3	Ethernet Port Enable	1-2	Front Panel Ethernet Port Enabled
		2-3	Front Panel Ethernet Port Disabled
4-6	ORB GND	4-5	ORB GND tied to Digital GND
		5-6	ORB GND Isolated

SW1:1-3 is used to configure the front panel Ethernet port. When this port is enabled the ETH1 signals are not available on the XVME-6500's P0 connector.

SW1:4-6 is used to configure the isolation of the Front Panel (ORB) GND.

7.3 mSATA Module Installation

One or two full-size (51mm) mSATA modules may be installed by using the screws provided. In a high-vibration environment the addition of a removable thread locker, such as Loctite 242, is recommended. For installation of half-size (26.8mm) mSATA modules please consult factory.

7. 4 Installation onto XVME-6500

The XBRD-9060 is installed onto the XVME-6500 in the same fashion as a PMC/XMC module. First insert the XBRD-9060 through the front panel at an angle, and then bring the back of the module down to seat into the expansion connector. Once the module is seated in the connector, install the four screws provided from the back side of the XVME-6500.

In a high-vibration environment the addition of a removable thread locker, such as Loctite 242, is recommended.

7.5 Specifications

7.5.1 Physical

The XBRD-9060 dimensions are shown below:

Length	128.0 mm (5.039 in)
Width	74..0 mm (2.913 in)
Height from XVME-6500 (includes PCB)	12.6 mm (0.496 in)
Unit Weight	2.3 oz (0.067 kg)

7.5.2 Connector Information

7.5.2.1 J3 Expansion Connector

This 60-pin Samtec QTH-030-03-L-D-A-K connector is used for I/O connection to the XVME-6500 CPU module.

PIN	SIGNAL	SIGNAL	PIN
1	ENET1_MDI2_N[1]	ENET1_MDI0_N[1]	2
3	ENET1_MDI2_P[1]	ENET1_MDI0_P[1]	4
5	GND	GND	6
7	ENET1_MDI3_N[1]	ENET1_MDI1_N[1]	8
9	ENET1_MDI3_P[1]	ENET1_MDI1_P[1]	10
11	GND	GND	12
13	SATA1_TX_N	SATA0_TX_N	14
15	SATA1_TX_P	SATA0_TX_P	16
17	GND	GND	18
19	SATA1_RX_N	SATA0_RX_N	20
21	SATA1_RX_P	SATA0_RX_P	22
23	GND	GND	24
25	Reserved	Reserved	26
27	Reserved	Reserved	28
29	GND	GND	30
31	Reserved	Reserved	32
33	Reserved	Reserved	34
35	GND	GND	36
37	USB2_N	USB3_N	38
39	USB2_P	USB3_P	40
41	SMB_CLK	SMB_DATA	42
43	+5V	+5V	44
45	USB_OC#	ENET1_ACT#	46
47	+5V	ENET1_LINK#	48
49	PLT_RST#	COM3_TXD	50
51	+3.3V	+3.3V	52
53	NC	COM3_RXD	54
55	+3.3V	GND	56
57	ENET1_SEL#	+3.3V	58
59	+3.3V	+1.5V	60

NC = NO CONNECT

[1] ENET1 signals are not available when SW1 is in position 2-3.

[2] ENET1_SEL# enables ENET1 signals when SW1 is in position 1-2.

7.5.2.2 J7 Ethernet Connector

This standard 8-pin RJ-45 connector, Bel Fuse L834-1G1T-S7, is for connection to an Ethernet network. The port can auto-sense 10-Base-T, 100Base-T, and 1000Base-TX connections. LIINK and ACTIVITY LEDs are built-in to the connector.

PIN	SIGNAL
1	ENET1_MX_P[1]
2	ENET1_MX_N[1]
3	ENET1_MX1_P[1]
4	ENET1_MX2_P[1]
5	ENET1_MX2_N[1]
6	ENET1_MX1_N[1]
7	ENET1_MX3_P[1]
8	ENET1_MX3_N[1]

[1] ENET1 signals are not available when SW1 is in position 2-3.

7.5.2.3 J2 RS-232 Serial Connector

This 5-pin USB-mini-B style connector, TE 1734035-2, is used for the COM3 RS-232 serial port connection.

PIN	SIGNAL
1	NC
2	COM3_RXD
3	COM3_TXD
4	NC
5	GND

7.5.2.4 RS-232 Serial Adapter Cable

Use the included shielded adapter cable to have a standard DB-9 connector wired as a DTE port.

PIN	SIGNAL
1	NC
2	COM3_TXD
3	COM3_RXD
4	NC
5	GND
6	NC
7	NC
8	NC
9	NC

7.5.2.5 J4 USB 2.0 Connector

This 9-pin USB 3.0 A-style, FCI 10117835-001LF, connector carries USB data at either USB 2.0 or USB 1.1 speeds. The power is current limited to 1A.

Note: Even though the connector is a USB 3.0 connector, it will only function at USB 2.0 or lower speeds. There is no USB 3.0 superspeed signal connection.

PIN	SIGNAL
1	+5V USB POWER
2	USB2_N
3	USB2_P
4	GND
5	NC
6	NC
7	GND
8	NC
9	NC

7.5.2.6 J5 USB 2.0 Connector

This 9-pin USB 3.0 A-style, FCI 10117835-001LF, connector carries USB data at either USB 2.0 or USB 1.1 speeds. The power is current limited to 1A.

Note: Even though the connector is a USB 3.0 connector, it will only function at USB 2.0 or lower speeds. There is no USB 3.0 superspeed signal connection.

PIN	SIGNAL
1	+5V USB POWER
2	USB3_N
3	USB3_P
4	GND
5	NC
6	NC
7	GND
8	NC
9	NC

7.5.2.7 J1 mSATA Connector

This standard 52-pin mSATA connector, TE 2041119-1, is used for connecting an mSATA drive module to the XBRD-9060.

PIN	SIGNAL	SIGNAL	PIN
1	NC	+3.3V	**2**
3	NC	GND	**4**
5	NC	+1.5V	**6**
7	NC	NC	**8**
9	GND	NC	**10**
11	NC	NC	**12**
13	NC	NC	**14**
15	GND	NC	**16**
17	NC	GND	**18**
19	NC	NC	**20**
21	GND	PLT_RST#	**22**
23	SATA0_RX_N	+3.3V	**24**
25	SATA0_RX_P	GND	**26**
27	GND	+1.5V	**28**
29	GND	SMB_CLK	**30**
31	SATA0_TX_N	SMB_DATA	**32**
33	SATA0_TX_P	GND	**34**
35	GND	NC	**36**
37	GND	NC	**38**
39	+3.3V	GND	**40**
41	+3.3V	NC	**42**
43	GND	NC	**44**
45	NC	NC	**46**
47	NC	+1.5V	**48**
49	NC	GND	**50**
51	NC	+3.3V	**52**

NC = NO CONNECT

7.5.2.8 J6 mSATA Connector

This standard 52-pin mSATA connector, TE 2041119-1, is used for connecting an mSATA drive module to the XBRD-9060.

PIN	SIGNAL	SIGNAL	PIN
1	NC	+3.3V	2
3	NC	GND	4
5	NC	+1.5V	6
7	NC	NC	8
9	GND	NC	10
11	NC	NC	12
13	NC	NC	14
15	GND	NC	16
17	NC	GND	18
19	NC	NC	20
21	GND	PLT_RST#	22
23	SATA1_RX_N	+3.3V	24
25	SATA1_RX_P	GND	26
27	GND	+1.5V	28
29	GND	SMB_CLK	30
31	SATA1_TX_N	SMB_DATA	32
33	SATA1_TX_P	GND	34
35	GND	NC	36
37	GND	NC	38
39	+3.3V	GND	40
41	+3.3V	NC	42
43	GND	NC	44
45	NC	NC	46
47	NC	+1.5V	48
49	NC	GND	50
51	NC	+3.3V	52

NC = NO CONNECT

7.6 Power Requirements

The power used by the XBRD-9060 board without any mSATA modules installed is negligible.

mSATA power draws from the available +3.3V on the XVME-6500. +1.5V is also available, but usage of this voltage on mSATA modules is not widespread.

7.7 Environmental Considerations

Operating Temperature:

-40°C to 75°C[1]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification.

Note: Temperature rating is exclusive of mSATA module(s). Commercial grade mSATA modules are normally rated 0°C to 70°C.

Relative Humidity: 5% to 95% Non-condensing (designed to comply)

Storage Temperature: -55° C to 100° C (designed to comply)

7.8 Reliability Prediction

Table7.8.a: MTBF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	16,280,016	1,858.4	61.4
40°C	10,353,596	1,181.9	96.6

[1] FIT is Failures in 10^9 hours.

7.9 XBRD-9060 Certificate of Volatility

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
XBRD-9060-XX</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
□ Yes ■ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)
none</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No (only with mSATA module(s) installed)</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)
Flash</td><td>Size:
mSATA module dependent</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Storage of User Data</td><td colspan="2">Process to Sanitize:
Refer to mSATA module documentation</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Joseph Primeau</td><td>Title:
Dir. of Sales and Marketing</td><td colspan="2">Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td>Office Fax:
248-624-9234</td></tr>
</table>

8.0 XVME-9640 Rear-Transition Accessory Module

The optional XVME-9640 module may be installed into the rear slot directly behind the XVME-6500 to easily access all of the available I/O on the XVME-6500's P2, and optionally P0 connectors, as well as allow mSATA SSD modules to be added for storage.

The following I/O is available on the front panel of the XVME-9640:

- Two Gigabit Ethernet ports are available on the front panel's optional RJ Point 5 connector (installed if the optional RJ0 connector is installed). One adapter cable is included with the XVME-9640 to connect from the front panel's RJ Point 5 connector to a standard RJ45 connector.
- One VGA port via standard DB-15 connector.
- One DVI-D port via standard 24-pin DVI connector.
- Two USB 2.0 ports. These ports use standard USB-A connectors.
- The Upper PMC/XMC module's P4 user I/O from the XVME-6500's P2 connector is available via a 68-pin SCSI-3 connector.

The following I/O is available via internal connectors on the XVME-9640:

- Stereo Audio Line-In & Line-Out are available via a 5-pin connector.
- One software-selectable RS-232/RS-485 serial port is available via a 10-pin header.
- The Lower PMC/XMC module's user I/O from the XVME-6500's optional RJ0 connector is available via two optional high-speed Samtec connectors (installed if the optional P0 connector is installed).

The XVME-9640 also contains 2 mSATA sockets that allow 2 SSD drives to be added while still remaining within a single VME slot. Using the software RAID functionality of the QM87 PCH, these drives can even be setup as a RAID0/1 array if redundancy or extra speed is desired.

WARNING: mSATA requires P0 on both the XVME-6500 and XVME-9640 for proper operation.

Note: The standard XVME-9640 cannot be used in a backplane that uses VITA 31.1 Ethernet. A custom build option is available that isolates the Ethernet lines for use in a VITA 31.1 system. Please consult factory for this option.

WARNING: The XVME-9640 should not be used with an XVME-6500 that is built with the 'XVME-6300 Compatible I/O' option. For this option instead use the XVME-9630 module (RTM for XVME-6300).

8.1 Ordering Information

The XVME-9640 is only available in a lead-free solder model. When ordering the XVME-9640-A-LF VMEbus CPU module, please select from and specify the available connector options (A) as defined below:

- Select the connector option (A):
  - ✓ 1: With RJ0, P3, P4, J8 Installed
  - ✓ 2: RJ0, P3, P4, J8 Not Installed – no mSATA

8.2 Hardware Information and Configuration

8.2.1 Switch SW1 Configuration

Table 8.2.1.a summarizes the functions, settings, and descriptions for dip switch SW1.

Table 8.2.1.a: XVME-9640 Configuration Switch SW1

Configuration Switch SW1			
Position	**Function**	**Switch Setting**	**Description**
1	Not Used		
2	Not Used		
3	Not Used		
4	ORB GND	OFF (default)	ORB GND Isolated from Digital GND
		ON	ORB GND Tied to Digital GND

SW1-4 is used to configure the isolation of the Front Panel (ORB) GND.

SW1-1, 1-2, and 1-3 are not used and can be in either position for normal operation.

8.3 mSATA Module Installation

One or two full-size (51mm) mSATA modules may be installed using the screws provided. In a high-vibration environment the addition of a removable thread locker, such as Loctite 242, is recommended. For installation of half-size (26.8mm) mSATA modules please consult factory.

8.4 Specifications

8.4.1 Physical

The XVME-9640 dimensions are shown below:

Height	233.35 mm (9.187 in)
Depth	80mm (3.150 in)
Minimum Backplane Pitch	20.32 mm (0.8 in)
Unit Weight (with RJ0, P3, P4, J8 installed)	7.8 oz (0.221 kg)

8.4.2 Connector Information

8.4.2.1 RJ0 VME Connector (Optional)

This optional connector is a standard 6-row, 2mm Type B, 95-pin Harting 17-25-095-2102. It contains 2 Ethernet and the Lower Site's PMC/XMC I/O.

ROW/PIN	A	B	C	D	E	F
1	GND	GND	GND	GND	GND	GND
2	ENET0_MX0_P	ENET0_MX0_N	GND	ENET0_MX2_P	ENET0_MX2_N	
3	ENET0_MX1_P	ENET0_MX1_N	GND	ENET0_MX3_P	ENET0_MX3_N	GND
4	ENET1_MX0_P[1]	ENET1_MX0_N[1]	GND	ENET1_MX2_P[1]	ENET1_MX2_N[1]	
5	ENET1_MX1_P[1]	ENET1_MX1_N[1]	GND	ENET1_MX3_P[1]	ENET1_MX3_N[1]	GND
6	ENET1_LINK#	ENET0_LINK#	+3.3V_FROM_CPU	ENET1_ACT#	ENET0_ACT#	
7	LWR_IO0_P	LWR_IO2_P	LWR_IO2_N	LWR_IO3_P	LWR_IO3_N	GND
8	LWR_IO0_N	LWR_IO4_P	LWR_IO4_N	LWR_IO5_P	LWR_IO5_N	
9	LWR_IO8_P	LWR_IO6_P	LWR_IO6_N	LWR_IO7_P	LWR_IO7_N	GND
10	LWR_IO8_N	LWR_IO1_P	LWR_IO1_N	LWR_IO9_P	LWR_IO9_N	
11	LWR_IO12_P	LWR_IO10_P	LWR_IO10_N	LWR_IO11_P	LWR_IO11_N	GND
12	LWR_IO12_N	LWR_IO25_N	LWR_IO25_P	LWR_IO13_P	LWR_IO13_N	
13	LWR_IO16_P	LWR_IO14_P	LWR_IO14_N	LWR_IO15_P	LWR_IO15_N	GND
14	LWR_IO16_N	LWR_IO31_N	LWR_IO31_P	LWR_IO17_P	LWR_IO17_N	
15	LWR_IO20_P	LWR_IO18_P	LWR_IO18_N	LWR_IO19_P	LWR_IO19_N	GND
16	LWR_IO20_N	LWR_IO29_N	LWR_IO29_P	LWR_IO21_P	LWR_IO21_N	
17	LWR_IO24_P	LWR_IO22_P	LWR_IO22_N	LWR_IO23_P	LWR_IO23_N	GND
18	LWR_IO24_N	LWR_IO26_N	LWR_IO26_P	LWR_IO27_N	LWR_IO27_P	
19	NC	LWR_IO30_N	LWR_IO30_P	LWR_IO28_N	LWR_IO28_P	GND

NC = NO CONNECT

[1] ENET1 signals not available when enabled on XBRD-9060 I/O Expander module.

8.4.2.2 RJ2 VME Connector

This standard VME RTM 5-row, 160-pin Harting 02-04-160-1101 connector brings in standard PC I/O, as well as the Upper Site's PMC I/O.

Note: The signals on the 'A' and 'Z' rows is not available when installed in a legacy, 3-row backplane.

ROW/PIN	Z	A	B	C	D
1	UPR_IO0_P	SATA_TX2_P	+5V	AUD_OUT_R	DVI_P0_P
2	GND	SATA_TX2_N	GND	AUD_OUT_L	DVI_P0_N
3	UPR_IO0_N	GND	NC	AUD_GND	GND
4	GND	SATA_RX2_P	NC	AUD_IN_L	DVI_P1_P
5	UPR_IO1_P	SATA_RX2_N	NC	AUD_IN_R	DVI_P1_N
6	GND	UPR_IO16_N	NC	UPR_IO16_P	GND
7	UPR_IO1_N	SATA_TX3_P	NC	UPR_IO17_N	DVI_P2_P
8	GND	SATA_TX3_N	NC	UPR_IO17_P	DVI_P2_N
9	UPR_IO2_P	UPR_IO24_P	NC	VGA_RED	GND
10	GND	SATA_RX3_P	NC	VGA_GRN	DVI_CLK_P
11	UPR_IO2_N	SATA_RX3_N	NC	VGA_BLUE	DVI_CLK_N
12	GND	UPR_IO24_N	GND	VGA_VSYNC	GND
13	UPR_IO3_P	USB_P4_P	+5V	VGA_HSYNC	DVI_HPD
14	GND	USB_P4_N	NC	UPR_IO18_N	DVI_SDA
15	UPR_IO3_N	UPR_IO25_P	NC	VGA_I2C_DAT	DVI_SCL
16	GND	USB_P5_P	NC	VGA_I2C_CLK	UPR_IO8_P
17	UPR_IO4_P	USB_P5_N	NC	UPR_IO18_P	UPR_IO8_N
18	GND	UPR_IO25_N	NC	COM2_TX	UPR_IO9_P
19	UPR_IO4_N	USB_+5V	NC	COM2_TX-[1]	UPR_IO9_N
20	GND	USB_+5V	NC	UPR_IO19_N	UPR_IO10_P
21	UPR_IO5_P	UPR_IO26_P	NC	COM2_RX	UPR_IO1R_N
22	GND	UPR_IO26_N	GND	COM2_RX-[1]	UPR_IO11_P
23	UPR_IO5_N	UPR_IO27_P	NC	UPR_IO19_P	UPR_IO11_N
24	GND	UPR_IO27_N	NC	UPR_IO20_N	UPR_IO12_P
25	UPR_IO6_P	UPR_IO28_P	NC	UPR_IO20_P	UPR_IO12_N
26	GND	UPR_IO28_N	NC	UPR_IO21_N	UPR_IO13_P
27	UPR_IO6_N	UPR_IO29_P	NC	UPR_IO21_P	UPR_IO13_N
28	GND	UPR_IO29_N	NC	UPR_IO22_N	UPR_IO14_P
29	UPR_IO7_P	UPR_IO30_P	NC	UPR_IO22_P	UPR_IO14_N
30	GND	UPR_IO30_N	NC	UPR_IO15_N	UPR_IO15_P
31	UPR_IO7_N	UPR_IO31_P	GND	UPR_IO23_P	GND
32	GND	UPR_IO31_N	+5V	UPR_IO23_N	+5V

NC = NO CONNECT

[1] TX- and RX- only used when serial port is in RS-422/RS-485 mode

8.4.2.3 J1 VGA Connector

This standard 15-pin D-SUB, Kycon K66X-E15S-N-VESA connector brings the VGA port out the front panel.

PIN	SIGNAL
1	VGA_RED
2	VGA_GRN
3	VGA_BLUE
4	NC
5	GND
6	GND_RED
7	GND_GREEN
8	GND_BLUE
9	+5V VGA (1A MAX)
10	GND
11	NC
12	VGA_I2C_DAT
13	VGA_HSYNC
14	VGA_VSYNC
15	VGA_I2C_CLK

NC = NO CONNECT

8.4.2.4 J4 USB 2.0 Connector

This 4-pin USB 2.0 A-style, Molex 67329-8001, connector Brings USB port 4 out the front panel. The power is current limited to 1A (shared with J3).

PIN	SIGNAL
1	+5V USB POWER
2	USB4_N
3	USB4_P
4	GND

8.4.2.5 J3 USB 2.0 Connector

This 4-pin USB 2.0 A-style, Molex 67329-8001, connector Brings USB port 5 out the front panel. The power is current limited to 1A (shared with J4).

PIN	SIGNAL
1	+5V USB POWER
2	USB5_N
3	USB5_P
4	GND

8.4.2.6 J7 DVI-D Connector

This standard 29-pin DVI, Molex 74320-1004, connector brings the DVI port out the front panel. Only the digital signals are available on this connector. It can be used simultaneously with the VGA connector.

PIN	SIGNAL
1	DVI_P2_N
2	DVI_P2_P
3	GND
4	NC
5	NC
6	DVI_I2C_CLK
7	DVI_I2C_DAT
8	NC
9	DVI_P1_N
10	DVI_P1_P
11	GND
12	NC
13	NC
14	+5V DVI (1A MAX)
15	GND
16	HOT PLUG DETECT
17	DVI_P0_N
18	DVI_P0_P
19	GND
20	NC
21	NC
22	GND
23	DVI_CLK_P
24	DVI_CLK_N
C1	NC
C2	NC
C3	NC
C4	NC
C5	GND

NC = NO CONNECT

8.4.2.7 J8 Dual Ethernet RJ Point 5 Connector

This 16-pin RJ-Point-Five Connector, TE 2170129-1, brings 2 Gigabit Ethernet ports out the front panel. These can be accessed through standard RJ-45 connectors by using the supplied adapter cables.

Note: Patch cables of various lengths with RJ Point 5 connectors on one end and standard RJ-45 connectors on the other are available from TE and Stewart Connector.

PIN	SIGNAL
1A	ENET0_MX0_P
2A	ENET0_MX0_N
3A	ENET0_MX1_P
4A	ENET0_MX1_N
5A	ENET0_MX2_P
6A	ENET0_MX2_N
7A	ENET0_MX3_P
8A	ENET0_MX3_N
1B	ENET1_MX0_P[1]
2B	ENET1_MX0_N[1]
3B	ENET1_MX1_P[1]
4B	ENET1_MX1_N[1]
5B	ENET1_MX2_P[1]
6B	ENET1_MX2_N[1]
7B	ENET1_MX3_P[1]
8B	ENET1_MX3_N[1]

[1] ENET1 signals not available when enabled on XBRD-9060 I/O Expander module.

8.4.2.8 J5 Upper PMC/XMC User I/O Connector

This 68-pin SCSI-3 style, TE 5787082-7, connector carries the PMC/XMC module rear I/O from the Upper PMC/XMC site on the XVME-6500.

PIN	SIGNAL	SIGNAL	PIN
1	UPR_IO0_P	UPR_IO0_N	35
2	UPR_IO1_P	UPR_IO1_N	36
3	UPR_IO2_P	UPR_IO2_N	37
4	UPR_IO3_P	UPR_IO3_N	38
5	UPR_IO4_P	UPR_IO4_N	39
6	UPR_IO5_P	UPR_IO5_N	40
7	UPR_IO6_P	UPR_IO6_N	41
8	UPR_IO7_P	UPR_IO7_N	42
9	UPR_IO8_P	UPR_IO8_N	43
10	UPR_IO9_P	UPR_IO9_N	44
11	UPR_IO10_P	UPR_IO10_N	45
12	GND	GND	46
13	UPR_IO11_P	UPR_IO11_N	47
14	UPR_IO12_P	UPR_IO12_N	48
15	UPR_IO13_P	UPR_IO13_N	49
16	UPR_IO14_P	UPR_IO14_N	50
17	UPR_IO15_P	UPR_IO15_N	51
18	UPR_IO16_P	UPR_IO16_N	52
19	UPR_IO17_P	UPR_IO17_N	53
20	UPR_IO18_P	UPR_IO18_N	54
21	UPR_IO19_P	UPR_IO19_N	55
22	UPR_IO20_P	UPR_IO20_N	56
23	GND	GND	57
24	UPR_IO21_P	UPR_IO21_N	58
25	UPR_IO22_P	UPR_IO22_N	59
26	UPR_IO23_P	UPR_IO23_N	60
27	UPR_IO24_P	UPR_IO24_N	61
28	UPR_IO25_P	UPR_IO25_N	62
29	UPR_IO26_P	UPR_IO26_N	63
30	UPR_IO27_P	UPR_IO27_N	64
31	UPR_IO28_P	UPR_IO28_N	65
32	UPR_IO29_P	UPR_IO29_N	66
33	UPR_IO30_P	UPR_IO30_N	67
34	UPR_IO31_P	UPR_IO31_N	68

8.4.2.9 P4 Lower PMC/XMC User I/O Connector (Optional)

This optional 40-pin connector, Samtec QTH-020-01-F-D-DP-A-K, carries the PMC/XMC module rear I/O from the Lower PMC/XMC site on the XVME-6500.

PIN	SIGNAL	SIGNAL	PIN
1	LWR_IO0_P	LWR_IO10_P	2
3	LWR_IO0_N	LWR_IO10_N	4
5	LWR_IO1_P	LWR_IO11_P	6
7	LWR_IO1_N	LWR_IO11_N	8
9	LWR_IO2_P	LWR_IO12_P	10
11	LWR_IO2_N	LWR_IO12_N	12
13	LWR_IO3_P	LWR_IO13_P	14
15	LWR_IO3_N	LWR_IO13_N	16
17	LWR_IO8_P	LWR_IO9_P	18
19	LWR_IO8_N	LWR_IO9_N	20
21	LWR_IO20_P	LWR_IO21_P	22
23	LWR_IO20_N	LWR_IO21_N	24
25	LWR_IO22_P	LWR_IO23_P	26
27	LWR_IO22_N	LWR_IO23_N	28
29	LWR_IO24_P	LWR_IO25_P	30
31	LWR_IO24_N	LWR_IO25_N	32
33	LWR_IO26_P	LWR_IO27_P	34
35	LWR_IO26_N	LWR_IO27_N	36
37	LWR_IO28_P	LWR_IO29_P	38
39	LWR_IO28_N	LWR_IO29_N	40

8.4.2.10 P2 RS-232/RS-485 Serial Port

This 10-pin standard 0.1" header, TE 5103310-1, is used for the COM2 serial connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM2_RX-[1]	2
3	COM2_RX	NC	4
5	COM2_TX	NC	6
7	COM2_TX-[1]	NC	8
9	GND	GND	10

[1] TX- and RX- only used when serial port is in RS-422/RS-485 mode

8.4.2.11 P3 Lower PMC/XMC User I/O Connector (Optional)

This optional 40-pin connector, Samtec QTH-020-01-F-D-DP-A-K, carries the PMC/XMC module rear I/O from the Lower PMC/XMC site on the XVME-6500.

PIN	SIGNAL	SIGNAL	PIN
1	LWR_IO4_P	LWR_IO14_P	2
3	LWR_IO4_N	LWR_IO14_N	4
5	LWR_IO5_P	LWR_IO15_P	6
7	LWR_IO5_N	LWR_IO15_N	8
9	LWR_IO6_P	LWR_IO16_P	10
11	LWR_IO6_N	LWR_IO16_N	12
13	LWR_IO7_P	LWR_IO17_P	14
15	LWR_IO7_N	LWR_IO17_N	16
17	LWR_IO18_P	LWR_IO19_P	18
19	LWR_IO18_N	LWR_IO19_N	20
21	LWR_IO30_P	LWR_IO31_P	22
23	LWR_IO30_N	LWR_IO31_N	24
25	NC	NC	26
27	NC	NC	28
29	NC	NC	30
31	NC	NC	32
33	NC	NC	34
35	NC	NC	36
37	NC	NC	38
39	NC	NC	40

NC = NO CONNECT

8.4.2.12 P1 Audio Connector

This 5-pin connector, Molex 533980571, is used for the stereo audio line-in and line-out connections. The mate to this audio connector is Molex 0510210500 and the crimp is 0500588000 (for 28-32AWG).

PIN	SIGNAL
1	AUD_OUT_L
2	AUD_OUT_R
3	AUD_AGND
4	AUD_IN_L
5	AUD_IN_R

8.4.2.13 J6 mSATA Connector

This standard 52-pin mSATA connector, TE 2041119-1, is used for connecting an mSATA drive module to the XBRD-9060.

PIN	SIGNAL	SIGNAL	PIN
1	NC	+3.3V	2
3	NC	GND	4
5	NC	NC	6
7	NC	NC	8
9	GND	NC	10
11	NC	NC	12
13	NC	NC	14
15	GND	NC	16
17	NC	GND	18
19	NC	NC	20
21	GND	NC	22
23	SATA2_RX_N	+3.3V	24
25	SATA2_RX_P	GND	26
27	GND	NC	28
29	GND	NC	30
31	SATA2_TX_N	NC	32
33	SATA2_TX_P	GND	34
35	GND	NC	36
37	GND	NC	38
39	+3.3V	GND	40
41	+3.3V	NC	42
43	GND	NC	44
45	NC	NC	46
47	NC	NC	48
49	NC	GND	50
51	NC	+3.3V	52

NC = NO CONNECT

8.4.2.14 J2 mSATA Connector

This standard 52-pin mSATA connector, TE 2041119-1, is used for connecting an mSATA drive module to the XBRD-9060.

PIN	SIGNAL	SIGNAL	PIN
1	NC	+3.3V	2
3	NC	GND	4
5	NC	NC	6
7	NC	NC	8
9	GND	NC	10
11	NC	NC	12
13	NC	NC	14
15	GND	NC	16
17	NC	GND	18
19	NC	NC	20
21	GND	NC	22
23	SATA3_RX_N	+3.3V	24
25	SATA3_RX_P	GND	26
27	GND	NC	28
29	GND	NC	30
31	SATA3_TX_N	NC	32
33	SATA3_TX_P	GND	34
35	GND	NC	36
37	GND	NC	38
39	+3.3V	GND	40
41	+3.3V	NC	42
43	GND	NC	44
45	NC	NC	46
47	NC	NC	48
49	NC	GND	50
51	NC	+3.3V	52

NC = NO CONNECT

8.5 Power Requirements

The power used by the XVME-9640 board without any mSATA modules installed is negligible.

mSATA power draws from the available +3.3V on the XVME-6500.

Note: +1.5V is NOT available, but usage of this voltage on mSATA modules is not widespread.

8.6 Environmental Considerations

Operating Temperature:
-40°C to 75°C[1]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification.

Note: Temperature rating is exclusive of mSATA module(s). Commercial grade mSATA modules are normally rated 0°C to 70°C.

Relative Humidity: 5% to 95% Non-condensing (designed to compy)

Storage Temperature: -55° C to 100° C (designed to comply)

Shock, Operating: 30g peak acceleration, 11ms duration half-sine shock in all three axes in accordance with MIL-STD-810, Method 516, Procedure I

Vibration, Operating: Class V2 plug-in unit in accordance with MIL-STD-810, Method 514, Procedure I, one hour per axis

- 5Hz to 100Hz, PSD increasing at 3 dB/octave
- 100Hz to 1000Hz, PSD = 0.04 g2/Hz
- 1000Hz to 2000Hz, PSD decreasing at 6 dB/octave

EMC Directives: The XVME-9640 RTM complies with EMC Directive 2014/30/EU with the exception of DVI.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2, Level 2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3, Class A.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4, Class A.
  Surge Immunity, per IEC 61000-4-5, Class A.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6, Class A.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16-2-3, Class A.
  Low Voltage AC Mains Port, per CISPR 16-2-3, Class A.
  Note: This is a Class A product with the exception of DVI.

8.7 Reliability Prediction

Table 6.6.a: MTBF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	4,370,820	499.0	228.8
40°C	3,070,800	350.5	325.6

[1] FIT is Failures in 10^9 hours.

8.8 XVME-9640 Certificate of Volatility

Certificate of Volatility				
Acromag Model XVME-9640-X-XX	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Type (SRAM, SDRAM, etc.) none	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No **(only with Msata module(s) installed)**				
Type(EEPROM, Flash, etc.) Flash	Size: Msata module dependent	User Modifiable ■ Yes □ No	Function: Storage of User Data	Process to Sanitize: Refer to Msata module documentation

Acromag Representative				
Name: Joseph Primeau	Title: Dir. of Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
22 FEB 2016	A	ENZ/MJO	Initial Acromag release.
17 MAR 3016	B	ENZ/MJO	Added CE approval information. Changed default SSD write protect settings from hardware to software.
27 JAN 2017	C	BLD/DAG/ARP	Changed the name of the referenced BIOS manual to *The APTIO Haswell Core BIOS Manual For Acromag Products*. Updated Environmental Considerations sections. Updated P1 Audio Connector information.
23 MAY 2017	D	ENZ/MJO	Updated information on SW4 and reset behavior.
06 NOV 2017	E	ARP/CAB	Updated XVME-9640 Msata compatibility.
19 NOV 2018	F	ENZ/ARP	Added SSD NAND Flash to Certificate of Volatility. Added new model numbers for batteryless option.
11 NOV 2019	G	ENZ/ARP	Added MTBF information. Added new model ordering information. Added shock and vibe information for XVME-6500/6700 and XVME-9640-RTM. Corrected Section 8.4.2.9, 8.4.2.10 and 8.4.2.11 pinout table.

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