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Find the *Acroamatics Telemetry Systems 504V* at our website: ***Click HERE***

Model 504V

VME Data Distribution & Host Interface

Merges eight PCM frame synchronizers, IRIG time port, and analog-to-digital port

Distributes ID-tagged data to four high speed data streams

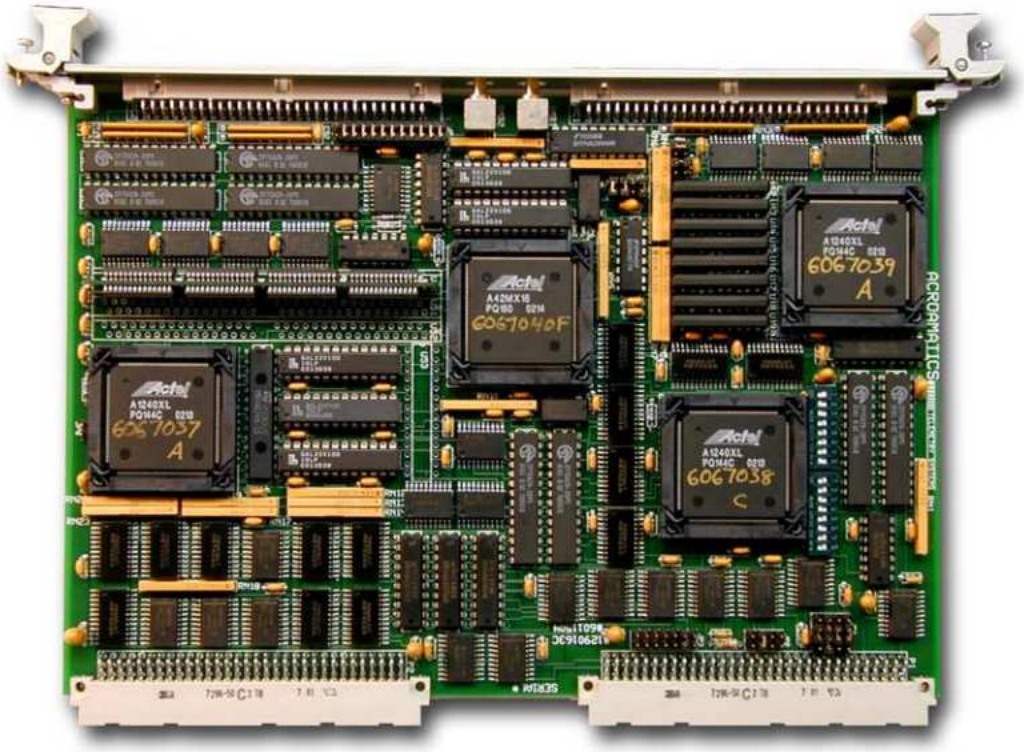
Provides for up to 64K unique ID tags

Provides for eight devices on the Device Output Bus

Host DMA channel routes processed data to memory or networking devices

DMA supports continuous block transfers of up to 64K 32-bit words

VME compatible 6U card



The Model 504V is the Data Distribution Interface, and is a core card of a TDP system. This card contains the data FIFO and the VME BUS DMA Interface, and contains the data token distribution system that is programmed to control each measurement in the data stream. It merges up to eight PCM frame synchronizers, IRIG time port and analog-to-digital port.

The card has a Current Value Table that captures data passing through the system, and contains 128K 32-bit words of algorithm program memory. The Distribution Interface usually requires a Model 505V VME Programmable Data Stream Processor to process the data.

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Model 504V VME Data Distribution & Host Interface

FEATURES

Input Bus

The Distribution System interfaces eight possible PCM frame synchronizers, an IRIG time port, and an analog-to-digital port. Two 32-bit words are multiplexed onto the bus and are queued to the Distribution System. The first word is the identifier that contains fine time, status, stream identification, and ID tag. The second word contains the data. The Distribution System supports up to 128k unique ID tags.

Distribution System

The Distribution System contains up to 256k 32-bit words of high speed static RAM. The ID tag accompanying each data sample addresses the lower 128k block of memory. The content of the word addressed by the tag is called the vector and points to the start of the processing table located in the upper 64k (256k optional) of memory. The processing table specifies the data stream processor, the algorithm to be performed, parameters required to process the raw input, and the final destination. The ID, data, and processing instructions are transmitted to four possible data stream processors across the bi-directional, 32-bit Distribution Bus.

Device Bus

Each stream processor performs a comprehensive set of algorithms for processing both floating point and integer data. The results of this processing are placed on the Device Bus. The Device Bus interfaces output devices such as: digital-to-analog outputs, digital discrete outputs, a feedback port to the Distribution input, and a VME Host DMA channel. The Device Bus supports up to eight output devices.

Host Interface

The Host Interface provides controls for single stepping and running the Distribution System and 505V Programmable Data Stream Processors, as well as outputting and receiving data on the Device Bus. The Host DMA channel provides a data path where processed data may be routed to memory and networking devices residing on the VME bus. The DMA circuitry includes bus master logic that supports continuous transfers of up to 64K 32-bit words.

GENERAL SPECIFICATIONS

Input Bus	Bandwidth 4M ID/Data samples per second, or 8M 32-bit words per second
Distribution Throughput	4M ID/Data samples per second without processing 2.6M ID/Data samples per second requiring processing
Device Bus Bandwidth	4M 16-bit data transfers per second
DMA Access Time	166ns from bus grant to falling edge of data strobe
DMA Recovery Time	115ns from rising edge of data acknowledge to data strobe falling

PHYSICAL

Format	Single Slot 6U VME
Cooling Requirements	30 Linear FPM
Power Requirements	+5VDC at 3 Amps
Temperature	Operating: 0º to +40º C, Non-Operating: -40º to +86º C
Relative Humidity	Up to 90% non-condensing
Shock	Operating: 6G, Non-Operating: 50G
Vibration	Operating: 0.5G, 5 to 2000Hz, Non-Operating: 1.2G, 5 to 500Hz

Specifications subject to change without notice

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