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IGLOO® Nano Starter Kit Quickstart Card

Introduction

IGLOO Nano Starter Kit provides a simple board with IGLOO nano AGLN250 device in the VQG100 package, Libero® System on Chip (SoC), and a Low-Cost Programming Stick (LCPS) for in-system programming. The IGLOO Nano Starter Kit is fully Restriction of Hazardous Substances (RoHS) compliant and enables you to quickly evaluate IGLOO family and prototype your design. The kit supports the following key functions:

- Detailed current monitoring capabilities of the industry's lowest power Field Programmable Gate Arrays (FPGA)
- Development with Microchip's Flash*Freeze technology
- Easy experimentation with In-System Programming (ISP), device serialization, and FlashLock on-chip system security
- USB-to-UART interface for HyperTerminal on PC connected to board
- On-board voltage regulation, enabling independent I/O bank voltages

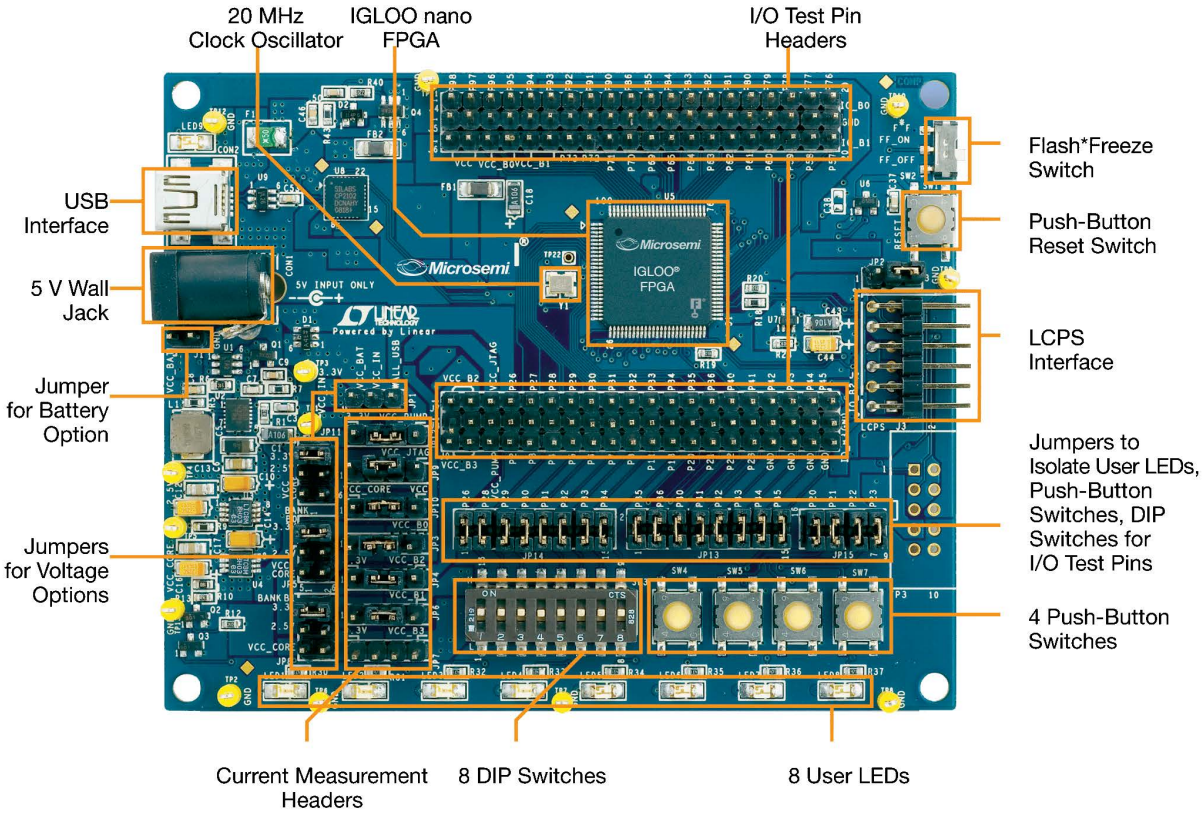
As IGLOO nano devices are footprint-compatible with ProASIC®3 nano devices, you can prototype designs for ProASIC3 nano and the low-power leader of IGLOO nano device.

Table 1. Kit Contents—AGLN-NANO-KIT

Quantity	Description
1	IGLOO® nano starter kit board with AGLN250V2-VQG100
1	LCPS
2	USB 2.0 A to mini-B cables
1	Quickstart card

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Figure 1. Kit Diagram



Jumper Settings

Set up the board with the default jumper settings listed in the following table. You require these settings to run the pre-programmed design. You must connect current measurement jumpers to permit the flow of current. The table order is from top to bottom and left to right on the board.

Table 2. Jumper Settings

Jumper	Pin	Comment
JP11[2]	1–2	Voltage selection for VCC_JTAG (JTAG supply), 3.3V. Pin 3–4 gives 2.5V, Pin 5–6 gives VCC_CORE
JP5[2]	1–2	Voltage selection for VCC_B0 (Bank 0), selecting 3.3V. Pin 3–4 gives 2.5V, Pin 5–6 gives VCC_CORE
JP8[2]	1–2	Voltage selection for VCC_B1 (Bank 1), selecting 3.3V. Pin 3–4 gives 2.5V, Pin 5–6 gives VCC_CORE
JP1[2]	2–3	Main power supply—connect Ic/USB input to VCC_IN
JP3	2–3	Current measurement header for Bank 0
JP4	2–3	Current measurement header for VCC_B2 (Bank 2)
JP6	2–3	Current measurement header for Bank 1
JP7	2–3	Current measurement header for VCC_B3 (Bank 3)

.....continued		
Jumper	**Pin**	**Comment**
JP9	2–3	Current measurement header for JTAG supply
JP10[1]	2–3	Current measurement header for VCC (FPGA core supply)
JP12	2–3	Current measurement header for VCC_PUMP (FPGA charge pump supply)
JP14	All	Dual pair jumpers must be placed on all locations
JP13	All	Dual pair jumpers must be placed on all locations
JP15	All	Dual pair jumpers must be placed on all locations
JP2[2]	2–3	VCC_CORE voltage (1.2V/1.5V), selecting 1.2V. Pin 1–2 selects 1.5V. Jumper is upper right of board

Notes:

1. To measure the device current, place a multimeter between Pin 2 and Pin 3 of JP10 (VCC_CORE). The multimeter must be able to read µA current range for Flash*Freeze mode.
2. Confirm the voltage selection jumper.

Running the Pre-Programmed Design

To power up the board, connect one end of the USB cable into a powered USB hub or a running PC and the other end to the board. On power-up, LED 9 indicates power, but the design is in reset. Press SW1 to activate the design and run it as indicated in the following table.

Table 3. Running the Pre-Programmed Design

Jumper	Setting	Comment
SW1	All 8 LEDs blinking	Do not care
SW2	Right Shift (LED1 to LED8)	Do not care
SW3	Left Shift (LED8 to LED1)	Do not care
SW4	LED on or off depending on DIP switch positions SW5 [1:8]	DIP switches control respective LEDs
SW7 (Reset)	All 8 LEDs off	Do not care

Flash*Freeze Mode and Power Measurement

Use the Flash*Freeze switch (SW6 F*F) to control Flash*Freeze mode. To enable Flash*Freeze mode, slide SW6 toward FF_ON, and to disable Flash*Freeze mode, slide SW6 toward FF_OFF. Flash*Freeze technology enables you to quickly (within 1 µs) enter and exit the Flash*Freeze mode by activating the Flash*Freeze pin, while all the power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be made to toggle without impact on power consumption; while the device retains all core registers, SRAM information, and I/O states. For more information about Flash*Freeze mode, see Documentation Resources.

Running the Flash*Freeze Demo

Press SW2 or SW3 to run the LEDs in either Right Shift or Left Shift mode. Use SW6 to activate the Flash*Freeze mode. The FPGA appears to be powered off and the LEDs are off. When you release Flash*Freeze, the sequence restarts from the same position, showing that register and I/O state are retained.

USB-UART Testing

For details on setting up and using the included UART, see Documentation Resources.

Switches and LEDs

To disconnect all switches and LEDs from the FPGA, remove the jumpers on JP15 for the four push-button switches SW[1:4], JP14 for the DIP switches SW5[1:8], and JP13 for the LED[1:8].

All the DIP switches, SW5[1:8], must be set to the closed ON state. This is the uppermost position of the switch.

Software and Licensing

Libero SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip's low power Flash FPGAs and SoC. The suite integrates industry standard Synplify Pro® synthesis and ModelSim® simulation with best-in-class constraints management and debug capabilities.

Download the latest Libero SoC release from Libero SoC v12.0 or later website.

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Documentation Resources

For more information about the IGLOO nano Starter Kit, including user's guides, tutorials, and design examples, see the documentation at www.microchip.com/en-us/development-tool/AGLN-NANO-KIT.

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