USER'S GUIDE

SCC-08

IP module:
Octal Serial Communication Controller

Edition 4003

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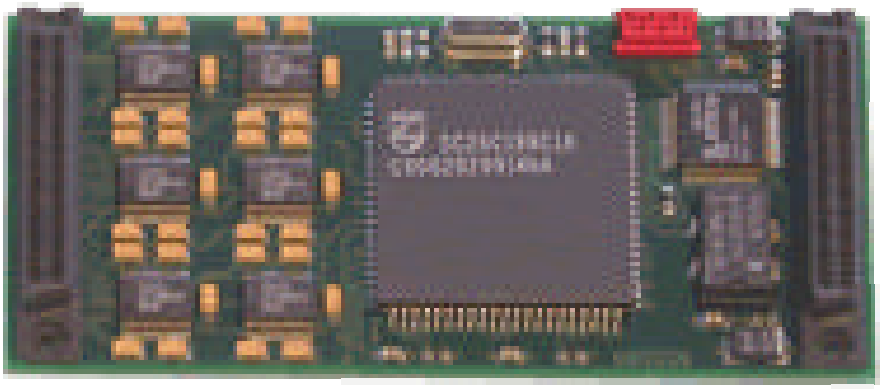
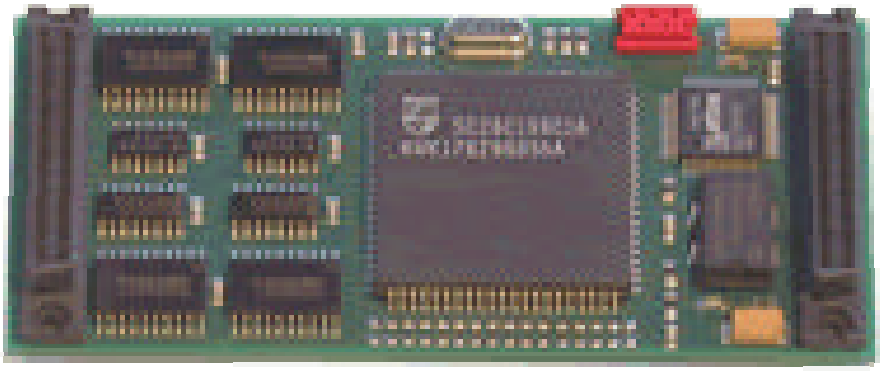


SCC-08A



SCC-08B

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1. Introduction

The SCC-08 module of ACTIS Computer S.A. is a high performance octal Serial Communication Controller according to the IP module specification. Two versions of this module are available:

Reference	Description
SCC-08A	Octal RS-232C serial channels
SCC-08B	Octal RS-422/RS-485 serial channels
SC-08	Transition module with: four RJ45 8-pin connectors, network terminators for RS-422/RS-485 interfaces and standard 4TEx3U front panel (Two SC-08 are required for one SCC-08)
SC-08D	Transition module with: eight RJ45 8-pin connectors, network terminators for RS-422/RS-485 interfaces and standard 4TEx6U front panel.
Option K	Engineering kit including: SCC-08A with two SC-08 and cables.

Both SCC-08 versions provide eight asynchronous full-duplex channels, with an independent Transmitter/Receiver baud rate generator for each channel. With its single chip SC26C198 octal UART device, the SCC-08 module has very high performance for date rate up to 115.2 kBaud with
RS-232D interfaces and up to 460.8 kBaud with RS-422/RS-485 interfaces.
The SCC-08A manages all modem signals with RS-232D interfaces, and the SCC-08B supports multi-drop capabilities with RS-422/RS-485 standard.
The single chip octal UART SC26C198 from Philips permits to minimize receiver overrun and the interrupt overhead through its larger FIFOs. For better FIFOs management, a watchdog function is able to generate a time-out interrupt when no characters are received after a fixed time (64 data rate clock).
Three programmable characters can be used for either an address recognition in multi-drop network or for hardware Xon/Xoff flow control. The SCC-08 control logic provides IP module timing access and the identification codes.

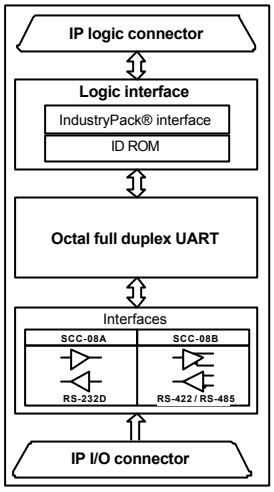
For both versions, the SCC-08 modules require only the 5 V power supply.
Two dedicated transition modules SC-08 (3U version, four ports) and SC-08D (6U version, eight ports) are available for easily user connection. For a complete 8-channel configuration, it is necessary to employ two SC-08 (3U version) which provide four serial channels on standard RJ45 8-pin connectors per module.
A complete industrial OS-9 environment is available for the SCC-08 modules.

2. Description

2.1. Summary of features

- Single-size IP module.
- Compatible with the IP module specification (Rev. 0.7.2).
- Eight asynchronous full-duplex serial communication channels.
- Separate transmitter/receiver baud rate generator for each channel.
- 16-Byte transmitter and 16-Byte receiver FIFOs on each channel.
- Data rate up to: 115.2 kBaud for SCC-08A (RS-232D).
- Data rate up to: 460.8 kBaud for SCC-08B (RS-422/RS-485).
- Manages all modem signals with RS-232D interfaces (SCC-08A).
- Support multi-drop 2-wire configuration (SCC-08B) with driver output enable through /RTS signal.
- Pseudo-synchronous transmission mode for the SCC-08A.
- Watchdog timer for each receiver.
- Three programmable characters for address recognition in multi-drop configuration and for Xon/Xoff flow control.
- Philips Octal UART SC26C198 controller.
- 5 V only power supply for both version.
- Industrial temperature grade available (-40 to +85 °C).

2.2. Block diagram



The hardware architecture of the SCC-08 is divided in 3 main sections:

- The IP module bus interface, controlling the timing access of the UART and the Identification memory.
- The SC26C198 Octal UART.
- The serial communication interface: RS-232D for the SCC-08A, or RS-422/RS-485 for the SCC-08B.

2.3. IP module spaces

The following table gives the four SCC-08 memory spaces.

MEM space	SC26C198 registers
ID space	IP module identification codes
I/O space	SC26C198 and board registers
INT Ack	Interrupt acknowledge

The base address of these spaces depends on the IP carrier.

The SCC-08 module supports the SC26C198 register access in both I/O and Memory space. In the Memory space, all the SC26C198 registers are directly accessible without page register use.

2.4. Memory space

When the SC26C198 is accessed through the memory space, all the eight UART address bits are directly driven by the IP bus.
For each channel, the SC26C198 registers are partitioned into two groups: the control and the data register.

Memory adr.	Register description	Acronym	Access
SC26C198 Control registers			
$01	Mode register 0 MR0 [a:h]	MR0	R/W
$03	Mode register 1 MR1 [a:h]	MR1	R/W
$05	I/O port config. reg. I/OPCR [a:h]	IOPCR	R/W
$07	Bid control, Break change [a:h]	BCRBRK	R/W
$09	Bid control, Change of state [a:h]	BCRCOS	R/W
$0D	Bid control, Xon/Xoff [a:h]	BCRX	R/W
$0F	Bid control, Address recognition [a:h]	BCRA	R/W
$11	Xon character [a:h]	XonCR	R/W
$13	Xoff character [a:h]	XoffCR	R/W
$15	Address recognition [a:h]	ARCR	R/W
$19	Receiver clock select [a:h]	RxCSR	R/W
$1D	Transmitter clock select [a:h]	TxCSR	R/W
SC26C198 Data registers			
$21	Mode register 2 [a:h]	MR2	R/W
$23	Status register [a:h]	SR	R
$23	Command register [a:h]	CR	W
$25	Interrupt status [a:h]	ISR	R
$25	Interrupt mask [a:h]	IMR	W
$27	Transmitter FIFO [a:h]	TxFIFO	W
$27	Receiver FIFO [a:h]	RxFIFO	R
$29	Input port register [a:h]	IPR	R
$2B	I/O port Interrupt and Output [a:h]	I/OPIOR	R/W
$2D	Xon/Xoff interrupt status [a:h]	XISR	R

Note:
Some control registers, for channels A and B, is used to configure the entire chip.

Data and control registers are independent for each channel (excepted global registers), in accordance for the corresponding address offset.

Memory Add.	Port	SC26C198
$001 $01D	A	Control registers
$021 $02D	A	Data registers
$041 $05D	B	Control registers
$061 $06D	B	Data registers
$081 $09D	C	Control registers
$0A1 $0AD	C	Data registers
$0C1 $0DD	D	Control registers
$0E1 $0ED	D	Data registers
$101 $11D	E	Control registers
$121 $12D	E	Data registers
$141 $15D	F	Control registers
$161 $16D	F	Data registers
$181 $19D	G	Control registers
$1A1 $1AD	G	Data registers
$1C1 $1DD	H	Control registers
$1E1 $1ED	H	Data registers

Global registers are accessible only at fixed address with the following map memory:

Memory adr.	Register description	Acronym	Access
SC26C198 GLOBAL Control registers			
$1B	• Test register	Reserved, set to 0	
$1F	• Global chip configuration	GCCR	R/W
$17	• Interrupt control	ICR	R/W
$1B	• Watch-dog timer run control	WDTRCR	R/W
$1F	• Interrupt vector	IVR	R/W
SC26C198 GLOBAL Data registers			
$2F	• GP output select	GPOSR	R/W
$31	• BRG timer register Upper a	BRGTRUa	R/W
$33	• BRG timer register Lower a	BRGTRLa	R/W
$35	• BRG timer control register a	BRGTCRa	R/W
$37	• GP output clk register	GPOC	R/W
$39	• Update current Interrupt	UCIR	W
$39	• Current interrupt	CIR	R
$3D	• Global receive Hold	GRxFIFO	R
$3D	• Global transmit hold	GTxFIFO	W
$3F	• Global chip configuration	GCCR	R/W
$2F	• Global output register	GPOR	R/W
$31	• BRG timer register Upper b	BRGTRUb	R/W
$33	• BRG timer register Lower b	BRGTRLb	R/W
$37	• GP output data register	GPOD	R/W
$39	• Global Interrupt channel	GICR	R
$3B	• Global interrupt byte count	GIBCR	R
$3F	• Global interrupt type	GITR	R

Notation:
The global registers are denoted by a "•" symbol.

2.5. I/O space

The IP module specification defines that the I/O allows to drive only 6 address lines. In this way, an additional page (PAGR) register is necessary to control all the eight UART address lines (when the SC26C198 is accessed through the memory space, all the eight UART address are directly driven by the IndustryPack bus). The SC26C198 register are partitioned into two groups: the control and the data register.

I/O adr.	PAGR	Register description	Acronym	Access
SC26C198 Control registers				
$01	ccc	Mode register 0 MR0 [a:h]	MR0	R/W
$03	ccc	Mode register 1 MR1 [a:h]	MR1	R/W
$05	ccc	I/O port config. reg. a I/OPCR [a:h]	IOPCR	R/W
$07	ccc	Bid control, Break change [a:h]	BCRBRK	R/W
$09	ccc	Bid control, Change of state [a:h]	BCRCOS	R/W
$0D	ccc	Bid control, Xon/Xoff [a:h]	BCRX	R/W
$0F	ccc	Bid control, Address recognition [a:h]	BCRA	R/W
$11	ccc	Xon character [a:h]	XonCR	R/W
$13	ccc	Xoff character [a:h]	XoffCR	R/W
$15	ccc	Address recognition [a:h]	ARCR	R/W
$19	ccc	Receiver clock select [a:h]	RxCSR	R/W
$1D	ccc	Transmitter clock select [a:h]	TxCSR	R/W
$1B	000	• Test register	Reserved, set to 0	
$1F	000	• Global chip configuration	GCCR	R/W
$17	001	• Interrupt control	ICR	R/W
$1B	001	• Watch-dog timer run control	WDTRCR	R/W
$1F	001	• Interrupt vector	IVR	R/W

Notation:

ccc = channel number defined in PAGR.

The global registers are denoted by a "•" symbol.

I/O adr.	PAGR	Register description	Acronym	Access
SC26C198 Data registers				
$21	ccc	Mode register 2 [a:h]	MR2	R/W
$23	ccc	Status register [a:h]	SR	R
$23	ccc	Command register [a:h]	CR	W
$25	ccc	Interrupt status [a:h]	ISR	R
$25	ccc	Interrupt mask [a:h]	IMR	W
$27	ccc	Transmitter FIFO [a:h]	TxFIFO	W
$27	ccc	Receiver FIFO [a:h]	RxFIFO	R
$29	ccc	Input port register [a:h]	IPR	R
$2B	ccc	I/O port Interrupt and Output [a:h]	I/OPIOR	R/W
$2D	ccc	Xon/Xoff interrupt status [a:h]	XISR	R
$2F	000	• GP output select	GPOSR	R/W
$31	000	• BRG timer register Upper a	BRGTRUa	R/W
$33	000	• BRG timer register Lower a	BRGTRLa	R/W
$35	000	• BRG timer control register a	BRGTCRa	R/W
$37	000	• GP output clk register	GPOC	R/W
$39	000	• Update current Interrupt	UCIR	W
$39	000	• Current interrupt	CIR	R
$3D	000	• Global receive Hold	GRxFIFO	R
$3D	000	• Global transmit hold	GTxFIFO	W
$3F	000	• Global chip configuration	GCCR	R/W
$2F	001	• Global output register	GPOR	R/W
$31	001	• BRG timer register Upper b	BRGTRUb	R/W
$33	001	• BRG timer register Lower b	BRGTRLb	R/W
$37	001	• GP output data register	GPOD	R/W
$39	001	• Global Interrupt channel	GICR	R
$3B	001	• Global interrupt byte count	GIBCR	R
$3F	001	• Global interrupt type	GITR	R
SCC-08 register				
$41	xxx	8-bit Page register	PAGR	R/W
$50	xxx	16-bit Page register	PAGR	R/W

Notation:
ccc = channel number defined in PAGR.
The global registers are denoted by a "•" symbol.

2.6. ID Space

All identification codes are factory programmed into a PLD (Programmable Logic Device), in this case these values are read only.

ID space adr.	Description	value
$01	ASCII "I"	$49
$03	ASCII "P"	$50
$05	ASCII "A"	$41
$07	ASCII "C"	$43
$09	Manufacturer identification	$99
$0B	Module type	*
$0D	Revision module	*
$0F	Reserved	$00

* See text below for description.

The four first bytes contain the ASCII text "IPAC". This clearly identifies the ROM beginning.
The manufacturer code identifies ACTIS IndustryPacks™.
The SCC-08 device is defined as follows by the module type byte.

Module	Module type byte
SCC-08A	$30
SCC-08B	$31

The next byte identifies the IP module revision, in accordance with the following definition.

Revision	ASCII car.	hex. value
first	"_" (space)	$5F
next	"A", "B", ...	$41, $42, ...

The byte $0F is reserved for future extension.

2.7. PAGR page register

In accordance with the IP module specification, the I/O space allows decoding of 64-word locations (6 address bits). Therefore the SC26C198 requires up to 256-word addressing (8 address bits) and one address bit is used for on-board registers. In this case, the page register PAGR is necessary to generate the SC26C198 A[6:4] address lines.

Two access modes, 8 or 16-bit, are available for PAGR access.

8-bit mode : address $41

IP data	D7	D6	D5	D4	D3	D2	D1	D0
SC26C198	x	x	x	x	x	PG2	PG1	PG0

16-bit mode : address $51

IP data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SC26C198	x	x	x	x	x	x	x	PG2	PG0	PG0	x	x	x	x	x	x

The following table gives the address bit assignment between the SC26C198 device, the PAGR page register and the IP logic interface.

SC26C198	I/O space		Memory space
	IP bus	PAGR	IP bus
A7	A5	-	A5
A6	-	PG2	A8 (D1)
A5	-	PG1	A7 (D0)
A4	-	PG0	A6
A3	A4	-	A4
A2	A3	-	A3
A1	A2	-	A2
A0	A1	-	A1

This PAGR definition allows, during interrupt context where only global registers are used, to minimize the page register access. In other context (initialization and pooling operations), the PAG[2:0] bits represent the channel number.
The PAGR 16-bit access mode may be used to ensure memory map compatibility between the I/O space and Memory space decoding. In this mode, no bit operation is required to control the PAGR value. The memory space address must be directly writing into the PAGR, where only CPU A[8:6] are significant.

2.8. Wait state cycles

The following table gives the number of wait states asserted in each IP module space.

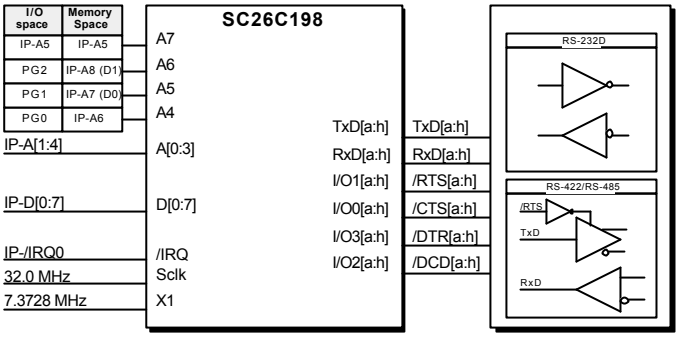
Space	Wait state	
	Read	Write
Memory	1	1
I/O (SC26C198) I/O (PAGR)	1 0	1 0
Identification	0	N.A.
Interrupt acknowledge	1	N.A.

3. SCC-08 characteristics

Symbol	Parameters	Test conditions	Max	Unit
BR	Baud rate	SCC-08A SCC-08B	115.2 460.8	kBaud
I_{CC}	Vcc supply current	 power-down mode	310 160	mA mA
SYSclk	System clock (sclk)		32	MHz
BRGclk	Baud rate generator clock, X1.		7.3728	MHz
Ta	Operating ambient temperature		0 to +70	°C
Tstg	Storage temperature		-60 to +150	°C

4. Philips SC26C198 Octal UART

The SC26C198 is interfaced to the IP module bus through an high-density PLD (Programmable Logic Device). This device manages the timing access on all IP module spaces, stores the identification codes and generates the system clocks. The following block diagram gives the SC26C198 external connection.



The SCC-08A supports the modem signals such as TxD, RxD, /RTS, /CTS, /DTR and /DCD.
The modem signals are generated and supported through the SC26C198 I/O ports in accordance to the following table.

SC26C198 I/O ports	Modem signals	Acronym	Direction
I/O0	Clear To Send	/CTS	input
I/O1	Request To Send	/RTS	output
I/O2	Data Carrier Detect	/DCD	input
I/O3	Data Terminal Ready	/DTR	output

The I/O port definition is accomplished through the IPR, I/OPIOR and I/OPCR registers of the SC26C198 device.
For more details on the register programming and SC26C198 functionalities, please refer to the Philips *"SC26/68C198 data sheet April 14, 1994"*.

4.1. TxFIFO and RxFIFO - Transmit/Receive FIFO

One of the useful capability provided by the SC26C198 device is its large FIFOs, which reduce CPU overhead and allow high speed communications.

Each transmit data path has a 16-Byte deep TxFIFO, with interrupt threshold definition (empty, 3/4 empty, 1/2 empty, not full).

Each receive data path has 16-location deep RxFIFO. Each FIFO position contains the 8-bit received character and its 3-bit status. The error status of a character can be provided in two ways: character mode or block mode.
In character mode, the status is applied only on the character at the top of the RxFIFO (the next character to be read). In block mode, the status is the logical OR of the status for all coming character to the RxFIFO top, since the last reset error command was issued. An interrupt generation can defined in accordance with the following threshold: one or more filled, 1/2 filled, 3/4 filled and full.
Five status bits are associated with each received character: receive error, framing error, parity error, overrun error, and change of break. Only the first three status are included into the RxFIFO.

4.2. Interrupt acknowledge cycle

During interrupt acknowledge cycle, two types of vector can be provided by the SC26C198 device. The interrupt vector may be a fixed value, the content of the interrupt vector register, or a modified vector which contains codes for the interrupt type and/or interrupt channel.
During the interrupt cycle, an interrupt context is defined in accordance with the UART channel register. This context provides global registers (19 in all) that appears at fixed memory map locations. For example, global registers allows the interrupt routine to access the TxFIFO, RxFIFO, interrupt channel and interrupt type registers always at the same memory position independently of the current channel requester.
The interrupt context remains until another IACK cycle occurs or until an "Update CIR" command is given to manage the next channel requester.

4.3. Interrupt priorities

An interrupt arbiter manages the several interrupt sources with a interrupt priority scheme depending of the interrupt type , the channel requester, the number of character into the FIFO, and additional user programmable fields.
Each priority level is defined into a 10-bit value with the following interrupt sources.

- Receive without error
- Receive with error
- Transmit
- Change of break
- Change of state
- Xon/Xoff recognition
- Address recognition
- Receiver watch-dog

In addition a interrupt priority threshold can be fixed to ignore the lowest priority sources, reducing the CPU overhead.

4.4. Wake-up mode

The SC26C198 may operate in two modes in multi-drop configuration available with the SCC-08B module.

- Host mode (default)
- Automatic mode with 3 sub-modes

In both modes, the parity bit is used to recognise an "address byte" or a "data byte".

In host mode, the slave station examines the received data stream and interrupts the CPU only upon reception of an address character.

In automatic mode, the slave station uses its on-board comparators to examine the incoming address characters. In addition, the receiver operation in accordance with received "address byte" depends with the three following sub-modes.

- Receiver auto enable.
- Receiver auto disable.
- Receiver auto enable and disable.

4.5. Data flow control

The SC26C198 provides two data flow controls.

The Xon/Xoff operation uses the programmable characters to control a remote transmitter activity.

The SCC-08A (RS-232D interface) module gives hardware flow control through the /RTS and /CTS signals.

4.6. I/O ports

Each UART channel provides four I/O ports with "change of state" detectors.
The SCC-08A use these ports to support the modem control signals /RTS, /CTS, /DTR and /DCD.
The following table gives the I/O port assignment.

I/O port	Direction	Modem signals
I/O0	input	/CTS
I/O1	output	/RTS
I/O2	input	/DCD
I/O3	output	/DTR

This configuration is defined through the I/OPCR register, which must be equal to $44.

Notes:
Using wrong codes could cause hardware damage on the SCC-08 module.

With SCC-08B module (RS-422/RS-485 interfaces), it is recommended in multi-drop configuration to use the transmitter Request To Send control. In this way, the /RTS signal, connected to the driver output enable, is automatically deasserted at the end of each character transmission.

4.7. Pseudo-synchronous transmission mode

With the SCC-08A, an enhanced mode is available for pseudo-synchronous transmission. This function is accomplished by the availability of the $TxC1x_{out}$, $TxC16x_{out}$ and RxC clock signals.

The following table gives the I/O ports assignment with the I/OPCR register definition.

I/OPCR

Bits[7:6] I/O3 control	**Bits[5:4] I/O2 control**	**Bits[3:2] I/O1 control**	**Bits[1:0] I/O0 control**
00 - Reserved	00 - RxCin	00 - Reserved	00 - /CTS
01 - /DTR (I/OPCR3 out)	01 - /DCD (I/OPCR2 in)	01 - /RTS	01 - Reserved
10 - TxCx16out	10 - Reserved	10 - Reserved	10 - Reserved
11 - TxCx1out	11 - Reserved	11 - Reserved	11 - Reserved

This configuration allows the transmitter to the clock source (via I/OPCR3) for the receiver device (via I/OPCR2).
In addition, the RxCSR (Receiver Clock Select) register must be set in "I/O2 rcvr mode".

Note:
Using the reserved code could cause hardware damage on the SCC-08 module

4.8. RS-422 / RS-485 interfaces

The SCC-08B supports both RS-422 and RS-485 standard.

The RS-422 interface allows network configuration with one master transmitter and up to 32 slave receiver.

The RS-485 standard is an enhanced RS-422 version and supports up to 32 transmitters and 32 receivers on same media. In multi-drop configuration, only one differential line can be used to transmit and receive asynchronous communication. In this mode, the driver output enable must be managed by the /RTS signal, which is necessary to configure in "Transmitter auto-reset control" operation. This configuration disable the RS-485 driver at the end of transmission (one bit time after the last stop bit).

4.9. Character recognition

Three programmable characters, specific to each of the eight UART, are provided for character recognition. These three characters can be used either for general-purpose application or for specific operations related to multi-drop address recognition or in-band Xon/Xoff flow control.

4.10. Watch-dog function

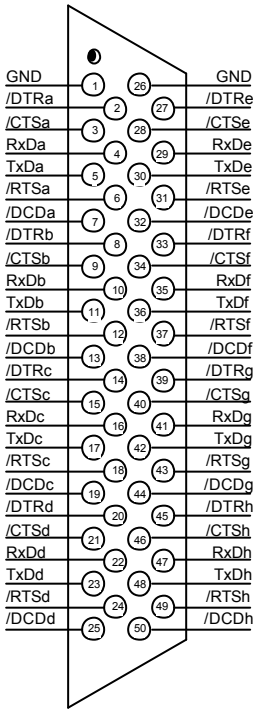
Each receiver channel provides a watch-dog timer when block transfer is required by the software application (i.e. file transfer protocol). An interrupt request is generated when no RxFIFO activity appears after 64 data rate clock cycle. If the numbers of characters stored into the RxFIFO are to few to initiate an interrupt, the watch-dog times out when no characters are push or read in the RxFIFO.

4.11. GCCR - Global Configuration Control Register

The on-board SCC-08 logic controls the SC16C198 logic interface in asynchronous cycles.
For correct functionality, some precautions must be care during GCCR initialization. Bit 6 controls the host logic interface and must be always set to '0' to define asynchronous cycle.

5. SCC-08A connection

The SCC-08A signals of the eight RS-232D serial communication channels are present on the 50-pin IP module I/O connector.

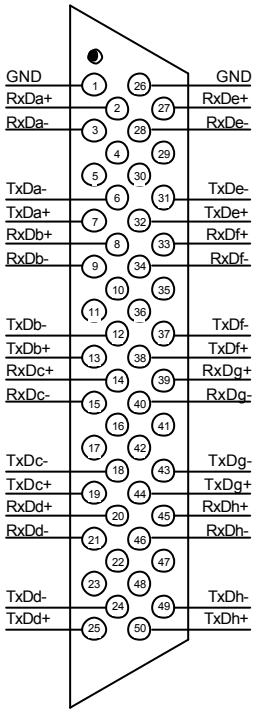


Signals	Description
TxD	Transmit Data
RxD	Receive Data
/RTS	Request To Send
/CTS	Clear To Send
/DTR	Data Set Ready
/DCD	Data Carrier Detect
GND	Ground

Two adaptor modules SC-08 (3U version) and SC-08D (6U version) from ACTIS Computer are also available for an easily user connection with RJ-45 8-pin connectors.

6. SCC-08B connection

The SCC-08B differential signals of the eight RS-422/RS-485 serial communication channels are present on the 50-pin IP module I/O connector.



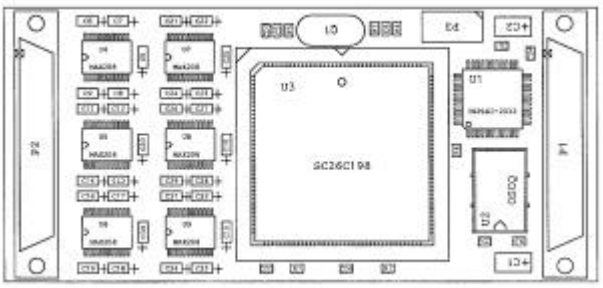
Signals	Description
TxD±	Transmit Data
RxD±	Receive Data
GND	Ground

This connection is compatible with the I/O connection standard, on the 50-pin IP module I/O connector, defined by ACTIS Computer.

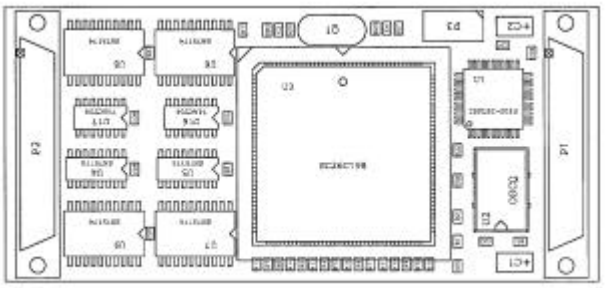
Two adaptor modules SC-08 (3U version) and SC-08D (6U version) from ACTIS Computer are also available for an easily user connection with RJ-45 8-pin connectors.

7. Component location

SCC-08A



SCC-08B



OS-9/68000® is a registered trademark of MICROWARE Systems Corp.

8. OEM Warranty

ACTIS Computer warrants that its Product sold hereunder, excluding software, will at the time of shipment be free from defects in material and workmanship and will conform to ACTIS Computer's applicable specifications or, if appropriate, to CUSTOMER's specifications previously accepted by ACTIS Computer in writing. If Products sold hereunder are not as warranted, ACTIS Computer shall, at its option and as CUSTOMER's exclusive remedy, either refund the purchase price, or repair or replace the Product, provided proof of purchase and written notice of nonconformance are received by ACTIS Computer within the applicable periods noted below and provided said nonconforming Products are, with ACTIS Computer's written authorization, returned in protected shipping containers FOB ACTIS Computer's plant within thirty (30) days after expiration of the warranty period. Upon verification by ACTIS Computer that the Product does not conform to this warranty, ACTIS Computer will reimburse CUSTOMER for the cost of transporting the goods to and from ACTIS Computer's plant. This warranty shall not apply to any Products ACTIS Computer determines have been, by CUSTOMER or otherwise, subjected to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been the subject of mishandling, misuse, neglect, improper testing, repair, alteration, damage, assembly or processing that alters physical or electrical properties.

This Limited Warranty is effective from the date of sale and shall expire on the expiration date of the applicable hardware product warranty period. The expiration date is defined as three-year for mezzanine modules and the relevant transition modules, and one-year for all cPCI and VME boards. CUSTOMER must notify ACTIS Computer, in writing, no later than thirty days after expiration of this Limited Warranty of Product that does not conform to this Limited Warranty. In the event that the Product does not conform to this Limited Warranty, ACTIS Computer shall, at its option, repair, replace or refund the purchase price of the non-conforming Product. The remedies provided herein are the sole and exclusive remedies for a breach of this Limited Warranty.
ACTIS Computer hereby disclaims all implied warranties, including implied warranties of merchantability or fitness for a particular purpose. ACTIS Computer shall not be liable for any special, incidental or consequential damages due to a breach of this (Limited) Warranty.

Warranty Service and Return Information
Please contact the place of purchase for return procedures. If customer purchased product(s) directly from ACTIS Computer, then customer shall return the product(s) to ACTIS Computer pursuant to the following terms. Customer must obtain a Return Material Authorization ("RMA") number by calling customer service at +41 (22) 794 43 91. Returned products should be shipped to the following address within 10 days of receiving an RMA number to avoid charges for the replacement product:

ACTIS Computer
Attn:RMA Dept RMA#_____
19,chemin du Champ-des-Filles
1228 Plan-Les-Ouates
Switzerland

Please retain shipping information, including tracking numbers. If ACTIS Computer determines that failure of the product(s) was not a result of a defect in materials or workmanship, ACTIS Computer reserves the right to charge customer for parts and labor at ACTIS Computer's then current labor rate. ACTIS Computer will advise customer prior to assessing these charges.

9. Notes

9. Ordering Information

Reference	Description
SCC-08A	**Octal-channel Serial Communication Controller with RS-232 interface.**
SCC-08B	**Octal-channel Serial Communication Controller with RS-422/RS-485 interface.**
SC-08	**Octal RJ45 8-pin panel, for RS-232D and RS-422/RS-485 interface. 6Ux8TE form factor.**
SC-08D	**Octal RJ45 8-pin panel, for RS-232D and RS-422/RS-485 interface. 6U form factor.**
SC-08DB	**Octal sub-D 25-pin female panel, for RS-232D and RS-422/RS-485 interface. 6U form factor.**