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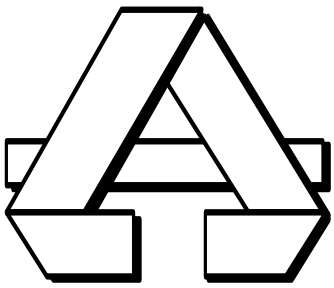
IP module:

Analog to digital conversion
Digital to analog conversion
Counter/Timer and parallel I/O

ADA-08

User's Guide

9715



ACTIS

COMPUTER S.A.

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1. Introduction

The ADA-08 IP module of ACTIS Computer S.A. include three fonctions :

- A counter/timer and parallel I/O unit (CIO). This module provides two general-purpose 8-bit ports, one special-purpose 4-bit ports, and three 16-bit counter/timers.

- An octal 12-bit digital to analog converter (DAC). These fonction provides eight single-ended buffered analog outputs (in bipolar and unipolar modes), which will accept an analog load on the DAC outputs.

- A 12-bit+sign analog to digital converter (ADC). This fonction provides eight single-ended or four differential analog inputs for unipolar and bipolar signals. An on-chip 8-word RAM can store the conversion sequence for up to eight acquisitions through the on-chip eight-input multiplexer.

The ADA-08 is compatible with the VITA-4 IP module specification.

A complete industrial OS-9 environment is available, other driver may be suppleed upon request.

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2. Summary of features

- Single-size IP module.
- Compatible with the VITA-4 IP Module specification.

- Two general-purpose 8-bit ports.
- One special-purpose 4-bit ports.
- Three 16-bit counter/timers.
- Flexible pattern-recognition logic for interrupt generation.
- All signals in TTL levels.

- Octal 12-bit digital to analog conversion.
- Integral non linearity of ±2 LSB.
- Settling time less than 35 µs.
- On-board output amplifiers.
- Output voltage range: ±10 V

- Octal 12-bit + sign analog to digital converter.
- Up to 140 kSample/s troughput.
- On-chip multiplexer and instruction sequencer.
- Conversion accuracy of ±1 LSB.
- Settling time less than 5 µs.
- Single-ended and differential input modes.
- Input voltage range : ±10 V (standard version)
  Factory option : ±5 V, 0 to +10 V and 0 to +5 V (min 25 pcs)
- Monitoring functions.
- Auto calibration and diagnostic mode.
- On-chip 32-word FIFO.
- External trigger capability.

- On-board two +5 V precision voltage reference.
- Industrial temperature range option (-40 to +85 °C).

A standard OS-9 driver is available from ACTIS Computer.

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3. Description

The ADA-08 contains two general-purpose 8-bit ports, one special-purpose 4-bit and three 16-bit counter/timers.
All I/O signals, TTL levels, are directly connected from CIO controllers to the IP 50-pin I/O connector.

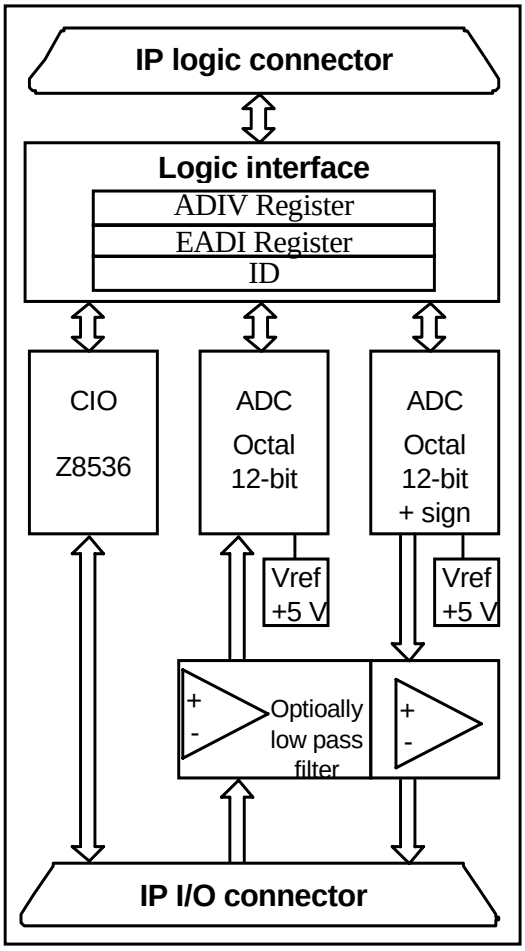
The DAC fonction is designed on the MP7611 (12-bit) digital to analog converter from Micro Power System. Each DAC output is followed by an analog amplifier, to directly drive an analog load. Each output voltage range is ±10 V.
The modules include a precision voltage reference, factory calibrated, for digital to analog conversion.

The ADC fonction is based on the LM12458 analog to digital converter from National Semiconductor. This device offers very useful capabilities for acquisition operations: monitoring functions, on-chip FIFO, auto-calibration and diagnostic mode, programmable acquisition time and conversion rates. This device also provides a sequencer, which executes up to eight instructions. Each instruction defines the internal multiplexer selection, the conversion resolution, the acquisition time and the timer capability.
The ADC fonction provides a voltage range for each analog input between ±10 V (standard version).
(Factory option for min qty 25 pcs : ±5 V, 0 to +10 V and 0 to +5 V).
The LM12458 also provides single-ended and differential input modes.
The module includes a second precision voltage reference (25 ppm/°C maximum temperature drift), factory calibrated, for the analog to digital conversion.

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3.1 Block diagram

The hardware architecture of the ADA-08 is divided in general main sections:



- The IP bus interface, controlling the timing access of the CIO controller and the converter devices.
- The CIO controller, Zilog Z8536.
- The MP7613 digital to analog converter.
- The LM12458 analog to digital converter.
- The output analog amplifiers.
- The input analog amplifiers and optionally low pass filter.

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3.2 IP spaces

The following table gives the four ADA-08 memory spaces.

IP space	Devices
MEMORY	No access
IDENTIFICATION	IP identification codes
I/O	• CIO controllers access • DAC Data registers • DAC Control register • DAC Reset register • DAC Interrupt vector register • DAC Eneble interrupt vector register • ADC Data registers • ADC control register • ADC Interrupt vector register
INTERRUPT ACK.	DAC Interrupt acknowledge cycle ADC Interrupt acknowledge cycle

The base address of these spaces depends on the IP carrier.

3.3 I/O space

The CIO controller is mapped into the IP I/O space. Data and command registers of the CIO controller are placed on 4 consecutive addresses (8-bit data path).

I/O space adr.	Register	Description
CIO controller		
$51	PCDR	Port C Data Register
$53	PBDR	Port B Data Register
$55	PADR	Port A Data Register
$57	CR0	Control Register 0

All port configurations are defined with the CIO control registers. The data registers allow the value of each ports to be accessed directly.

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The LM12458 interrupt vector registers are mapped into the IP I/O space.

I/O space adr.	Access	Bus wide	Register	Description
LM12458 registers				
$00	R/W	16-bit	RAM0	Instruction RAM0
$04	R/W	16-bit	RAM1	Instruction RAM1
$08	R/W	16-bit	RAM2	Instruction RAM2
$0C	R/W	16-bit	RAM3	Instruction RAM3
$10	R/W	16-bit	RAM4	Instruction RAM4
$14	R/W	16-bit	RAM5	Instruction RAM5
$18	R/W	16-bit	RAM6	Instruction RAM6
$1C	R/W	16-bit	RAM7	Instruction RAM7
$20	R/W	16-bit	CONF	Configuration register
$24	R/W	16-bit	ENINT	Enable Interrupt register
$28	R	16-bit	INTST	Interrupt Status register
$2C	R/W	16-bit	TIMER	Timer register
$30	R	16-bit	FIFO	Conversion FIFO
$34	R	16-bit	LIMIT	Limit status register
$60	R/W	8-bit	ADIV	ADC Interrupt vector register
$70	R/W	8-bit	EADI	Eneble ADC Interrupt register

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The DAC converter is mapped into the IP I/O space and provides eight 16-bit data registers and one 8-bit command registers.

I/O space adr.	Access	Bus wide	Register	Description
$40	R/W	16-bit	DAC0	DAC code for channel 0
$42	R/W	16-bit	DAC1	DAC code for channel 1
$44	R/W	16-bit	DAC2	DAC code for channel 2
$46	R/W	16-bit	DAC3	DAC code for channel 3
$48	R/W	16-bit	DAC4	DAC code for channel 4
$4A	R/W	16-bit	DAC5	DAC code for channel 5
$4C	R/W	16-bit	DAC6	DAC code for channel 6
$4E	R/W	16-bit	DAC7	DAC code for channel 7
$78	W	8-bit	DACREG	DAC Output Update and reset register

3.4 ID space

The identification space is defined as follows:

ID space adr.	Description	value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$99
$0B	Module type	$24
$0D	Revision module	$5F
$0F	Reserved	$00

The four first bytes contain the ASCII text "IPAC". This clearly identifies the ROM beginning.
The manufacturer code $99 identifies ACTIS IP.
The ADA-08 device is defined by the module type byte $24.
The next byte identifies the IP revision, in accordance with the following definition.

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Revision	ASCII car.	hex. value
first	"_" (space)	$5F
next	"A", "B", ...	$41, $42, ...

The byte $0F is reserved for future extension.

3.5 Wait state cycles

The following tables gives the number of wait states asserted in each IP space.

Space	Wait state	
	Read	Write
Identification	0	N.A.
I/O CIO		
o CIO registers	4	4
o Interrupt acknowledge	5	N.A.
I/O ADC		
o ADC registers	2	2
o Interrupt Vector (IV) register	0	0
o Eneble interrupt Vector (EIV) register	0	0
o Interrupt acknowledge	0	N.A.
I/O DAC		
o DAC data registers	6	2
o DACOU register	N.A.	2
o DACRST register	N.A.	0

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4. Characteristics

4.1 CIO

Symbol	Parameters	Test conditions	Min	Max	Unit
V_{IH}	Input high voltage		2	Vcc + 0.3	V
V_{IL}	Input low voltage		-0.3	0.8	V
V_{OH}	Output high voltage	I_{OH}=-250 µA	2.4		V
V_{OL}	Output low voltage	I_{OL}=+2 mA I_{OL}=+3.2 mA		0.4 0.5	V
I_{CC}	Vcc supply current			560	mA
PCLK	Peripheral clock			4	MHz

4.2 DAC

Symbol	Parameters	Test conditions	Min	Max	Unit
N	Resolution			14	bit
INL	Integral non linearity	Ta=25 °C		±2	LSB
DNL	Differential non linearity	Ta=25 °C		±1	LSB
ZOFS	Bipolar zero offset	Ta=25 °C		±2	LSB
_E	Channel-to-channel max. error (all code)	Ta=25 °C		±1	LSB
ME	All channels maximum error	Ta=25 °C		±4	LSB
MES	All channel error span	Ta=25 °C		5	LSB
τ_{sd}	Settling time from DAC output writing to DAC output valid	Zero to Full scale. (20 V step)		55 (typ. 35)	µs
R_{LOAD}	Analog load	±10 V range ±5 V range 0 to +10V range	2 400 2		kΩ Ω kΩ

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Symbol	Parameters	Test conditions	Min	Max	Unit
TCVo	Voltage reference tempreature coefficient			25	ppm/°C
Vref	Voltage reference	FS DAC0 min. error		typ. 5	V
Vcc	Vcc analog voltage		11.4	12.75	V
Vee	Vee analog voltage		-12.75	-11.4	V
Vdd	Vdd digital voltage		4.5	5.5	
Icc	Positive supply current		90	210	mA
Iee	Negative supply current		90	210	mA
Idd	Digital supply current		95	120	mA

4.3 ADC

Symbol	Parameters	Test conditions	Min	Max	Unit
N	Resolution	After auto-cal.		12+sign	bit
INL	Integral non linearity	After auto-cal.		±1.5	LSB
DNL	Differential non linearity	After auto-cal.		±1	LSB
ZOFS	Bipolar zero offset	After auto-cal.		±1.5	LSB
FSE	Full-scale error	After auto-cal.		±2	LSB
Tc	Conversion time	12-bit + sign 9-bit + sign		11 5.3	µs
Tc	Conversion time	12-bit + sign 8-bit + sign		11 5.3	µs
Tacq	Acquisition time	12-bit + sign 8-bit + sign		2.3 0.6	µs
Tz	Auto-zero time	Sequencer S2		19	µs
Tcal	Full calibration time	Sequencer S2		1.2	ms
	Throughput rate	Standard version. Option H.		70 140	kS/s
Symbol	**Parameters**	**Test conditions**	**Min**	**Max**	**Unit**

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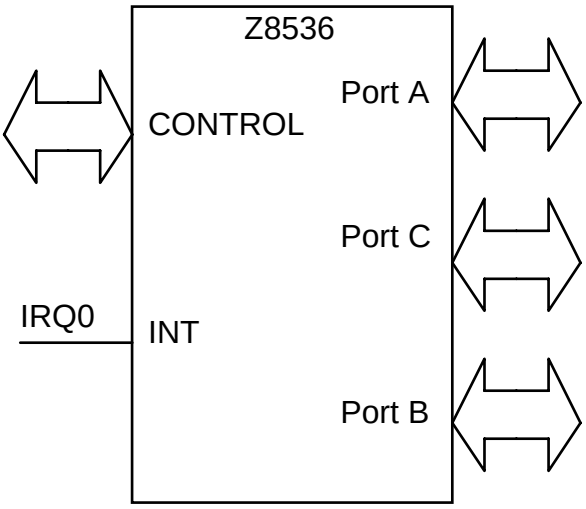
τ_{sd}	Settling time, analog interface propagation delay.	10 V step		2	µs
Z_{IN}	Impedance input on input multiplexer		10		kΩ
Rs	Source resistance to LM12458 converter			< 10	Ω
TCVo	Voltage ref. temp. coefficient			25	ppm/°C
CLK	LM12458 clock	Standard version		typ . 8	MHz
Vref	Voltage reference			typ. 5	V
Vcc	Vcc analog voltage		11.4	12.75	V
Vee	Vee analog voltage		-11.4	-12.75	V
Vdd	Vdd digital voltage		4.5	5.5	V
Icc	Positive quiescent current			50	mA
Iee	Negative quiescent current			40	mA
Idd	Digital quiescent current			180	mA
Ta	Operating ambient temperature	Standard version	0	+70	°C
Tstg	Storage temperature		-60	+150	°C

All limit parameters are specified for the commercial temperature grade. For the extended version (X option : -40 to +85 °C), the parameters can be different.

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5. Zilog CIO Z8536

The ADA-08 IP contains a Z8536 devices, and the following description gives you the features of these CIO controller.
The Z8536 device provides two general-purpose 8-bit ports (port A and B), one special-purpose 4-bit port (port C), and three 16-bit counter/timers (timer 1 to 3).



The CIO controller provide an interrupt connected to IRQ0 of the IP logic interface.

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5.1 General-purpose ports

These ports can be programmed either as a handshake-driven, and as single or as double buffered port (input, output, or bidirectional) with the direction of each bit individually programmable. These two ports (ports A and B) can also be linked to form a 16-bit I/O port with handshake. Each port can generate an interrupt when a specific pattern-recognition is detected. This pattern offers a very large flexibility for a specific OR/AND condition, the polarity and the transition detection (state or edge) are independently programmable for each bit-port.
The second port (port B) allows an external access to the first and second software counter/timers (counter/timers 1and 2).
To program these capabilities, both ports contain 12 registers. The command and status registers define the primary port functionalities. Two registers are used to define the port specification and handshake modes. The I/O data is accessed through the input, output and buffer registers. The data direction, data path polarity and special I/O control registers allow programming each bit. The pattern-recognition is defined with the pattern polarity, pattern transition and pattern mask registers.

5.2 Special-purpose port

The function of this port (port C) is defined in accordance with the role of the general-purpose ports. This port can provide either handshake lines for the general-purpose ports, either an external access to the third counter/timer (counter/timers 3) or either conventional I/O lines.
Only three registers (data path polarity, data direction, and special I/O control) are necessary to control the port C when the general-purpose ports functionalities (ports A and B) have been specified.

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5.3 Counter/Timers

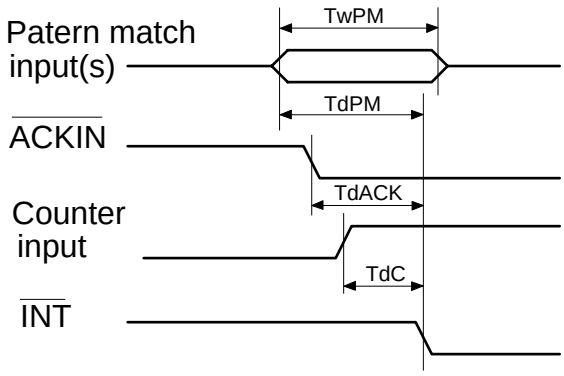
All the three counter/timers (counter/timers 1 to 3) are functionality identical.
Three output modes are available: pulse, one-shoot, and square-wave. The operating mode of the counter/timer can be programmed either as retriggerable or as non-retriggerable.
Up to four control lines are provided for timer/counter operation : counter input, gate input, trigger input, and counter/timer output.
Each counter/timer provides a time-constant register containing the initial value of the down-counter. At any time the current count register shows the content of the down-counter. Two other registers are used the control register to set the timer/counter configuration, and the timer/counter status register.

5.4 CIO Interrupt function

Five registers control the CIO interrupt functions: the master interrupt control, three interrupt vector registers, and the current interrupt vector register.

5.5 Interrupt timing

The following timing descriptions give the delay for interrupt generation.
In bit port mode, an interrupt is generated when the pattern-recognition is detected.
In handshake port operation, the external ACKIN signal strobes the input data into the CIO and an interrupt is actived to indicate to the host that a valid input data is present.



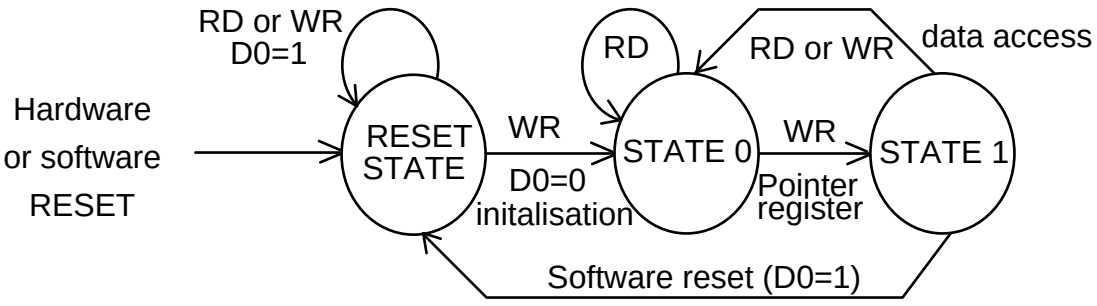
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Symbol	Parameters	Min	Max	Unit
TwPM	Pattern match input valid (bit port)	750		ns
TdPM	Pattern match to INT delay (bit port)		1.3	µs
TdACK	ACKIN to INT delay (port with handshake)		3.1	µs
Td	Counter input to INT delay (timer mode)		1.2	µs

5.6 Z8536 registers access

Two cycles are necessary to address an internal register, as the internal CIO registers are accessed through an internal pointer register.The first cycle is the write pointer operation, into the control register (CR0) which select the internal register.
The next cycle is the data access operation.

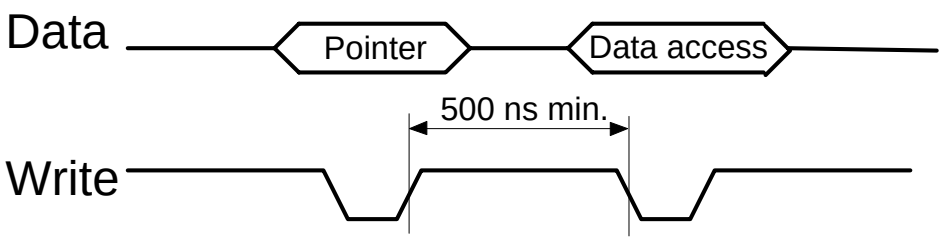
The following state machine shows the internal register operation.



The CIO is on the reset state, after hardware or software reset. The software reset is accomplished by writing D0=1 in CR0 register. On the CIO controller,

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the hardware reset is accomplished when the reset signal is asserted on the IP logic interface. To leave this state, an initialisation cycle is necessary: write D0=0 in the control register, otherwise during a read cycle the CIO device returns always D0=1. The state 0 waits for the pointer writing (in the control register) for the internal register selection. After the data access (read or write cycle), the state machine returns to the state 0, waiting for the next pointer writing.
A **minimum time of 500 ns** is required between the pointer writing and the data access operation.



All internal CIO registers, including the internal data register, are accessed through this method. The pointer register is automatically cleared after each following read or write cycle.
A direct register access, without pointer writing cycle, is available for the data register with the PADR to PDDR registers (see I/O space section).

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The following table shows the internal CIO registers.

CIO Internal addr.	Cycle	Registers
Main control registers		
$00	R/W	Master interrupt control
$01	R/W	Master configuration control
$02	R/W	Port A interrupt vector
$03	R/W	Port B interrupt vector
$04	R/W	Counter/timer interrupt vector
$05	R/W	Port C data path polarity
$06	R/W	Port C data direction
$07	R/W	Port C special I/O control
Most often accessed registers		
$08	R/partial W	Port A command and status
$09	R/partial W	Port B command and status
$0A	R/partial W	Counter/Timer 1 command and status
$0B	R/partial W	Counter/Timer 2 command and status
$0C	R/partial W	Counter/Timer 3 command and status
$0D	R/W	Port A data
$0E	R/W	Port B data
$0F	R/W	Port C data
Port A specification registers		
$20	R/W	Port A mode specification
$21	R/W	Port A handshake specification
$22	R/W	Port A data path polarity
$23	R/W	Port A data direction
$24	R/W	Port A special I/O control
$25	R/W	Port A pattern polarity
$26	R/W	Port A pattern transition
$27	R/W	Port A pattern mask

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Port B specification registers		
$28	R/W	Port B mode specification
$29	R/W	Port B handshake specification
$2A	R/W	Port B data path polarity
$2B	R/W	Port B data direction
$2C	R/W	Port B special I/O control
$2D	R/W	Port B pattern polarity
$2E	R/W	Port B pattern transition
$2F	R/W	Port B pattern mask
Counter/Timer related registers		
$10	R	Counter/Timer 1 current count MSB
$11	R	Counter/Timer 1 current count LSB
$12	R	Counter/Timer 2 current count MSB
$13	R	Counter/Timer 2 current count LSB
$14	R	Counter/Timer 3 current count MSB
$15	R	Counter/Timer 3 current count LSB
$16	R/W	Counter/Timer 1 time constant MSB
$17	R/W	Counter/Timer 1 time constant LSB
$18	R/W	Counter/Timer 2 time constant MSB
$19	R/W	Counter/Timer 2 time constant LSB
$1A	R/W	Counter/Timer 3 time constant MSB
$1B	R/W	Counter/Timer 3 time constant LSB
$1C	R/W	Counter/Timer 1 Mode Specification
$1D	R/W	Counter/Timer 2 Mode Specification
$1E	R/W	Counter/Timer 3 Mode Specification
$1F	R	Current vector

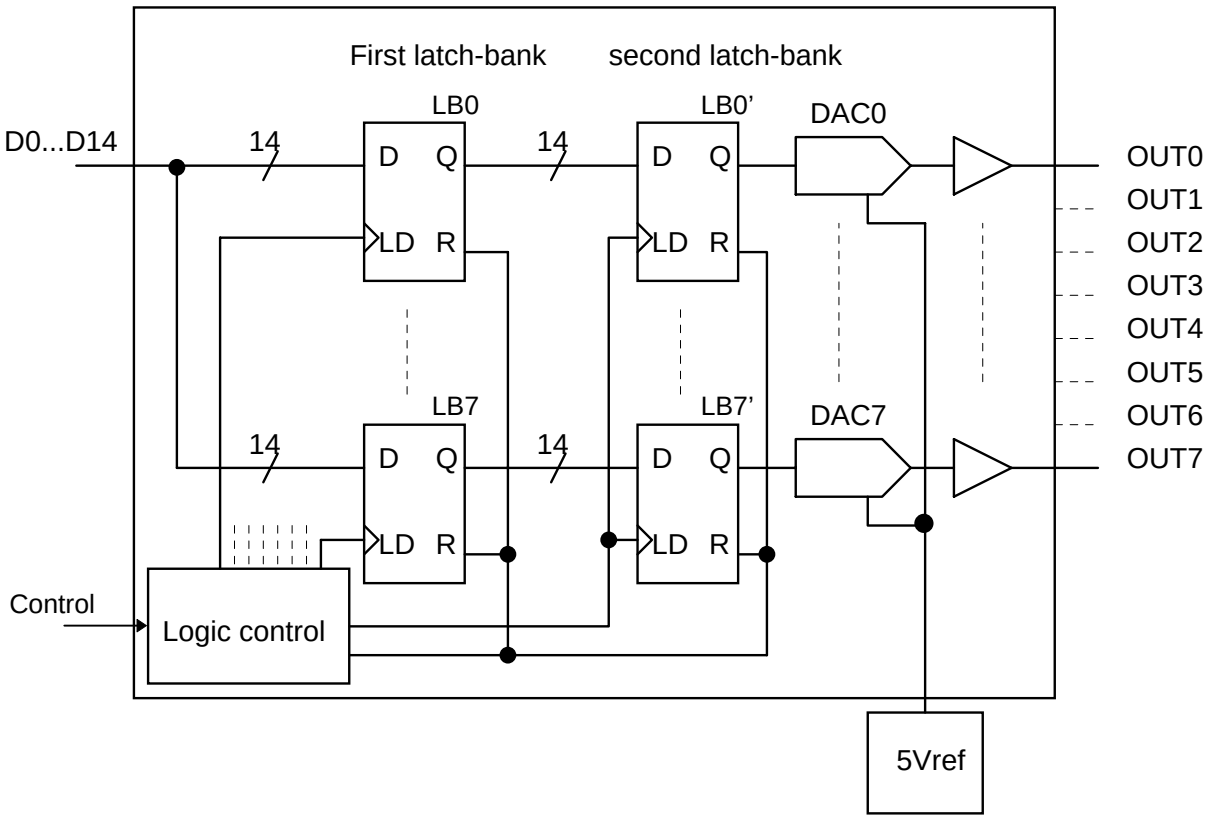
For more details on register programming and SCC functionalities, please refer to the Zilog *"Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel I/O Unit" technical manual.*

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6. MPS MP7613/MP7611

The IP modules work with octal DAC devices from Micro Power System to achieve to digital to analog conversion. One of these devices is used as per the conversion resolution required. The MP7611 converts in 12-bit resolution.

The internal architecture of these devices is divided in two latch sections. The first contains eight 16-bit data registers (first latch-bank, LB0 to LB7 registers), which store the DAC conversion codes. These registers may be individually accessed for each DAC output. However, the relevant DAC analog output is not updated when a new value is writing. The DAC Output Update register (DACREG, bit D1) allows the transfer, in a single cycle, of the content in the eight first latches (LB0 to LB7 registers) into the second latch-bank (LB0' to LB7') and update the analog output.



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The reset DAC (DACREG register) is used to execute a general reset cycle into the converter (see the 6.2. section).

An on-board precision voltage reference of +5 V provides a very high temperature stability of 25 ppm/°C drift to the DAC converter.

6.1 DAC code registers

The eight independant, read or write, DAC code registers contain the conversion codes for each analog output. The 12-bit data are aligned to the Low Significant Bit (D0 = LSB). When a new value is stored, the corresponding output is not affected. To update the analog output , it is necessary to make a write cycle in the DACREG register (see the following section).

DAC format

IP-BUS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC	-	-	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- : Undefined.

6.2 DACREG : Output Update and reset register

This register transfers the first latch-bank content into the second latch-bank, which are directly connected to the MP7611 internal output amplifiers. In general application, the eight DAC code registers are set in a first step and then the DACREG operation is executed. At that time, only the required DAC outputs are changed, without alteration for the other not concerned outputs.

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To execute this operation, the D1 bit of DACREG register (Update bit) must be set to 1.

To execute a reset operation, the D0 bit of DACREG register (Reset bit) must be set to 1.

IP-Bus	D7	D6	D5	D4	D3	D2	D1	D0
DACREG	-	-	-	-	-	-	Update	Reset

- : Undefined.

The following table shows the DAC states after a reset cycle.

First latch value	`$0000`
Second latch value	`$1000`
Analog output voltage ±10 V range	0 V

Note that the DAC fonction execute also a hardware reset at each system reset.

6.3 Conversion codes

The following equation gives the analog output voltage according to the conversion code (D parameter) for a 14-bit conversion in ±10V analog output ranges.

DAC 14-bit converter	
Output range	**Conversion code**
±10 V	$10 * (-1 + 2 * D / 2^{14})$

6.4 Precision reference voltage

The ADA-08 IP module provides a voltage reference for digital to analog conversion. It offers a very good temperature stability, less than 25 ppm/°C

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rift. It is factory calibrated, with a potentiometer, to give to DAC0 a minimum total error, in full scale conditions.

7. LM12458 acquisition system

The ADC fonction works with the enhanced LM12458 converter. This highly integrated data acquisition system is a 12-bit + sign with integrated sample-and-hold. This acquisition system operates in three different modes: 12-bit + sign, 8-bit + sign, and watchdog. The watchdog function generates an interrupt request when the input goes out from the range defined by the two-limit references. The acquisition and conversion times are software programmable with the on-chip timers.
An internal 32-word FIFO reduces the CPU overhead. When this FIFO is used, it is possible to stores up to 32 consecutive conversions before reading the FIFO values.
The LM12458 has an auto-calibration mode, which executes an auto-zero offset voltage correction and an ADC linearity calibration with eight samples of the offset voltage. A short auto-zero correction is also provided for every conversion.
A synchronization signal SYNC is present to operate either as an input or an output. When the SYNC signal is programed as an input, a rising edge applied to this pin starts a conversion cycle or a watchdog comparison.
The LM12458 internal architecture includes a sequencer, which executes programmable instructions. The instruction RAM holds up to eight executable instructions. The conversion modes, sequencer operation (continue or single), synchronization capability, conversion resolution and the timer functions are defined into this instruction RAM.
One option with the "Sync" signal wired to the bus "Strobe" line is also available.

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Recommended initialization:

The following steps must be acheived to insure correct analog conversions.

Execute a full LM12H458 auto-calibration through the CONF register.

As the instrumentation amplifier output resistor is less than 100 Ω, the acquisition time can be set to 0 in the instruction RAM.

For more details on register programming and ADC functionalities, please refer to the National Semiconductor *"LM12454/ LM12H454/ LM12458/ LM12H458 12-bit + sign data acquisition system with self-calibration"* data sheets.

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7.1 Interrupt vector (ADIV) register

This read and write ADIV register includes the 8-bit vector for the interrupt acknowledge cycle, generates in response of a LM12458 interrupt request.

IP-Bus	D7	D6	D5	D4	D3	D2	D1	D0
ADIV	D7	D6	D5	D4	D3	D2	D1	D0

7.2 Enable ADC interrupt (EADI) register

The LM12H458 interrupt is enable when the D0 bit (eneble bit) of read and write EAI register must be set to 1.

IP-Bus	D7	D6	D5	D4	D3	D2	D1	D0
EADI	-	-	-	-	-	-	-	Eneble

- : Undefined

7.3 External synchronization

The ADA-08 provides, on the 50-pin I/O connector interface, an external synchronization signal (input or output). The SYNC signal controls the LM12458 start conversion, and allows the synchronization with another converter modules in multiple acquisitions system.
The synchronization signal from the I/O connector is directly connected from the LM12458 device, and detects a rising edge.
(One option with the "Sync" signal wired to the bus "Strobe" line is also available.)

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7.4 Conversion codes

The following table gives the conversion codes for the 12-bit + sign and 8-bit + sign resolutions.

Voltage range	Conversion codes
±10 V	$\frac{V_{IN} + 10}{20} \cdot N - 1$
±5 V *	$\frac{V_{IN} + 5}{10} \cdot N - 1$
0 to +5 V *	$\frac{V_{IN}}{5} \cdot N - 1$
0 to +10 V *	$\frac{V_{IN}}{10} \cdot N - 1$

* Factory options

The N parameter defines the acquisition resolution for the analog to digital conversion (4096 for 12-bit, 256 for 8-bit conversions).

7.5 Precision reference voltage

The ADA-08 module provides a second voltage reference for the analog to digital conversion. It offers a very good temperature stability, less than 25 ppm/°C drift. It is factory calibrated, with a potentiometer, in order to give the minimum full scale error.

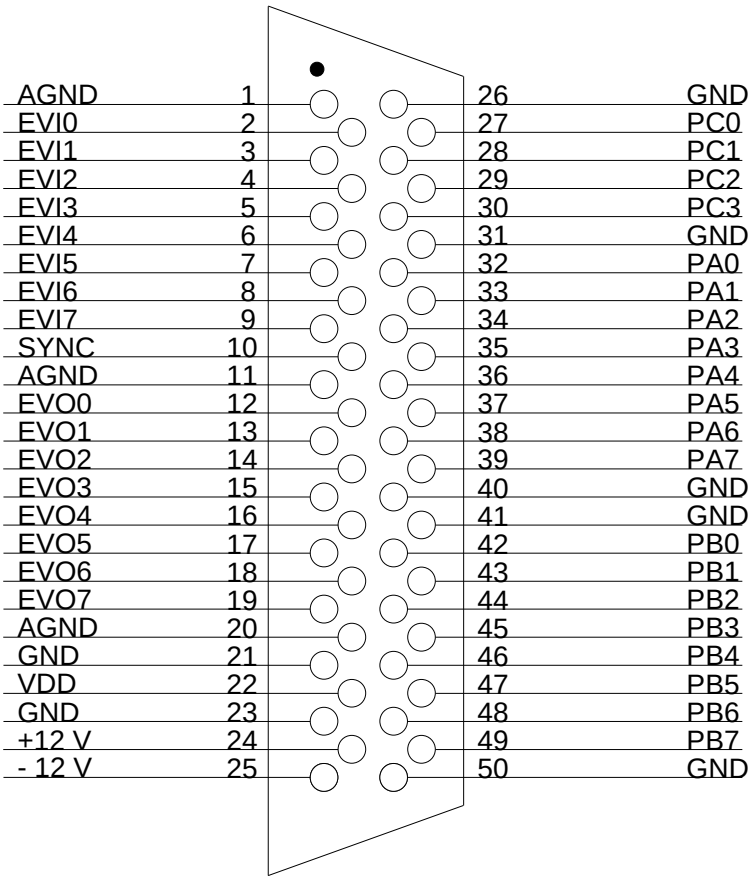
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7.6 Voltage range selection

The output voltage is ±10 V on the standard vertion.
The bipolar ±5 V, unipolard 0 to 5 V and 0 to 10 V ist also available as a factory option or special order with minimum quantity(please contact ACTIS Computer marketing dpt).

8. Connection

The ADA-08 signals of the two general-purpose 8-bit ports and the special-purpose 4-bit ports, the eight analog output, and the eigth single-ended or the four differential analog input are present on the 50-pin IP I/O connector. The power supply (+5V and ±12V) is also provided for external signal conditioning, and it's short-circuit protected.



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CIO	
Signals	**Description**
PortA[7:0]	Port A general-purpose 8-bit port
PortB[7:0]	Port B general-purpose 8-bit port
PortC[3:0]	Port C general-purpose 8-bit port

DAC	
Signals	**Description**
DAC0	DAC output 0
DAC1	DAC output 1
DAC2	DAC output 2
DAC3	DAC output 3
DAC4	DAC output 4
DAC5	DAC output 5
DAC6	DAC output 6
DAC7	DAC output 7

ADC	
Signals	**Description**
ADC0	ADC input 0
ADC1	ADC input 1
ADC2	ADC input 2
ADC3	ADC input 3
ADC4	ADC input 4
ADC5	ADC input 5
ADC6	ADC input 6
ADC7	ADC input 7
SYNC	External synchro.

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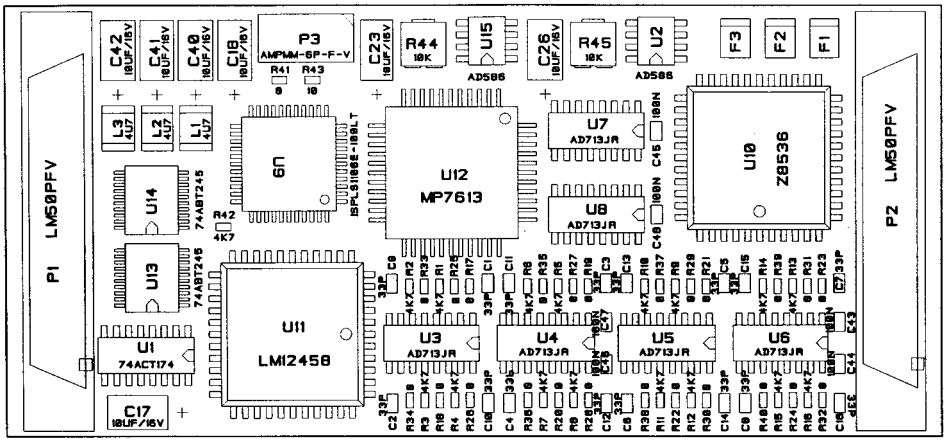
POWER	
Signals	**Description**
+12 V	+12 V, 500 mA max. fuse protected.
-12 V	-12 V, 500 mA max. fuse protected.
VDD	+ 5 V, 500 mA max. Fuse protected.
GND	Digital ground
AGND	Analogic ground

This connection is compatible with the I/O connector specification, defined by ACTIS Computer.
A transition module (IO50A) from ACTIS Computer is also available for an easily user connection. It provides 5x10-pin industrial connectors, with external power connections, and measures 6HE x 4TE on front panel.

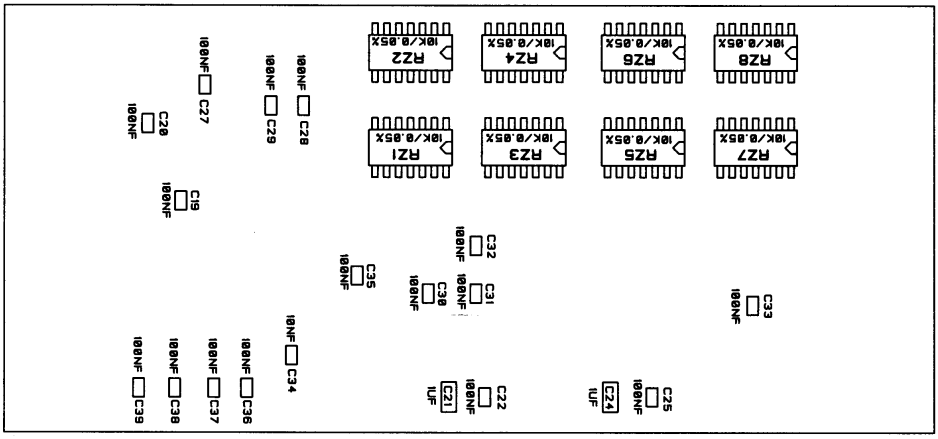
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9. Component location

Component side:



Back side :



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