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USER'S GUIDE

CIO-32

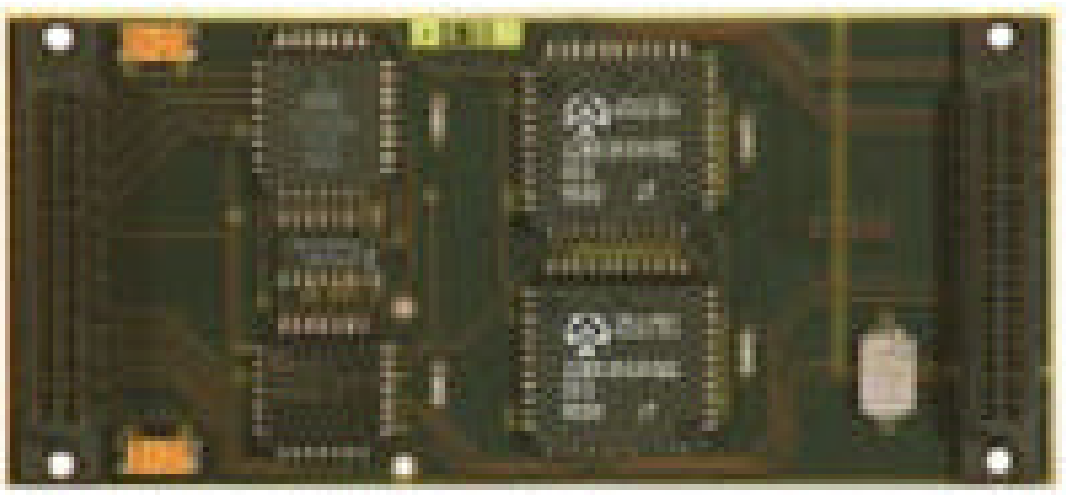
IP module:
Counter/Timer and parallel I/O

Edition 4003



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CIO-32

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1. Introduction

The CIO-32 module of ACTIS Computer S.A. is a Counter/timer and parallel I/O unit (CIO) compatible with the IP specification. This module provides four general-purpose 8-bit ports, two special-purpose 4-bit ports, and six 16-bit counter/timers.
An on-board 2 kByte EEPROM provides IP identification codes and module specific data.
A complete industrial OS-9 environment is available for the CIO-32 module.

2. Summary of features

- Single-size IP module.
- Compatible with the IP specification (Rev. 0.7.1).
- Four general-purpose 8-bit ports.
- Two special-purpose 4-bit ports.
- Six 16-bit counter/timers.
- Flexible pattern-recognition logic for interrupt generation.
- All signals in TTL levels.
- 2 kByte of non-volatile memory (EEPROM).
- Industrial temperature grade available (-40 to +85 °C).

3. Description

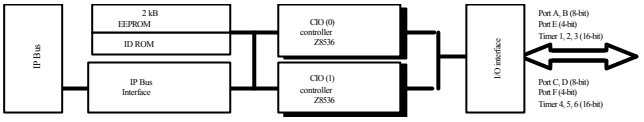
The CIO-32 IP contains two Zilog Counter/timer and parallel I/O Z8536. Each device has two general-purpose 8-bit ports, one special-purpose 4-bit and three 16-bit counter/timers.
All CIO-32 I/O signals, TTL levels, are directly connected from CIO controllers to the IP 50-pin I/O connector.
A 2 kByte, 8-bit data path, of non-volatile memory is present on the CIO-32 module, this memory is divided in two sections. The first contains the identification data (64 Byte), providing the module information such as; the module type, the manufacturer code, the module and driver revision, etc.
This information defines an auto-configuration system on each power up. The second is less than 2 kByte (2 kByte - 64 Byte) and contains specific user's data such as: calibration data, configuration information, driver for operation system, etc.

3.1. Block diagram

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The hardware architecture of the CIO-32 is divided in 3 main sections:

- The IP bus interface, controlling the timing access of the CIO controllers and the on-board memory.
- The CIO controllers, Zilog Z8536.
- The 2 kByte of non-volatile memory including the identification ROM and module specific data.



3.2. IP spaces

The following table shows the four CIO-32 memory spaces.

MEM space	(2 kByte - 64 Byte) of non-volatile memory
ID space	IP identification codes
I/O space	CIO controllers access
INT Ack	Interrupt acknowledge

The base address of these spaces is depending on the IP carrier.

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3.3. I/O space

The two CIO controllers are mapped into the IP I/O space. Data and command registers of the CIO controllers are placed on 16 consecutive addresses (8-bit data path).

I/O space adr.	Register	Description
CIO (0) controller		
$1	PEDR	Port E Data Register
$3	PBDR	Port B Data Register
$5	PADR	Port A Data Register
$7	CR0	Control Register 0
CIO (1) controller		
$9	PFDR	Port F Data Register
$B	PDDR	Port D Data Register
$D	PCDR	Port C Data Register
$F	CR1	Control Register 1

All port configurations are defined with the CIO control registers. The data registers allow the value of each ports to be accessed directly.

3.4. ID space

The identification space is defined as follows:

ID space adr.	Description	value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$99
$0B	Module type	$03
$0D	Revision module	
$0F	Reserved	$00
$11	Driver ID, low byte	
$13	Driver ID, high byte	
$15	Number of bytes used	$0C
$17	CRC	

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$3F $19	User space	

The fourth bytes contain the ASCII text "IPAC". This clearly identifies the ROM beginning.
The manufacturer code identifies ACTIS IP.
The CIO-32 device is defined by the module type byte.
The next byte identifies the IP revision, in accordance with the following definition.

Revision	ASCII car.	hex. value
first	"_" (space)	$5F
next	"A", "B", ...	$41, $42, ...

The byte $0F is reserved for future extension.
The byte $11 and $13 allows identification of the IP software driver.
The number of bytes used in the identification space is stored at the address $15.
To verify the identification data integrity, the byte $17 contains a 8-bit Checksum Redundant Code (CRC). This CRC covers only the number of identification codes set by the manufacturer. The CRC used is an industry standard. It's the low 8-bit of the FCS as described in CCITT T.30 (Fascicle VII.3) section 5.3.7.
The next bytes $19 to $3F are free for user data storage.

3.5. MEM space

As 2 kByte memory device is present on the board and only 64 Byte are used for identification space, the rest is mapped into the IP memory space.
The first usable address of this memory is $40.
A minimum time of 2 ms must be asserted between the last write and the next read cycle to guarantee the correct data writing. If a read cycle is produced before the achievement of the previous writing, the data bus D7 provides an inverted value of the last data loaded.
A minimum time of 2 ms must be asserted between the reset and the first write cycle.
Note: only IP carrier asserting no hold cycle can access this space.

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3.6. Wait state cycles

The following table shows the number of wait states asserted in each IP space.

Space	Wait state	
	Read	Write
I/O	2	2
Identification	2	2
Memory	2	2
Interrupt acknowledge	4	N.A.

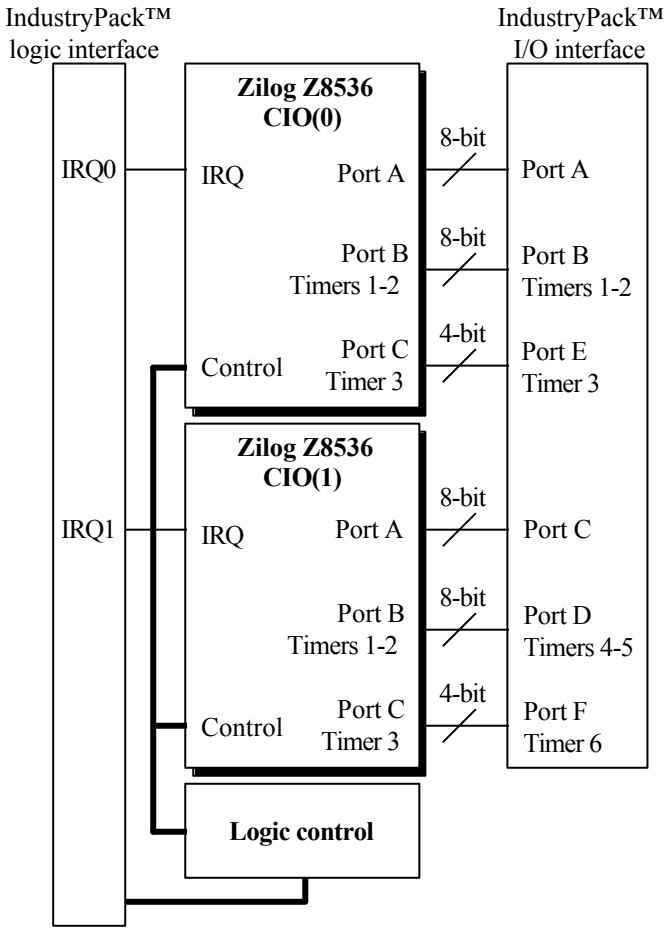
4. CIO-32 characteristics

Symbol	Parameters	Test conditions	Min	Max	Unit
V_{IH}	Input high voltage		2	Vcc + 0.3	V
V_{IL}	Input low voltage		-0.3	0.8	V
V_{OH}	Output high voltage	I_{OH}=-250 µA	2.4		V
V_{OL}	Output low voltage	I_{OL}=+2 mA I_{OL}=+3.2 mA		0.4 0.5	V
I_{CC}	Vcc supply current			560	mA
PCLK	Peripheral clock			4	MHz
Ta	Operating ambient temperature CIO-32 (commercial) CIO-32X (industrial)			 0 to +70 -40 to +85	°C
Tstg	Storage temperature			-60 to +150	°C

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5. Zilog CIO Z8536

The CIO-32 IP contains two Z8536 devices, and the following description gives you the features of these CIO controllers.
Each Z8536 device provides two general-purpose 8-bit ports (port A-B or C-D of the CIO-32 respectively), one special-purpose 4-bit port (port E or F of the CIO-32 respectively), and three 16-bit counter/timers (timer 1 to 6 of the CIO-32).



Each CIO controller provides an interrupt connected to IRQ0 and IRQ1 of the IP logic interface respectively.

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5.1. General-purpose ports

These ports can be programmed either as a handshake-driven, and as single or as double buffered port (input, output, or bi-directional) with the direction of each bit individually programmable. These two ports (ports A-B or C-D of the CIO-32) can also be linked to form a 16-bit I/O port with handshake. Each port can generate an interrupt when a specific pattern-recognition is detected. This pattern offers a very large flexibility for a specific OR/AND condition, the polarity and the transition detection (state or edge) are independently programmable for each bit-port.
The second port (port B or D of the CIO-32) allows an external access to the first and second software counter/timers (counter/timers 1-2 or 4-5 of the CIO-32).
To control these capabilities, both ports contain 12 registers. The command and status registers define the primary port functionalities. Two registers are employed to define the port specification and handshake modes. The I/O data is accessed through the input, output and buffer registers. The data direction, data path polarity and special I/O control registers allow programming each bit. The pattern-recognition is defined with the pattern polarity, pattern transition and pattern mask registers.

5.2. Special-purpose port

The function of this port (port E or F of the CIO-32) is defined in accordance with the role of the general-purpose ports. This port can provide either handshake lines for the general-purpose ports, either an external access to the third counter/timer (counter/timers 3 or 6 of the CIO-32) or either conventional I/O lines.
Only three registers (data path polarity, data direction, and special I/O control) are necessary to control the port C when the general-purpose ports functionalities (ports A-B or C-D of the CIO-32) have been specified.

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5.3. Counter/Timers

All the three counter/timers (counter/timers 1 to 6 of the CIO-32) are functionality identical.
Three output modes are available: pulse, one-shoot, and square-wave. The operating mode of the counter/timer can be programmed either as retriggerable or as non-retriggerable.
Up to four control lines are provided for timer/counter operation: counter input, gate input, trigger input, and counter/timer output.
Each counter/timer provides a time-constant register containing the initial value of the down-counter. At any time the current count register shows the content of the down-counter. Two other registers are used: the control register to set the timer/counter configuration, and the the timer/counter status register.

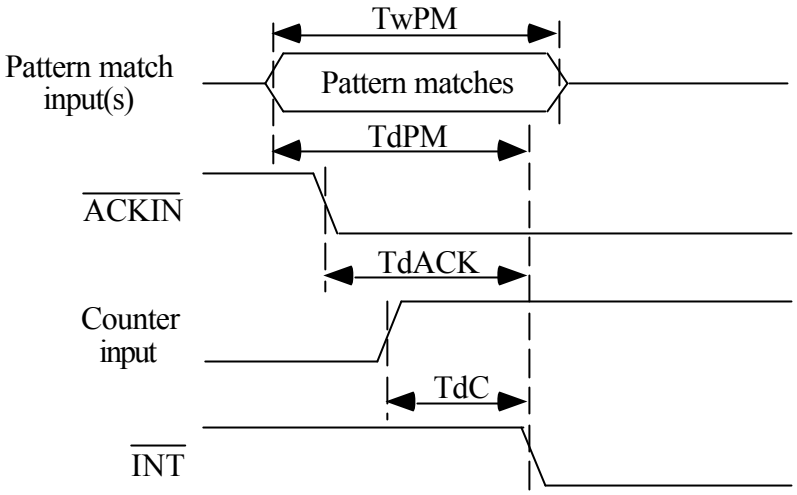
5.4. CIO Interrupt function

Five registers control the CIO interrupt functions: the master interrupt control, three interrupt vector registers, and the current interrupt vector register.
The hardware daisy-chain operation is not implemented, because each CIO controllers has its own interrupt request line into the IP logic interface.

5.5. Interrupt timing

The following timing descriptions give the delay for interrupt generation.
In bit port mode, an interrupt is generated when the pattern-recognition is detected.
In handshake port operation, the external ACKIN signal strobes the input data into the CIO and an interrupt is actived to indicate to the host that a valid input data is present.

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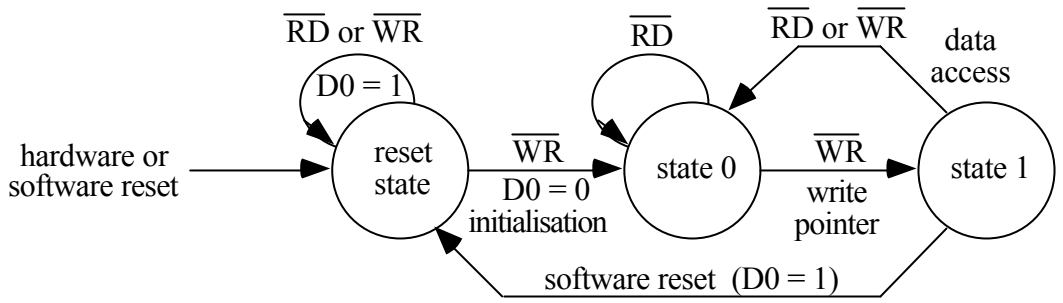
Symbol	Parameters	Min	Max	Unit
TwPM	Pattern match input valid (bit port)	750		ns
TdPM	Pattern match to INT delay (bit port)		1.3	µs
TdACK	ACKIN to INT delay (port with handshake)		3.1	µs
TdC	Counter input to INT delay (timer mode)		1.2	µs

5.6. Z8536 registers access

Two cycles are necessary to address an internal register, as the internal CIO registers are accessed through an internal pointer register.
The first cycle is the write pointer operation, into the control register (CR0 and CR1, on CIO-32) which selects the internal register. The next cycle is the data access operation.

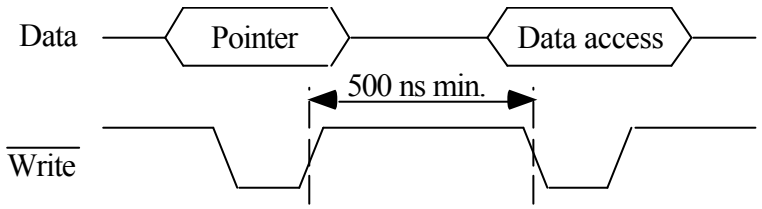
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The following state machine shows the internal register operation.



The CIO is on the reset state, after hardware or software reset. The software reset is accomplished by writing D0=1 in CR0 or CR1 registers of the CIO-32. On the CIO-32 IP, the hardware reset is accomplished when the reset signal is asserted on the IP logic interface. To leave this state, an initialization cycle is necessary: write D0=0 in the control register, otherwise during a read cycle the CIO device returns always D0=1. The state 0 waits for the pointer writing (in the control register) for the internal register selection. After the data access (read or write cycle), the state machine returns to the state 0, waiting for the next pointer writing.

A **minimum time of 500 ns** is required between the pointer writing and the data access operation.



All internal CIO registers, including the internal data register, are accessed through this method. The pointer register is automatically cleared after each following read or write cycle.

A direct register access, without pointer writing cycle, is available for the data register with the PADR to PDDR registers (see I/O space section).

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The following table shows the internal CIO registers.

CIO Internal addr.	Cycle	Registers
Main control registers		
$00	R/W	Master interrupt control
$01	R/W	Master configuration control
$02	R/W	Port A or C interrupt vector
$03	R/W	Port B or D interrupt vector
$04	R/W	Counter/timer interrupt vector
$05	R/W	Port E or F data path polarity
$06	R/W	Port E or F data direction
$07	R/W	Port E or F special I/O control
Most often accessed registers		
$08	R/partial W	Port A or C command and status
$09	R/partial W	Port B or D command and status
$0A	R/partial W	Counter/Timer 1 or 4 command and status
$0B	R/partial W	Counter/Timer 2 or 5 command and status
$0C	R/partial W	Counter/Timer 3 or 6 command and status
$0D	R/W	Port A or C data
$0E	R/W	Port B or D data
$0F	R/W	Port E or F data
Port A specification registers		
$20	R/W	Port A or C mode specification
$21	R/W	Port A or C handshake specification
$22	R/W	Port A or C data path polarity
$23	R/W	Port A or C data direction
$24	R/W	Port A or C special I/O control
$25	R/W	Port A or C pattern polarity
$26	R/W	Port A or C pattern transition
$27	R/W	Port A or C pattern mask
Port B specification registers		
$28	R/W	Port B or D mode specification
$29	R/W	Port B or D handshake specification
$2A	R/W	Port B or D data path polarity
$2B	R/W	Port B or D data direction
$2C	R/W	Port B or D special I/O control
$2D	R/W	Port B or D pattern polarity
$2E	R/W	Port B or D pattern transition
$2F	R/W	Port B or D pattern mask

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Counter/Timer related registers		
$10	R	Counter/Timer 1 or 4 current count MSB
$11	R	Counter/Timer 1 or 4 current count LSB
$12	R	Counter/Timer 2 or 5 current count MSB
$13	R	Counter/Timer 2 or 5 current count LSB
$14	R	Counter/Timer 3 or 6 current count MSB
$15	R	Counter/Timer 3 or 6 current count LSB
$16	R/W	Counter/Timer 1 or 4 time constant MSB
$17	R/W	Counter/Timer 1 or 4 time constant LSB
$18	R/W	Counter/Timer 2 or 5 time constant MSB
$19	R/W	Counter/Timer 2 or 5 time constant LSB
$1A	R/W	Counter/Timer 3 or 6 time constant MSB
$1B	R/W	Counter/Timer 3 or 6 time constant LSB
$1C	R/W	Counter/Timer 1 or 4 Mode Specification
$1D	R/W	Counter/Timer 2 or 5 Mode Specification
$1E	R/W	Counter/Timer 3 or 6 Mode Specification
$1F	R	Current vector

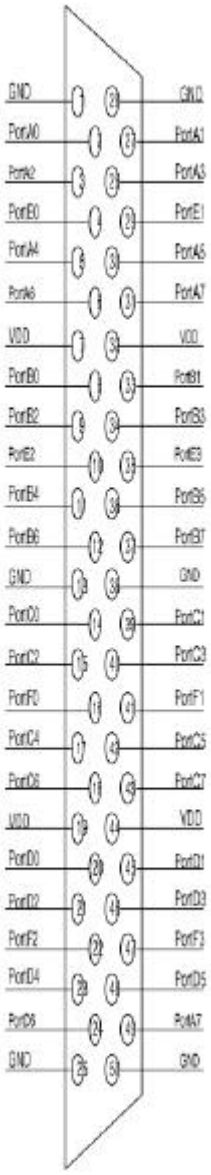
For more details on register programming and SCC functionalities, please refer to the Zilog *"Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel I/O Unit" technical manual*.

A standard OS-9 driver is available from ACTIS Computer.

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6. Connection

The CIO-32 signals of the four general-purpose 8-bit ports and the two special-purpose 4-bit ports are present on the 50-pin IP I/O connector. The power supply +5V is also provided for external signal conditioning, and it's short-circuit protected from CIO-32 revision "A" module.



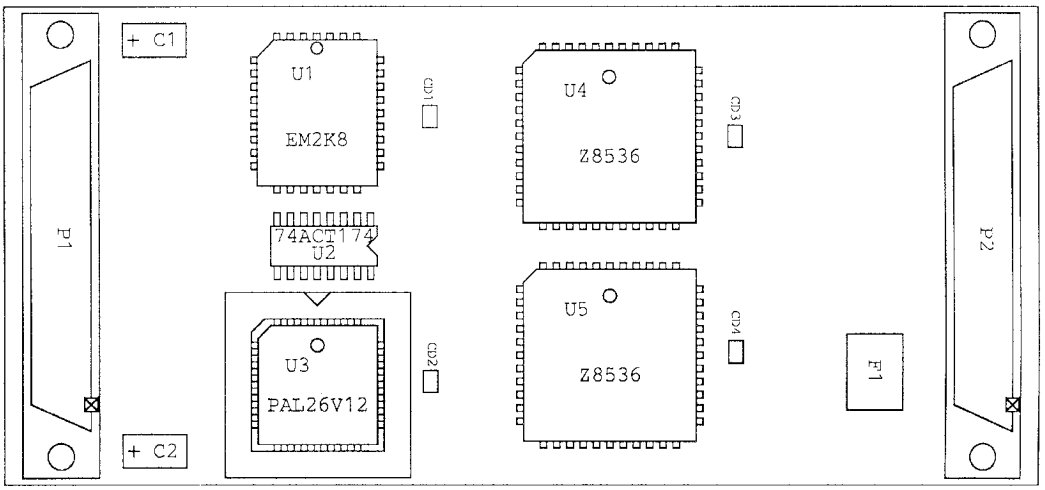
Signals	Description
PortA[7:0]	Port A general-purpose 8-bit port
PortB[7:0]	Port B general-purpose 8-bit port
PortC[7:0]	Port C general-purpose 8-bit port
PortD[7:0]	Port D general-purpose 8-bit port
PortE[3:0]	Port E special-purpose 4-bit ports
PortF[3:0]	Port F special-purpose 4-bit ports
VDD	+ 5 V, 500 mA max. Fuse protected on revision A.
GND	Ground

This connection is compatible with the I/O connection standard, on the 50-pin IP I/O connector, defined by ACTIS Computer.

An adaptor module (DB25D) from ACTIS Computer is also available for an easily user connection. It provides two DB-25 connectors and measures 3HE x 4TE on front panel.

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7. Component location



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8. OEM Warranty

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This Limited Warranty is effective from the date of sale and shall expire on the expiration date of the applicable hardware product warranty period. The expiration date is defined as three-year for mezzanine modules and the relevant transition modules, and one-year for all cPCI and VME boards. CUSTOMER must notify ACTIS Computer, in writing, no later than thirty days after expiration of this Limited Warranty of Product that does not conform to this Limited Warranty. In the event that the Product does not conform to this Limited Warranty, ACTIS Computer shall, at its option, repair, replace or refund the purchase price of the non-conforming Product. The remedies provided herein are the sole and exclusive remedies for a breach of this Limited Warranty.

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Please contact the place of purchase for return procedures. If customer purchased product(s) directly from ACTIS Computer, then customer shall return the product(s) to ACTIS Computer pursuant to the following terms. Customer must obtain a Return Material Authorization ("RMA") number by calling customer service at +41 (22) 794 43 91. Returned products should be shipped to the following address within 10 days of receiving an RMA number to avoid charges for the replacement product:

ACTISComputer S.A.
Attn:RMA Dept RMA#_____
19,chemin du Champ-des-Filles
1228 Plan-Les-Ouates
Switzerland

Please retain shipping information, including tracking numbers. If ACTIS Computer determines that failure of the product(s) was not a result of a defect in materials or workmanship, ACTIS Computer reserves the right to charge customer for parts and labor at ACTIS Computer's then current labor rate. ACTIS Computer will advise customer prior to assessing these charges.

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9. Ordering Information

Reference	Description
CIO-32	**Quad 8-bit TTL I/Os ports with 4-bit handshake, includes six 16-bit timers.**
IO-50	**Universal 50-pin screw terminals connectors. 6U form factor.**

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