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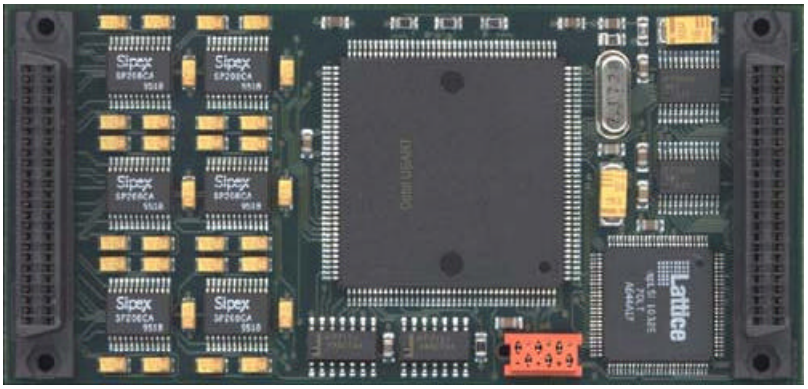
UCC-08

Universal Serial Communication Controller

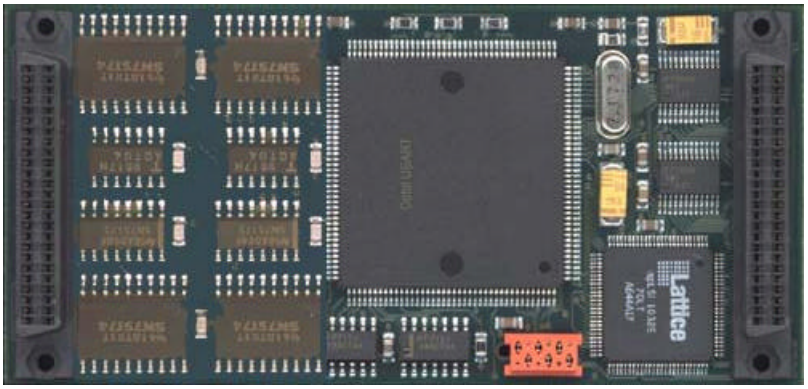
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IP-UCC-08A



IP-UCC-08B

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1. Introduction

With the increase of communication applications, ACTIS Computer introduces a highly integrated, eight-channel Universal Communication Controller.
This IP-UCC-08 module supports both synchronous and asynchronous transmission modes with full-duplex capabilities. A flexible baud rate generator allows independent speed rate for both transmitting and receiving data paths on each channel.

To achieve high performance, the IP-UCC-08 is based on a single chip octal USART, which provides a very large FIFO memory to minimize the receiver overrun or the interrupt overhead (64-Byte receiver and 64-Byte transmitter FIFOs for each channel).

For both versions, the IP-UCC-08 modules require only a 5V power supply.

Three dedicated transition modules SC-08 (3Ux8TE version, eight RJ-45 ports), SC-08D (6Ux4TE version, eight RJ-45ports), and SC-08DB are available for an easily user connection.

A complete industrial environment for LynxOS, OS-9, VxWorks and Linux is available for the IP-UCC-08 modules.

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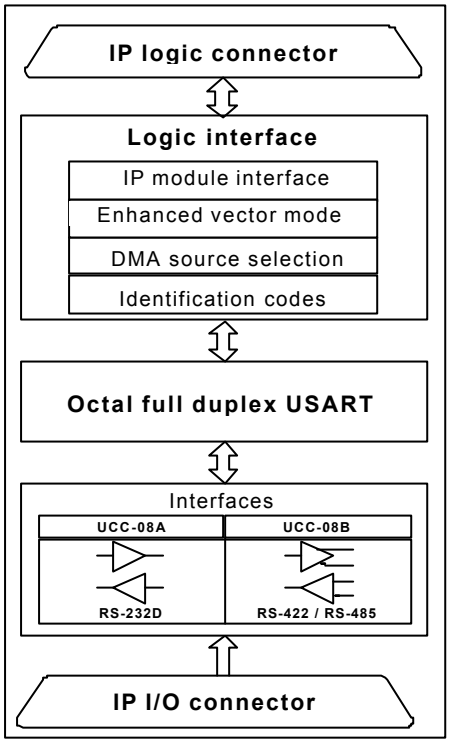
2. Description

2.1. Summary of Features

- Single-size IP module (type I).
- Compatible with the VITA-4 specification.
- Eight Synchronous/Asynchronous full-duplex serial communication channels.
- Asynchronous/Synchronous character oriented (MONOSYNC / BISYNC) or HDLC/SDLC modes (including SDLC LOOP).
- NRZ, NRZI, FM and Manchester encoding.
- Eight independent baud rate generators for each channel.
- 64-Byte transmitter and 64-Byte receiver FIFOs on each channel.
- Enhanced interrupt vector management.
- Data rate up to: 115.2 kBaud for IP-UCC-08A (RS-232D).
- Data rate up to: 5 Mbit/s for IP-UCC-08B (RS-422/RS-485).
- CRC support: CRC-CCITT, CRC-16, CRC-32.
- Manages all modem signals with RS-232D interfaces (IP-UCC-08A).
- Supports multi-drop 2-wire configuration (IP-UCC-08B) with driver output enable capability, and collision detection and resolution.
- Dual DMA channel support to transmit and receive data transfer, with sixteen sources.
- 5V only power supply requirement.

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2.2. Block Diagram



UCC-08 block diagram

The hardware architecture of the IP-UCC-08 is divided into 3 main sections:

- The IP module bus interface which controls the timing access of the USART, the identification codes, the enhanced vector mode management and the DMA configuration.
- The Universal Synchronous/ Asynchronous controller (USART).
- The serial communication interface: RS-232D for the IP-UCC-08A, or RS-422/RS-485 for the IP-UCC-08B.

3. UCC-08 Characteristics

Symbol	Parameters	Test conditions	Typ	Unit
BR	Baud rate	UCC-08A UCC-08B	115.2 5	kbps Mbps
I_{CC}	Vcc supply current	UCC-08A UCC-08B	400 600	mA mA
BRGclk	Baud rate generator clock, X1.		7.3728	MHz
Ta	Operating ambient temperature		0 to +70	°C
Tstg	Storage temperature		-60 to +150	°C

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4. IP Module Spaces

The following table gives the four IP-UCC-08 memory spaces.

MEM space	USART registers
ID space	IP module identification codes
I/O space	USART and board registers
INT Ack	Interrupt acknowledge

The base address of these spaces depends on the IP carrier.

The USART register accesses are available in both I/O and Memory spaces. Refer to the related memory I/O Space sections for more details about register's declaration.

4.1. Memory Space

When the USART is accessed through the memory space, all nine USART address bits are directly driven by the IP bus.
Bus access is made in 16-bit mode.

Memory offset	Mode	Registers
$00 - $1FF	8/16-bit	USART registers

For further information about USART register details, refer to the USART documentation indicated on the Related Documentation section.

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4.2. ID Space

All identification codes are factory programmed into a PLD (Programmable Logic Device). In this case, these values are read only.

ID Space Addr.	Description	Value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$99
$0B	Module type	*
$0D	Revision module	*
$0F	Reserved	$00

* See text below for description.

The four first bytes contain the ASCII text "IPAC". This clearly identifies the ROM beginning. The manufacturer code identifies ACTIS VITA-4 modules.
The UCC-08 device is defined as follows by the module type byte.

Module	Module Type Byte
UCC-08A	$36
UCC-08B	$37

The next byte identifies the IP module revision, in accordance with the following definition.

Revision	ASCII Char.	Hex. value
First	"_" (space)	$5F
Next	"A", "B", ...	$41, $42, ...

The byte $0F is reserved for future extensions.

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4.3. I/O Space

The I/O space allows access to both USART and UCC-08 specific registers either in 8- or 16-bit access width.

The VITA-4 specification states that the I/O allows only 6 address lines to be driven. In this case, an additional page (PAGR) register is necessary to control all 9 USART address lines (when the USART is accessed through the memory space, all nine addresses are directly driven by the IP module address lines).
In this mode, the three upper address lines A[8:6] of the USART are driven by the PAGR[2:0] bits. This address line arrangement was made so that the page register value corresponds to the USART channel selection.

I/O Offset	PAGR	Mode	Register Description
$00 - $3E	0	8/16-bit	Channel 0 registers
$00 - $3E	1	8/16-bit	Channel 1 registers
$00 - $3E	2	8/16-bit	Channel 2 registers
$00 - $3E	3	8/16-bit	Channel 3 registers
$00 - $3E	4	8/16-bit	Channel 4 registers
$00 - $3E	5	8/16-bit	Channel 5 registers
$00 - $3E	6	8/16-bit	Channel 6 registers
$00 - $3E	7	8/16-bit	Channel 7 registers
$41	x[1)]	8-bit	PAGR register
$43	x[1)]	8-bit	DM0R register
$45	x[1)]	8-bit	DM1R register
$49	x[1)]	8-bit	MSK register
$4B	x[1)]	8-bit	LIV register

[1)] PAGR value has no effect for these register accesses.

For further information about USART register details, refer to the USART documentation indicated on the Related Documentation section.

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4.3.1. PAGR Register

The PAGR function is only used when the USART is addressed from the I/O space area. The 3-bit register handles the A8 to A6 address lines of the USART device, which correspond to the (0 to 7) channel selection.
A typical access to the USART register is made in a two step operation:

1. Write the PAGR register for serial channel selection.
2. For read or write operation, address the USART register.

Note that the PAGR value is held until the next PAGR write cycle action.

8-bit mode, R/W: address $41

IP data	D7	D6	D5	D4	D3	D2	D1	D0
PAGR	x	x	x	x	x	PG2	PG1	PG0

Value after reset, $00.

The PAGR bits selection is as follows:

PAGR PG[2:0] bits	Serial Channel Selection
$0	0
$1	1
$2	2
$3	3
$4	4
$5	5
$6	6
$7	7

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4.3.2.DM0R Register

One the great advantage of the UCC-08 module is to authorize high data flow transfer thanks to its dual DMA channel capabilities. These DMA channels, DAM0 and DMA1 (refer to VITA-4 specification for more details) can be assigned to one of the 16 DMA requesters available (one per transmission, one per reception and for all serial channels).
The DM0R register allows the set-up of the first DMA channel provided by the UCC-08. This DMA may be used either for the transmitting or receiving data path.

8-bit mode, Read only: address $43

IP data	D7	D6	D5	D4	D3	D2	D1	D0
DM0R	x	x	x	EN	S3	S2	S1	S0

Value after reset, $00.

EN : enable DMA0 request. When this bit is clear, the DMA0 function is disabled. When this bit is set, the DMA0 function is enabled with the S[3:0] source selection.
S[3:0]: DMA0 source selection. These four bits define the DMA0 requester between one of the 16 available sources, as follows:

S3	S2	S1	S0	Source for DMA0
0	0	0	0	Channel 0 receive
0	0	0	1	Channel 1 receive
0	0	1	0	Channel 2 receive
0	.....	.....	.....	.....
0	1	1	1	Channel 7 receive
1	0	0	0	Channel 0 transmit
1	0	0	1	Channel 1 transmit
1	0	1	0	Channel 2 transmit
1	.....	.....	.....	.....
1	1	1	1	Channel 7 transmit

Refer also to the USART Device and System Board documentation for the complete DMA0 configuration.

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4.4. DM1R Register

The function of this register is the same as the DM0R register except that it manages the second DMA channel DMA1.

8-bit mode, Read only: address $45

IP data	D7	D6	D5	D4	D3	D2	D1	D0
DM1R	x	x	x	EN	S3	S2	S1	S0

Value after reset, $00.

EN : enable DMA1 request

S3	S2	S1	S0	Source DMA1
0	0	0	0	Channel 0 receive
0	0	0	1	Channel 1 receive
0	0	1	0	Channel 2 receive
0	.....	.....	.....	.....
0	1	1	1	Channel 7 receive
1	0	0	0	Channel 0 transmit
1	0	0	1	Channel 1 transmit
1	0	1	0	Channel 2 transmit
1	.....	.....	.....	.....
1	1	1	1	Channel 7 transmit

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4.4.1.MSK Register

The MSK (mask) register is used for enhanced vector mode management. With this mode, the MSK register allows some bits of the vector to be returned by the USART part (during the interrupt acknowledge cycle) which could be hidden in relation with this register setting.

8-bit mode R/W: address $49

IP Data	D7	D6	D5	D4	D3	D2	D1	D0
MSK	-	-	MSK5	-	-	-	MSK1	MSK0

Value after reset, $00.

After reset, the MSK register is cleared and all incoming vector bits are directly sent to the logic interface. When a MSK bit is set, the corresponding vector bit is always clear during the interrupt acknowledge cycle.

The typical MSK value is $23 which hides the interrupt source type information (for further details about the interrupt vector assignment, refer to the SAB82538 user's manual in section 2.2.3.3). In addition, if the IVA.EDA bit = 0, the present set-up provides a range of 8 different vectors instead of 64 for easier interrupt acknowledge handling.

T7	T6	T5	T4	T3	T2	T1	T0	Original USART vector
0	0	1	0	0	0	1	1	MSK Register
T7	**T6**	0	**T4**	**T3**	**T2**	0	0	Final vector

V[7:6] represents a fixed and programmable value (vector base), stored in the IVA register.
V[4:2] represents the channel identification.

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4.4.2.LIV Register

The LIV register (latched interrupt vector) is used with the enhanced interrupt vector mode.This register stores the complete vector value given by the USART device during the interrupt acknowledge cycle. Note that the MSK setting has no influence on the LIV contents.

8-bit mode, read only: address $4B

IP Data	D7	D6	D5	D4	D3	D2	D1	D0
LIV	LIV7	LIV6	LIV5	LIV4	LIV3	LIV2	LIV1	LIV0

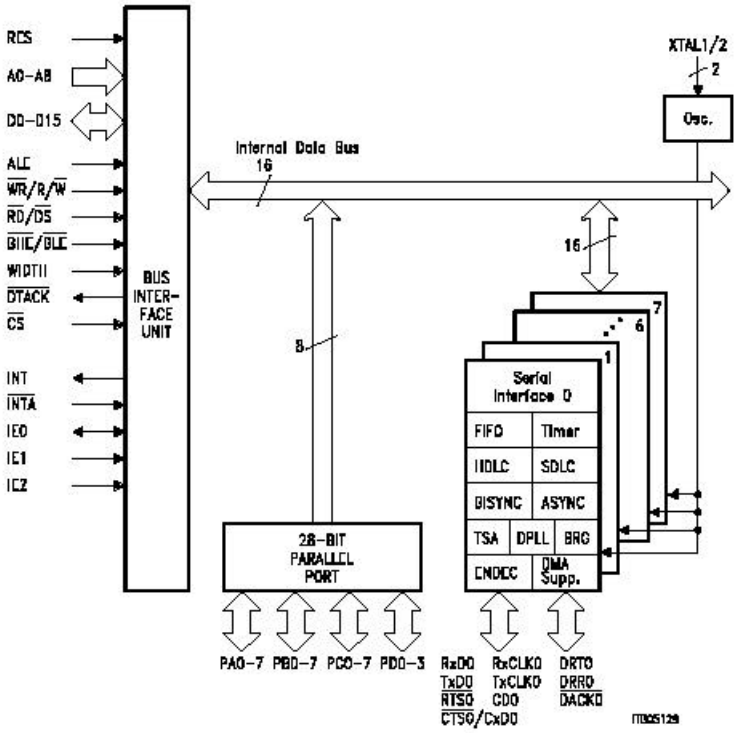
Value after reset, $00.

This register must be read into the ISP routine in order to get the complete USART vector. Note that a new value is stored into the LIV register during each interrupt acknowledge cycle. For this reason, this value must be read into the ISP service routine in order to ensure that no other IACK occurs, leaving the previous value.

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5. USART Controller

The UCC-08 module is based on the octal USART 82538 part. This device offers a high performance level in term of communication handling. It also offers great versatility which make it an appropriate device to target complex telecom applications such as serial link concentrators.
Both asynchronous and synchronous transmission modes could be handled with either asynchronous or synchronous characters oriented protocols.
Its integrated 1 kByte FIFO, subdivided in eight 64-Byte TxFIFO and eight 64-Byte Rx-FIFO, allows the UCC-08 module to support an intensive communication data flow with a reduced Rx overrun and CPU overhead.



82538 block diagram

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6. Enhanced Vector Mode

This mode could be very helpful if used in accordance with the vector provided by the USART. Depending on the USART vector set-up, this device is able to give up to 64 different vector values during the interrupt acknowledge cycle which may be too heavy for some real-time operating system.

In this case, the enhanced vector mode is used providing a partial vector during the IACK cycle and storing a complete vector into the LIV register.

This mode is enabled when the MSK register value is not zero. In this case, some bits of the USART vector are hidden during the IACK cycle. After that, the interrupt service routine needs to read the complete vector previously stored in the LIV register.

For more details about these register declarations, please refer to the relevant MSK Register and LIV Register sections.

7. Dual DMA Function

Both UCC-08A and UCC-08B modules handle DMA transfer for transmitting and receiving data path. The DMA mode is set in a three step sequences.

1. Define the UCC-08 DMA channel assignment. Refer to the relevant DM0R Register and DM1R Register sections for more details.
2. Set-up the USART DMA capability. Refer to the SAB82538 User's Manual for more software details.
3. Configure the DMA controller and the specific IP carrier requirements. Refer to the relevant documentation for more software and hardware details.

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8. UCC-08A Version

The UCC-08A, with its RS-232D interface, is typically dedicated to asynchronous transmission mode. This mode is set-up with the USART CCR1[CM2, CM1, CM0] bits. The transmission speed is handled by the internal Baud Rate Generator (BRG) or the clock recovery (DPLL) functions with the data encoding capability.
Note that the BRG clock source is driven by a 7.3728 MHz quartz connected to the XTAL inputs.

8.1. UCC-08A I/O Assignment

With UCC-08A version, the USART I/O assignment is as follows.

USART Signals	Signal Function
TxD[7:0]	TxD[7:0], transmit data
RxD[7:0]	RxD[7:0], receive data
/RTS[7:0]	/RTS[7:0], request to send
/CTS[7:0]	/CTS[7:0], clear to send
/PA[7:0][1)]	/DTR[7:0], data terminal ready
/CD[7:0]	/CD[7:0], carrier detect

[1)] All bits of the port A must be set as outputs. Refer to the UCC-08A Initialization Sequences section for more details.

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8.2. UCC-08A Initialization Sequences

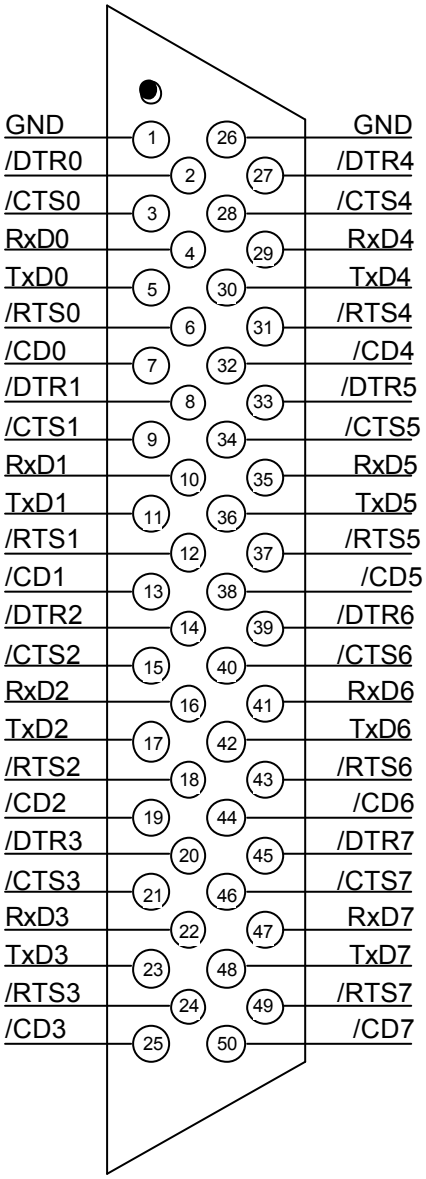
The following section describes the required initialization in order to define the specific USART input/output configuration for the UCC-08A.

1. Set CCR0.PU	Power up
2. Set CCR0.MCE	Master clock enable
3. Set CCR0.SM[1:0]	Asynchronous mode
4. Set CCR1.ODS	TxD pin as push-pull output
5. Set CCR1.BCR	Bit clock rate = 16
6. Set CCR1.CM[2:0]	Clock mode 7
7. Set BGR	Division factor for the baud rate generator
8. Set MODE.RAC	Receiver enable
9. Reset PCR (channel 4)	Define port C as output
10. Set PVR (channel 4)	Enable /CTS function
11. Set CMDR.RRES	Receiver reset
12. Read START.CEC = 0	Wait until previous command completed
13. Set CMDR.XRES	Transmitter reset
14. Read START.CEC = 0	Wait until previous command completed

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8.3. UCC-08A Connection

The UCC-08A signals of the eight RS-232D serial communication channels are present on the 50-pin IP module I/O connector.



Signals	DIR	Description
TxD[7:0]	O	Transmit Data
RxD[7:0]	I	Receive Data
/RTS[7:0]	O	Request To Send
/CTS[7:0]	I	Clear To Send
/DTR[7:0]	O	Data Set Ready
/CD[7:0]	I	Carrier Detect
GND	-	Ground

Three transition modules from Actis Computer, SC-08 (3Ux8TE version, eight RJ-45 connectors), SC-08D (6Ux4TE version, eight RJ-45 connectors), and SC-08DB (6Ux4TE version, eight DB-25 connectors) are also available for an easy user connection.

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9. UCC-08B Version

The UCC-08B, with its RS-422/RS-485 interface, can be used for both asynchronous and synchronous transmission modes.

This mode is set-up with the USART CCR1[CM2, CM1, CM0] bits. The transmission speed is handled by the external clock signals (RxC) or with the clock recovery (DPLL) function and data encoding capability. Note that the BRG clock source is driven by a 7.3728 MHz quartz connected to the XTAL inputs.

9.1. UCC-08B I/O Assignment

With the UCC-08B version, the USART I/O assignment is as follows:

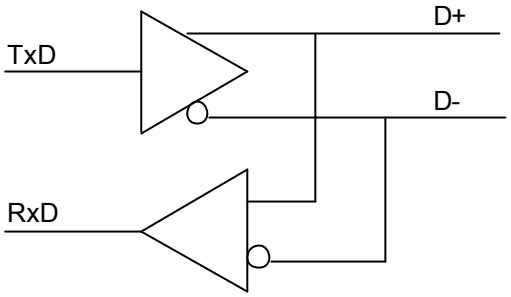
USART Signals	Signal Function
TxD[7:0]	TxD±[7:0], transmit data
RxD[7:0]	RxD±[7:0], receive data
/TxC[7:0][1)]	/CLK±[7:0], transmit/receive clock
/RxC[7:0][1)]	/CLK±[7:0], transmit/receive clock
/PB0[2)]	/ETxC0, control CLK[3:0] transmit clock enable
/PB1[3)]	/ETxC1, control CLK[7:4] transmit clock enable
/PC[7:0][4)]	/ECxD[7:0], enable collision detect function

[1)] Both TxC and RxC clock signals are connected together on the UCC-08B. Refer to the Clock Configuration section for more details about clock configuration.
[2)] The port B0 bit controls the transmit clock enable for the four first (0 to 3) serial channels.
[3)] The port B1 bit controls the transmit clock enable for the four first (4 to 7) serial channels.
[4)] All bits of port C must be set as outputs. These bits enable the collision detection function.

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9.2. Bus Configuration

In synchronous operation, the UCC-08B is able to handle the bus configuration mode for multi-drop network. This is achieved when both TxD and RxD data signals are connected together.



Bus configuration

This type of configuration, in relation with the RS-422 and RS-485 specifications, allows the following bus definition:

	RS-422	RS-485
Number of transmitters	1	32
Number of receivers	32	32

When more than one transmitter is connected to the same media (like the RS-485 specification), some caution must be taken to ensure that only one transmitter drives the data line at each time.

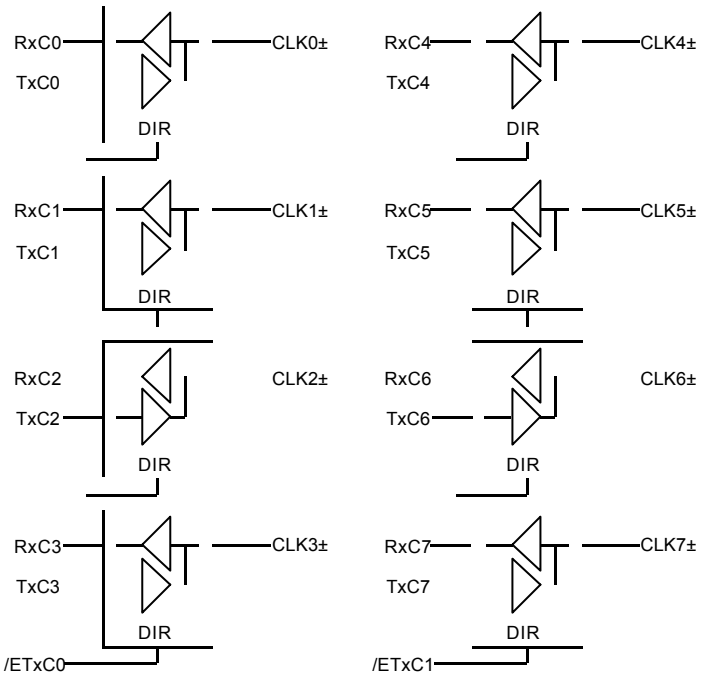
Two possibilities could be used to be compliant:

- Token like protocol, where a station transmits its data only when it receives the token acknowledge.
- Collision detection. In this case if more than one station drives the bus, a collision may occur which would abort the current transmission. A new transmission retry is issued until a collision is achieved. Refer to the Bus Configuration section for more details.

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9.3. Clock Configuration

Due to the number of I/O lines available on the P2 connector, the UCC-08B handles both TxC and RxC clock signals on the same differential signals. The transmitting clock activation is controlled by the port bits PB0 and PB1 with the following assignments:



UCC-08B clock configuration

CLK[7:0]±: represents the differential clock signals, in accordance with the CLKD0/CLKD1 set-up. They support either the transmitting or receiving clock path.

/ETxC0: controls the clock path direction. It is controlled by port B0. When set, the CLK0± to CLK3± signals are defined as receiving clock. When cleared, the CLK0± to CLK3± signals are defined as transmitting clock.

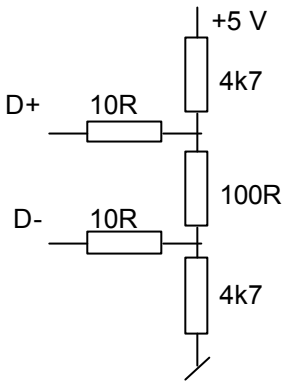
/ETxC1: controls the clock path direction. It is controlled by port B1. When set, the CLK4± to CLK7± signals are defined as receiving clock. When cleared, the CLK4± to CLK7± signals are defined as transmitting clock.

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9.4. Bus Terminators

For both RS-422 and RS-485 specifications, it is necessary to place a bus terminator circuit at the end of each network in order to ensure the signal adaptation.

The typical circuit is as follows:



Network terminator

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9.5. UCC-08B Initialization Sequences

The following section describes the required initialization in order to define the specific USART input/output configuration for the UCC-08B in both synchronous and asynchronous modes.

9.5.1.Synchronous Transmission Mode

1. Set CCR0.PU	Power up
2. Set CCR0.MCE	Master clock enable
3. Reset CCR0.SM[1:0]	Synchronous mode
4. Set CCR1.ODS	TxD pin as push-pull output
5. Reset CCR1.CM[2:0]	Clock mode 0
6. Set BGR	Division factor for the baud rate generator
7. Set MODE.RAC	Receiver enable
8. Reset PCR (channel 4)	Define port C as output
9. Reset PVR (channel 4)	Enable collision detect function
10. Set CMDR.RRES	Receiver reset
11. Read START.CEC = 0	Wait until previous command completed
12. Set CMDR.XRES	Transmitter reset
13. Read START.CEC = 0	Wait until previous command completed

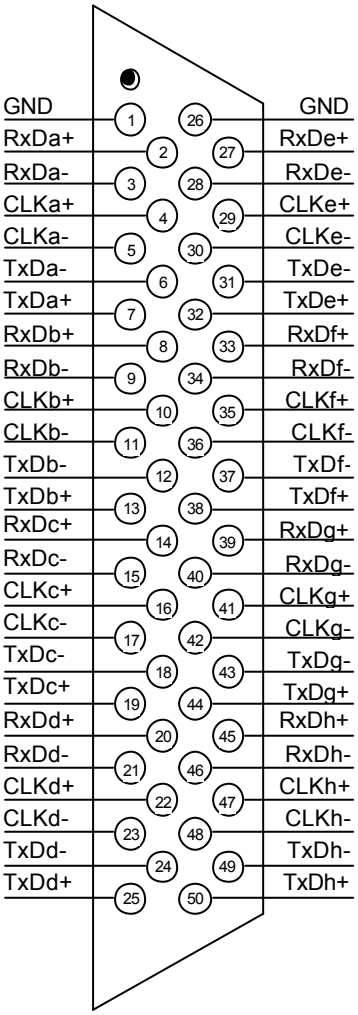
9.5.2.Asynchronous Transmission Mode

1. Set CCR0.PU	Power up
2. Set CCR0.MCE	Master clock enable
3. Set CCR0.SM[1:0]	Asynchronous mode
4. Set CCR1.ODS	TxD pin as push-pull output
5. Set CCR1.BCR	Bit clock rate = 16
6. Set CCR1.CM[2:0]	Clock mode 7
7. Set BGR	Division factor for the baud rate generator
8. Set MODE.RAC	Receiver enable
9. Reset PCR (channel 4)	Define port C as output
10. Set PVR (channel 4)	Enable /CTS function
11. Set CMDR.RRES	Receiver reset
12. Read START.CEC = 0	Wait until previous command completed
13. Set CMDR.XRES	Transmitter reset
14. Read START.CEC = 0	Wait until previous command completed

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9.6. UCC-08B Connection

The following figure gives the connector assignment for the eight serial ports (channel A to H) with the related RS-422/RS-485 interface signals.



Signals	Dir	Description
TxD+	O	Positive transmit data
TxD-	O	Negative transmit data
RxD+	I	Positive transmit data
RxD-	I	Negative transmit data
CLK+	I/O	Positive transmit/receive clock
CLK-	I/O	Negative transmit/receive clock
GND	O	Ground

Note that signal direction for CLK± is defined by the CLKG0 and CLKG1 bit settings.

Three transition modules from ACTIS Computer, SC-08 (3Ux8TE version, eight RJ-45 connectors), SC-08D (6Ux4TE version, eight RJ-45 connectors), and SC-08DB (6Ux4TE version, eight DB-25 connectors) are also available for an easy user connection.

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10. Sample Codes

10.1. SAB82538 Structure

```
struct _ucc08
{
   unsigned char rsvd0;
   unsigned char pgr;
   unsigned char rsvd1;
   unsigned char dma0;
   unsigned char rsvd2;
   unsigned char dma1;
   unsigned char rsvd3;
   unsigned char rsvd4;
   unsigned char rsvd5;
   unsigned char msk;
   unsigned char rsvd6;
   unsigned char liv;
   unsigned char rsvd7;
};

struct _sab82538
{
   struct
   {
      unsigned char fifo[32];
      unsigned char star_cmdr;
      unsigned char rsvd0;
      unsigned char mode;
      unsigned char timr;
      unsigned char xon;
      unsigned char xoff;
      unsigned char tcr;
      unsigned char daf0;
      unsigned char rfc;
      unsigned char rsvd1;
```


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```
    unsigned char rbcl_xbcl;
    unsigned char rbch_xbch;
    unsigned char ccr0;
    unsigned char ccr1;
    unsigned char ccr2;
    unsigned char ccr3;
    unsigned char tsax;
    unsigned char tsar;
    unsigned char xccr;
    unsigned char rccr;
    unsigned char vstr_bgr;
    unsigned char tic;
    unsigned char mxn;
    unsigned char mxf;
    unsigned char gis_iva;
    unsigned char ipc;
    unsigned char isr0_imr0;
    unsigned char isr1_imr1;
    unsigned char pvr;
    unsigned char pis_pim;
    unsigned char pcr;
    unsigned char rsvd2;
  }channel[8];
};
```


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10.2. Asynchronous Transmission

```
void test_ucc08a()
{
  long error;

  printf("  Test Transmit/Receive\n");
  for(channel = 0; channel < 8; channel++)
  {
     sab_ptr->channel[channel].ccr0= 0xc3;
     sab_ptr->channel[channel].ccr1= 0x1f;
     sab_ptr->channel[channel].ccr2= 0x30;
     sab_ptr->channel[channel].vstr_bgr = 0x18;
     sab_ptr->channel[channel].rfc = 0x0c;
     sab_ptr->channel[channel].mode= 0x0c;
     sab_ptr->channel[4].pcr= 0x00;
     sab_ptr->channel[4].pvr= 0xff;
     sab_ptr->channel[channel].star_cmdr= 0x41;
     while((sab_ptr->channel[channel].star_cmdr & 0x04) != 0);

     sab_ptr->channel[7-channel].ccr0= 0xc3;
     sab_ptr->channel[7-channel].ccr1= 0x1f;
     sab_ptr->channel[7-channel].ccr2= 0x30;
     sab_ptr->channel[7-channel].vstr_bgr = 0x18;
     sab_ptr->channel[7-channel].rfc = 0x0c;
     sab_ptr->channel[7-channel].mode= 0x0c;
     sab_ptr->channel[7-channel].star_cmdr= 0x41;
     while((sab_ptr->channel[7-channel].star_cmdr & 0x04) != 0);

      for(i = 30; i < 255; i++)
      {
      tsleep(1);
      while(sab_ptr->channel[channel].isr0_imr0 != 0);
      while(sab_ptr->channel[7-channel].isr0_imr0 != 0);
      while(sab_ptr->channel[channel].isr1_imr1 != 0);
      while(sab_ptr->channel[7-channel].isr1_imr1 != 0);
```


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```
        for(error = 0; error < 10000; error++)
          if(((sab_ptr->channel[channel].star_cmdr & 0x0a)) == 0x02)   /* check TEC */
   {
     error = 0;
     break;
   }

if(error != 0)
{
   printf("Transmission error channel %d\7\n",channel);
   exit(0);
}

        sab_ptr->channel[channel].tic = i;                    /* transmit immediate char */

for(error = 0; error < 10000; error++)
   if ((sab_ptr->channel[7-channel].star_cmdr & 0x20) != 0)
   {
     error = 0;
     break;
   }
if(error != 0)
{
          printf("Reception error channel %d\7\n",7-channel);
                exit(0);
        }

        sab_ptr->channel[7-channel].star_cmdr = 0x20;
while((sab_ptr->channel[7-channel].star_cmdr & 0x04) != 0);

if(sab_ptr->channel[7-channel].fifo[0] != i)
        {
          printf("Error read/write channel %d to %d\n",channel,7-channel);
          tot_err++;
          break;
        }
```


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```
            sab_ptr->channel[7-channel].star_cmdr = 0x80;
      while((sab_ptr->channel[7-channel].star_cmdr & 0x04) != 0);
     }
}
}
```

10.3. Synchronous Transmission

```
void test_ucc08b()
{
  long error;
  unsigned char RxFIFO;

  printf("  Test Transmit/Receive\n");
  for(channel = 0; channel < 8; channel++)
  {
     sab_ptr->channel[channel].ccr0= 0xc4;
     sab_ptr->channel[channel].ccr1= 0x10;
     sab_ptr->channel[channel].ccr2= 0x38;
     sab_ptr->channel[channel].vstr_bgr = 0x18;
     sab_ptr->channel[channel].mode= 0x88;
     sab_ptr->channel[4].pcr= 0x00;
     sab_ptr->channel[4].pvr= 0x00;

     sab_ptr->channel[7-channel].ccr0= 0xc4;
     sab_ptr->channel[7-channel].ccr1= 0x11;
     sab_ptr->channel[7-channel].ccr2= 0x18;
     sab_ptr->channel[7-channel].vstr_bgr = 0x18;
     sab_ptr->channel[7-channel].mode= 0x88;

      for(i = 30; i < 255; i++)
      {
        tsleep(1);
        sab_ptr->channel[channel].star_cmdr= 0x41;
        while((sab_ptr->channel[channel].star_cmdr & 0x04) != 0);
              sab_ptr->channel[7-channel].star_cmdr= 0x41;
                    while((sab_ptr->channel[7-channel].star_cmdr & 0x04) != 0);
```


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```
  sab_ptr->channel[7-channel].ipc = 0x80;

                sab_ptr->channel[channel].fifo[0] = i;

     for(error = 0; error < 10000; error++)
         if(((sab_ptr->channel[channel].star_cmdr & 0x4c)) == 0x48)
         {
    error = 0;
    break;
}

if(error != 0)
{
    printf("Transmission error channel %d\7\n",channel);
    exit(0);
}

sab_ptr->channel[channel].star_cmdr = 0x0a;
while((sab_ptr->channel[channel].star_cmdr & 0x04) != 0);

         for(error = 0; error < 10000; error++)
    if ((sab_ptr->channel[7-channel].isr0_imr0 & 0x80) != 0)
    {
       error = 0;
       break;
    }

if(error != 0)
{
           printf("Reception error channel %d\7\n",7-channel);
                 exit(0);
         }
RxFIFO = sab_ptr->channel[7-channel].fifo[0];

         if(RxFIFO != i)
         {
```

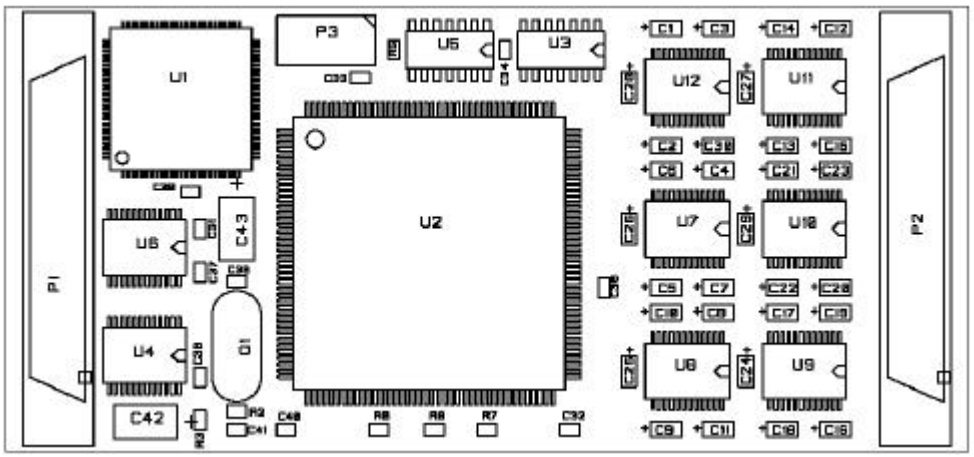

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```
                    printf("Error read/write channel %d to %d, write = %x, read =  %x\n",channel,7-
channel,i,RxFIFO);
                    tot_err++;
                    break;
                }
                sab_ptr->channel[7-channel].star_cmdr = 0x80;
            while((sab_ptr->channel[7-channel].star_cmdr & 0x04) != 0);
        }

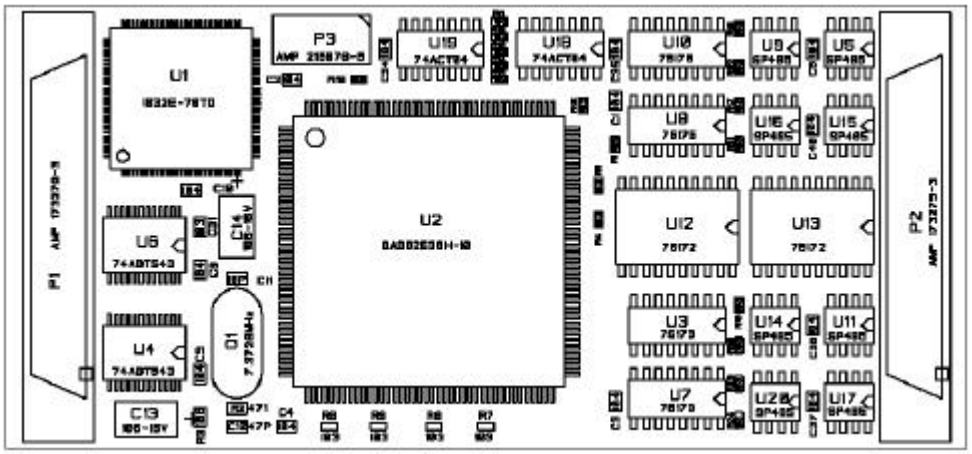
    }
}
```


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11. Components Location



IP-UCC-08A



IP-UCC-08B

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12. OEM Warranty

ACTIS Computer warrants that its Product sold hereunder, excluding software, will at the time of shipment be free from defects in material and workmanship and will conform to ACTIS Computer's applicable specifications or, if appropriate, to CUSTOMER's specifications previously accepted by ACTIS Computer in writing. If Products sold hereunder are not as warranted, ACTIS Computer shall, at its option and as CUSTOMER's exclusive remedy, either refund the purchase price, or repair or replace the Product, provided proof of purchase and written notice of nonconformance are received by ACTIS Computer within the applicable periods noted below and provided said nonconforming Products are, with ACTIS Computer's written authorization, returned in protected shipping containers FOB ACTIS Computer's plant within thirty (30) days after expiration of the warranty period. Upon verification by ACTIS Computer that the Product does not conform to this warranty, ACTIS Computer will reimburse CUSTOMER for the cost of transporting the goods to and from ACTIS Computer's plant. This warranty shall not apply to any Products ACTIS Computer determines have been, by CUSTOMER or otherwise, subjected to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been the subject of mishandling, misuse, neglect, improper testing, repair, alteration, damage, assembly or processing that alters physical or electrical properties.

This Limited Warranty is effective from the date of sale and shall expire on the expiration date of the applicable hardware product warranty period. The expiration date is defined as three-year for mezzanine modules and the relevant transition modules, and one-year for all cPCI and VME boards. CUSTOMER must notify ACTIS Computer, in writing, no later than thirty days after expiration of this Limited Warranty of Product that does not conform to this Limited Warranty. In the event that the Product does not conform to this Limited Warranty, ACTIS Computer shall, at its option, repair, replace or refund the purchase price of the non-conforming Product. The remedies provided herein are the sole and exclusive remedies for a breach of this Limited Warranty.
ACTIS Computer hereby disclaims all implied warranties, including implied warranties of merchantability or fitness for a particular purpose. ACTIS Computer shall not be liable for any special, incidental or consequential damages due to a breach of this (Limited) Warranty.

Warranty Service and Return Information
Please contact the place of purchase for return procedures. If customer purchased product(s) directly from ACTIS Computer, then customer shall return the product(s) to ACTIS Computer pursuant to the following terms. Customer must obtain a Return Material Authorization ("RMA") number by calling customer service at +41 (22) 794 43 91. Returned products should be shipped to the following address within 10 days of receiving an RMA number to avoid charges for the replacement product:

ACTIS Computer
Attn: RMA Dept - RMA# _____
19, chemin du Champ-des-Filles
1228 Plan-Les-Ouates
Switzerland

Please retain shipping information, including tracking numbers. If ACTIS Computer determines that failure of the product(s) was not a result of a defect in materials or workmanship, ACTIS Computer reserves the right to charge customer for parts and labor at ACTIS Computer's then current labor rate. ACTIS Computer will advise customer prior to assessing these charges.

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13. Ordering Information

Reference	Description
UCC-08A	Universal Synch/Asynch Serial I/O communication controller, eight-channel, up to 115.2 kbit/s, RS-232D interface.
UCC-08B	Universal Synch/Asynch Serial I/O communication controller, eight-channel, up to 10 Mbit/s, RS-422/RS-485 interface.
SC-08	Transition module with eight RJ-45 8-pin connectors, network terminators for RS-422/RS-485 interfaces and standard 3Ux8TE front panel
SC-08D	Transition module with eight RJ-45 8-pin connectors, network terminators for RS-422/RS-485 interfaces and standard 6Ux4TE front panel.
SC-08DB	Transition module with eight DB-25 connectors, DTE and DCE mode selectable by jumpers, network terminators, 6Ux8TE front panel.

14. Related Documentation

1. ESCC8 SAB82538 SAF82538 User's Manual,
   Siemens ordering code B115-H6750-G1-X-7600.
2. ESCC2 - ESCC8 Application Note,
   Siemens ordering code B115-H6784-X-X-7600.
3. SC-08 User's Guide, Actis ordering code UG/SC08.

Note that these documents are available on the ACTIS Computer web site at http://www.actis-computer.com

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