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VME IP Carrier

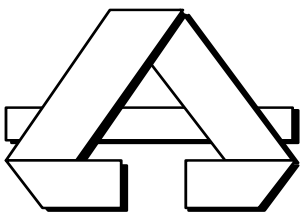
for four IP modules

VIPC-400

User's Guide

9724

DRAFT



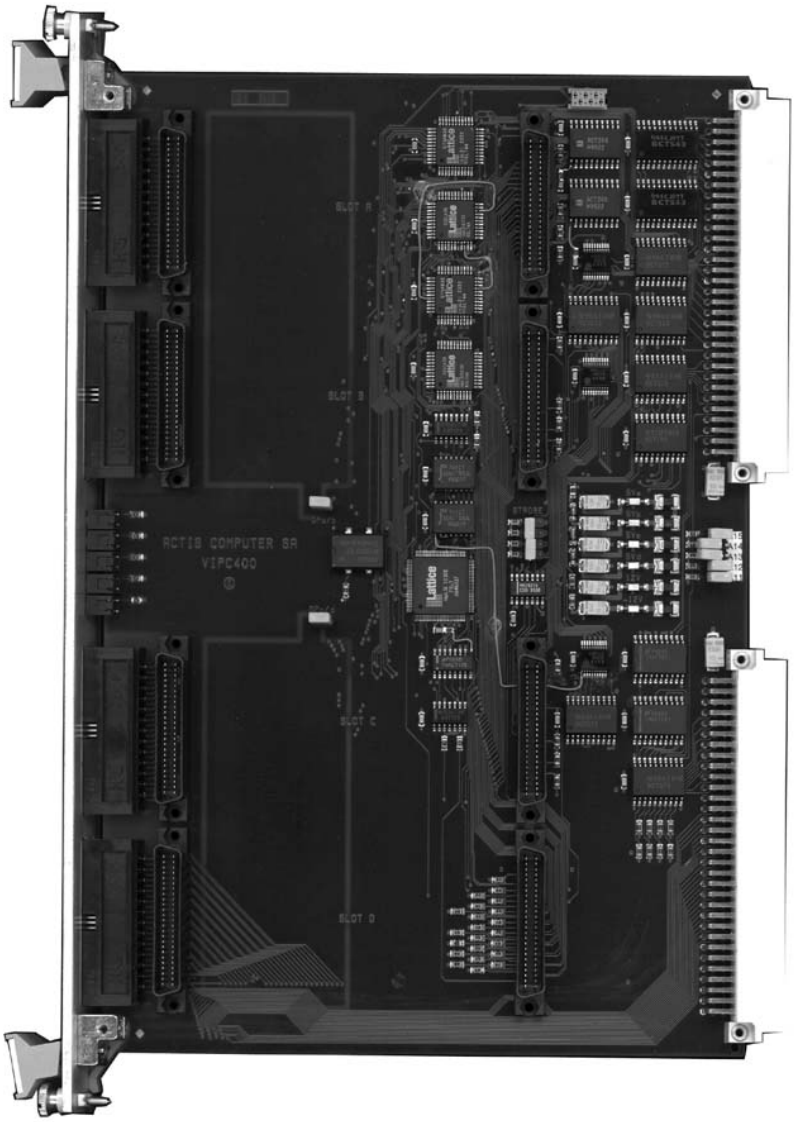
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COMPUTER S.A.

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1. Introduction

The VIPC-400 from ACTIS Computer is an IP carrier for the VME Bus, able to accept up to 4 IP modules. Each IP may be operated at 8 MHz or 32 MHz interface clock frequencies.

The input-output spaces and ID spaces for the IPs are accessed in A16:D16 mode from the VME Bus, selected by jumpers at offsets multiples of hex. $0800.

Memory access may be defined in A24 space or in A32 space. The base address, access mode and size are software controlled. In the A32 mode, each IP is allocated 8 Mbytes of memory while in the A24 mode the allocated memory space of the VME Bus may be set to 128 Kbytes per IP (minimum) to 2 Mbytes per IP (maximum). It is possible to set the upper memory address bits in the A24 modes by means of a register: if this register is not set the default values of the upper bits are zeros. Memory access is disabled at reset, and then may be enabled or disabled at will by software.

A very easily managed interrupt routing scheme provides for up to 3 interrupt lines on the VME Bus to be driven. Each group can accept either of the two interrupt lines from each IP. A rotating priority scheme is used within each group for the 4 possible inputs. The output from each group is set to drive any of the 7 VME Bus interrupt lines by means of a software-set register. This is cleared by reset, so disabling interrupts. An interrupt acknowledge vector (STATUS/ID) register is included, and may be set by software to return a vector in cases where an IP does not have the capability to do so.

The following manual will give you the required information for the use of our board. However, in case you need more support, please contact your distributor or:

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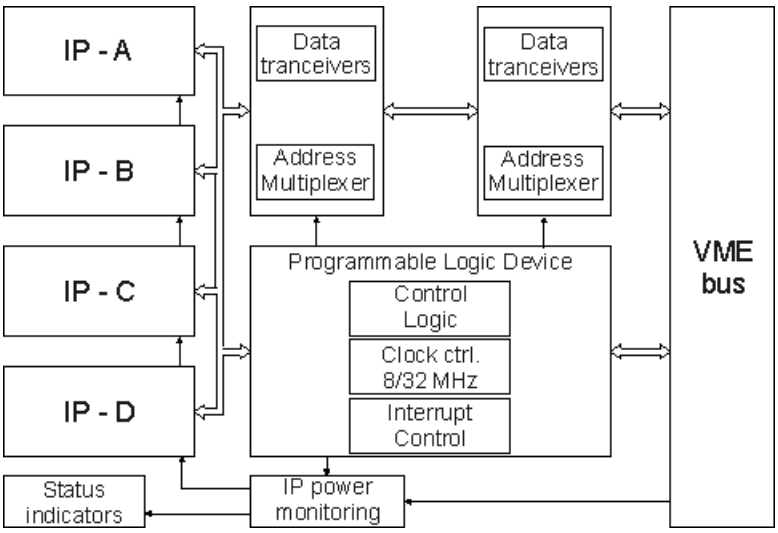
2. Main Features

2.1. Summary of features

- VME Bus double-height (6U) carrier board
- Accepts 4 IP modules (or 2 double-width modules)
- Conforms to IP Specification 0.7.1 (VITA-4 draft)
- Each IP can be operated at 8MHz or 32 MHz
- Conforms to VME Bus specification C.1 (IEC 821)
- I/O and ID access mode A16/D16
- A16 base address defined by 5 jumpers
- Very few jumpers to set: easily configured by the user
- Memory access in A24/D16 or A32/D16 modes
- A24 or A32 memory space access base address and size of block in A24 space set up by software
- All 22 address bits can be controlled in A24 access modes
- Memory access disabled on reset, avoids problems with any operating system initialisation memory-search process
- Read-modify-write cycles supported
- IP interrupts directed to any 3 of the 7 VME Bus interrupt lines
- Carrier board can generate a vector (STATUS/ID byte) if any IP can not do so
- input-output connectors on front panel, compatible with ACTIS Computer standard cables to external adaptors
- LED indicators on front panel show IP access
- Flashing red LED shows IP power faults

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2.2. Block Diagram



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3. Description

3.1. Input-Output and ID Addressing.

The VIPC-400 input-output space is accessible in A16:D16 mode at offsets defined by a set of 5 jumpers.

These offsets are at multiples of $0800 - hexadecimal.

The factory setting of the jumpers is to a base address of $6000 and this will be used to illustrate further details.

The selection of each IP, numbered 0 to 3, is controlled by address lines A09 and A08. Thus the I/O space for IP 0 starts at $6000, that for IP1 at $6100 etc. The ID space is accessed by setting A07 to 1, so that the ID space fr IP 0 starts at $6080. Table 1 shows how these spaces are arranged.

IP module	Space	Offset
A	I/O	Base + $0000
A	ID	Base + $0080
B	I/O	Base + $0100
B	ID	Base + $0180
C	I/O	Base + $0200
C	ID	Base + $0280
D	I/O	Base + $0300
D	ID	Base + $0380
Various	Configuration	Base + $0400

Table 1: I/O Space Assignments

A few configuration registers are located at higher offsets: with A10 set to 1. The module occupies a total A16 address space extending to offsets of $047F above the base address (to $647F in the example). Other modules in the VME Bus crate can be allowed to use addresses such as $6500 if need be.

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The base address settings are achieved by setting jumpers 1 to 5 to correspond to address lines A11 to A15 respectively. A jumper bridging a pin to the ground row will define a logical 0 for its address bit. Thus, to take the example of a base address of $6000, address bits A11, A12 and A15 must be 0 and A13 plus A13 at 1, so jumpers 1, 2 and 5 must be inserted to link to pins 6, 7 and 10 as shown in Figure 1. Table 2 lists the hexadecimal values set by each jumper NOT inserted.

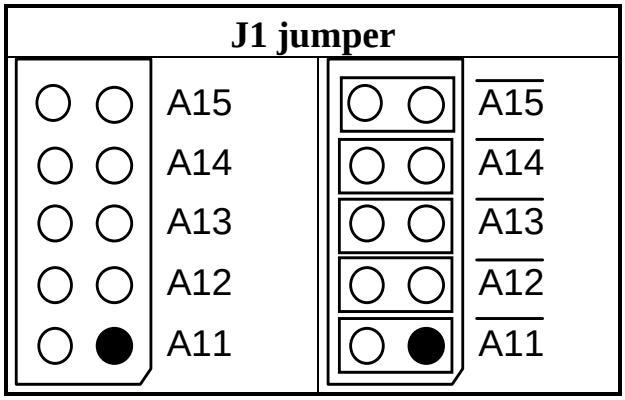


Figure 1: A16 Selection

Jumper pin	Address line when not linked	Offset
5/6	A15	$8000
4/7	A14	$4000
3/8	A13	$2000
2/9	A12	$1000
1/10	A11	$0800

Table 2: A16 Base Address

Not that in many cases the IP registers will be of 8 bits, using data lines D0..D7. In the VME Bus environment these registers will be accessed at ODD offsets.

It should also be pointed out that the carrier board provides an essentially transparent link between the VME Bus and each IP module. It does not provide a time-out, so that any attempt to access a non-existent feature of an IP might, depending on its design, produce a time-out on the VME Bus.

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3.2. Memory Space Access.

The VIPC-400 provides for access in A24:D16 and A32:D16 modes. The A32 mode should be used when available, but is not always provided as it uses signals on the P2 connector of the bus.

3.2.1. 32 Memory Space Access.

In this mode the full 22-bit address is available to each IP; address lines A24 and A23 are used to select the IP. The base address is defined by the MBA register, in which data bits D7..D1 correspond to A31..A24 respectively.

Thus the base address could be set to $ 1600 0000 hex. by loading data pattern $16 into the MBA register.

On reset, memory access is disabled. To enable it in A32 mode, the MAM (memory access mode) register is used, and it should be set to $07. To disable access, clear this register.

Offsets for the four modules are:

IP module	MEM space Offset
IP A	Base address + $ 0000 0000
IP B	Base address + $ 0080 0000
IP C	Base address + $ 0100 0000
IP D	Base address + $ 0180 0000

3.2.2. A24 Memory Space Access.

The total VME Bus address space in A24 mode is limited to 16 Mbytes, so there is no question of assigning 8 Mbytes to each IP of the VIPC-400 in this mode. Instead, the areas mapped from the A24 addresses to the IP addresses can be set to 128 kbytes, minimum, up to 2 Mbytes each at a maximum.

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The same base register, the MAR register, is used but in this case bits D7..D1 correspond to some part of the group of address lines A23..A17 respectively. There are 5 possible A24 modes, validated by writing code $01 to $05 to the MAM register. This is cleared on reset.

In the same way as for the other modes, two address lines are used to select each of the four IPs. It should be noted that for each mode a different pair of address bits is used.

Table 3 shows how all this works out in practice.

Mode A16 (MAM reg.)	**A23**	**A22**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**
1	MS	MS	MS	MS	MS	IPS	IPS	IPA
2	MS	MS	MS	MS	IPS	IPS	IPA	IPA
3	MS	MS	MS	IPS	IPS	IPA	IPA	IPA
4	MS	MS	IPS	IPS	IPA	IPA	IPA	IPA
5	MS	IPS	IPS	IPA	IPA	IPA	IPA	IPA
HAR bits	D7	D6	D5	D4	D3	D2	D1	-----

Table 3: A24 Addressing Possibilities.

Key: IPA: Address lines passed to each IP
IPS: Address lines used to select each IP
MS: Define base address of VIPC-400
HAR: These bits are passed to the IP as high address bits if not marked IPA.

The IP address is never completely defined by the VME Bus address lines in the A24 modes, so in the VIPC-400 the remaining bits are taken from a "High Address Register" which is set to 0 on reset, and may be loaded with any value defined. In this way the bits corresponding to IPS and MS bits are not seen on the IP address bus, but are set to 0 by default. Furthermore, any full 22-bit address may be generated at any time by means of the HAR register, if required.

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3.3. Interrupts.

3.3.1. Groups.

Each IP is able to generate two interrupt requests, identified as IntReq0 and IntReq1. The interrupt handling scheme of the VIPC-400 takes these, in up to 3 groups, and each group may drive any of the 7 interrupt request lines of the VME Bus. (In many cases these 7 request lines correspond to 7 levels of priority in the host computer module.)

The assignment of the 8 interrupts into groups is controlled by three mask registers, each having 8 bits.

For this discussion, these groups will be labelled X, Y and Z, so the mask registers are called the XIG, YIG and XIG registers. Table 4 shows the functions of the 8 bits in each of these.

XIG..ZIG Bits	7	6	5	4	3	2	1	0
IP Module Number	3	2	1	0	3	2	1	0
Interrupt line	1	1	1	1	0	0	0	0

Table 4: Interrupt Mask Register Functions

There are two restrictions. The first is obvious: no two of the above registers may have corresponding bits set, so an interrupt may be assigned to one group only. The second is that no group may have both interrupts from one IP enabled. This means that no group will have more than 4 interrupts enabled.

In practice, many applications will be handled very simply, as it is rare to find the second interrupt used. Thus the XIG register might typically be set to $07, enabling three of the IP IntReq0 lines, with YIG and ZIG cleared. More complex applications may profit by being able to assign the various interrupts to 3 priority levels.

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Within a group, the four possible validated interrupts are dealt with on a rotating priority basis, such that the module most recently serviced has lowest priority on that level in the next interrupt acknowledge cycle.

3.3.2. Interrupt Levels.

For each group, a 3-bit register defines the VME Bus interrupt line to be driven. These registers, called the XID, YID and ZID registers, are cleared on reset, and may be loaded with values $01 to $07 to select the output. The obvious restriction is that each group must drive a different interrupt line, i.e. each of these registers must hold a different code.

3.3.3. Register.

Although most IP modules are able to supply a Status/ID code, or interrupt vector, during the interrupt acknowledge process, some do not have this capability.

The VIPC-400 provides an interrupt vector register for this situation, and a control register to validate it for any IP.

The IVR has 8 bits, but only the m.s. 6 bits are valid when writing to it. The two l.s. bits, returned in the interrupt acknowledge cycle, are coded to identify the module which generated the interrupt to which the VME Bus master is responding.

The control register, the IVRE register, is cleared on reset, and to validate the IVR response for IPs 0 to 3 one sets bits 0 to 3 respectively of the IVRE register.

Note that there is no attempt made to show which of the two interrupt lines of the IP is concerned. The use of the second line is very rare, and if both lines are used the information might be deduced from the particular group (i.e. level) to which the IACK is directed.

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3.3.4. Clock Frequency.

When the VIPC-400 starts up, the default clock frequency of 8 MHz is selected for each IP. Any IP capable of dealing with a 32MHz clock will have this shown in the contents of the ID ROM, readable at 8MHz in all cases.

A control register permits IPs 0 to 3 to be operated at 32 MHz by setting data bits 0 to 3 respectively. Note that this register, the FIPC register, is write-only so it may be neccessary in some applications to hold a copy as a global variable in the software, so that application programs may switch the individual clock frequencies at will. In most applications, the hardware configuration will be stable and well defined, so that a suitable constant will be loaded into the FIPC register on initialisation of the module.

3.4. Configuration Registers.

The following table shows the address offsets of the configuration registers from the base address of the modules, in A16 space. They are all 8-bit registers, at odd offsets in the usual environment. All other addresses in the range $0400 to $047F are reserved.

Register	Function	R/W	Offset (hex)
IVR	Interrupt vector	R/W	$0401
MAM	Memory access mode	W	$0403
HAR	High address	R/W	$0405
FIPC	Clock frequency set	W	$0407
IVRE	Enable VIPC-400 IV	W	$0409
MAR	Memory base address	W	$040D
XIG	Group X mask	W	$0415
XID	Group X drive	W	$0417
XIG	Group Y mask	W	$0425
XID	Group Y drive	W	$0427
XIG	Group Z mask	W	$0435
XID	Group Z drive	W	$0437

Table 5: Configuration Registers

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3.5. Other Features

3.6. Fuses.

There are four fuses installed to protect the IP modules. Each pair has one fuse for its +5 volt supply: note that a pair might be in fact a double-width module.

The other two fuses are for the +12 volt and -12 volt lines.

3.7. Front Panel Indicators.

Five LED indicators are installed. One of these is a red indicator of power problems, such as a blown fuse, and in case of a fault it will flash at 400ms intervals.

The other four are green, and are lit when a valid operation takes place on each of the four IPs. They triggered by the ACK* lines, so might not always indicate an access in case of an error, and they stay illuminated for about 300ms after any isolated events. They show all forms of access including reset, so that all four will flash briefly on power-up.

3.7.1. Ground Planes.

Each pair of IPs has a local ground plane on the carrier board under its input-output zone. Jumpers are fitted to link these to the local ground of the VME Bus, but may be removed if required to alter the screening situation. There is a 47 kohm resistor wired across each of these jumpers.

3.7.2. Strobe lines.

Each IP has a "strobe" line on the carrier board interface connector and these lines are undefined in the specification. They may be used as required in any special circumstances. A pair of pins, connected to Strobe and Ground, is provided on the carrier board for each IP.

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3.8. Compatibility.

3.9. Environment.

•The VIPC-400 is designed to function over the temperature range 0 to 70 °C. All integrated circuits are of CMOS type so that the power taken is quite low: about 300mA at +5 volts without the IPs, rising to twice that if intensively used, to which the IP current consumption must be added. On request, a version for the temperature range

•-40° to +85°C temperature range can be supplied.

3.9.1. VME Bus.

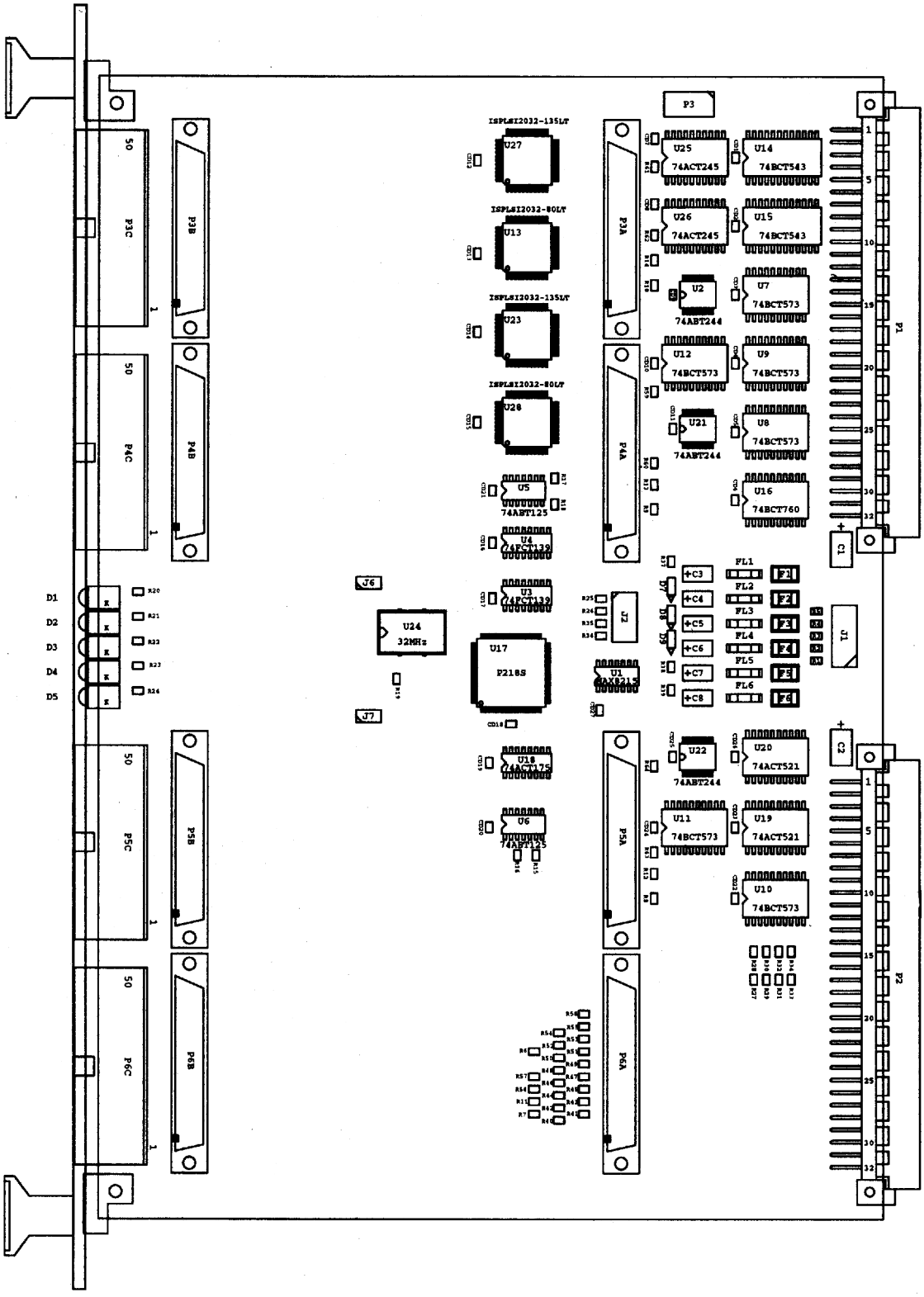
•Double height VME Bus module (160mm x 233.5 mm).
•Connects to backplane via P1 and by P2 Row b.
•No connections to P2 rows a and c.
•Complies with specification revision C.1 (IEC 821).
•A16/D16 slave for IP I/O and ID space
•A16/D08(O) slave for configuration registers
•A24 and A31 D16/D08(EO) slave for IP memory
•D08(O) interrupter
•Accepts supervisor mode and non-supervisor AM codes.

3.9.2. IP Modules.

•Accepts up to four standard IP modules, or two double-width modules.
•Controls IO, ID, MEM and IACK functions in each IP.
•Individually selectable 8 or 32MHz clocks to each IP.
•Four front panel I/O connectors linked to the corresponding IP connectors via the carrier board.
•Conforms to specification Rev. 0.7.1 (VITA-4 draft)

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4. Component location



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