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USER'S GUIDE

VSBC-6862

VME Single Board Computer with PowerQUICC II processor

Revision 1.43
3105

ACTIS Computer

www.actis-computer.com
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1 Product description

1.1. Introduction

Today industrial applications are growing in telecom market due to the demand of networked architecture. This method offers great advantage where complex processes are handled and where real time tasks are the critical features.
The VSBC-6862 combines the best possibilities with its flexible industrial interface and its wide range of communications ports.

This single board computer is built around a communication-oriented processor: The PowerQUICC II (MPC-8260) is a member of the PowerPC family of MOTOROLA semiconductors division. This processor provides a very efficient architecture with two RISC processors built in the same chip: a PowerPC core controls all host system operations, and a dedicated RISC processor for the communication part.

The MPC-8260 integrates two main components, the embedded PowerPC core and the Communications Processor Module (CPM). This dual-processor architecture is more efficient than traditional architectures because the CPM offloads peripheral tasks from the embedded PowerPC core.

This single board computer, in 6U form factor, is VME bus master and slave designed as a flexible solution for communication applications. The VSBC-6862 is designed to offer a very open architecture through two Fast Ethernet ports, four multi-protocol communication ports, and two RS-232 serial ports.

An other advantage is the flexible I/Os extension, which is implemented through the four VITA-4 standard IP Module slots supporting high performance 16-bit modules at up to 8 MHz clock with DMA capabilities. These four slots offer to the user the possibility to customize its system very easily with these cost saving modules.

The combination of the PowerPC core and the CPM dedicated RISC processor, along with the versatility and performance of the MPC-8260 I/Os provides customers with an enormous potential in developing networking and communications products while significantly reducing time-to-market development stages.

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1.2. Features

This board has been designed to integrate the most required functions, including several Fast Ethernet ports, communication ports, and the flexibility of four IP modules slots for easy user's customization.

- Designed with Motorola PowerQUICC II processor
- A 32-bit EC603 ™ processor core rated at 280.0 MIPS at 200 MHz (Dhrystone 2.1)
- Dedicated 32-bit RISC processor for communication protocol handling (CPM)
- Up to 128 MByte of SDRAM memory with burst capabilities, 64 bit data bus width
- 8 or 16 MByte of Flash memory for non-volatile information, divided on two bootables banks, one bank dual-port with the VME bus
- 1 MByte of SRAM memory dual-port with the VME bus Non-volatile operation through the VME stand-by signal
- A separate real time clock device with 32 kByte of battery backed-up SRAM
  Dual-port with the VME bus
- 8 kbit I^2C EEPROM for board and user configuration
- Two Fast Ethernet 100Base-TX/10Base-T interfaces with auto-negotiation capability
- Four HDLC serial ports selectable between RS-232 / RS-422 / RS-485 or V.35
- Two RS-232 serial ports
- I^2C bus for local extensions
- JTAG port for debug
- VME master, slave, system controller interface
- Four IP Modules slots, compatible with the ANSI/VITA-4 1995 specification, support for 8 MHz clock with DMA capabilities

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1.3. Photograph

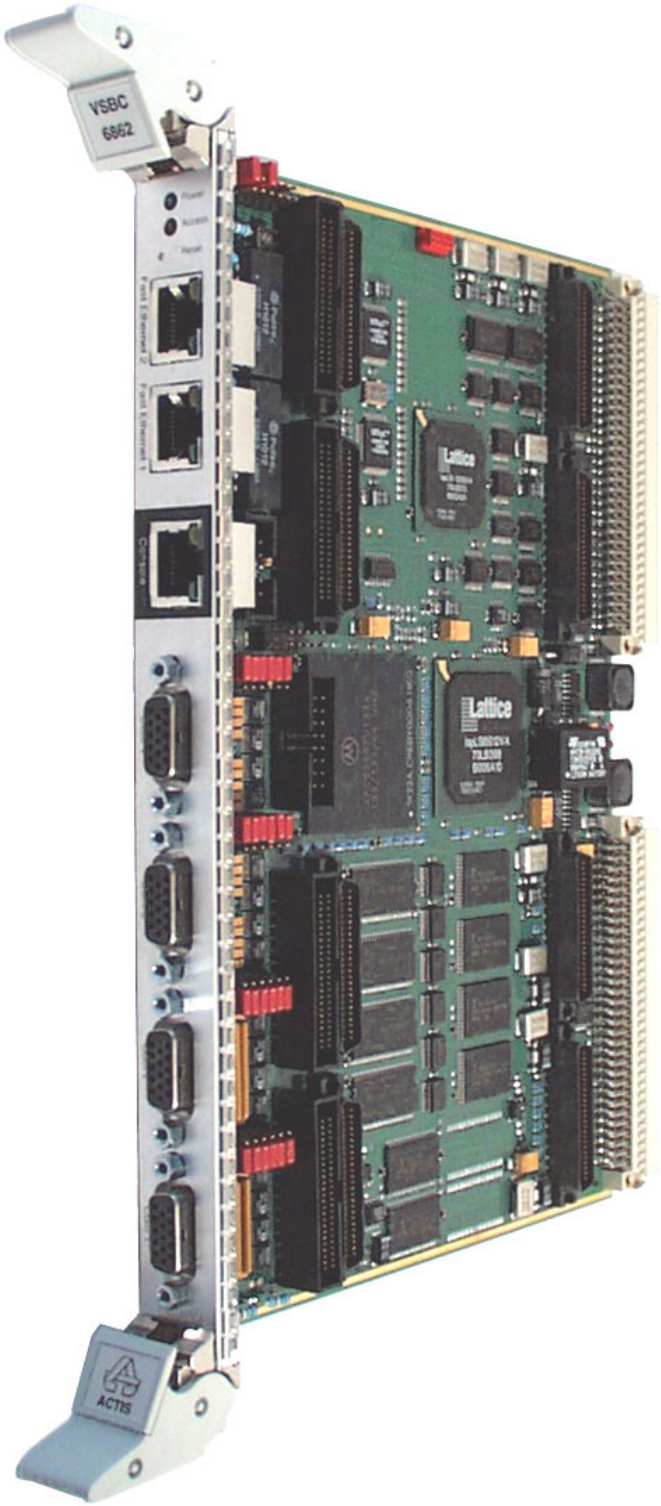


Figure 1: Photograph

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1.4. Block diagram

The VSBC-6862 architecture is divided in four main sections:

The CPU
This is the heart of the board, it is the MPC-8260 'PowerQUICC II' with a bus speed of 66MHz, CPM speed of 133MHz and Core speed of 133 or 200MHz.

The memory section
This section includes the 128 MByte SDRAM on a 64-bit bus, the two 8 MByte Flash memory banks on a 32-bit bus, the 1 MByte SRAM memory, and the battery backed-up RTC with SRAM.

The internal logic section including the IP carrier and the VME interface
This section handles all internal board logic like board registers, plus the handling of IP modules and VME functions.

The I/O section
This section is the external part of the PowerQUICC II I/O ports; it contains the two RS-232 ports, the four serial ports, and the two Fast Ethernet ports.

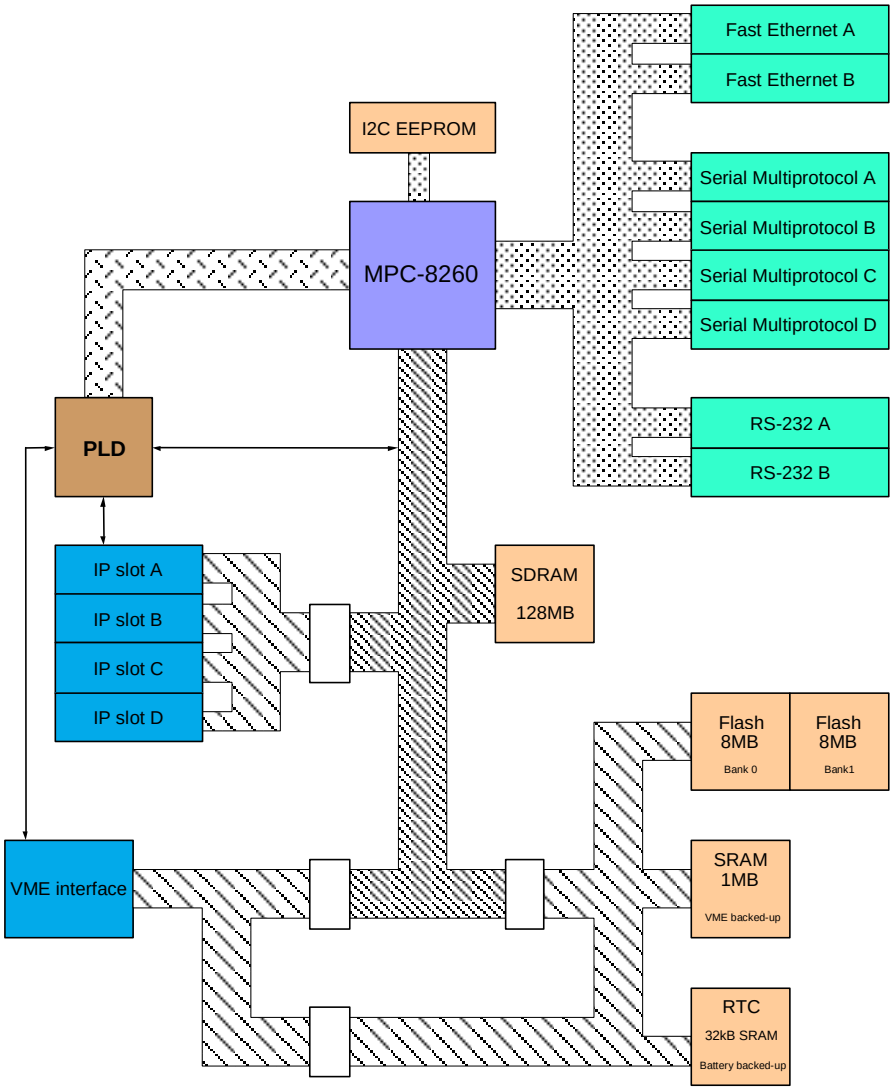


Figure 2: Block diagram

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1.5. Component location

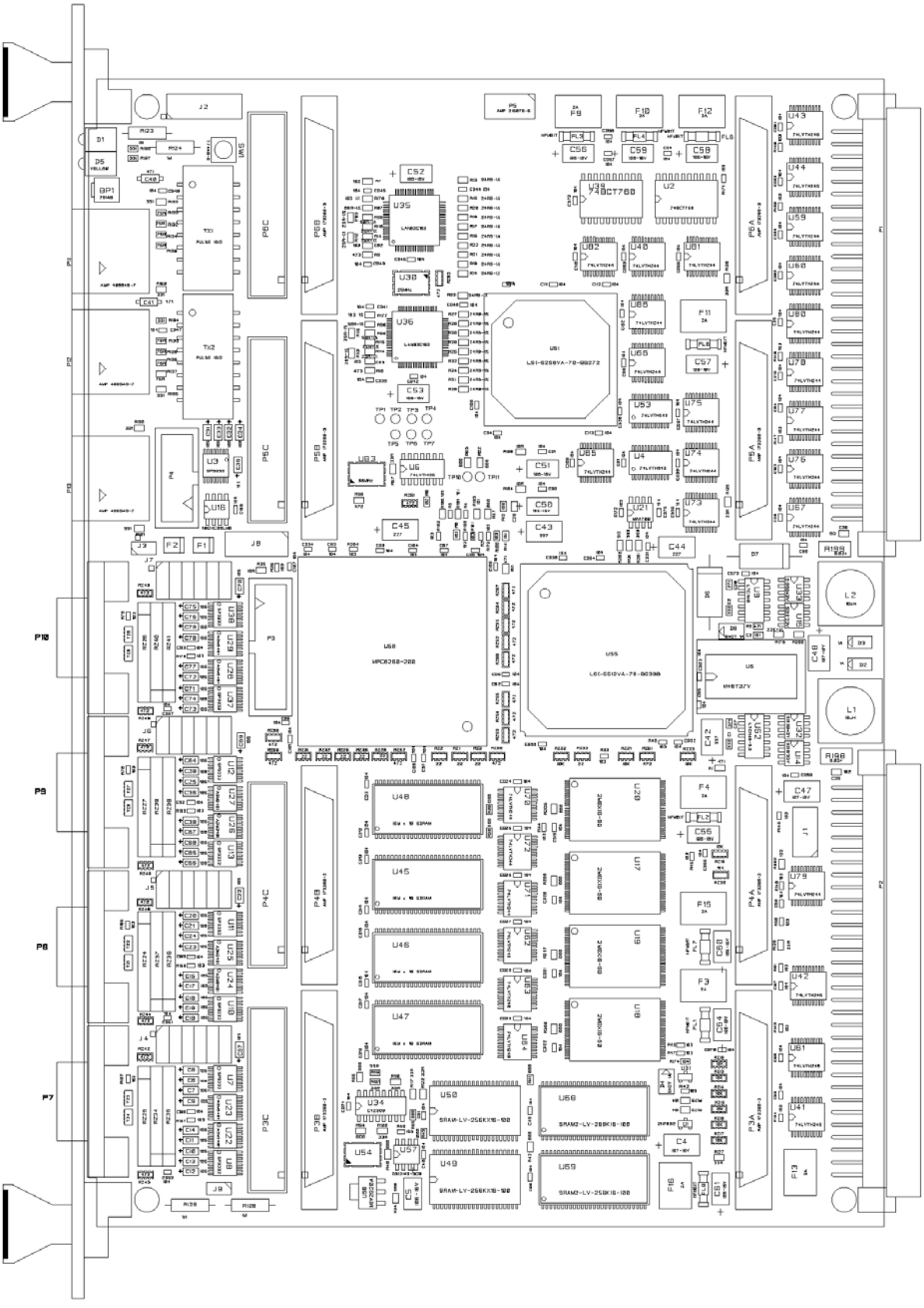


Figure 3: Component location

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Please note that on the VSBC-6862, some locations are not populated.
This was done either to avoid problems of component availability, either for debug purposes.
From the user side, its totally transparent, nothing has to be modified.
For special uses that need a precise component implementation, please contact ACTIS.

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2
Peripherals description

The VSBC-6862 offers a wide choice of on-board peripheral or bus interface, which makes this board very versatile. Most of these peripherals comes either directly from the processor interface, like the serial ports, or from other interface unit, like the real time clock calendar.

The following sections will describe these peripheral features.

2.1. FLASH memory

Two banks of 4 or 8 MBytes Flash memory devices are available, for a total of 8 or 16 MBytes Flash.

Each Flash bank is formed by a group of two 16-bit devices, which provide a resulting 32-bit bus interface for efficient instruction program storage.

Each bank is controlled by the Chip Select 0 (CS0) or Chip Select 2 (CS2) signal.

The Flash memory bank connected to the Chip Select 0 is the boot device. This bank must contain both ResetWord used by the PowerQUICC II configuration and the boot code.

The VSBC-6862 provides a 'Bootbank' jumper to provide the ability to invert the CS0 and CS2 signals, thus inverting the bootable Flash memory bank.

One Flash memory bank is also shared with the VME bus. This permits an external master to reprogram the VSBC-6862 Firmware or use this memory as non-volatile device.

This device is command set compatible with JEDEC standard E^2PROMs.
Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry.

2.2. SDRAM memory

This memory is handled by the powerful SDRAM timing machine contained in the MPC-8260.
The Chip Select 1 is used to control this memory.

The SDRAM machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve the highest performance. This controller supports directly all the SDRAM possibilities, like pipelining and interleaving.

The VSBC-6862 is supplied with 128 MBytes SDRAM on-board, organized with four 16 Mbitsx16 devices.
The 64 bits wide data bus is directly connected on the 60x bus of the MPC-8260 to achieve the best performance.

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2.3. SRAM memory

1 MBytes of SRAM memory are provided on-board, this memory is controlled with the Chip Select 9.
This memory is shared between the PowerQUICC II and the VME bus.
It is organized in memory width of 32 bits.

A special function is provided for memory saving with the usage of the Stand-By power signal from the VME bus. When the Board Power is shutdown, the SRAM memory will switch its power lines to the VME Stand-By power signal.

2.4. Real Time Clock with SRAM memory

The VSBC-6862 includes a real time clock device, with as an additional feature, a battery backed 32 kbyte SRAM. This device is controlled by the Chip Select 3.

Its 32 kbyte SRAM provides flexible user data storage with retention capability by its SNAPHAT battery pack. This device is connected on an 8 bits wide data path.

This device provides also functions like Alarm, Battery Test, and Watchdog function.

The RTC data are accessible like SRAM Bytes.

This device is also accessible from the VME bus.

Note: The SNAPHAT housing plugged on the M48T37V contains both battery and crystal. Thus, for the minimum frequency error, the user has to calibrate the RTC in case of battery replacement.

2.5. IP modules

The VSBC-6862 provides four IP module slots, which are compliant with the ANSI/VITA 4-1995.
It provides support for 8 MHz type as well as DMA modules.

The IP interface offers an architecture for I/O extension through inexpensive mezzanine modules for various categories like:

- Digital and analog functions
- Serial communication controllers
- Network and fieldbus interfaces

This interface gives the possibility to easily customize the VSBC-6862.

This IP bus interface is implemented on the VSBC-6862 through a specific CPLD, which provides the interface between the PowerQUICC II processor and the four IP module slots.

For overall information, please consult the Appendix: List of main ACTIS IP modules.



A choice of IP modules and transition modules from ACTIS Computer is available on our web site: www.actis-computer.com

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The IP interface uses two processor chip selects to address all IP module spaces.
The Chip Select 4 is used to control the IP I/O, ID, and INT spaces.
The Chip Select 5 is used to control the IP memory spaces.

Each IP slot has is own set of registers to have the four IP slots fully independent.

The VSBC-6862 supports the two IRQ available on the IP modules.
Each IP slot has an own IRQ level attributed to the MPC-8260. If the both IRQ are active at the same time on an IP module, the VSBC-6862 handles the IP IRQ 0 first, and then IP IRQ 1.

The IP DMA channels are controlled by the IDMA channels, with IP Slot A controlled by IDMA1, Slot B controlled by IDMA2, Slot C controlled by IDMA3 and Slot D controlled by IDMA4

2.6. Board registers

The VSBC-6862 contains several registers for board features.
These registers are mapped in the same Chip Select 4 than the IP ID and I/O spaces.

These features can be divided in three functions:

- General board functions
  Two registers are used to generate Reset on the board and to read the rotary switch value.
- IP functions
  Each of the four IP slot owns his set of registers to define and use IP modules.
- VME functions
  Each VME window owns his set of registers to define and use the VME bus.

2.7. VME interface

There is a VME master, slave, interrupter, interrupt-handler and system controller modules.
Each module can be considered as an independent module.

Some functions are controlled by jumpers for the VME module, as for Slot1function or Reset utilization.

The VME master A32/A24/A16/D32/D16/D8

Two windows are available to access the VME bus.
They are controlled by the chip selects CS6 and CS7.

The release modes are selectable between ROR and RWD modes.

The VME slave A24/A16/D32/D16/D8

Two windows are available from VME bus:
An A16 window to access VME registers, including mailbox
An A24 window to access the VSBC-6862 memory spaces.

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The VME interrupter I(1-7)

The interrupter is able to generate any VME IRQ level and send a user-defined vector.

The VME interrupt-handler IH(1-7)

This interrupt-handler is able to recognize all IRQ VME levels.
All levels can be masked with the VHM register.

When an IRQ is coming from the VME side, an IRQ1 is sent to the MPC-8260.
The user can then read the IRQ levels active in the VHIL register.
Depending of the IRQ level to be acknowledged, the user can read the vector in the corresponding offset in the VHV register.
When reading the vector, the interrupt acknowledge cycle is initiated.

The VME system controller.

This function can be enabled or disabled with the Slot1 jumper.

When the system controller is enabled, the VSBC-6862 provides the following functions:
- VME arbiter: SGL, PRI, or RRS depending of the VAM register.
- VME bus monitor: BTO(30)
- IACK daisy-chain driver.
- 16 MHz system clock generator.

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2.8. I^2C EEPROM

8 kbits of non-volatile memory is provided on the I2C bus.

This memory is used for board internal configuration (for example to store physical Fast Ethernet addresses) and can also be used for user purposes.

2.9. Fast Ethernet ports

The two Fast Ethernet interfaces come directly from the MPC-8260 processor.
The physical layer is achieved with on-board fast Ethernet transceivers from SMSC: the LAN83C183.

The SMSC-LAN83C183 provides all of the IEEE 802.3u 100Base-TX and ISO802.3 10Base-T Physical Layer (PHY) functions needed for workstations, bridge, router, and switch applications. It can operate as a 100Mbps only device, or as a dual speed 10/100Mbps device with built-in auto-negotiation possibility for speed selection. The SMSC-LAN83C183 supports the standard Media Independent Interface (MII) for glueless interface with 10/100 Ethernet Media Access Controllers (MAC).
The built-in IEEE 802.3u Auto-Negotiation feature automatically selects internal 10Base-T or 100Base-TX, full or half-duplex, as a result of negotiation between the station and its link partner.
The SMSC-LAN83C183 supports half and full-duplex operation at both 10Mbps and 100Mbps speeds. It complies with ANSI X3T9 TP-PMD and includes MLT-3 Encoder/Decoder and Stream Cipher scrambler/ de-scrambler functions for 100Base-TX.The SMSC-LAN83C183 supports Category 5 Unshielded Twisted Pair and Type 1 Shielded Twisted Pair wiring. The on-chip Serial Management Interface features the Basic and Extended registers set. The 4B/5B Encoder and Decoder are also included.

An on-board transformer provides a direct connection for a 10Base-T and 100Base-TX interface

2.10.SMC1 and SMC2 serial ports

The VSBC-6862 offers two RS-232 serial ports.
One of these general-purpose serial ports is available on the front panel RJ-45 connector, the other one is available on an internal connector.

These serial ports can be typically used as system console ports.

Note that this type of port has no hardware flow control capability.

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2.11.SCC multi-protocols serial ports

The VSBC-6862 offers four independent serial ports.
In synchronous mode, all four ports have independents RX clock signals, but only SCC1 and SCC2 have TX Clocks signals.

These ports are directly controlled by the Serial Communication Controllers (SCC) included in the PowerQUICC II. These SCC includes functions like support of many protocols like UART and HDLC, it contains also FIFO buffers: 32 byte deep, and many more powerful options.

All the four ports are available on four Sub-D-HD-15 connectors on front panel.

The interface level of these ports can be RS-232/RS-422/RS-485 or V.35.
Switching between these options can be done through the 'serial mode' jumpers.

The serial ports 1 and 2 have an added function: they can be internally used to synchronize the internal Baud Rate Generators (BRG) with external clock signals.

Note that due to pin multiplexing in the PowerQUICC II, the Transmit Clock for the serial port 4 can't be used in same time with the IP slot B DMA channel. The user must use either DMA on IP B, either Transmit Clock on serial port 4.

RS-232 mode

These VSBC-6862 ports are in a standard RS-232 mode.
The following signals are controlled by the PowerQUICC II:
TxD, RxD, TxC, RxC, CTS, RTS, and DCD

All ports support hardware handshaking and synchronous functions.
DSR signals are pulled-up to VCC to indicate that the board is powered-up.

RS-422/RS-485/V.35 modes

These VSBC-6862 ports are compatible with these three modes.
The following signals are controlled by the PowerQUICC II:

TxD, RxD, TxC, RxC	in differential mode for RS-422, RS-485 and V.35
CTS, RTS and DCD	in RS-232 mode for V.35

Note: As described above, the VSBC-6862 did not provides all defined signals for V.35, it provides all 'transmission signals' but not for example, the loopback or ring indicator signals.

All ports support full and half-duplex mode, and supports also synchronous operations.

The internal I/O ports dedicated to RTS is connected to the internal data transmit enable signal.
This permits to determine the function for half or full-duplex modes as:

Full-duplex:	configure RTS always active
Half-duplex:	configure RTS as normal RTS

The PowerQUICC II has also the possibility to disable his receiver while emitting (see bit DRT in register PSMR).

Each port has its own network resistors.
These resistors are on sockets. ACTIS choose to implement manual network resistors to keep the RS-485 network always working, independently of the power state of the VSBC-6862.
These resistors network are to be installed only when the corresponding serial port is at one of both ends of the RS-485 network cable.

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2.12. I^2C interface

The VSBC-6862 provides an I^2C interface bus for on-board serial EEPROM accesses and user purposes.
The board provides external accesses to this bus through an internal connector.

2.13. LED displays

The VSBC-6862 allows monitoring for a wide range of board activities, these status are available for user check on the front panel.

The Power and Access LEDs functions are hardware fixed.

The Fast Ethernet LEDs can be reconfigured by setting the corresponding parameters in the transceivers. The configuration of these LEDs is described in the Fast Ethernet transceiver description.

The two Auxiliary LEDs are user defined with PowerQUICC II I/O ports. They are intended to provide the user a flexible meaning to signal states on the front panel. These indicators have to be handled by the user.
These two LEDs are active low.

The following table provides the relation between the front panel LED's and their corresponding condition sources.

LED reference	Source	Ref	Color
Power OK	5V power ok and 5V IP ok	D1	Green
Access	Internal logic (SDRAM, Reset, Slave)	D5	Yellow
Auxiliary 0	MPC-8260 I/O port C24	P13	Yellow
Auxiliary 1	MPC-8260 I/O port C30	P13	Green
Fast Ethernet 1 Link	SMSC-83C183 1, signal LED3	P12	Green
Fast Ethernet 1 Activity	SMSC-83C183 1, signal LED2	P12	Yellow
Fast Ethernet 2 Link	SMSC-83C183 2, signal LED3	P11	Green
Fast Ethernet 2 Activity	SMSC-83C183 2, signal LED2	P11	Yellow

The 'Power' Led blinking can typically indicate a problem on an IP module. This LED indicates the power state after the protecting fuses.

The 'Access' Led indicates:

- the Reset state
- an local access to SDRAM
- an slave access to the board

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3
Connectors & jumpers

This chapter will describe all connectors and jumpers on the VSBC-6862.

One of specificity of this board is that the four IP slots occupy most of the board's surface. And it is not possible to locate connector or jumpers on this area.
In spite of this fact, ACTIS placed the connectors and jumpers in a very straightforward location.

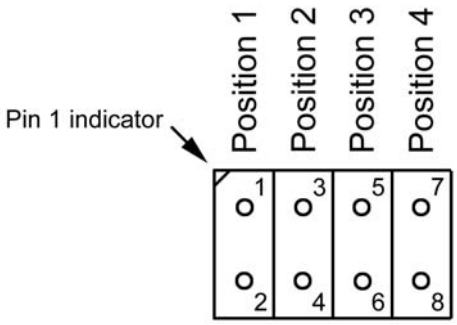
The connectors are numbered upwards: the first connectors for IP, serial ports and Fast Ethernet ports are in the bottom of the board.
Behind each serial port, are the corresponding termination resistors and jumpers.

Pin numbering convention

The pin numbering is indicated on the 'jumpers and connectors location', on the next page.

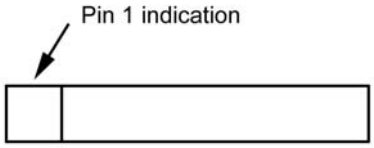
- The jumpers have pin 1 indicated by a triangle on the corresponding corner.

For example:



- The connectors and network resistors have pin 1 indicated with a square on the corresponding side.

Example for network resistor:



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Locations

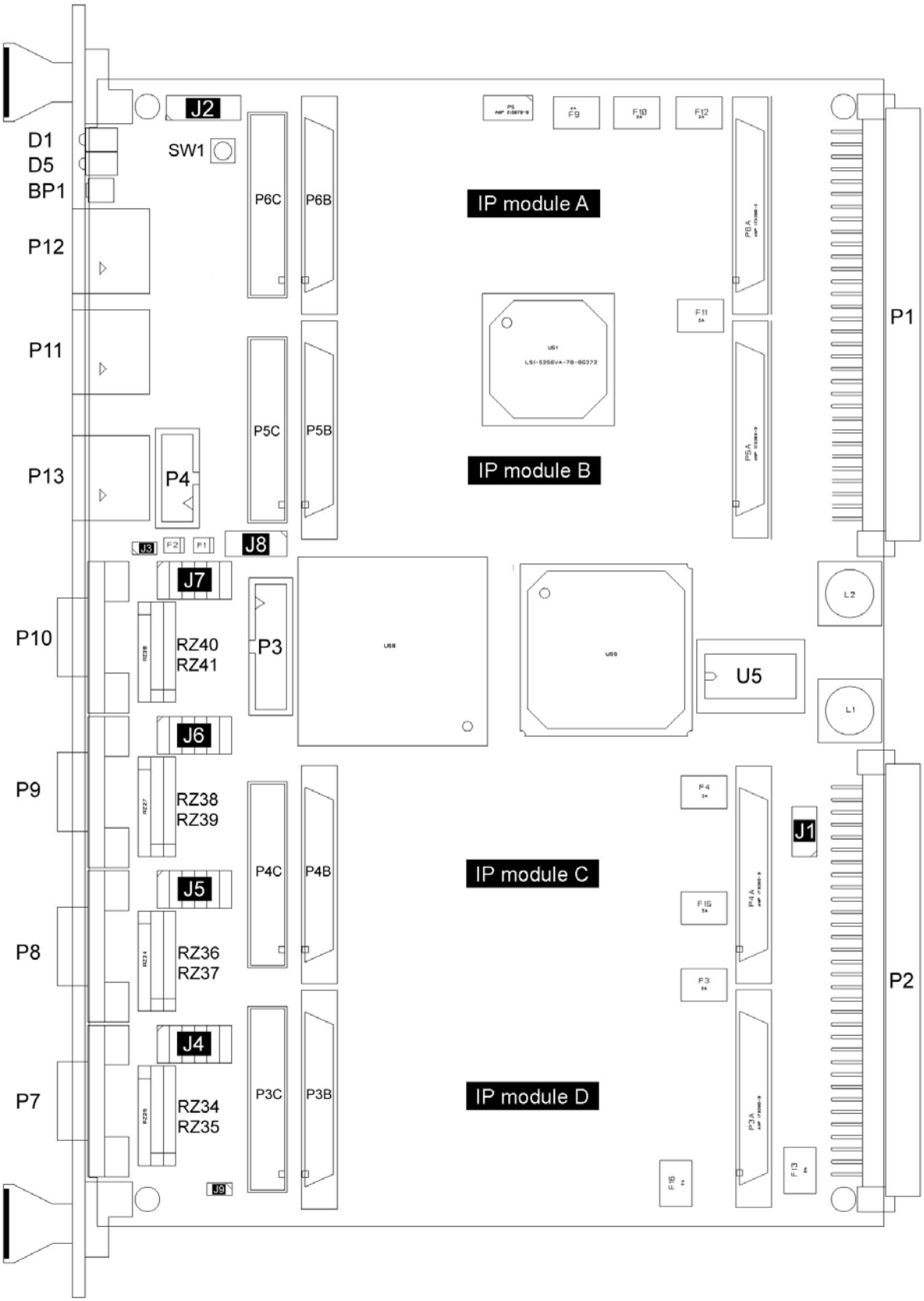


Figure 4: Connectors and jumpers location

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3.1. Push Button: BP1

In the front panel, the push button generates a Power-On Reset to the board.
This button is debounced.

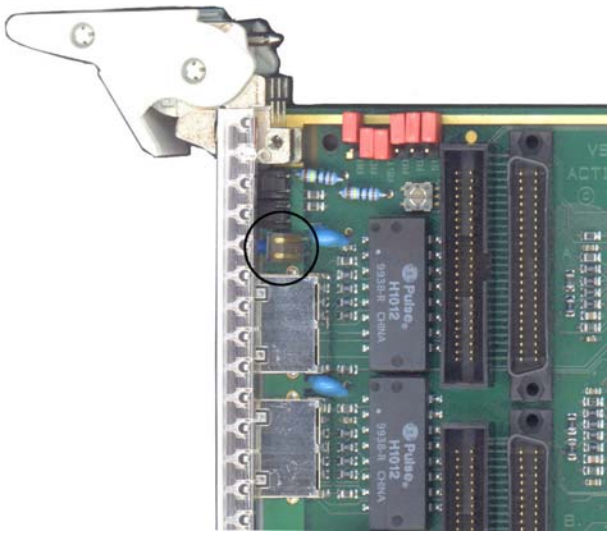


Figure 5: Push button location

☞	Before SN:10135, the Push Button was generating a Hardware Reset instead of Power-On Reset.

3.2. Rotary switch: SW1

The eight position rotary switch is a facility provided for user purposes.
This switch can be used, for example, to select the board working modes.
It can be read with the SWPR register.

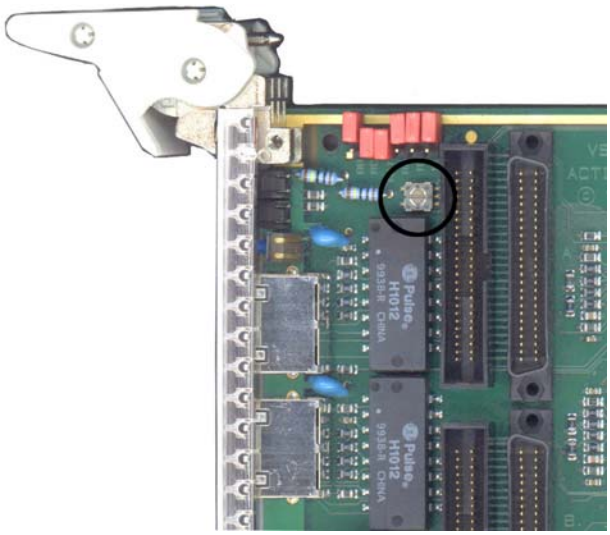


Figure 6: Rotary switch location

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3.3. IP module strobes, header J1

For IP module operations, an optional "STROBE" signal is provided for each IP module sockets. This signal is provided for general purpose use, the J1 header allows the selection for both signals with the following assignment.
The VSBC-6862 has internals pull-ups connected to these Strobe signals.
Jumpers permit to access or connect pull-downs to these signals.

These jumpers are located near P2

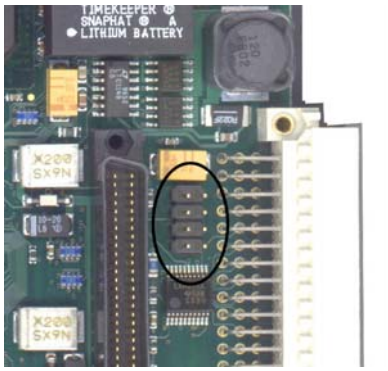


Figure 7: Jumper J1 location

The pins are assigned as follows:

Pin	Signal	Description
1	Strobe A	Strobe for IP slot A
2	GND	Ground
3	Strobe B	Strobe for IP slot B
4	GND	Ground
5	Strobe C	Strobe for IP slot C
6	GND	Ground
7	Strobe D	Strobe for IP slot D
8	GND	Ground

For more details about the strobe signals use, please refer to the ANSI/VITA-4 1995 specification.

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3.4. Jumper: J2

A jumper with six positions provides some basic functions.

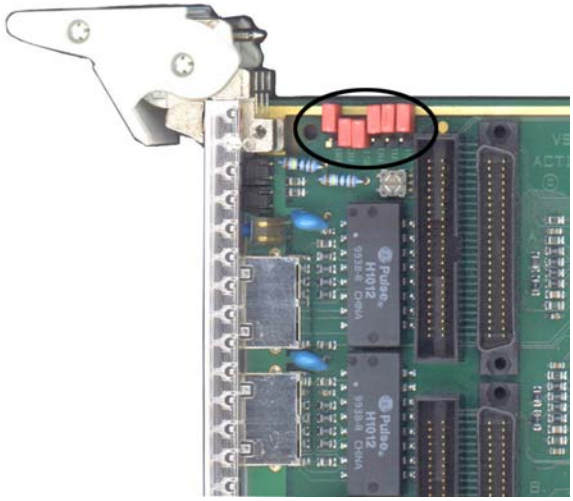


Figure 8: Jumper J2 location

Position 1

BootBank1	Description
Unplugged	The board boots on the Flash memory bank 0
Plugged-in	The board boots on the Flash memory bank 1

Description: This jumper is used to define which Flash memory bank is the boot bank.
The VSBC-6862 as two Flash memory banks.
The usage of this jumper allows the user to reverse the bootable bank.
This function will be very helpful to test new software versions during software debugging.
This provides the facility to come back with the previous software version loaded in the other bank.

Position 2

ResetConf	Factory setting	Description
Unplugged	X	The RSTCONF pin is at GND: normal operation
Plugged-in		The RSTCONF pin is at VCC

Description: This jumper is used to force the PowerQUICC II to use the default ResetWord.
The main usage of this jumper is to boot the board for the first time, before the Flash memory is loaded with the ResetWord.
The board must not function more than few minutes using the default ResetWord.
This is due to the internal clocks sets a little bit higher than normal with default values.
For more information, please consult the MPC-8260 User's manual.
For normal operation, this jumper must never be plugged-in.

Position 3

Power On Reset	Factory setting	Description
Unplugged	X	No external Power-On reset: normal operation
Plugged-in		External Power-On Reset

Description: This jumper provides the ability to generate an external power-on Reset on the board.
This input is internally debounced, it doesn't need external debouncing logic.

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Position 4

VME Reset Out	Factory seting	Description
Unplugged	X	Board is not authorized to generate a VME Reset
Plugged-in		Board in Slot1 mode is authorized to generate a VME Reset

Description: When this jumper is plugged, if the board is in Slot1 mode, it will generate a VME Reset when the board is under Hardware Reset.

Position 5

VME Reset In	Factory setting	Description
Unplugged	X	VME Reset is not connected to board Reset
Plugged-in		VME Reset generates a board Reset when not in Slot1 mode

Description: When this jumper is plugged, if the board is not in Slot1 mode, a VME Reset will generate a board Hardware Reset.

Position 6

VME Slot1 function	Factory setting	Description
Unplugged	X	The VME Slot1 functions are disabled
Plugged-in		The VME Slot1 functions are enabled

Description: This jumper defines if the Slot1 function for VME bus is enabled or disabled. When the Slot1 function is enabled, the board activates the functions to be the VME System Controller: Arbiter, Clock generation, Daisy-Chain Handling, Bus timer

Warning

Activate the Slot1 function only if the VSBC-6862 is physically installed in the first VME Slot.

3.5. Jumper: J3

This jumper is only used for debug purpose.

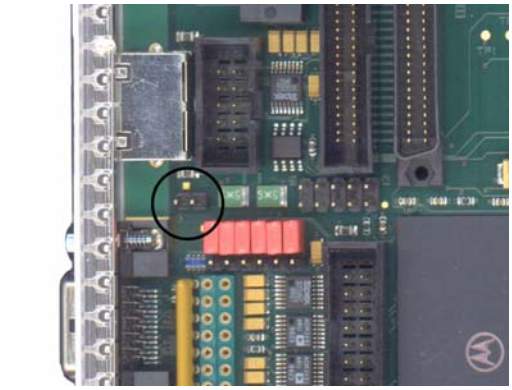


Figure 9: Jumper J3 location

Warning

It must not be connected without explicit instruction from ACTIS Computer.

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3.6. Jumpers: J4, J5, J6, J7

This are the 'serial mode' jumpers, they have six position.
They permits to select the mode used for the corresponding serial port.
All the six positions of these jumpers must be either all in RS-232 position, either all in RS-485 position.
They are located near its corresponding serial ports:

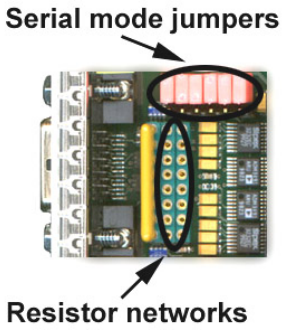


Figure 10: Communication ports jumpers in RS-232 mode

J4 correspond to serial port SCC1, J5 correspond to serial port SCC2
J6 correspond to serial port SCC3, J7 correspond to serial port SCC4

For RS-232 protocols, set all six jumpers in RS-232 position: 1-2, 4-5, 7-8, 10-11, 13-14, 16-17
For RS-422, RS485 or V.35, set all six jumpers in RS-485 position: 2-3, 5-6, 8-9, 11-12, 14-15, 17-18

Example for ports 1 & 2 in RS-485 mode and ports 3 & 4 in RS-232 mode:

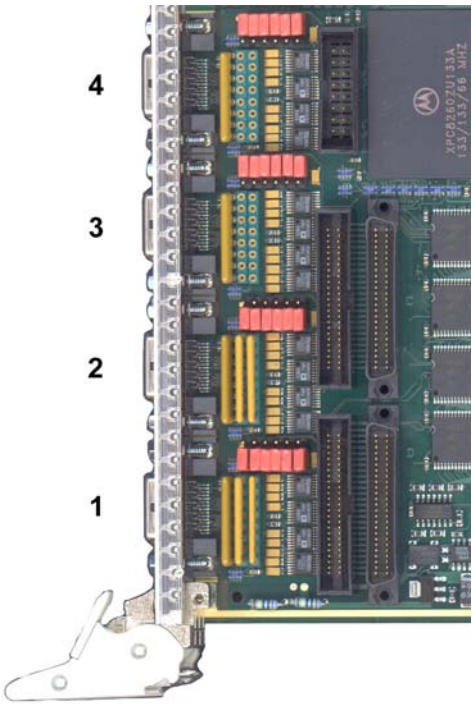


Figure 11: Communication ports jumpers example

Warning	ALL six jumpers must always be in the same position, other configuration can damage the board.

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3.7. Jumper: J8

This jumper sets the base address for the A16 slave window. This window contains all registers accessible from an external VME master.

A jumper plugged represents an address line in the state '0', with:

position 1:	VME address A11
position 2:	VME address A12
position 3:	VME address A13
position 4:	VME address A14
position 5:	VME address A15

Example:

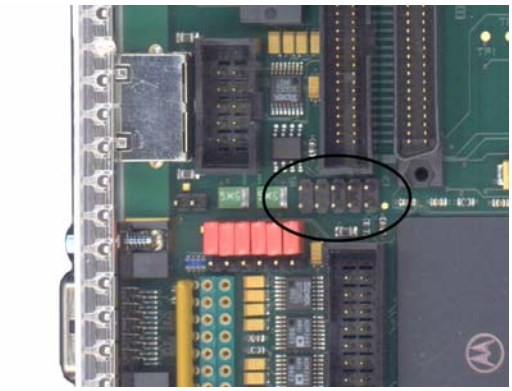


Figure 12: Jumper J8 location

This configuration indicates a A16 window base address of $F800.

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3.8. Two RS-232 terminal ports, and I^2C bus: P13, P4

These serial ports are provided for general purpose application, its interface levels comply with the RS-232 specification. In most environments, these interfaces will be used as a console port for board configuration and monitoring functions.

These ports are handled by the SMC1 and SMC2 functions of the PowerQUICC II processor.
P13 is available on the front panel with an RJ-45 connector defined as following:

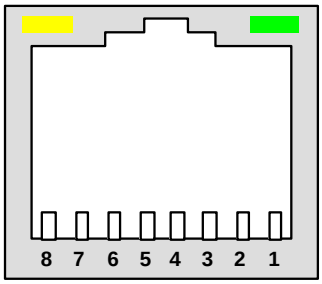


Figure 13: Connector P13 pinout

Pin	Signal	Description
1	n.u.	Not used
2	n.u.	Not used
3	GND	Ground
4	TxD1	Transmit data SMC1
5	RxD1	Receive data SMC1
6	GND	Ground
7	n.u.	Not used
8	n.u.	Not used

❖ ***This connector accepts standard RJ45 8-pin plug connector.***

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The second serial port is available in an internal connector shared with the I^2C bus.

P4 contains the signals for the SMC2, power lines for user purposes (max 500mA, fused), and the I^2C bus extension.

This connector is available on-board through a HE-10 connector defined as following:

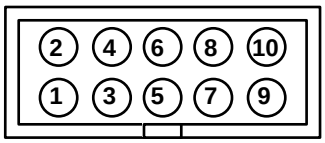


Figure 14: Connector P4 pinout

Pin	Signal	Description
1	n.u.	Not used
2	3.3V	3.3 V, 500mA fuse
3	5V	5.0 V, 500mA fuse
4	n.u.	Not used
5	GND	GND
6	GND	GND
7	I2CSCL	I^2C bus SCL
8	I2CSDA	I^2C bus SDA
9	TXD2	Transmit data SMC2
10	RXD2	Receive data SMC2

❖ ***This connector accepts standard DIN41651 10-pin female plug connector.***

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3.9. Four multi-protocols serial ports P7,P8,P9, P10

These four serial ports are provided for user applications

These four ports are available in the front panel on four HD-15 connectors with:
Port SCC1: connector P7
Port SCC2: connector P8
Port SCC3: connector P9
Port SCC4: connector P10

All signals on these connectors are in full-duplex mode.
For Half-duplex mode, please connect externally RX and TX.

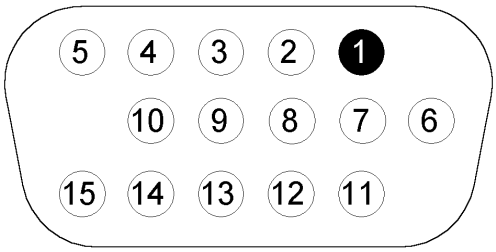


Figure 15: Communication ports pinout

Pin	Signal	Direction	Description for RS-232 option	Description for RS-422/485/V.35 option
1	GND	---	Shield	Shield
2	TxD+	Out	Transmit Data	Transmit Data+
3	TxD-	Out	n.u.	Transmit Data-
4	TxC+	Out	Transmit Clock	Transmit Clock +
5	TxC-	Out	n.u.	Transmit Clock -
6	RTS	Out	Request To Send	Request To Send
7	GND	---	Ground	Ground
8	CTS	In	Clear To Send	Clear To Send
9	DTR	Out	Data Terminal Ready	Data Terminal Ready
10	DCD	In	Data Carrier Detect	Data Carrier Detect
11	RxC-	In	n.u.	Receive Clock -
12	RxC+	In	Receive Clock	Receive Clock +
13	RxD-	In	n.u.	Receive Data-
14	RxD+	In	Receive Data	Receive Data+
15	DSR	Out	Data Set Ready: pulled-up	Data Set Ready: pulled-up

❖ ***This connector accepts standard HD-15 SubD type plug.***

Note: In RS-232 mode, all 'n.u.' pins are physically connected to the corresponding RS-485 function, thus, the RS-232 device must not use or connect these pins.

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Termination network resistors

When the RS-422/RS-485/V.35 is chosen, the VSBC-6862 is provided with removable network resistors.

Each resistor network is located as:

RZ34, RZ35:	port SCC 1
RZ36, RZ37:	port SCC 2
RZ38, RZ39:	port SCC 3
RZ40, RZ41:	port SCC 4

Note that the pins 1 of these removable networks are in opposed side than the already soldered resistor network.

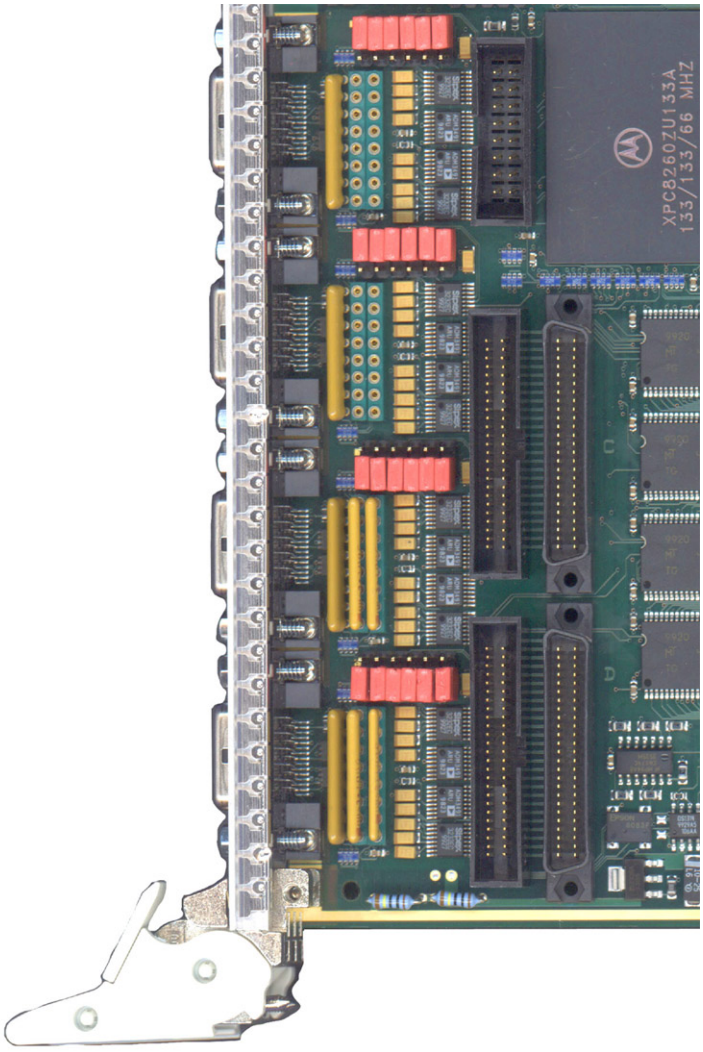


Figure 16: Termination resistor networks example

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3.10. Two Fast Ethernet ports, connectors P11, P12

For LAN based applications, two fast Ethernet connections are available for twisted-pair interface which is compliant for both 100Base-TX and 10Base-T specification described below.
The PHY part of the BSBC-6862 is based on the SMSC83C183 transceiver.
Front panel, connector Fast Ethernet 1 = connector P12, corresponds to FCC2.
Front panel, connector Fast Ethernet 2 = connector P11, corresponds to FCC1.

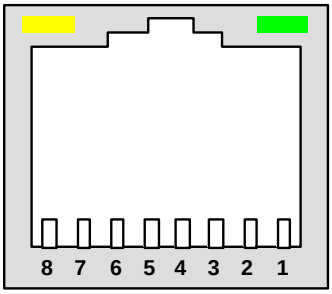


Figure 17: Fast Ethernet ports pinout

Pin	Signal	Description
1	TxD+	Transmit data positive output
2	TxD-	Transmit data negative output
3	RxD+	Receive data positive input
4	n.u.	Not used
5	n.u.	Not used
6	RxD-	Receive data negative input
7	n.u.	Not used
8	n.u.	Not used

❖ ***This connector accepts standard RJ45 8-pin plug connector.***

The green LED is connected to the SMSC-LAN83183 LED_3 pin, which can indicate 100Mb/s link.
The yellow LED is connected to the SMSC-LAN83183 LED_2 pin, which can indicate activity.

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3.11. IEEE-1149.1 interface, connector P3

The MPC-8260 provides a dedicated user-accessible test access port (TAP) that is fully compatible with the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. Problems associated with testing high-density circuit boards have led to development of this standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The MPC-8260 implementation supports circuit-board test strategies based on this standard.
This connector definition complies with the industry standard definition for its assignment.

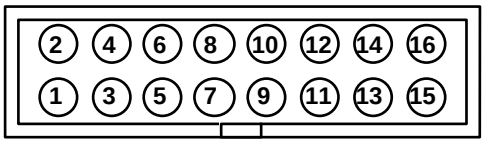


Figure 18: JTAG port pinout

Pin	Signal	Description
1	TDO	Serial output data
2	3.3V	3.3V, max 0.3 mA
3	TDI	Serial input data
4	/TRST	Scan chain logic reset
5	/QREQ	Quiescent request
6	+3.3V	+3.3 V power supply, max 100 mA
7	TCK	Serial clock
8	n.u.	Not used
9	TMS	Mode select
10	n.u.	Not used
11	/SRESET	Software reset
12	GND	Ground
13	/HRESET	Hardware reset
14	n.u.	Not used, used as connector 'key'
15	/CKSTP_OUT	Checkstop output
16	GND	Ground

❖ ***This connector accepts standard DIN41651 16-pin female plug connector.***

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3.12. VME bus, P1 connector

Row A		Row B		Row C	
Pin	Signal	Pin	Signal	Pin	Signal
A1	D0	B1	/BBSY	C1	D8
A2	D1	B2	/BCLR	C2	D9
A3	D2	B3	/ACFAIL	C3	D10
A4	D3	B4	/BG0IN	C4	D11
A5	D4	B5	/BG0OUT	C5	D12
A6	D5	B6	/BG1IN	C6	D13
A7	D6	B7	/BG1OUT	C7	D14
A8	D7	B8	/BG2IN	C8	D15
A9	GND	B9	/BG2OUT	C9	GND
A10	SYSCLK	B10	/BG3IN	C10	/SYSFAIL
A11	GND	B11	/BG3OUT	C11	/BERR
A12	/DS1	B12	/BR0	C12	/SYSRESET
A13	/DS0	B13	/BR1	C13	/LWORD
A14	/WRITE	B14	/BR2	C14	AM5
A15	GND	B15	/BR3	C15	A23
A16	/DTACK	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	/AS	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	/IACK	B20	GND	C20	A18
A21	/IACKIN	B21	-	C21	A17
A22	/IACKOUT	B22	-	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	/IRQ7	C24	A14
A25	A6	B25	/IRQ6	C25	A13
A26	A5	B26	/IRQ5	C26	A12
A27	A4	B27	/IRQ4	C27	A11
A28	A3	B28	/IRQ3	C28	A10
A29	A2	B29	/IRQ2	C29	A9
A30	A1	B30	/IRQ1	C30	A8
A31	-12 V	B31	+5V STDBY	C31	+12 V
A32	+5 V	B32	+5 V	C32	+5 V

❖ ***This connector is compliant with the DIN-41612 specification.***

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3.13. VME bus, P2 connector

This connector has its VME user's pins attributed to the IP I/O slot D

Row A		Row B		Row C	
Pin	Signal	Pin	Signal	Pin	Signal
A1	IP D, I/O 2	B1	+5 V	C1	IP D, I/O 1
A2	IP D, I/O 4	B2	GND	C2	IP D, I/O 3
A3	IP D, I/O 6	B3	-	C3	IP D, I/O 5
A4	IP D, I/O 8	B4	A24	C4	IP D, I/O 7
A5	IP D, I/O 10	B5	A25	C5	IP D, I/O 9
A6	IP D, I/O 12	B6	A26	C6	IP D, I/O 11
A7	IP D, I/O 14	B7	A27	C7	IP D, I/O 13
A8	IP D, I/O 16	B8	A28	C8	IP D, I/O 15
A9	IP D, I/O 18	B9	A29	C9	IP D, I/O 17
A10	IP D, I/O 20	B10	A30	C10	IP D, I/O 19
A11	IP D, I/O 22	B11	A31	C11	IP D, I/O 21
A12	IP D, I/O 24	B12	GND	C12	IP D, I/O 23
A13	IP D, I/O 26	B13	+5 V	C13	IP D, I/O 25
A14	IP D, I/O 28	B14	D16	C14	IP D, I/O 27
A15	IP D, I/O 30	B15	D17	C15	IP D, I/O 29
A16	IP D, I/O 32	B16	D18	C16	IP D, I/O 31
A17	IP D, I/O 34	B17	D19	C17	IP D, I/O 33
A18	IP D, I/O 36	B18	D20	C18	IP D, I/O 35
A19	IP D, I/O 38	B19	D21	C19	IP D, I/O 37
A20	IP D, I/O 40	B20	D22	C20	IP D, I/O 39
A21	IP D, I/O 42	B21	D23	C21	IP D, I/O 41
A22	IP D, I/O 44	B22	GND	C22	IP D, I/O 43
A23	IP D, I/O 46	B23	D24	C23	IP D, I/O 45
A24	IP D, I/O 48	B24	D25	C24	IP D, I/O 47
A25	IP D, I/O 50	B25	D26	C25	IP D, I/O 49
A26	-	B26	D27	C26	-
A27	-	B27	D28	C27	-
A28	-	B28	D29	C28	-
A29	-	B29	D30	C29	-
A30	-	B30	D31	C30	-
A31	-	B31	GND	C31	-
A32	TM 5 V	B32	+5 V	C32	TM 5 V

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Signal	Description
+5 V	Main power supply
+12 V	Power used for IP module slots and Flash protection feature
-12 V	Power used for IP module slots
GND	Ground
+5 V STDBY	Power supply furnished by an non-interruptible power source
TM 5 V	5 V provided by the VSBC-6862 to an optional transition module. Fuse protected

- ***This connector is compliant with the DIN-41612 specification.***

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3.14. Four IP module logic interface, connectors P3A, P4A, P5A, P6A

For input/output extensions, the VSBC-6862 board provides a four slot IP module interface. This bus interface complies with the ANSI/VITA-4 1995 specification and handles 16-bit wide modules and supports 8 MHz mode.

These slots are assigned as:

connector P6A: IP slot A
connector P5A: IP slot B
connector P4A: IP slot C
connector P3A: IP slot D

The following table gives the connectors assignment which refers to the VITA-4 specification.

Pin	Signal	Pin	Signal
1	GND	26	GND
2	CLK	27	5 V
3	/RESET	28	R/W
4	D0	29	/IDSEL
5	D1	30	/DMAREQ0
6	D2	31	/MEMSEL
7	D3	32	/DMAREQ1
8	D4	33	/INTSEL
9	D5	34	/DMACK
10	D6	35	/IOSEL
11	D7	36	reserved
12	D8	37	A1
13	D9	38	/DMAEND
14	D10	39	A2
15	D11	40	/ERROR
16	D12	41	A3
17	D13	42	/INTREQ0
18	D14	43	A4
19	D15	44	/INTREQ1
20	/BS0	45	A5
21	/BS1	46	/STROBE
22	- 12 V	47	A6
23	+ 12 V	48	/ACK
24	+ 5 V	49	reserved
25	GND	50	GND

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3.15. Four IP module I/O signals, connectors P3C, P4C, P5C, P6C

The four IP modules slots present on the VSBC-6862 have their I/O connections available on four high density connectors. They are connectors from Hirose (Ref: HIF6A-50PA-1,27DSA). The corresponding Hirose cable connector reference is: HIF6-50D-1,27R.
These connectors are assigned as:

connector P6C: IP slot A connector P5C: IP slot B
connector P4C: IP slot C connector P3C: IP slot D

These connectors are pin to pin wired (1 to 1, 2 to 2, ..., 49 to 49 and 50 to 50) with the IP modules IO connectors (P3B to P3C, P4B to P4C, ...).
Note that the IP module slot D I/O pins are also connected to the VME connector P2.



The connector assignment provides the straight connection from the IP module I/O connector with ACTIS cable set reference CAB-85B.

Pin	Signal	Pin	Signal
1	I/O_D 1	2	I/O_D 2
3	I/O_D 3	4	I/O_D 4
5	I/O_D 5	6	I/O_D 6
7	I/O_D 7	8	I/O_D 8
9	I/O_D 9	10	I/O_D 10
11	I/O_D 11	12	I/O_D 12
13	I/O_D 13	14	I/O_D 14
15	I/O_D 15	16	I/O_D 16
17	I/O_D 17	18	I/O_D 18
19	I/O_D 19	20	I/O_D 20
21	I/O_D 21	22	I/O_D 22
23	I/O_D 23	24	I/O_D 24
25	I/O_D 25	26	I/O_D 26
27	I/O_D 27	28	I/O_D 28
29	I/O_D 29	30	I/O_D 30
31	I/O_D 31	32	I/O_D 32
33	I/O_D 33	34	I/O_D 34
35	I/O_D 35	36	I/O_D 36
37	I/O_D 37	38	I/O_D 38
39	I/O_D 39	40	I/O_D 40
41	I/O_D 41	42	I/O_D 42
43	I/O_D 43	44	I/O_D 44
45	I/O_D 45	46	I/O_D 46
47	I/O_D 47	48	I/O_D 48
49	I/O_D 49	50	I/O_D 50

❖ ***These connector are compliant with the Hirose HIF6 series, it provides a 50-pin arrangement organized for a dual 25-pin flat cable***

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3.16. Real time clock battery, circuit U5

The VSBC-6862 provides a real time clock for calendar function. This device includes also a 32 kByte SRAM with battery backed capability.
It also include an on-chip watchdog that can be used as board's Watchdog.
The battery used by this part is a Lithium type and is designed for user replacement.

Warning	**For this operation, caution must be taken in order to avoid hardware damage**

Please use the following instructions for the battery replacement:

1) Turn the main power supply off.
2) Remove the used battery located on the U5 position, refer to the next figure for assembly details.
3) Plug the new battery pack into the U5 location, refer to the next figure for assembly details.

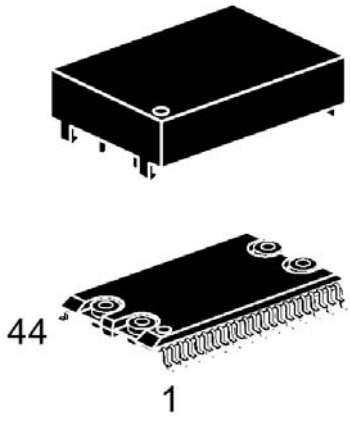


Figure 19: Real Time Clock battery

Replacement battery pack part reference:
ST Microelectronics part number: M4T28-BR12SH1

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3.17. Fuses protection

The VSBC-6862 offers a flexible I/O extension facility through its quad IP module interface. Therefore some cautions must be taken to avoid hardware damage in case of short circuit.
This function is handled by a set of on-board fuses.
These fuses are thermal controlled, when a short-circuit arise, the fuse will automatically break the circuit. When it will be cold, it becomes again normal.

Fuse	Intensity	Power supply
F16	2A	IP module A, +5 V
F15	2A	IP module B, +5 V
F11	2A	IP module C, +5 V
F12	2A	IP module D, +5 V
F3	2A	IP module A/B, +12 V
F10	2A	IP module C/D, +12 V
F4	2A	IP module A/B, -12 V
F9	2A	IP module C/D, -12 V
F1	500mA	RS-232/I2C jumper P4, pin 3: 5V
F2	500mA	RS-232/I2C jumper P4, pin 2: 3.3V
F13	2A	VME connector P2, pin A32 and C32: 5V out for TM

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4
Software description

4.1. Introduction

The PowerQUICC II includes a very versatile and powerful memory controller.
This controller permits to define by software the base memory for each chip select, thus to define the memory map.

The memory controller is composed of three internal machines:

- The general purpose chip select machine: GPCM provides signal generation for local resources: SRAM and FLASH memory, and Real Time Clock.
- The synchronous DRAM machine provide signal generation for SDRAM devices. This internal machine supports many special features for SDRAM.
- The user programmable machines: UPM can be programmed by the user through an internal array to provide specific patterns on signals. These UPMs are used to control the IP and VME devices.

The error generation is mainly handled with the internal bus monitor included in the 8260. See the SYPCR register and bus monitor description in the 8260 User's manual.

Here follows the description of all used chip select on the VSBC-6862:

Chip Select	Port size (bits)	Device	Size
CS0	32	Flash bank 0: boot device 0	8 MBytes
CS1	64	SDRAM	128 MBytes
CS2	32	Flash Bank 1: boot device 1	8 MBytes
CS3	8	Real Time Clock and SRAM	32 kBytes
CS4	16	IP ID, I/O + Board registers	32 kBytes
CS5	16	IP Mem	32 MBytes
CS6	8, 16, 32	VME window A	64 MBytes
CS7	8, 16, 32	VME window B	64 MBytes
CS9	32	SRAM	1 MBytes

In addition, the PowerQUICC II provides many internal peripherals as Fast Ethernet controllers, serial controllers, etc...
These peripherals are internally handled by the MPC-8260 and the control signals are directly connected to the external transceivers.

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4.2. FLASH memory

Two banks of Flash devices are available.
Each bank is 4 or 8 MBytes wide for a total of 8 or 16 MBytes Flash.
The GPCM is used to control the Flash memory.
Each bank is controlled by the Chip Select 0 (CS0) or Chip Select 2 (CS2) signal.
The Flash memory has boot capability in accordance with the 'Bootbank' jumper setting.
The granularity is 16 bits, it means that the minimum size accessible in the Flash memory is two bytes.
This device is command set compatible with JEDEC standard E^2PROMs.
Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry.

This Chip Select (CS0) is the Boot Chip Select, it is connected to a Flash memory bank.
When the power goes to ON, the Flash memory bank connected to this chip select must contain the Reset initialization Word for the PowerQUICC II, and is boot code. If the Reset Word is not valid, the board can be started with a default Reset initialization Word using the 'Resetconf' jumper on J2.

For more convenience, we have added the possibility to switch the Flash memory bank 0 and the bank 1 between CS0 and CS2, thus inverting the bootable bank.
This is done by manipulating the 'BootBank1' jumper.

The bootable Flash memory bank is also accessible from the VME bus. See the VME slave chapter for more information.

4.2.1. FLASH initialization

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	11	Port size:	32 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	000	Machine select:	GPCM on 60x bus
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR0 = $xxxx 1801

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Typical Option Register:

Bit	Field	Value	Function	
0-16	AM	$FFC0 0	Address mask:	for 4 MBytes
17-18	Reserved	00	---	
19	BCTLD	0	Buffer control:	on
20	CSNT	0	Chip select negation time:	normal
21-22	ACS	00	Address to CS setup:	0
23	Reserved	0	---	
24-27	SCY	0110	Cycle length:	6
28	SETA	1	External access termination:	external
29	TRLX	0	Timing relaxed:	off
30	EHTR	0	Extended hold time:	off
31	Reserved	0	---	

-> OR0 = $FFC0 0068

This example is for a 8MByte VSBC-6862. There is two 4MByte Flash memory banks.

This Chip Select is connected to the second bank of Flash memory, depending of the 'BootBnk' jumper. The GPCM is used to control the Flash memory.

As this chip select controls the same device as CS0, it will have the same register values:

Typical Base Register:

-> BR2 = $zzzz 1801

Typical Option Register:

-> OR2 = $FFC0 0068

Once these Chip Select registers are configured, access to the Flash memory can be done.
The Flash memory recognize the standard JEDEC commands, these commands will be described below.

4.2.2. FLASH Programming

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm, which is an internal algorithm that automatically setup the program pulse widths and verifies proper cell margin. Each sector can be programmed and verified in less than 0.5 seconds.
The program sequence is the following:

Sequence	Address	Data
1	Base + $555	$AAAA
2	Base + $2AA	$5555
3	Base + $555	$A0A0
4	Address	Data: 16 bits

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4.2.3. FLASH chip erase

Chip erase operation is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm, which is an internal algorithm that automatically programs the array if it is not already programmed before executing the erase operation. During erase, the device automatically defines the erase pulse widths and verifies proper cell margin.
The chip erase sequence is the following:

Sequence	Address	Data
1	Base + $555	$AAAA
2	Base + $2AA	$5555
3	Base + $555	$8080
4	Base + $555	$AAAA
5	Base + $2AA	$5555
6	Base + $555	$1010

Note that after executing this command, it is important to wait until completion.
Read cycles on Flash indicates the current state of the Flash, while read results are not equal to $FFFF, the chip erase cycle is not finished. This command can last up to 2 minutes.

4.2.4. FLASH sector erase

This device features sector erase architecture. The sector erase mode allows for sectors of memory to be erased and reprogrammed without affecting other sectors. A sector is typically erased and verified within 1 second. (if already completely programmed)
The sector erase sequence is the following:

Sequence	Address	Data
1	Base + $555	$AAAA
2	Base + $2AA	$5555
3	Base + $555	$8080
4	Base + $555	$AAAA
5	Base + $2AA	$5555
6	Sector Address	$3030

Note that depending of the Flash device installed, the sector's organisation can be different.
The following table gives the different types of Flash that can be installed.

Flash type	Manufacturer	Reference	Manufacturer code	Device code
1	AMD	AM29DL324B	0001	225f
	FUJITSU	MBM29DL324B	0004	225f
	TOSHIBA	TC58FVB321	0098	009c
2	AMD	AM29LV160B	0001	2249
	FUJITSU	MBM29LV160B	0004	2249
	TOSHIBA	TC58FVB160	0098	0043
	ST	M29W160BB	0020	2249
3	AMD	AM29LV160T	0001	22c4
	FUJITSU	MBM29LV160T	0004	22c4
	TOSHIBA	TC58FVT160	0098	00c2
	ST	M29W160BT	0020	22c4
4	AMD	AM29DL164B	0001	2235
	FUJITSU	MBM29DL164B	0004	2235

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With Flash type organization as:

Sector	Size for type 1	Size for type 2	Size for type 3	Size for type 4
0	8 kword	16 kword	8 kword	64 kword
1	8 kword	8 kword	8 kword	64 kword
2	8 kword	8 kword	8 kword	64 kword
3	8 kword	32 kword	8 kword	64 kword
4	8 kword	64 kword	8 kword	64 kword
5	8 kword	64 kword	8 kword	64 kword
6	8 kword	64 kword	8 kword	64 kword
7	8 kword	64 kword	8 kword	64 kword
8	64 kword	64 kword	64 kword	64 kword
9	64 kword	64 kword	64 kword	64 kword
10	64 kword	64 kword	64 kword	64 kword
11	64 kword	64 kword	64 kword	64 kword
12	64 kword	64 kword	64 kword	64 kword
13	64 kword	64 kword	64 kword	64 kword
14	64 kword	64 kword	64 kword	64 kword
15	64 kword	64 kword	64 kword	64 kword
16	64 kword	64 kword	64 kword	64 kword
17	64 kword	64 kword	64 kword	64 kword
18	64 kword	64 kword	64 kword	64 kword
19	64 kword	64 kword	64 kword	64 kword
20	64 kword	64 kword	64 kword	64 kword
21	64 kword	64 kword	64 kword	64 kword
22	64 kword	64 kword	64 kword	64 kword
23	64 kword	64 kword	64 kword	64 kword
24	64 kword	64 kword	64 kword	64 kword
25	64 kword	64 kword	64 kword	64 kword
26	64 kword	64 kword	64 kword	64 kword
27	64 kword	64 kword	64 kword	64 kword
28	64 kword	64 kword	64 kword	64 kword
29	64 kword	64 kword	64 kword	64 kword
30	64 kword	64 kword	64 kword	64 kword
31	64 kword	64 kword	64 kword	32 kword
32	64 kword	64 kword	64 kword	8 kword
33	64 kword	64 kword	64 kword	8 kword
34	64 kword	64 kword	64 kword	16 kword
35	64 kword	---	64 kword	---
36	64 kword	---	64 kword	---
37	64 kword	---	64 kword	---
38	64 kword	---	64 kword	---
39	64 kword	---	---	---
40	64 kword	---	---	---
41	64 kword	---	---	---
42	64 kword	---	---	---
43	64 kword	---	---	---
45	64 kword	---	---	---
46	64 kword	---	---	---
47	64 kword	---	---	---
48	64 kword	---	---	---
49	64 kword	---	---	---
50	64 kword	---	---	---
51	64 kword	---	---	---
52	64 kword	---	---	---
53	64 kword	---	---	---
54	64 kword	---	---	---
55	64 kword	---	---	---
56	64 kword	---	---	---
57	64 kword	---	---	---
58	64 kword	---	---	---
59	64 kword	---	---	---
60	64 kword	---	---	---
61	64 kword	---	---	---
62	64 kword	---	---	---
63	64 kword	---	---	---
64	64 kword	---	---	---
65	64 kword	---	---	---
66	64 kword	---	---	---
67	64 kword	---	---	---
68	64 kword	---	---	---
69	64 kword	---	---	---
70	64 kword	---	---	---

Remark: the sector size is specified in words (16-bit) because the Flash granularity is 16-bit on the data bus.

4.2.5. FLASH sector protection: option on request

The VSBC-6862 can also provides the possibility to protect or enable sectors writing.
To implement this feature, the board has the capability to supply 12V on the Flash Reset pin. This voltage is supplied on both banks.
This function is accessible with the FLPROT bit in the BSCR register.

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4.3. SDRAM memory

This memory is handled by the powerful SDRAM timing machine contained in the MPC-8260.
The SDRAM machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve the highest performance. This controller supports directly all the SDRAM possibilities, like pipelining and interleaving.

The VSBC-6862 is supplied with 128 MBytes SDRAM on-board, organized with four 16Mbitsx16 devices.
The 64 bits wide data bus is directly connected on the 60x bus of the MPC-8260 to achieve the best performance.
The SDRAM is controlled by the Chip Select 1 signal.

4.3.1. SDRAM initialization

This device have specific operation for initialization, both SDRAM machine and SDRAM devices have to be set-up.
The SDRAM machine is configured with its own set of registers as OR1, BR1, PSDMR.
The SDRAM device is configured by accessing the PSDMR register in a specific manner.

Here follows the full description to initialize the SDRAM devices:

- Configure MPTPR: timer prescaler
- Configure PSRT: refresh timer prescaler
- Configure OR1
- Configure BR1
- With PSDMR, issue a PRECHARGE-ALL-BANKS command
- " issue eight CBR REFRESH commands
- " issue a MODE-SET command to initialize the mode register with the below recommended value
- The SDRAM can now be used as normal memory

With:

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	00	Port size:	64 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	010	Machine select:	SDRAM on 60x bus
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR1 = $xxxx 0041

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Typical Option Register:

Bit	Field	Value	Function	
0-16	AM	$FE00 0	Address mask:	for 32 MBytes
17-18	BPD	01	Bank per device:	4
19-22	ROWST	0111	Row start address bit:	A7
23-25	NUMR	011	Number of Row lines:	12
26	PMSEL	0	Page mode select:	normal
27	IBID	0	Int. bank interleaving:	enable
28-31	Reserved	0000	---	

-> OR1 = $FE00 2EC0 For 32 MB version

-> OR1 = $F800 2B00 For 128 MB version

Typical 60x SDRAM Mode Register:

Bit	Field	Value	Function	
0	PBI	1	Page based interleaving:	yes
1	RFEN	1	Refresh enable:	yes
2-4	OP	000	SDRAM operation:	normal
5-7	SDAM	010	Address mux size:	MPCA18 -> (SDA28)
8-10	BSMA	010	Bank select address lines:	not used
11-13	A10	010	A10 control:	A8
14-16	RFRC	100	Refresh recovery:	4 clocks
17-19	PRETOACT	010	Precharge to activate interval:	2 clocks
20-22	ACTTORW	010	Activate to Read/Write interval:	2 clocks
23	BL	0	Burst length:	for 64 bits
24-25	LDOTOPRE	01	Last data out to precharge:	-1 clock
26-27	WRC	10	Write recovery time:	2 clock
28	EAMUX	0	External address multiplexing:	disabled
29	BUFCMD	0	External buffers:	no
30-31	CL	10	CAS latency:	2

-> PSDMR = $C24A 2462 For 32 MB version

-> PSDMR = $C32E 2462 For 128 MB version

Typical 60x bus-assigned Refresh Timer Register:

Bit	Field	Value	Function
0-7	PSRT	00111110	Refresh timer period

-> PSRT = $1F

Typical Memory Periodic Timer Pre-scaler Register:

Bit	Field	Value	Function
0-7	PTP	00100000	Refresh timers prescaler
8-15	Reserved	00000000	---

-> MPTPR = $2000

These settings configure the refresh period to 15.5 µs.

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4.4. SRAM memory

The VSBC-6862 includes 1 MByte SRAM for fast exchanges with external VME masters.
With its backup capability with the VME Stand-By power line, this memory can be also useful to backup critical data.
This memory is handled with the GPCM through the Chip Select 9.
It is organized with two 16 bits wide chips to achieve a data width of 32 bits.

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	11	Port size:	32 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	000	Machine select:	GPCM on 60x bus
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR9 = $xxxx 1801

Typical Option Register:

Bit	Field	Value	Function	
0-16	AM	$FFF0 0	Address mask:	for 1 MBytes
17-18	Reserved	00	---	
19	BCTLD	0	Buffer control:	on
20	CSNT	0	Chip select negation time:	normal
21-22	ACS	00	Address to CS setup:	0
23	Reserved	0	---	
24-27	SCY	0110	Cycle length:	6
28	SETA	1	External access termination:	external
29	TRLX	0	Timing relaxed:	off
30	EHTR	0	Extended hold time:	off
31	Reserved	0	---	

-> OR9 = $FFF0 0068

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4.5. Real Time Clock with SRAM memory

The VSBC-6862 includes a real time clock device, with as an additional feature, a battery backed 32 kByte SRAM.

This 32 kByte SRAM provides a flexible user data storage with retention capability by its SNAPHAT battery pack. This device is connected on an 8 bits wide data path.

This device provides also functions like Alarm, Battery Test, and Watchdog function.

The GPCM is used to control the Real Time Clock and the battery backed SRAM.
The RTC data are mapped in the SRAM memory map.

The RTC is also accessible from VME bus.

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	01	Port size:	8 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	000	Machine select:	GPCM on 60x bus
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR3 = $xxxx 0801

Typical Option Register:

Bit	Field	Value	Function	
0-16	AM	$FFFF 1	Address mask:	for 32 kBytes
17-18	Reserved	00	---	
19	BCTLD	0	Buffer control:	on
20	CSNT	0	Chip select negation time:	normal
21-22	ACS	00	Address to CS setup:	0
23	Reserved	0	---	
24-27	SCY	0111	Cycle length:	7
28	SETA	1	External access termination:	external
29	TRLX	0	Timing relaxed:	off
30	EHTR	0	Extended hold time:	off
31	Reserved	0	---	

-> OR3 = $FFFF 8078

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48T37V partial register map is:

Base +	D7	D6	D5	D4	D3	D2	D1	D0	Function (Range) BCD format
$7FFF	10 Years				Year				Year (00-99)
$7FFE	0	0	0	10M.	Month				Month (01-12)
$7FFD	0	0	10 Date		Date				Date (01-31)
$7FFC	0	FT	0	0	0	Day			Century/Day (0-1/01-07)
$7FFB	0	0	10 Hours		Hours				Hour (00-23)
$7FFA	0	10 Minutes			Minutes				Minutes (00-59)
$7FF9	ST	10 Seconds			Seconds				Seconds (00-59)
$7FF8	W	R	S	Calibration					Control
$7FF7	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog
$7FF6	AFE	0	ABE	0	0	0	0	0	Interrupts
$7FF5	RPT4	0	Alarm 10 Date		Alarm Date				Alarm Date (01-31)
$7FF4	RPT3	0	Alarm 10 Hours		Alarm Hours				Alarm Hours (00-23)
$7FF3	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes (00-59)
$7FF2	RPT1	Alarm 10 Second			Alarm Seconds				Alarm Seconds (00-59)
$7FF1	1000 Years				100 Years				Century
$7FF0	WDF	AF	Z	BL	Z	Z	Z	Z	Flags

With:
S = sign bit
FT = Frequency Test bit
R = Read Bit
W = Write Bit
ST = Stop Bit
0 = Must be set to '0'
Z = '0' and are Read only
WDS = Watchdog Steering Bit
WDF = Watchdog Flag
AF = Alarm Flag
BL = Battery Low Flag
WDS = Watchdog Steering Bit
BMB0-BMB4 = Watchdog Multiplier Bits
RB0-RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1-RPT4 = Alarm Repeat Mode Bits

4.5.1. RTC registers read operation

The RTC registers are continuously updated by the device.
Updates to the RTC registers should be halted before clock data is read to prevent reading data in transition.
Because the registers are only copy of the clock counters, updating the registers can be halted without disturbing the clock itself. Updating is halted when a '1' is written to the READ bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that was current at the moment the halt command was issued. All of the RTC registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

4.5.2. RTC registers write operation

Bit D7 of the Control Register 7FF8h is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the RTC registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format. Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual RTC counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in approximately one second.



See the ST Microelectronics Application Note AN923 "TIMEKEEPER rolling into the 21st century" on the ST Web site for information on Century Rollover.

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The Watchdog can be activated by setting the RTC's Watchdog register (internal offset $7ff7) with the desired time-out value.
When the Watchdog is active, it decrement its internal counter until 0. To reload the counter, you can either write again the RTC's watchdog register, either toggling the RTCWDI pin. (connected to the 8260's I/O PD12)
If the Watchdog counter reachs zero, the M48T37V generate an interrupt to its IRQ pin.
This pin is connected on two devices: the 8260 I/O port C5 and the programmable logic. This permits to use the Watchdog in two manners:
A) The Watchdog pin is directly connected to the 8260's port C5, this pin has for special feature to be able to generate an IRQ to the core.
B) For a more securised application, it is possible to connect, using a register, the Watchdog pin to the Board's Power-On Reset signal. This is made writing the value $1 in the SRESR register. Once activated, this connection can not be disabled until next Power-On Reset. In this case, when the Watchdog's counter reachs zero, the VSBC-6862 will be completely Resetted.

The connection of the IRQ signal to the 8260 permits also to use the Alarm feature contained in the M48T37V.

The following table gives the connection to MPC-8260 I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
RTC					
PC5	PC5	I		RTCIRQ	IRQ from RTC
PD12	PD12	O		RTCWDI	Watchdog to RTC



Warning

Before the 'connection' of the Watchdog signal to the Power-On Reset with the SRESR register, please clear the internal RTC's Watchdog register to avoid unintended Reset.



Warning

The SNAPHAT housing plugged on the M48T37V contains both battery and crystal. Thus, for the minimum frequency error, the user has to calibrate the RTC after each battery replacement.



For detailed software setup, please refer to the corresponding ST Microelectronics M48T37V datasheet and application notes.

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4.6. IP modules

The VSBC-6862 board provides four IP module slots, which are compliant with the ANSI/VITA 4-1995, except the clock timing. (see the following Warning) It provides support for 8 MHz type and DMA modules.

The IP interface offers a flexible architecture for I/O extension through inexpensive mezzanine modules for different applications like:

- Digital and analog functions
- Serial communication controllers
- Network and fieldbus interfaces
- Graphic display
- Transducer conditioning
- Etc...

These interfaces give the possibility to easily customize the VSBC-6862.

This IP bus is implemented on the VSBC-6862 through a specific CPLD, which provides the interface between the PowerQUICC II processor and the four IP module slots.



Warning

To avoid internal resynchronizations, the IP clock has been defined as derived from the bus clock (66MHz). This permits the logic to be more efficient in terms of speed. Thus, the IP clock is not VITA-4 compliant, the 8MHz is in fact 8.333 MHz.
This configuration has been successfully tested with our IP modules. However, this can cause problems with some IP modules that use the IP clock to synchronize with other boards.
Two solutions are possible:

1) Select another clock source on the IP clock (if possible)
2) Request a clock modification to ACTIS Computer. The bus clock will be replaced by a 64MHz clock. The IP clock are correct, but the board will run at 128MHz instead of 133MHz or 192MHz instead of 200MHz.
   Some ratios for communication port can also be adjusted



A choice of IP modules and transition modules from ACTIS Computer is available on our web site: www.actis-computer.com

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The IP interface uses two processor chip selects to cover all IP module spaces.
The I/O, ID, and INT spaces are controlled by the Chip Select 4.
The memory space is controlled by the Chip Select 5.

Chip Select 4 configuration

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	10	Port size:	16 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	100	Machine select:	UPM A
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR4 = $xxxx 1081

Typical Option Register:

Bit	Field	Value	Function	
0-16	AM	$FFFF 1	Address mask:	for 32 kBytes
17-18	Reserved	00	---	
19	BCTLD	0	Buffer control:	on
20-22	Reserved	000	---	
23	Burst inhibit	1	Burst disabled	
24-28	Reserved	00000	---	
29-30	EHTR	00	No idle clock inserted	
31	Reserved	0	---	

-> OR4 = $FFFF 8100

Chip Select 5 configuration

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	10	Port size:	16 bits
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	101	Machine select:	UPM B
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR5 = $xxxx 10A1

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Typical Option Register:

Bit	Field	Value	Function
0-16	AM	$FE00 0	Address mask: for 32 MBytes
17-18	Reserved	00	---
19	BCTLD	0	Buffer control: on
20-22	Reserved	000	---
23	Burst inhibit	1	Burst disabled
24-28	Reserved	00000	---
29-30	EHTR	00	No idle clock inserted
31	Reserved	0	---

-> OR5 = $FE00 0100

Both UPM A and UPM B must be loaded with the following values:

UPM's RAM address	Value
Single Read Access	
0x0	0x00fcec00
0x1	0x00fcfc40
0x2	0x00fcfc40
0x3	0x11fdec05
Single Write Access	
0x18	0x00fccc00
0x19	0x00fcfc40
0x1A	0x00fcfc40
0x1B	0x11fdec05
Exception cycle	
0x3C	0xffffcc01

These values define the needed patterns for the memory controller signals.
The Wait Mechanism is defined in this definition to accomodate the unprevisible acknowledge time for the VME and IP cycles.

This UPM Ram must be loaded as described in the MPC8260 Reference Manual, Memory Controller chapter. This will be resumed as:

Description	Example
Set the Base Register	*BR4=0xfa001081
Set the Option Register	*OR4=0xffff8100
Set the MxMR to write at offset 0 for Single Read	*MAMR=0x10040000
Set the MDR with the value to write	*MDR=0x00fcec00
Make an access in the corresponding Chip Select space (write UPM RAM)	*CS4=0
Set the MDR with the next value (the MxMR is auto-incremented)	*MDR=0x00fcfc40
Access the CSx memory space	*CS4=0
(Continue for all Single Read UPM Words)	...
Set the MxMR to write at offset 18 for Single Write	*MAMR=0x10040018
Set the MDR with the value to write	*MDR=0x00fccc00
Make an access in the corresponding UPM space to load the UPM RAM	*CS4=0
Set the MDR with the next value (the MxMR is auto-incremented)	*MDR=0x00fcfc40
Access the CSx memory space	*CS4=0
(Continue for all Single Write UPM Words)	...
Set the MxMR to write at offset 3C for Exception cycle	*MAMR=0x1004003C
Set the MDR with the value	*MDR=0xffffcc01
Access the CSx memory space	*CS4=0
Set the MxMR in normal mode	*MAMR=0x00040000

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4.6.1. Memory spaces

Partial Chip Select 4 memory map:

Offset	Description
$000 - $07e	IP module A: IO zone
$080 - $0fe	IP module A: ID zone
$100 - $17e	IP module B: IO zone
$180 - $1fe	IP module B: ID zone
$200 - $27e	IP module C: IO zone
$280 - $2fe	IP module C: ID zone
$300 - $37e	IP module D: IO zone
$380 - $3fe	IP module D: ID zone

Chip Select 5 memory map:

Offset	Description
$000'0000 - $07f'ffff	IP module A MEM space
$080'0000 - $0ff'ffff	IP module B MEM space
$100'0000 - $17f'ffff	IP module C MEM space
$180'0000 - $1ff'ffff	IP module D MEM space

4.6.2. Registers

The VSBC-6862 contains registers to configure the IP slots operations.
All IP slot has is own set of registers to have the four IP slots fully independent.
These registers are controlled by the Chip Select 4.
For detailed register description, please see the chapter Register Description.

Partial Chip Select 4 memory map:

Offset	Name	Mode	Description
$401	IPGCRA	RW	IP A General Configuration Register
$403	IPDCRA	RW	IP A DMA Configuration Register
$481	IPIVRA	RO	IP A Interrupt Vector
$501	IPGCRB	RW	IP B General Configuration Register
$503	IPDCRB	RW	IP B DMA Configuration Register
$581	IPIVRB	RO	IP B Interrupt Vector
$601	IPGCRC	RW	IP C General Configuration Register
$603	IPDCRC	RW	IP C DMA Configuration Register
$681	IPIVRC	RO	IP C Interrupt Vector
$701	IPGCRD	RW	IP D General Configuration Register
$703	IPDCRD	RW	IP D DMA Configuration Register
$781	IPIVRD	RO	IP D Interrupt Vector

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With:

The GCRx registers allow configuration of the IP module main capabilities, as following:

ENIRQ bit: When set, it enables interrupt request to the processor. Both interrupt sources, of the IP slot, are controlled with ENIRQ.
After system reset, all interrupt sources are disabled.

IPF5V bit: Indicates the 5V status on the IP slots.

4.6.3. Interrupt functions

Each IP slot is able to provide up to two interrupt sources. In order to acknowledge these requests, an interrupt acknowledge cycle was generated by the host processor on the common type like the 68k family. Since that the PowerPC no more handles this type of bus access, the VSBC-6862's internal logic provides specific function in order for ensuring interrupt acknowledge compatibility. The process becomes as follows.

1) An interrupt request is generated by the IP module.
2) If the <GCRx.ENIRQ> bit is set, an interrupt is generated on the processor.
3) The processor goes in interrupt exception.
4) The processor must generate a read cycle to the IVRx register.
5) This action starts an interrupt acknowledge cycle (with activation of the /INTSEL signal) on the IP module and the interrupt vector result is showed on the IVRx register.
The level to be acknowledged on the IP module is automatically selected.
If both IP IRQ are active, the IP IRQ 0 is acknowledged first.

The IVRx registers contains the 8-bit interrupt vector provided by the IP module during the interrupt acknowledge cycle.

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4.6.4. DMA functions

The DMA is controlled by the IDMA channels of the MPC-8260.

The DCR registers set-up the DMA channels configuration, as following:

ENDMA bit: It enables the DMA request to the PowerQUICC II processor, in accordance with the S0 bit definition.
After system reset, all DMA request sources are disabled.



When this bit is set, the Transmit Clock line for the serial port 4 is not accessible.

S0 bit: It allows selection between both DMA channels (/DREQ[1:0]) present on the IP slot.

The DMA channels are controlled by the IDMA channels, with IP Slot A controlled by IDMA1, Slot B controlled by IDMA2, Slot C controlled by IDMA3

The DMA signals are assigned on the PowerQUICC II as the following table:

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
DMA					
PC0	IDMA1: DREQ	I		DMARQ1	IDMA request 1
PC1	IDMA2: DREQ	I		DMARQ2	IDMA request 2
PA0	IDMA3: DREQ	I		DMARQ3	IDMA request 3
PA5	IDMA4: DREQ	I		DMARQ4	IDMA request 4
PD6	IDMA1: DACK	I		DMACK1	IDMA acknowledge 1
PC3	IDMA2: DACK	I		DMACK2	IDMA acknowledge 2
PA2	IDMA3: DACK	I		DMACK3	IDMA acknowledge 3
PA3	IDMA4: DACK	I		DMACK4	IDMA acknowledge 4
PC22	IDMA1: DONE	I/O		DMADONE1	IDMA done 1
PC2	IDMA2: DONE	I/O		DMADONE2	IDMA done 2
PA1	IDMA3: DONE	I/O		DMADONE3	IDMA done 3
PA4	IDMA4: DONE	I/O		DMADONE4	IDMA done 4

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Board control registers

The VSBC-6862 contains some registers for general board features.
They are mapped in the Chip Select 4 memory map and VME slave A16 memory map as:

Local Offset	VME offset	Name	Mode	Description
$1001	$9	SRESR	WO	Software Reset Register
$1011	---	SWPR	RO	Switch Position Register

With:

The SRESR register

This register permits to generate by software, Reset signals to the board.
Resets can be initiated to the MPC8260, board peripherals, and Flash memory.
It permits also to 'connect' the external RTC's Watchdog to the Power-On Reset.
Please refer to the 'Registers Description' chapter for detailed information.

The SWPR register

Reading this registers allows to read the status of the eight position switch.
The position is coded on three bits.

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4.7. VME operations

The VSBC-6862 includes also modules to handle VME operations.
There is VME master, slave, interrupter, interrupt-handler and system controller modules.
Each module can be considered as an independent module.
The next chapters will describe these modules.

4.7.1. Jumpers

Some functions are controlled by jumpers for the VME module.

The first jumpers block controls generic master purposes:

The main function is to set the SLOT1 function that activates the VME controller when the VSBC-6862 is plugged in the slot1.
See jumper 'Slot1' description.

The other functions are for Reset operations between VME and the VSBC-6862. These functions are described in the above corresponding chapter.
See jumpers 'Sysresetin' and 'Sysresetout' description.

The second jumpers block sets the base address of the slave VME registers.
See the 'Jumper 8' description

4.7.2. Registers

The VSBC-6862 contains registers to configure the VME operations.
These registers are controlled by the Chip Select 4.

Partial Chip Select 4 memory map and VME A16 slave map:

CS4 Offset	Slave offset	Name	Mode	Description
$1051	---	VMBA	RW	VME Master: Bus access
$1053	---	VAM	RW	VME Arbiter: Mode
$1055	---	VMBMA	RW	VME Master: A32 Base address for window A
$1057	---	VMBMB	RW	VME Master: A32 Base address for window B
$105b	---	VMAMA	RW	VME Master: Address Modifier for window A
$105d	---	VMAMB	RW	VME Master: Address Modifier for window B
$1061	---	VHIL	RO	VME interrupt Handler: Incoming interrupt Level
$1063	---	VHM	RW	VME interrupt Handler: Mask register
$1065	$1	VSMAIL	WO	VME Slave Mailbox register
$1067	---	VINTER	WO	VME Interrupter command register
$1069	$3	VSBA24	RW	VME Slave Base A24 register
$106b	$5	VSWA24	RW	VME Slave Window A24 management register
$106d	$7	VIVEC	RW	VME Interrupter Vector register
$1071-$107f	---	VHV	RO	VME interrupt Handler: Vector register

For detailed description, please consult the Register Definition chapter.

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4.7.3. VME master

The VSBC-6862 is VME master A32/A24/A16/D32/D16/D8

The VME master can use two windows to access the VME bus.
They are controlled by the UPM, with the chip selects CS6 and CS7.
All VME chip select takes a CPU space of 64 MBytes.

The selection for A16, A24 and A32 modes are made by accessing different offsets in the chip select memory:

Offset	VME Zone	Size
$000'0000-$1ff'ffff	A32	32 MBytes
$200'0000-$2ff'ffff	A24	16 MBytes
$300'0000-$300'ffff	A16	64 kBytes

For A16 and A24 modes, all VME memory map is directly available.

For A32 mode, the VMBMx registers define the seven high order bits for A32 VME addresses.
Thus, the VME 32MBytes windows can be moved in all A32 memory space: 4GBytes.

Depending of the offset accessed, the AM5 to AM3 are automatically set with the corresponding value to indicate the address mode used.
The AM0 to AM2 bits are user definable with the VMAMx registers.

The selection for D8, D16, and D32 are made dynamically with the software. A byte access generates automatically a VME D8 access, a word access a D16 access, and a long word access a D32 access. It is possible to restrict the maximum size of the VME access modifying the BaseRegister[Port Size] bits.



D16 and D32 accesses are only allowed on even addresses

Typical Base Register:

Bit	Field	Value	Function	
0-16	BA	$xxxxb	Base address:	user defined
17-18	Reserved	00	---	
19-20	PS	11	Port size:	32 bits, user defined
21-22	DECC	00	Data error correction:	off
23	WP	0	Write protect:	off
24-26	MS	110	Machine select:	UPM C
27	EMEMC	0	External mem cntrl enable:	off
28-29	ATOM	00	Atomic operation:	off
30	DR	0	Data pipelining:	no
31	V	1	Valid bit:	on

-> BR6-7 = $xxxx 18c1

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Typical Option Register:

Bit	Field	Value	Function
0-16	AM	$FC00 0	Address mask: for 64 MBytes
17-18	Reserved	00	---
19	BCTLD	0	Buffer control: on
20-22	Reserved	000	---
23	Burst inhibit	1	Burst disabled
24-28	Reserved	00000	---
29-30	EHTR	01	One idle clock inserted
31	Reserved	0	---

-> OR6-7 = $FC00 0102

The UPM C must also be defined. The definition is the same as for the UPM A and UPM B described in the IP modules chapter.



The two VME windows have the same VME request level.
(see the VMBA register description)

For the VME master, the release mode is selectable between ROR and RWD modes with the VMBA register.

- ROR mode: Release On Request, the VSBC-6862 keeps the bus until an VME Bus Clear signal is coming. This mode permits the VSBC-6868 to access the VME bus without having to request the bus, thus, accelerates the bus access.

- RWD mode: Release When Done, the VSBC-6866 releases the VME bus after each access.

The VME Master also includes a 'pseudo-RMW' cycle to facilitate the usage of sharable memory.
It is called 'pseudo-RMW' cycle because it does not comply with the VME standard 'RMW' definition, but it can achieve the same result. This function is available through the VSBA24[VME_RMW] bit.
In fact, when the 'pseudo-RMW' cycle is active, the VME Master do not release the BBSY and AS signals. This permits to keep the bus to our exclusive usage.
The normal usage of this function is as:

- Activation of the 'pseudo-RMW' cycle function
- Make VME master cycles, please limit the number of these cycles to a minimum amount
- Deactivation of the 'pseudo-RMW' cycle function



Warning

The 'pseudo-RMW' cycle is not time-limited. If the bus as not been released between either the VME bus timeout, either the local slave's timeout, it will create respectively either VME bus errors for the other VME masters, either local bus error on the slave. Thus please use the minimum VME cycles between the activation and the deactivation of this function.



If a VME bus error occurs on a 'pseudo-RMW' cycle, the VME bus is released and the 'pseudo-RMW' cycle is also deactivated to avoid bus lockout.

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4.7.4. VME slave

The VSBC-6862 is slave A16/A24/D32/D16/D8.

The board contains an independent slave module. This module doesn't need the local processor to be initialized to be active.

From VME, many zones are accessible:
- The VME slave registers
- The Flash memory bank 0
- The SRAM memory
- The Real Time Clock device

Accessing one of these zone at the same time from VME and local processor will naturally start an internal arbitration between these two masters and keep the 'loosing' master in a wait state while the 'winning' master can use the zone.

It’s to be noticed that an external VME access to one of these zones (VSBC-6862 slave access), will not block the local processor with the SDRAM, IP modules, or communication ports. For example, the MPC-8260 can access the SDRAM at the same time an external VME master accesses the local SRAM. Moreover, an external master can access the VSBC-6862, while it is not initialized. All slave functions are independent of the MPC-8260 state.

These zones are divided in two windows:

The A16 window
- This window contains all VME registers.
- This windows occupies 2kBytes.
- Its base address is defined with 5 jumpers, for detailed information, please see J8 description.

VME slave register memory map:

Offset	Name	Mode	Description	Access
$1	VSMAIL	RW	VME Slave Mailbox	D8/D16
$3	VSBA24	RW	VME Slave Base Window Address	D8/D16
$5	VSWA24	RW	VME Slave Window A24 management	D8/D16
$7	VIVEC	RW	VME Interrupter Vector	D8/D16
$9	SRESR	WO	VME Software Reset Register	D8/D16

For more flexibility, these registers are also accessible from the MPC-8620. This implies that for each register, the user must choose to initialize the register either from VME, either from local processor to avoid accesses at the same time by both sides.

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The A24 window

This window contains Flash, SRAM, and RTC zones.
This window occupies 1 MBytes and must be enabled with the VSBA24[WinA24On] bit before use.
Its base address into the VME A24 space is defined with the VSBA24 register.

The Flash, SRAM, or RTC are accessed depending on the offset in this window as:

VME Offset	Device	Size	Access
$0'0000-$7'ffff	SRAM memory	512 kBytes	D8/D16/D32
$8'0000-$b'ffff	Flash memory	256 kBytes	D16/D32
$c'0000-$c'7fff	RTC device	32 kBytes	D8

Except for the RTC device, this window doesn't include all memory map for Flash and SRAM memory. The VSWA24 register is used to complete the high order local addresses for these two devices.

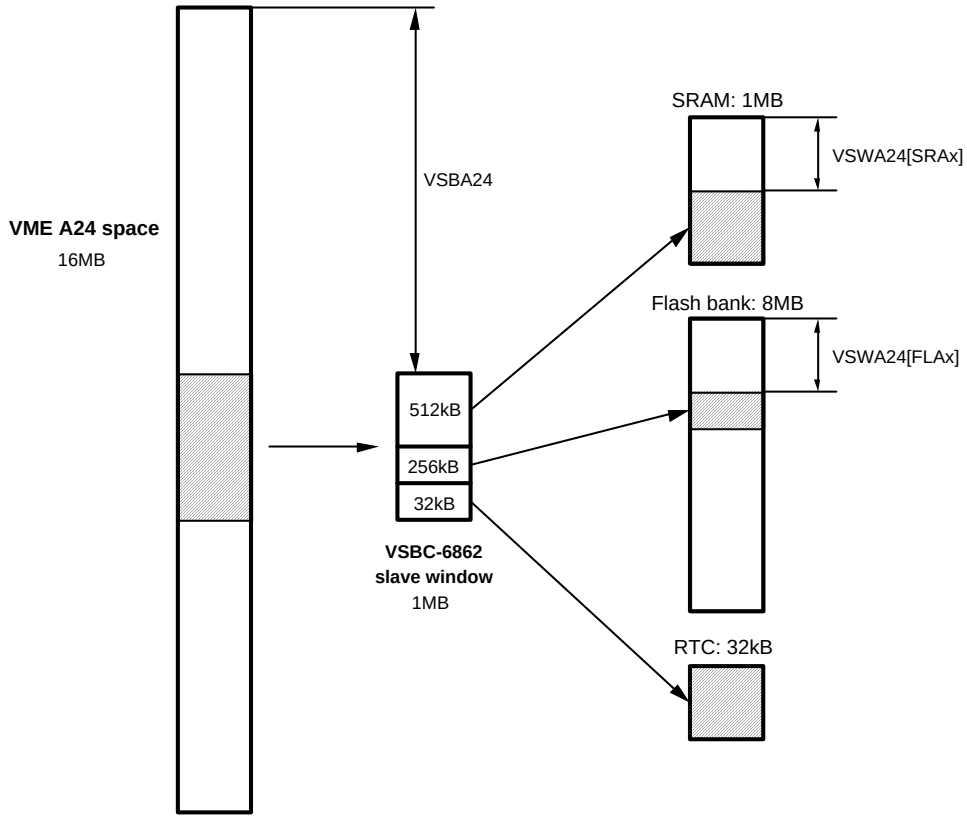


Figure 20: VME slave window

The bootable Flash memory bank 0 is 8 MBytes, the VME slave window for Flash is 256 kBytes.
32 positions are needed to cover all Flash memory map. This is done using the VSWA24 register, bits FLA18-FLA22. These bits are the respective high order addresses sent to the local Flash memory.
It's to be noticed that the Flash memory is not accessible in D8 mode from VME. A D8 access will always select 16 bits on the Flash memory.
When the J2[BootBank1] jumper is plugged-in, the VME bus can access the non-bootable Flash memory bank, otherwise it can access the bootable Flash memory bank.

The SRAM memory is 1 MBytes, the VME slave window for SRAM is 512 kBytes.
2 positions are needed to cover this memory map. This is done using the VSWA24 register, bit SRA19.

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The VMEA24 Slave window accepts the 'pseudo-RMW' cycles as described on the VME master chapter.
We also implement a function to have an local exclusive access to the shared memory. This is useful to keep the memory coherency by avoiding an external VME access between two critical local access.
This function is called 'local_RMW' cycle, and is available through the BSCR[local_rmw] bit.
It has to be used as:

- Activation the 'local-RMW' cycle function
- Make some local cycles, please limit the number of these cycle to a minimum amount
- Deactivation of the 'local-RMW' cycle function

 Warning	**The 'local-RMW' cycle is not time-limited. If function is not released before the VME bus timeout, and an external VME master is waiting on this VME slave Window, it will create an VME bus error. Thus please use the minimum number of cycles between the activation and the deactivation of this function.**

	In case of Bus Error, the 'local-RMW' cycle is not automatically deactivated. We advice that the Software Exception routine include the deactivation of the 'local-RMW' function.

4.7.5. VME interrupter

The VSBC-6862 can send any interrupt level to the VME bus with its interrupter I(1-7) D08(O) ROAK.
Before generating this interrupt, the interrupt level and the vector must be defined with the VIVEC register.
The corresponding interrupt signal is activated when writing any value to the VINTER register.
This interrupt stay active until interrupt-handler treats this interrupt. For debug purposes, this interrupt can be locally deactivated using the SRESR register.
When an interrupt-acknowledge is detected, the vector is returned, and the interrupt is deactivated.

4.7.6. VME interrupt handler

The VSBC-6862 is VME interrupt-handler IH(1-7) D08(O).

This interrupt-handler is able to recognize all IRQ VME levels.
All levels can be masked with the VHM register.

When an IRQ is coming from the VME side, an IRQ1 is sent to the MPC-8260.
The user can then read the IRQ levels active in the VHIL register.
Depending on the IRQ level to be acknowledged, the user can read the vector in the corresponding offset in the VHV register.
When reading the vector, the interrupt acknowledge cycle is initiated.

4.7.7. VME Mailbox

The VSBC-6862 provides a single Mailbox system. From the VME side, it is composed of a single register: VSMAIL.
Before using this function, the VSBA24[MailOn] bit must be set to unmask the local IRQ.
When an external master writes to this register, an IRQ6 is sent to the PowerQUICC II.
To clear this IRQ, the PowerQUICC II must write any value to the VSMAIL register.

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4.7.8. VME system controller

The VSBC-6862 can work as a system controller.
This function can be enabled or disabled with the Slot1 jumper.

When the system controller feature is enabled, the VSBC-6862 provides the following functions:

- VME arbiter: SGL, PRI or RRS depending of the VAM register.

  - In SGL mode: Single Level, the arbiter uses only the BusRequest3 signal from VME. and activates only the BusGrant3 signal. The board with the higher relative priority is the nearest to slot1.
  - In PRI mode: Prioritized, the arbiter uses the BusRequest3 as higher priority and BusRequest0 as lower priority.
    If a master with **higher** priority requests the bus, a BCLR is generated.
  - In RRS mode: Round Robin Select, the level of the priority of the request lines change in a circular manner. For example: If the Arbiter granted the bus to a Requester with level 2, the next most higher level is the level 1, with all other level shifted respectively in the level priority.

- VME bus monitor: BTO(30)
  The BERR signal is activated if DS0 or DS1 stays actives more than 30 us.

- IACK daisy-chain driver.

- 16 MHz system clock generator.

4.7.9. Specific features for VME

Jumpers can modify the links between VME reset and VSBC-6862 reset as:

When the VME_Reset_In jumper is plugged, and if the board is not in Slot1 mode, a VME Reset will generate a board Hardware Reset.
Otherwise, the VME Reset has no effect on the VSBC-6862.

When the VME_Reset_Out jumper is plugged, if the board is in Slot1 mode, it will generate a VME Reset when the board is under Hardware Reset.
Otherwise, the VME Reset is not generated by the VSBC-6862.

4.7.10. General remarks for VME

Please keep in mind that the configuration of the VME master release mode with the VME arbiter mode have influence in the system performance.
Both parameters have to be set in a global system logic.
For example: If two boards are used as master ROR on the same level, with a PRI arbiter; the first master will keep the bus while the second will never have an access... The solution is to change the release mode to RWD, or change the arbiter to RRS and have the masters with two different request level.



The VME bus numbers its bits 31 to 0 from msb to lsb (little-endian), while the MPC-8260 numbers its bits from 0 to 31 msb to lsb (big-endian).

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4.8. Serial I^2C EEPROM

8 kbits of non-volatile memory is provided on the I^2C bus.
This memory can be used for board initialization and user purposes, they will generally contains some boards specific information like physical Ethernet addresses.

Please see the chapter Board initialization for more details .

The chip used is a M24C08 and is configured at address 0xb '1 0 1 0 0 x x r/!w' and occupies four addresses on I^2C bus.

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4.9. Fast Ethernet ports

4.9.1. Transceivers description

The two fast Ethernet interfaces come directly from the MPC-8260 processor. The physical layer is achieved with on-board fast Ethernet transceivers.
The SMSC-LAN83C183 provides all of the IEEE 802.3u 100Base-TX and ISO802.3 10Base-T Physical Layer (PHY) functions needed for workstations, bridge, router, and switch applications. It can operate as a 100Mbps only device, or as a dual speed 10/100Mbps device with built-in auto-negotiation possibility for speed selection. The SMSC-LAN83C183 supports the standard Media Independent Interface (MII) for glueless interface with 10/100 Ethernet Media Access Controllers (MAC).
The built-in IEEE 802.3u Auto-Negotiation feature automatically selects internal 10Base-T or 100Base-TX, full or half-duplex, as a result of negotiation between the station and its link partner.
The SMSC-LAN83C183 supports half and full-duplex operation at both 10Mbps and 100Mbps speeds. It complies with ANSI X3T9 TP-PMD and includes MLT-3 Encoder/Decoder and Stream Cipher scrambler/ de-scrambler functions for 100Base-TX.The SMSC-LAN83C183 supports Category 5 Unshielded Twisted Pair and Type 1 Shielded Twisted Pair wiring. The on-chip Serial Management Interface features the Basic and Extended registers set. The 4B/5B Encoder and Decoder are also included.

An on-board transformer provides a direct connection for a 10Base-T and 100Base-TX interface

Specific hardware configuration as defined by the VSBC-6862 is like the following:

Fast Ethernet Port 1

PHY address:	$1
Speed select:	100 Mbps
Auto-negotiation:	enabled
Duplex:	full

Fast Ethernet Port 2

PHY address:	$1
Speed select:	100 Mbps
Auto-negotiation:	enabled
Duplex:	full

Note that these default values (expected PHY address) can be changed at any time through the serial management interface.

It's to be noted that the two Fast Ethernet PHY have the same address. Each transceiver is connected on an independent MII channel.

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4.9.2. MPC-8260 I/O ports

The following table gives the connection to MPC-8260 I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
Fast Ethernet port 1					
PB6	MII_MDC	O		ECMDC	data clock
PB7	MII_MDIO	O		MIIMDIO	data
PB26	MII_CRS	I		MIICRS	carrier sense
PB27	MII_COL	I		MIICOL	collision
PB29	MII_TX_EN	O		MIITXEN	transmission enable
PC19	CLK13	O		MII_TX_CLK	transmission clock
PB31	MII_TX_ER	I		ECTXER	transmit error
PB25	MII_TXD3	O		ECTXD3	transmit data
PB24	MII_TXD2	O		ECTXD2	transmit data
PB23	MII_TXD1	O		ECTXD1	transmit data
PB22	MII_TXD0	O		ECTXD0	transmit data
PB30	MII_RX_DV	I		ECRXDV	receive valid data
PC18	CLK14	I		MII_RX_CLK	receive clock
PB28	MII_RX_ER	I		ECRXER	receive error
PB18	MII_RXD3	I		ECRXD3	receive data
PB19	MII_RXD2	I		ECRXD2	receive data
PB20	MII_RXD1	I		ECRXD1	receive data
PB21	MII_RXD0	I		ECRXD0	receive data
PC4	MII_IRQ2	I		MII_IRQ2	irq
Fast Ethernet port 2					
PB4	MII_MDC	O		ECMDC	data clock
PB5	MII_MDIO	O		MIIMDIO	data
PA30	MII_CRS	I		MIICRS	carrier sense
PA31	MII_COL	I		MIICOL	collision
PA28	MII_TX_EN	O		MIITXEN	transmission enable
PC21	CLK11	O		MII_TX_CLK	transmission clock
PA29	MII_TX_ER	I		ECTXER	transmit error
PA21	MII_TXD3	O		ECTXD3	transmit data
PA20	MII_TXD2	O		ECTXD2	transmit data
PA19	MII_TXD1	O		ECTXD1	transmit data
PA18	MII_TXD0	O		ECTXD0	transmit data
PA27	MII_RX_DV	I		ECRXDV	receive valid data
PC20	CLK12	I		MII_RX_CLK	receive clock
PA26	MII_RX_ER	I		ECRXER	receive error
PA14	MII_RXD3	I		ECRXD3	receive data
PA15	MII_RXD2	I		ECRXD2	receive data
PD16	MII_RXD1	I		ECRXD1	receive data
PD17	MII_RXD0	I		ECRXD0	receive data
PC6	MII_IRQ1	I		MII_IRQ1	irq

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4.9.3. Transceivers operations

Each transceiver has many registers to handle Fast Ethernet operation.

These registers are accessed with set of command on the MII bus.
Commands must use a serial format starting with an idle pattern that is a series of at least 32 1's of data, with clock pulses having at least 400ns period.
The frame then starts with 0101 for a Write, or 0110 for Read,
The next 5 bits are PHY address.
The next 5 bits are register address select bits.
The next 1 bit is a turnaround bit which is not an actual register bit but extra time to switch MDIO from write to read if necessary.
The final 16 bits are the register data. They are then sent, most significant bit first.
Data are TTL positive logic, and are set by the master near to the negative transition of the clock and sampled on the positive clock edge. Data are returned from the slave up to 300ns after the positive edge of the clock, and can be sampled by the master just before it sets the clock high for the subsequent pulse.

It is recommended that all the procedures listed below should start with the following two step sequence, especially during initialization time:

- Reset PHY by writing 8000h to PHY register 0.
- Poll bit 15 (*Reset*) in PHY register 0 until it is 0 for the reset completion. Timeout and report failure if it takes longer than 0.5 seconds.

Static 10BaseT Half duplex configuration:

1. Write 0000h to PHY register 0.
2. Set the duplex configuration of the MAC accordingly.

Static 100BaseTX Full duplex configuration:

1. Write 2100h to PHY register 0.
2. Set the duplex configuration of the MAC accordingly.

Here follows the description of the most used registers.

PHY register address 0: Control Register

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15	Reset	1 = reset all register bits to defaults 0 = normal	R/W, SC	0
14	Loopback	1 = loopback mode enabled 0 = normal	R/W	0
13	Speed select	1 = 100Mb/s 0 = 10Mb/s	R/W	1
12	Auto negotiation	1 = auto negotiation enabled 0 = normal	R/W	1
11	Power down	1 = power down active 0 = normal	R/W	0
10	MII disable	1 = MII interface disabled 0 = normal operation	R/W	0
9	Restart auto negotiation	1 = restart auto negotiation 0 = normal	R/W, SC	0
8	Duplex mode	1 = Full duplex mode 0 = Half duplex mode	R/W	0
7	Collision Test	1 = enable COL signal test 0 = normal	R/W	0
6:0	Reserved	Reserved	R/W	0

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PHY register address 1: Status Register

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15	100BASE-T4	1 = 100BASE-T4 capability 0 = no 100BASE-T4 capability	RO	0
14	100BASE-TX full duplex	1 = full duplex 100BASE-TX capability 0 = No full duplex 100BASE-TX capability	RO	1
13	100BASE-TX half duplex	1 = half duplex 100BASE-TX capability 0 = no half duplex 100BASE-TX capability	RO	1
12	10Mb/s full duplex	1 = full duplex 10Mb/s capability 0 = No full duplex 10Mb/s capability	RO	1
11	10BASE-T half duplex	1 = 10BASE-T (half duplex) capability 0 = No 10BASE-T (half duplex) capability	RO	1
10	100Base-T2 full duplex	1 = full duplex 100BASE-T2 capability 0 = No full duplex 100BASE-T2 capability	RO	0
9	100Base-T2 half duplex	1 = half duplex 100BASE-T2 capability 0 = No half duplex 100BASE-T2 capability	RO	0
8 :7	Reserved	Reserved	RO	0
6	MF Preambule suppression	1 = accept management frames with short preamble 0 = normal preamble only	RO	0
5	Auto negotiation compl.	1 = auto negotiation process complete 0 = auto negotiation not complete	RO	0
4	Remote fault	1 = Remote fault condition detected 0 = No Remote fault condition detected	RO LH	0
3	Auto negotiation ability	1 = auto negotiation capability available 0 = auto negotiation capability not available	RO	1
2	Link status	1 = link is up 0 = link is down	RO LL	0
1	Jabber detect	1 = Jabber condition detected 0 = Normal operation	RO	0
0	Extended capability	1 = extended register capabilities 0 = basic register set only registers)	RO	1

PHY register address 2: Identifier Register #1

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15:0	OUI	SMSC OUI bits	RO	$xxxx

PHY register address 3: Identifier Register #2

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15:0	OUI/Device ID	next SMSC OUI bits and device code	RO	$xxxx

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PHY register address 4: Auto-Negotiation Advertisement Register

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15	Next Page	1 = additional link code word pages 0 = no additional pages	RO	0
14	Acknowledge	1 = received ANeg Word recognized 0 = not recognized	RO	0
13	Remote fault	1 = ANeg remote fault detected 0 = no remote fault detected	R/W	0
12:10	Reserved	Reserved	R/W	0
9	T4	1 = capable of 100Base-T4 0 = not capable	R/W	0
8	TX_FDX	1 = capable of 100Base-TX Full-Duplex 0 = not capable	R/W	1
7	TX_HDX	1 = capable of 100Base-TX Half-Duplex 0 = not capable	R/W	1
6	10_FDX	1 = capable of 10Base-T Full-Duplex 0 = not capable	R/W	1
5	10_HDX	1 = capable of 10Base-T Half-Duplex 0 = not capable	R/W	1
4:1	Reserved	Reserved	RO	0
0	CSMA 802.3 capable	1 = capable of 802.3 CSMA operation 0 = not capable	RO	1

PHY register address 17: Structure and Bit definition

Bit	NAME	DESCRIPTION	R/W	DEFAULT
15, 14	Programmable LED output 3	11 = normal 10 = LED blink 01 = LED on 00 = LED off	R/W	11
13,12	Programmable LED output 2	11 = normal 10 = LED blink 01 = LED on 00 = LED off	R/W	11
11, 10	Programmable LED output 1	11 = normal 10 = LED blink 01 = LED on 00 = LED off	R/W	11
9,8	Programmable LED output 0	11 = normal 10 = LED blink 01 = LED on 00 = LED off	R/W	11
7,6	LED function	See table 'LED function' below	R/W	00
5	Auto-polarity disable	1 = MII interface disabled 0 = normal operation	R/W	0
4	Jabber disable	1 = restart auto negotiation 0 = normal	R/W	0
3	Multiple register access	1 = Full duplex mode 0 = Half duplex mode	R/W	0
2	Interrupt scheme	1 = enable COL signal test 0 = normal	R/W	0
1	R/J configuration	1 = RX_EN/nJAM pin is nJAM 0 = RX_EN/nJAM pin is RX_EN	R/W	0
0	Reserved	Reserved, must be 0	R/W	0

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LED Function: **Description for PHY register 17, bits 7 and 6**

Bits 7, 6	LED_5	LED_4	LED_3	LED_2	LED_1	LED_0
11	Receive Activity	Transmit Activity	Link	Collision	Full Duplex	10 Mb/s
10	Receive Activity	Transmit Activity	Link	Activity	Full Duplex	10 Mb/s
01	Receive Activity	Transmit Activity	Link + Activity	Collision	Full Duplex	10 Mb/s
00	Receive Activity	Transmit Activity	Link 100Mb/s	Activity	Full Duplex	Link 10 Mb/s

The RJ-45 green LED for the link indication is connected to the LED_3 signal.
The RJ-45 yellow LED for the activity indication is connected to the LED_2 signal.

NOTE: All unnamed or unused register locations will return 0 values when accessed.
KEY: LL = latch low until read, LH = latch high until read, R/W = read/write, RO = read only, SC = self-clearing.



For detailed software setup, please refer to the SMSC-LAN83C183 datasheet and application notes.

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4.10.SMC1 and SMC2 serial ports

One of these general-purpose serial ports is available on the front panel RJ-45 connector.
The other one is available on an internal connector.
These serial ports can be typically uses as system console ports.

Note that this type of port has no hardware flow control capability.

4.10.1. MPC-8260 I/O ports

The following table gives its connection to MPC-8260T I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
SMC1					
PD9	SMTXD1	O		TxD	Transmit data
PD8	SMRXD1	I		RxD	Receive data
SMC2					
PA9	SMTXD2	O		TxD	Transmit data
PA8	SMRXD2	I		RxD	Receive data



For related software setup, please refer to the corresponding Motorola MPC-8260 user's manual and application notes.

4.10.2. ACTIS Console Cable

ACTIS can provide a serial cable for this Console port. Its reference is CAB-RJ45-DB9.
This DTE cable connects the VSBC-6862's Console port (SMC) to a standard PC serial port in RS-232 with software handshake.

Connectors: RJ-45 8-pin male
Sub-D 9-pin female
Length: 1.8m
Pinout:

Pin function on Sub-D 9 side	Sub-D 9, 2 rows, female		Pin function on RJ-45 side	RJ-45
Not connected	---		Not connected	1
Not connected	---		Not connected	2
Not connected	---		Not connected	3
RxD	2		TxD	4
TxD	3		RxD	5
Ground	5		Ground	6
Not connected	---		Not connected	7
Not connected	---		Not connected	8

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4.11.SCC serial ports

The VSBC-6862 offers four independent serial ports.
In synchronous mode, all four ports have independents RX clock signals, but only SCC1 and SCC2 have TX Clocks signals.

These ports are directly controlled by the Serial Communication Controllers (SCC) included in the PowerQUICC II. These SCC includes functions like support of many protocols like UART and HDLC, it contains also FIFO buffers: 32-byte deep, and many more powerful options.

All the four ports are available on four Sub-D-HD-15 connectors on front panel.

The protocols of these ports can be either RS-232, either RS-422/RS-485/V.35.
Switching between these two option can be done through the 'protocolx' jumpers.

The serial ports 1 and 3 have an added function: they can be internally used to synchronize the internal Baud Rate Generators (BRG) with external clock signal.

4.11.1. RS-232 option

These VSBC-6862 ports are in an standard RS-232 mode.
The following signals are controlled by the PowerQUICC II:
TxD, RxD, TxC, RxC, CTS, RTS, and DCD

All ports support hardware handshaking functions.
DSR signals are pulled-up to VCC to indicate that the board is powered-up.

In DCE mode (to connect a modem), the recommended cable pinout is:

Pin function	Sub-D 15, 3 rows, male	Sub-D 25, 2 rows, male
Shield	1	1
Transmit Data	2	2
Receive Data	14	3
Request To Send	6	4
Clear To Send	8	5
Data Set Ready	15	6
Ground	7	7
Data Carrier Detect	10	8
Transmit Clock	4	15
Receive Clock	12	17
Data Terminal Ready	9	20

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4.11.2. RS-422/RS-485/V.35 option

These VSBC-6862 ports are compatible with these three modes.
The following signals are controlled by the PowerQUICC II:

TxD, RxD, TxC, RxC in differential mode
CTS, RTS and DCD in RS-232 mode for V.35

> ☞ As described above, the VSBC-6862 did not provides all defined signals for V.35, it provides all 'transmission signals' but not for example, the loopback or ring indicator signals.

All ports support full and half-duplex mode, and two ports supports also support full synchronous operations.

The internal I/O ports dedicated to RTS is connected to the internal data transmit enable signal.
This permits to determine the function for half or full-duplex modes as:

Full-duplex: configure RTS always active
Half-duplex: configure RTS as normal RTS

The PowerQUICC II has also the possibility to disable his receiver while emitting (see bit DRT in register PSMR).

Each port has its own resistor network.
These resistors are on sockets. ACTIS choose to implement manual resistor networks to keep the RS-485 network always working, independently of the power state of the VSBC-6862.
These resistor networks are to be installed only when the corresponding serial port is at one of both ends of the RS-485 network cable.

In DCE mode (to connect a modem), the recommended cable pinout is:

Pin function	Sub-D 15, 3 rows, male	Sub-D 25, 2 rows, male
Shield	1	1
Transmit Data+	2	2
Receive Data+	14	3
Request To Send	6	4
Clear To Send	8	5
Data Set Ready	15	6
Ground	7	7
Data Carrier Detect	10	8
Receive Clock-	11	9
Transmit Clock-	5	12
Transmit Data-	3	14
Transmit Clock+	4	15
Receive Data-	13	16
Receive Clock+	12	17
Data Terminal Ready	9	20

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4.11.3. ACTIS Serial Cable

ACTIS can provide a serial cable for these multi-protocol serial ports. Its reference is CAB-V6862-SCC-01. This cable connects the VSBC-6862 multi-protocols serial ports (SCC) in RS-232/RS-422/RS-485/V.35 mode to a DCE equipment, for example a modem.

Connectors: Sub-D high-density 15-pin male width max: 31,3mm
Sub-D 25-pin male
Length: 1.8m
Pinout:

Pin function RS-232/V.35	Sub-D 15, 3 rows, male	Sub-D 25, 2 rows, male
Shield / Shield	1	1
TxD / TxD+	2	2
RxD / RxD+	14	3
RTS / RTS	6	4
CTS / CTS	8	5
DSR / DSR	15	6
GND / GND	7	7
DCD / DCD	10	8
Not used / RxC-	11	9
Not connected	---	10
Not connected	---	11
Not used / TxC-	5	12
Not connected	---	13
Not used / TxD-	3	14
TxC / TxC+	4	15
Not used / RxD-	13	16
RxC / RxC+	12	17
Not connected	---	18
Not connected	---	19
DTR / DTR	9	20
Not connected	---	21
Not connected	---	22
Not connected	---	23
Not connected	---	24
Not connected	---	25

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4.11.4. MPC-8260 I/O ports

The following table gives the connection to MPC-8260 I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
SCC1					
PD30	TXD1	O		TxD	Transmit data
PD31	RXD1	I		RxD	Receive data
PD29	RTS1	O		RTS	Request to send
PC15	CTS1	I		CTS	Clear to send
PA22	PA22	O		DTR	Data terminal ready
PC14	CD1	I		DCD	Data carrier detect
PC31	BRG1	O		TxC	Transmit clock
PC29	CLK3	I		RxC	Receive clock
SCC2					
PB12	TXD2	O		TxD	Transmit data
PB15	RXD2	I		RxD	Receive data
PD26	RTS2	O		RTS	Request to send
PC13	CTS2	I		CTS	Clear to send
PA23	PA23	O		DTR	Data terminal ready
PC12	CD2	I		DCD	Data carrier detect
PD17	BRG2	O		TxC	Transmit clock
PC28	CLK4	I		RxC	Receive clock
SCC3					
PB8	TXD3	O		TxD	Transmit data
PB14	RXD3	I		RxD	Receive data
PD23	RTS3	O		RTS	Request to send
PC11	CTS3	I		CTS	Clear to send
PA24	PA24	O		DTR	Data terminal ready
PC10	CD3	I		DCD	Data carrier detect
PC27	BRG3	O		TxC	Transmit clock
PC25	CLK7	I		RxC	Receive clock
SCC4					
PD21	TXD4	O		TxD	Transmit data
PD22	RXD4	I		RxD	Receive data
PD20	RTS4	O		RTS	Request to send
PC9	CTS4	I		CTS	Clear to send
PA25	PA25	O		DTR	Data terminal ready
PC8	CD4	I		DCD	Data carrier detect
PD10	BRG4	O		TxC	Transmit clock
PC26	CLK6	I		RxC	Receive clock



For related software setup, please refer to the corresponding Motorola MPC-8260 user's manual and application notes.

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4.12. I²C interface

The VSBC-6862 provides an I²C interface bus for on-board serial EEPROM accesses and user purposes.
For example, this non-volatile memory store the Ethernet addresses for the two Fast Ethernet ports.

The serial EEPROM is placed at I²C address 0xb '1 0 1 0 0 x x r/!w'
It occupies four addresses.

All other addresses can be used for external add-on peripherals. The I²C interface is present on the P4 connector.

The following table gives its connection to MPC-8260 I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
I2C					
PD14	I2CSCL	O		I2CSCL	clock
PD15	I2CSDA	I/O		I2CSDA	data



For related software setup, please refer to the corresponding Motorola MPC-8260 user's manual and application notes.

4.13. Auxiliary LEDs

The VSBC-6862 provides two auxiliary LEDs, controlled by the PowerQUICC II I/O port.

The following table gives its connection to MPC-8260 I/O ports.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
Auxiliary LEDs					
PC24	PC24	O		LED_AUX0	Auxiliary LED 0
PC30	PC30	O		LED_AUX1	Auxiliary LED 1

These LEDs are located on the P1, RJ-45 connector: LED_AUX0 is the yellow LED
LED_AUX1 is the green LED

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5 Summary of board resources

5.1. Chip Select

Chip Select	Port size (bits)	Device	Size
CS0	32	Flash bank 0: boot device 0	8 MBytes
CS1	64	SDRAM	128 MBytes
CS2	32	Flash Bank 1: boot device 1	8 MBytes
CS3	8	Real Time Clock and SRAM	32 kBytes
CS4	16	IP ID, I/O + Board registers	32 kBytes
CS5	16	IP Mem	32 MBytes
CS6	8, 16, 32	VME window A	64 MBytes
CS7	8, 16, 32	VME window B	64 MBytes
CS9	32	SRAM	1 MBytes

5.2. Local Board registers

Local Offset	VME offset	Name	Mode	Description
$401	---	IPGCRA	RW	IP A General Configuration Register
$403	---	IPDCRA	RW	IP A DMA Configuration Register
$481	---	IPIVRA	RO	IP A Interrupt Vector
$501	---	IPGCRB	RW	IP B General Configuration Register
$503	---	IPDCRB	RW	IP B DMA Configuration Register
$581	---	IPIVRB	RO	IP B Interrupt Vector
$601	---	IPGCRC	RW	IP C General Configuration Register
$603	---	IPDCRC	RW	IP C DMA Configuration Register
$681	---	IPIVRC	RO	IP C Interrupt Vector
$701	---	IPGCRD	RW	IP D General Configuration Register
$703	---	IPDCRD	RW	IP D DMA Configuration Register
$781	---	IPIVRD	RO	IP D Interrupt Vector
$1001	$9	SRESR	WO	Software Reset Register
$1011	---	SWPR	RO	Switch Position Register
$1021	---	BSCR	RW	Board special configuration register
$1051	---	VMBA	RW	VME Master: Bus access
$1053	---	VAM	RW	VME Arbiter: Mode
$1055	---	VMBMA	RW	VME Master: A32 Base address for window A
$1057	---	VMBMB	RW	VME Master: A32 Base address for window B
$105b	---	VMAMA	RW	VME Master: Address Modifier for window A
$105d	---	VMAMB	RW	VME Master: Address Modifier for window B
$1061	---	VHIL	RO	VME interrupt Handler: Incoming interrupt Level
$1063	---	VHM	RW	VME interrupt Handler: Mask register
$1065	$1	VSMAIL	WO	VME Slave Mailbox register
$1067	---	VINTER	WO	VME Interrupter command register
$1069	$3	VSBA24	RW	VME Slave Base Window A24 register
$106b	$5	VSWA24	RW	VME Slave Window management register
$106d	$7	VIVEC	RW	VME Interrupter Vector register

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With: Local offset: offset from local CS4
VME offset: offset from VME A16 slave window, defined with J8
Mode: RW=Read/Write, RO=Read only, WO=Write only

5.3. Interrupt sources

Interrupt	Source
IRQ0	not used
IRQ1	VME interrupt-handler
IRQ2	IP module D
IRQ3	IP module C
IRQ4	IP module B
IRQ5	IP module A
IRQ6	VME mailbox
IRQ7	not used

The two Ethernet controllers have each one interrupt request line.
These lines are connected on the PowerQUICC II I/O ports as:
Fast Ethernet controller 1: I/O port C6
Fast Ethernet controller 2: I/O port C4
The Real Time Clock is also able to generate an IRQ. This line is connected as:
RTC IRQ : I/O port C5

All these MPC-8260 I/O ports are able to generate IRQ to the CPU.

5.4. Reset sources

The PowerQUICC II has three external Reset sources:

The Power-On Reset:	PORESET	input only	
The Hardware Reset:	HRESET	input/output	open-collector
The Software Reset:	SRESET	input/output	open-drain



For a complete description of the Reset signals, please see the MPC-8260 user's manual.

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The VSBC-6862 uses these reset signals with an equivalent circuitry than following:

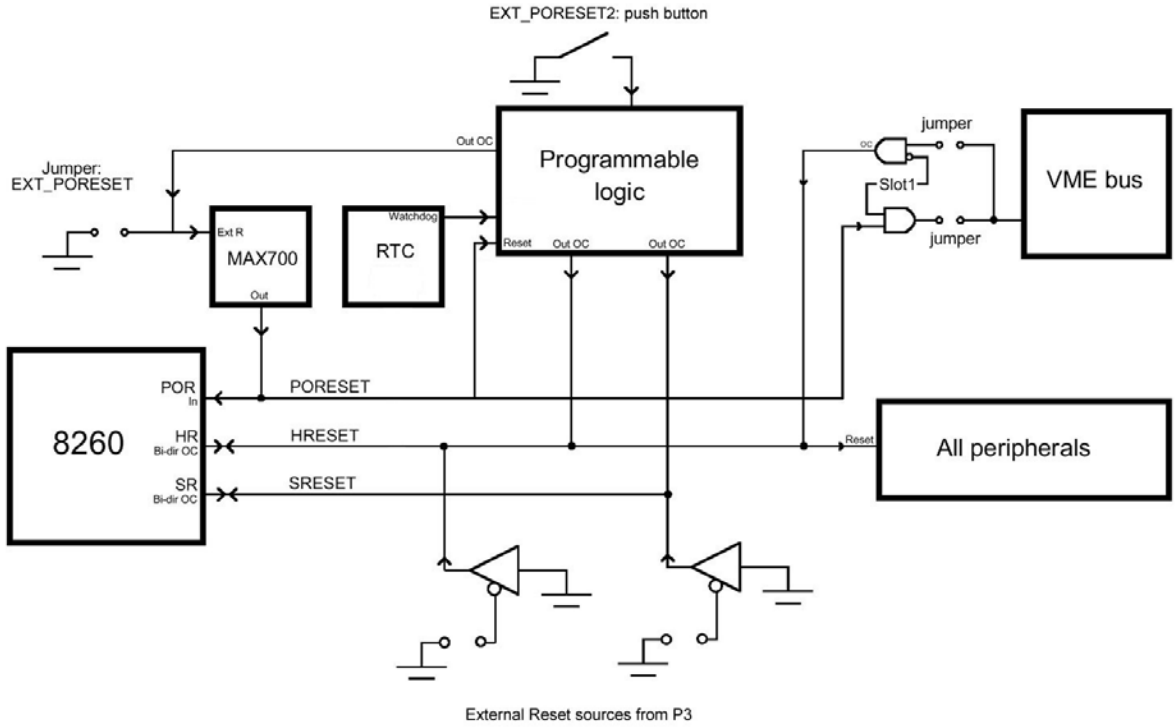


Figure 21: Reset scheme

The PORESET can be generated by:

- the VSBC-6862's power monitor (MAX700)
- the RTC's watchdog, depending of the SRESR register settings
- the push-button on front panel
- an external jumper
- a specific write operation in register of programmable logic

and is sent to:

- the PowerQUICC II
- the programmable logic
- the VME bus when board in not in slot 1 and specific jumper is installed

The HRESET can be generated by:

- a specific write operation in register of programmable logic
- the P3 connector

and is sent to:

- the PowerQUICC II
- all board's devices excepted the programmable logic and Flash devices
- the VME bus when board is in slot 1 and specific jumped is installed

The SRESET can be generated by:

- a specific write operation in register of programmable logic
- the P3 connector

and is sent to:

- the PowerQUICC II



The Flash memory is connected to his own Reset line commanded by the SRESR register. This memory is not connected to any other Reset signal.

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5.5. Power description

For the majority of the applications, the VSBC-6862 uses only the +5V power supply.
Internally, many modules use 3.3V, and the MPC-8260 use also 2.5 or 2.0V.
The internal 3.3V, and 2.5V or 2.0V voltages are generated on-board.

An internal power fail monitor generates a Power-On Reset signal when the +3.3V line fall below 2.97V.

The +12V is used for special protection feature on Flash memory (optional) and some IP modules.

The -12V is only used by some IP modules.

The +5V STDBY is used for the backup of the SRAM memory. (1MByte)
This line need 0.15 mA when the board is powered-on, and 0.5 mA when the board is powered-off.

All IP modules power lines are filtered, and fuse protected.
A power fail logic monitors if the +5V voltages are present on the IP slots.
If one of these voltages is not detected, the PowerLed on front panel is then OFF.
You have to check the cause of the problem and make the relevant correction.

5.6. Power consumption

This chapter will discuss of VSBC-6862 power consumption without IP modules.
Each IP module can consume 5V, +12V and/or -12V.

Device	Consumption 3.3V	Consumption 5V
MPC 8260 @ 200MHz	900	---
Programmable logic: 2 x Lattice	1100	---
Flash memory	200	---
SDRAM	500	---
SRAM	100	
Fast Ethernet transceivers	300	---
Communication port transceivers	400	---
Real Time Clock	60	---
VME and internal buffers	500	200
Oscillators	30	---
LEDs	64	---
Total	4154	200

For the 200MHz version:

Total estimated power = 4.154 x 3.3 + 0.200 x 5 = **14.7 W**

Typical measured power, running ECMon, no activity = 1.8 x 5 = 9 W

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5.7. MPC-8260 I/O ports assignment

The MPC-8260 processor provides four I/O ports (A, B, C and D) which have the abilities for handling several hardware functions like serial communication interfaces, DMA control handling and general purpose I/Os.

MPC-8260				Peripheral function	
I/O	**Function**	**I/O**		**Signal**	**Description**
SMC1					
PD9	SMTXD1	O		TxD	Transmit data
PD8	SMRXD1	I		RxD	Receive data
SMC2					
PA9	SMTXD2	O		TxD	Transmit data
PA8	SMRXD2	I		RxD	Receive data
SCC1					
PD30	TXD1	O		TxD	Transmit data
PD31	RXD1	I		RxD	Receive data
PD29	RTS1	O		RTS	Request to send
PC15	CTS1	I		CTS	Clear to send
PA22	PA22	O		DTR	Data terminal ready
PC14	CD1	I		DCD	Data carrier detect
PC31	BRG1	O		TxC	Transmit clock
PC29	CLK3	I		RxC	Receive clock
SCC2					
PB12	TXD2	O		TxD	Transmit data
PB15	RXD2	I		RxD	Receive data
PD26	RTS2	O		RTS	Request to send
PC13	CTS2	I		CTS	Clear to send
PA23	PA23	O		DTR	Data terminal ready
PC12	CD2	I		DCD	Data carrier detect
PD17	BRG2	O		TxC	Transmit clock
PC28	CLK4	I		RxC	Receive clock
SCC3					
PB8	TXD3	O		TxD	Transmit data
PB14	RXD3	I		RxD	Receive data
PD23	RTS3	O		RTS	Request to send
PC11	CTS3	I		CTS	Clear to send
PA24	PA24	O		DTR	Data terminal ready
PC10	CD3	I		DCD	Data carrier detect
PC27	BRG3	O		TxC	Transmit clock
PC25	CLK7	I		RxC	Receive clock
SCC4					
PD21	TXD4	O		TxD	Transmit data
PD22	RXD4	I		RxD	Receive data
PD20	RTS4	O		RTS	Request to send
PC9	CTS4	I		CTS	Clear to send
PA25	PA25	O		DTR	Data terminal ready
PC8	CD4	I		DCD	Data carrier detect

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PD10	BRG4	O		TxC	Transmit clock
PC26	CLK6	I		RxC	Receive clock
Fast Ethernet port 1					
PB6	MII_MDC	O		ECMDC	data clock
PB7	MII_MDIO	I/O		MIIMDIO	data
PB26	MII_CRS	I		MIICRS	carrier sense
PB27	MII_COL	I		MIICOL	collision
PB29	MII_TX_EN	O		MIITXEN	transmission enable
PC19	CLK13	I		MII_TX_CLK	transmission clock
PB31	MII_TX_ER	O		ECTXER	transmit error
PB25	MII_TXD3	O		ECTXD3	transmit data
PB24	MII_TXD2	O		ECTXD2	transmit data
PB23	MII_TXD1	O		ECTXD1	transmit data
PB22	MII_TXD0	O		ECTXD0	transmit data
PB30	MII_RX_DV	I		ECRXDV	receive valid data
PC18	CLK14	I		MII_RX_CLK	receive clock
PB28	MII_RX_ER	I		ECRXER	receive error
PB18	MII_RXD3	I		ECRXD3	receive data
PB19	MII_RXD2	I		ECRXD2	receive data
PB20	MII_RXD1	I		ECRXD1	receive data
PB21	MII_RXD0	I		ECRXD0	receive data
PC4	IRQ2	I		IRQ	irq
Fast Ethernet port 2					
PB4	MII_MDC	O		ECMDC	data clock
PB5	MII_MDIO	I/O		MIIMDIO	data
PA30	MII_CRS	I		MIICRS	carrier sense
PA31	MII_COL	I		MIICOL	collision
PA28	MII_TX_EN	O		MIITXEN	transmission enable
PC21	CLK11	I		MII_TX_CLK	transmission clock
PA29	MII_TX_ER	O		ECTXER	transmit error
PA21	MII_TXD3	O		ECTXD3	transmit data
PA20	MII_TXD2	O		ECTXD2	transmit data
PA19	MII_TXD1	O		ECTXD1	transmit data
PA18	MII_TXD0	O		ECTXD0	transmit data
PA27	MII_RX_DV	I		ECRXDV	receive valid data
PC20	CLK12	I		MII_RX_CLK	receive clock
PA26	MII_RX_ER	I		ECRXER	receive error
PA14	MII_RXD3	I		ECRXD3	receive data
PA15	MII_RXD2	I		ECRXD2	receive data
PA16	MII_RXD1	I		ECRXD1	receive data
PA17	MII_RXD0	I		ECRXD0	receive data
PC6	IRQ1	I		IRQ	irq
I2C (on SEM)					
PD14	I2CSCL	O		I2CSCL	clock
PD15	I2CSDA	I/O		I2CSDA	data
DMA					
PC0	IDMA1: DREQ	I		DMARQ1	IDMA request
PC1	IDMA2: DREQ	I		DMARQ2	IDMA request
PA0	IDMA3: DREQ	I		DMARQ3	IDMA request

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PA5	IDMA4: DREQ	I		DMARQ4	IDMA request
PD6	IDMA1: DACK	I		DMACK1	IDMA acknowledge
PC3	IDMA2: DACK	I		DMACK2	IDMA acknowledge
PA2	IDMA3: DACK	I		DMACK3	IDMA acknowledge
PA3	IDMA4: DACK	I		DMACK4	IDMA acknowledge
PC22	IDMA1: DONE	I/O		DMADONE1	IDMA done
PC2	IDMA2: DONE	I/O		DMADONE2	IDMA done
PA1	IDMA3: DONE	I/O		DMADONE3	IDMA done
PA4	IDMA4: DONE	I/O		DMADONE4	IDMA done
RTC					
PD12	PD12	O		RTC_WDI	Watchdog signal to RTC
PC5	PC5	I		RTC_IRQ	IRQ from RTC
Auxiliary LEDs					
PC24	PC24	O		LED_AUX0	Auxiliary LED 0
PC30	PC30	O		LED_AUX1	Auxiliary LED 1
Reserved					
PA10	PA10	O		Clock	Reserved
PA11	PA11	O		Data In	Reserved
PA12	PA12	I		Data Out	Reserved
PA13	PA13	O		Mode	Reserved

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6
Board initialization

The VSBC-6862 must set up the specific hardware organization for the PowerQUICC II processor. This setup must be completed on software initialization to ensure an adequate operation.

Three steps are needed to initialize the board:

1) ResetWord configuration
2) 8260 internals registers configuration
3) 8260 internals registers board dependants and board registers configuration

The first step configures the 8260 low level functions like clocks configuration and pins multiplexing. The ResetWord is loaded by the 8260 from the boot Flash memory bank.
When the ResetWord is invalid in Flash memory, the VSBC-6862 must be started with the ResetConf jumper plugged-in in order to use the 8260 default ResetWord, and then the ResetWord can be programmed in the Flash memory through the JTAG port.
The ResetWord is stored in the first addresses in the Flash memory and can be modified like any data in Flash memory. This step is described below.

The second step configures the main 8260 functions like bus modes.
This is done writing internal registers in the 8260. The base address is defined by the ISB bits in the ResetWord. This base address can be modified later using the ISB bits in the IMMR register. This step is described below.

The third step is to configure the VSBC-6862 specific registers for purposes like memory control and pin multiplexing.
This is done programming registers with the values specified in this manual. These registers are described above in the corresponding peripherals chapters.



In the following descriptions, **bold** values are to be respected in order to obtain the board working correctly.

6.1. Clock configuration

The main clock is a 66 MHz crystal controlled oscillator. It is used for the external bus.
The PowerQUICC II uses this external bus frequency to create two internal clocks. One for the CPM and the other for the core. Internally, two multiplication factors are used to generated these internal clocks. To define these multiplication factors, two values called MODCK are to be fixed.
The first MODCK[1-3] bits are fixed by defining the levels on the corresponding pins. These pins are factory defined at 101 or 111 depending on the processor speed mounted.
The next MODCK_H bits are contained in the Reset Word (see below). ACTIS defined these bits at 0101.
It sets the CPM frequency at 133 MHz and the core frequency at 133 or 200 MHz, depending of the board version.

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6.2. Reset Word

The ResetWord is a 32 bits field read by the PowerQUICC II during Power-On sequence. This word set several important options for the hardware operations.

The Reset Word must be located in the bootable device, on the VSBC-6862, it will be in the Flash memory bank, at offset 0.

For the VSBC-6862, the ResetWord is recommended as:

Bit	Field	Value	Function	
0	EARB	**0**	Arbitration:	internal
1	EXMC	**0**	Memory controller:	internal
2	CDIS	**0**	Core:	active
3	EBM	**0**	Bus mode:	MPC-8260 mode
4-5	BPS	**11**	Boot port size:	32 bits
6	CIP	1	Exceptions addresses:	$000n nnnn
7	ISPS	0	Internal space port size:	not used
8-9	L2CPC	**10**	Pin mux:	BADDR
10-11	DPPC	00	Pin mux:	IRQ
12	Reserved	0	---	
13-15	ISB	111	Internal space address start:	$FFF0 0000
16	BMS	1	BR0[BA] for boot:	$0000 0000
17	BBD	0	Pin mux:	DBB
18-19	MMR	00	All external bus master:	not used
20-21	LBPC	00	Local bus pins as:	local bus
22-23	APPC	**10**	Pin mux:	BNKSEL
24-25	CS10PC	00	Pin mux:	CS10
26	Reserved	0	---	
27	Reserved	0	---	
28-31	MODCK_H	**0101**	Clock configuration: bus 66, CPM 133, core 133 or 200	

Then the Reset Word mapping in Flash memory is :

Byte 0, address $0000 = $0E
Byte 1, address $0008 = $87
Byte 2, address $0010 = $82
Byte 3, address $0018 = $05



If the two banks contains an invalid ResetWord, the ResetConf jumper (J2) can force the PowerQUICC II to uses his default ResetWord.
The ResetWord is then programmed through the JTAG port.



Some JTAG tools may need the CheckStop signal on the JTAG connector.
In this case, due to the 8260 pin multiplexing, the ResetWord must be modified with DPPC = 10 while using the JTAG tool.
For normal board use, keep the value 00.



Warning

The MODCK_H bits must be set to the described value.
If other values are set, the internal speeds can be higher than expected by the processor, and then it will heat more than acceptable thus can be destroyed.

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6.3. MPC-8260 internal registers

The MPC-8260 contains some registers to configure for correct operations.
Here follows the specific configuration of these registers for the VSBC-6862:

Internal Memory Map Register: IMMR

This register set the memory map for the MPC-8260 internal registers.

Bit	Field	Value	Function	
0-14	ISB	$XXXY	Internal space base:	user defined
15	Reserved	0	---	
16-23	Partnum	$00	Part number, read only:	$00 = MPC-8260
24-31	Masknum	$xx	Mask number, read only:	mask number

Typical value: IMMR = $XXXX0000

Bus Configuration Register: BCR

This register configures various features on the PQII, and is mainly already defined by the ResetWord.

Bit	Field	Value	Function	
0	EBM	**0**	External bus mode:	single MPC8260 mode
1-3	APD	0	Address phase delay:	0
4	L2C	**0**	Secondary cache:	no
5-7	L2D	00	L2 cache hit delay:	0
8	PLDP	0	Pipeline max. depth:	0
9	EAV	0	Enable address visibility:	no
10-11	Reserved	00	---	
12	ETM	0	Extended transfer mode:	disabled
13	LETM	0	Local bus extended mode:	disabled
14	EPAR	0	Even parity:	no
15	LEPAR	0	Local bus even parity: no	
16-18	NPQM	0	Non PQII master:	no
19-20	Reserved	00	---	
21	EXDD	0	Ext. master delay disable:	no
22-26	Reserved	00000	---	
27	ISPS	0	Int. space port size:	64 bits
28-31	Reserved	0000	---	

Typical value: BCR = $00000000

60x bus Arbiter Configuration Register: PPC_ACR

This register defines the arbiter modes and parked master for the 60x bus. These bits are already defined in the ResetWord.

Bit	Field	Value	Function	
0-1	Reserved	00	---	
2	DBGD	0	Data bus grant delay:	DBG asserted with TS
3	EARB	**0**	External arbitration:	internal
4-7	PRKM	0000	Parking master:	CPM high level

Typical value: PPC_ACR = $00

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SIU Module Configuration Register: SIUMCR

This register contains bits that configure various features in the SIU module.

Bit	Field	Value	Function	
0	BBD	0	Bus busy disable:	pin is DBB
1	ESE	1	External snoop enable:	pin is GBL
2	PBSE	0	Parity byte select enable:	disable, pin as GPL4
3	CDIS	**0**	Core disable:	core enabled
4-5	DPPC	**00**	Data parity pin config:	pins are IRQ
6-7	L2CPC	10	L2 cache pin config:	pins are BADDR
8-9	LBPC	00	Local bus pin config:	pins are local bus
10-11	APPC	**10**	Address pin parity config:	pin are BNKSEL
12-13	CS10PC	00	Chip select 10 config:	pin is CS10
14-15	BCTLC	**00**	Buffer control BCTLx pins cfg:	BCTL0 = /Read
16-17	MMR	00	Mask masters request:	no mask
18	LBPSE	0	Local bus parity byte select:	disabled
19-31	Reserved	0000000000000	---	

Typical value: SIUMCR = $42200000

System Protection Control Register: SYPCR

This register controls the system monitors, software watchdog, and bus monitor timing.
SYPCR can be read at any time but can be written only once after system reset.

Bit	Field	Value	Function	
0-15	SWTC	$FFFF	Software watchdog timer count	
16-23	BMT	**11111111**	Bus monitor timing:	30us
24	PBME	**1**	60x bus monitor enable:	enabled
25	LBME	**0**	local bus monitor enable:	disabled
26-28	Reserved	000	---	
29	SWE	0	Software watchdog enable:	disabled
30	SWRI	0	Software watchdog reset/interrupt	
31	SWP	0	Software watchdog prescaler	

Typical value: SYPCR = $FFFFFF80



All reserved fields in the above registers should be cleared when writing.

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6.4. MPC-8260 I/O ports

The PowerQUICC II contains 120 I/O pins that are used for communication ports and general purpose I/Os. Many different functions are multiplexed on I/O pins, and need to be defined depending on the board configuration.

For the VSBC-6862, the I/O pins have to be defined as:

I/O	Function	PPARA	PDIRA	PODRA	PSORA
PA0	IDMA3_DREQ	1	0	0	1
PA1	IDMA3_DONE	1	0	1	1
PA2	IDMA3_DACK	1	1	0	1
PA3	IDMA4_DACK	1	1	0	1
PA4	IDMA4_DONE	1	0	1	1
PA5	IDMA4_DREQ	1	0	0	1
PA6	not used	0	1	0	0
PA7	not used	0	1	0	0
PA8	SMC2_RXD	1	0	0	0
PA9	SMC2_TXD	1	1	0	0
PA10	Rsrv1_CK	0	1	0	0
PA11	Rsrv2_IN	0	1	0	0
PA12	Rsrv3_OUT	0	0	0	0
PA13	Rsrv4_MOD	0	1	0	0
PA14	FCC1_MII_RXD3	1	0	0	0
PA15	FCC1_MII_RXD2	1	0	0	0
PA16	FCC1_MII_RXD1	1	0	0	0
PA17	FCC1_MII_RXD0	1	0	0	0
PA18	FCC1_MII_TXD0	1	1	0	0
PA19	FCC1_MII_TXD1	1	1	0	0
PA20	FCC1_MII_TXD2	1	1	0	0
PA21	FCC1_MII_TXD3	1	1	0	0
PA22	SCC1_DTR	0	1	0	0
PA23	SCC2_DTR	0	1	0	0
PA24	SCC3_DTR	0	1	0	0
PA25	SCC4_DTR	0	1	0	0
PA26	FCC1_MII_RX_ER	1	0	0	1
PA27	FCC1_MII_RX_DV	1	0	0	1
PA28	FCC1_MII_TX_EN	1	1	0	1
PA29	FCC1_MII_TX_ER	1	1	0	1
PA30	FCC1_MII_CRS	1	0	0	1
PA31	FCC1_MII_COL	1	0	0	1
I/O	**Function**	**PPARB**	**PDIRB**	**PODRB**	**PSORB**
PB4	FCC1_MII_MDC	0	0	0	0
PB5	FCC1_MII_MDIO	0	0/1	0	0
PB6	FCC2_MII_MDC	0	0	0	0
PB7	FCC2_MII_MDIO	0	0/1	0	0
PB8	SCC3_TXD	1	1	0	1
PB9	not used	0	1	0	0
PB10	not used	0	1	0	0
PB11	not used	0	1	0	0

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PB12	SCC2_TXD	1	1	0	1
PB13	not used	0	1	0	0
PB14	SCC3_RXD	1	0	0	0
PB15	SCC2_RXD	1	0	0	0
PB16	not used	0	1	0	0
PB17	not used	0	1	0	0
PB18	FCC2_MII_RXD3	1	0	0	0
PB19	FCC2_MII_RXD2	1	0	0	0
PB20	FCC2_MII_RXD1	1	0	0	0
PB21	FCC2_MII_RXD0	1	0	0	0
PB22	FCC2_MII_TXD0	1	1	0	0
PB23	FCC2_MII_TXD1	1	1	0	0
PB24	FCC2_MII_TXD2	1	1	0	0
PB25	FCC2_MII_TXD3	1	1	0	0
PB26	FCC2_MII_CRS	1	0	0	0
PB27	FCC2_MII_COL	1	0	0	0
PB28	FCC2_MII_RX_ER	1	0	0	0
PB29	FCC2_MII_TX_EN	1	1	0	1
PB30	FCC2_MII_RX_DV	1	0	0	0
PB31	FCC2_MII_TX_ER	1	1	0	0
I/O	**Function**	**PPARC**	**PDIRC**	**PODRC**	**PSORC**
PC0	IDMA1_DREQ	1	0	0	0
PC1	IDMA2_DREQ	1	0	1	0
PC2	IDMA2_DONE	1	0	1	1
PC3	IDMA2_DACK	1	1	0	1
PC4	FCC2_IRQ2	0	0	0	0
PC5	RTC_IRQ	0	0	0	0
PC6	FCC1_IRQ1	0	0	0	0
PC7	not used	0	1	0	0
PC8	SCC4_CD	1	0	0	0
PC9	SCC4_CTS	1	0	0	0
PC10	SCC3_CD	1	0	0	0
PC11	SCC3_CTS	1	0	0	0
PC12	SCC2_CD	1	0	0	0
PC13	SCC2_CTS	1	0	0	0
PC14	SCC1_CD	1	0	0	0
PC15	SCC1_CTS	1	0	0	0
PC16	not used	0	1	0	0
PC17	not used	0	1	0	0
PC18	FCC2_RXCLK	1	0	0	0
PC19	FCC2_TXCLK	1	0	0	0
PC20	FCC1_RXCLK	1	0	0	0
PC21	FCC1_TXCLK	1	0	0	0
PC22	IDMA1_DONE	1	0	1	1
PC23	not used	0	1	0	0
PC24	LED_AUX0	0	1	0	0
PC25	SCC3_RXCLK	1	0	0	0
PC26	SCC4_RXCLK	1	0	0	0
PC27	SCC3_TXCLK	1	1	0	1
PC28	SCC2_RXCLK	1	0	0	0
PC29	SCC1_RXCLK	1	0	0	0

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PC30	LED_AUX1	0	1	0	0
PC31	SCC1_TXCLK	1	1	0	0
I/O	**Function**	**PPARD**	**PDIRD**	**PODRD**	**PSORD**
PD4	not used	0	1	0	0
PD5	not used	0	1	0	0
PD6	IDMA1_DACK	1	1	0	1
PD7	not used not used	0	1	0	0
PD8	SMC1_RXD	1	0	0	0
PD9	SMC1_TXD	1	1	0	0
PD10	SCC4_TXCLK	1	1	0	1
PD11	not used	0	1	0	0
PD12	RTC_WDI	0	1	0	0
PD13	not used	0	1	0	0
PD14	I2C_SCL	1	0	1	1
PD15	I2C_SDA	1	0	1	1
PD16	not used	0	1	0	0
PD17	SCC2_TXCLK	1	1	0	0
PD18	not used	0	1	0	0
PD19	not used	0	1	0	0
PD20	SCC4_RTS	1	1	0	0
PD21	SCC4_TXD	1	1	0	0
PD22	SCC4_RXD	1	0	0	0
PD23	SCC3_RTS	1	1	0	0
PD24	not used	0	1	0	0
PD25	not used	0	1	0	0
PD26	SCC2_RTS	1	1	0	0
PD27	not used	0	1	0	0
PD28	not used	0	1	0	0
PD29	SCC1_RTS	1	1	0	0
PD30	SCC1_TXD	1	1	0	1
PD31	SCC1_RXD	1	0	0	0

Typical values:

```
PPARA  =  $FCC3FC3F
PDIRA  =  $33743FCC
PODRA  =  $48000000
PSORA  =  $FC00003F
PPARB  =  $008B3FFF
PDIRB  =  $0FFCC3C5
PODRB  =  $00000000
PSORB  =  $00880004
PPARC  =  $F0FF3E7D
PDIRC  =  $1100C193
PODRC  =  $60000200
PSORC  =  $30000210
PPARD  =  $02E34F27
PDIRD  =  $0F7CFDFE
PODRD  =  $00030000
PSORD  =  $02230002
```


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6.5. Chip select

Before accessing a internal peripheral, the corresponding chip select must be initialized.

The description of all chip select initializations are described in the Software description.

It's important to note the order in which OR0 and BR0 are programmed. When coming out of reset and CS0 is the global chip select, OR0 MUST be programmed AFTER BR0. In all other cases BRx would be programmed after ORx.

Note that for SDRAM, some registers are to be programmed in addition to the chip select. These registers initialization are described in the corresponding chapter.

6.6. Serial EEPROM

The VSBC-6862 provides one on-board serial EEPROM on the I^2C bus which handle most of the configuration attributes.

General Information Format

Field	Offset	Size	Values
Magic Cookie	$00	8	$41 $43 $54 $49 $53 $00 $00 $00 ("ACTIS")
Size of EEPROM	$08	2	$01 $00
Reserved	$0A	4	$00 $00 $00 $00
Date	$0E	2	YY MM (BCD Format)
Options	$10	240 max	XX

Options may be fixed length or variable length. All options begin with a tag octet, which uniquely identifies the option (values 128 to 254 are reserved for user). Fixed-length options without data consist of only a tag octet. Only options 0 and 255 are fixed length. All other options are variable-length with a length octet following the tag octet. The value of the length octet does not include the two octets specifying the tag and length. The length octet is followed by "length" octets of data. In the case of some variable-length options the length field is a constant but must still be specified.

Pad Option

The pad option can be used to cause subsequent fields to align on word boundaries.
The code for the pad option is 0, and its length is 1 octet.
E.g.: $00

End Option

The end option marks the end of valid information in the vendor field. Subsequent octets should be filled with pad options.
The code for the end option is 255, and its length is 1 octet.
E.g.: $FF

Product Identifier Option (optional)

This option specifies the name of the product (ASCII terminated by a zero byte).
The code for this option is 1, and its minimum length is 1.
E.g.: $01 $0E 'V' 'S' 'B' 'C' '-' '6' '8' '6' '2' '/' '0' '0' '0' $00

Factory Identifier Option (optional)

This option specifies the name of the product in factory (ASCII terminated by a zero byte).
The code for this option is 2, and its minimum length is 1.
E.g.: $02 $02 '?' $00

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Serial Number Option (optional)
This option specifies the serial number of the product (ASCII terminated by a zero byte).
The code for this option is 3, and its minimum length is 1.
E.g.: $03 $06 'P' 'R' 'O' 'T' 'O' $00

Revision Option (optional)
This option specifies the revision / version of the board.
The code for this option is 8, and its length is 2 (Revision/Edition).
E.g.: $08 $02 $01 $00

MPU Type Option (optional)
This option specifies the name of the processor (ASCII terminated by a zero byte).
The code for this option is 32, and its minimum length is 1.
E.g.: $20 $0B 'P' 'P' 'C' '8' '6' '0' 'T' '-' '4' '0' $00

MPU Clock Speed Option
This option specifies the output clock speed in hertz (4 Bytes, MSB first).
The code for this option is 33, and its length is 4.
E.g.: $21 $04 $02 $62 $5A $00

Dynamic RAM Option
This option specifies the dynamic RAM configuration (binary code which can prevent use of SDRAM).
E.g.: $30 $04 $3F $8A $04 $06

Static RAM Option (optional)
This option specifies the static RAM configuration (binary code).
The code for this option is 52, and its length is 4.
E.g.: $34 $04 $00 $12 $E3 $00

EPROM Option (optional)
This option specifies the EPROM configuration (binary code).
The code for this option is 56, and its length is 4.
E.g.: $38 $04 $04 $2E $51 $0F

Flash Memory Option (optional)
This option specifies the Flash memory configuration (binary code).
The code for this option is 60, and its length is 4.
E.g.: $3C $04 $00 $71 $58 $5A

IP Interface Option (optional)
This option specifies the IP interface configuration (binary code).
The code for this option is 64, and its length is 4.
E.g.: $40 $04 $00 $00 $05 $03

VME Interface Option (optional)
This option specifies the VME interface configuration (binary code).
The code for this option is 66, and its length is 4.
E.g.: $42 $04 $00 $00 $00 $00

Ethernet Address #1 Option (optional, first Ethernet devices)
This option specifies the first Ethernet address (6 Bytes, MSB first).
The code for this option is 112, and its length is 6.
E.g.: $70 $06 $00 $20 $15 $00 $00 $00

Ethernet Address #2 Option (optional, second Ethernet devices)
This option specifies the second Ethernet address (6 Bytes, MSB first).
The code for this option is 113, and its length is 6.
E.g.: $71 $06 $00 $20 $15 $00 $00 $01

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6.7. Boot code

The boot code is mapped as standard PowerPC map.

The exception table is located from offset $0100 to $2FFF.
With the offset $0100 corresponding to the System Reset Exception.
Thus the boot code will start at the offset $0100 of the bootable Flash memory bank.

The addresses below $0100 are reserved for the PowerQUICC II reset configuration.

By default, the VSBC-6862 is provided with one Flash memory bank factory loaded with the ECMon debugger.
Detailed information can be found in the Annex, chapter ECMon.

If ECMon is not needed , all addresses above $0100 thus are available for user purposes: main code, user data, etc...



Please see the PowerPC EC603 user's manual for more information.

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7
Registers definition

IPGCRA CS4 + $401	*IP General Configuration Register A*	RW
IPGCRB CS4 + $501	*IP General Configuration Register B*	RW
IPGCRC CS4 + $601	*IP General Configuration Register C*	RW
IPGCRD CS4 + $701	*IP General Configuration Register D*	RW

These registers permit to configure general purposes for IP slot x.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	x	PF5V	ENIRQ	x
Default	x	x	x	x	x	0	0	x

With:

ENIRQ	Enable IRQ
0	Interrupt from IP to processor are disabled
1	Interrupt from IP to processor are enabled

PF5V	Power Fail on IP 5V
0	5V is present on IP slots
1	5V is not present on IP slots, check fuses

Note: This bit is read only

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IPDCRA *IP DMA Configuration Register A* RW
CS4 + $403

IPDCRB *IP DMA Configuration Register B* RW
CS4 + $503

IPDCRC *IP DMA Configuration Register C* RW
CS4 + $603

IPDCRD *IP DMA Configuration Register D* RW
CS4 + $703

These register permits to configure the DMA access for IP slot x.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	x	x	ENDMA	DMASRC
Default	x	x	x	x	x	x	0	0

With:

ENDMA	Enable DMA
0	DMA for IP x is disabled
1	DMA for IP x is enabled

DMASRC	DMA Source
0	DMA source is IP x DREQ0
1	DMA source is IP x DREQ1



When ENDMA in the register IPDCRB is set, the Transmit Clock line for the serial port 4 is not accessible.

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IPIVRA *IP Interrupt Vector Register A* RO
CS4 + $481

IPIVRB *IP Interrupt Vector Register B* RO
CS4 + $581

IPIVRC *IP Interrupt Vector Register C* RO
CS4 + $681

IPIVRD *IP Interrupt Vector Register D* RO
CS4 + $781

These registers permit to acknowledge the IRQ for IP slot x.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	V7	V6	V5	V4	V3	V2	V1	V0
Default	0	0	0	0	0	0	0	0

With: V[7:0]: This 8-bit value represents the interrupt vector provided by the IP module during the interrupt acknowledge cycle.

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SRESR *Software Reset Register* WO
CS4 + $1001
VME slave + $9

This register permits to perform Software or Hardware Reset by software

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	R0	R1	R2	R3
Default	x	x	x	x	0	0	0	0

Writing this register with the value $1 'connects' the RTC's Watchdog pin to the Power-On Reset
Writing this register with the value $3 generates a Reset on Flash Devices
Writing this register with the value $6 generates a Hardware Reset on board.
Writing this register with the value $9 generates a Software Reset on board.
Writing this register with the value $A resets the VME interrupter. The VME interrupt is deactivated.
Writing this register with the value $C generates a Power-On Reset on board.



All reset commands, except for the Flash, are automatically cleared after completion.
The Reset for the Flash memory stays active until its corresponding bits are cleared by software.

SWPR *Switch Position Register* RO
CS4 + $1011

This register permits to read the state of the external rotary switch

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	x	RC2	RC1	RC0
Default	x	x	x	x	x	0	0	0

With:
RC0, RC1, RC2: position binary coded of the eight position switch

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BSCR *Board Special Configuration Register* RW
CS4 + $1021

This register permits to access the protection purpose of the Flash memory.
This option is available on request.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	FLPROT	x	Local_rmw	x	x	x	x	x
Default	0	x	0	x	x	x	x	x

With:

FLPROT	Release Mode
0	Normal operation
1	Put 12V on the Flash memory Reset pin to protect/unprotect sectors, please see Flash memory datasheet

Local_rmw	Local Read-Modify-Write cycle on shared memory
0	Normal operation, the Flash, RTC and SRAM are shared
1	Local exclusive access: the Flash, RTC and SRAM are accessible only by the 8260.



Warning

The 'local-RMW' cycle is not time-limited. If the function is not released before the VME bus timeout, and an external VME master is waiting on this VME slave Window, this will create an VME bus error. Thus please use the minimum number of cycles between the activation and the deactivation of this function.

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VMBA *VME Master Bus Access* RW
CS4 + $1051

This register permits to select the mode for VME bus access and release

	D8	D9	D10	D11	D12	D13	D14	D15
Value	RM	RL1	RL0	x	x	x	x	x
Default	1	1	1	x	x	x	x	x

With:

RL1	RL0	Request Level
0	0	Bus Request 0
0	1	Bus Request 1
1	0	Bus Request 2
1	1	Bus Request 3

RM	Release Mode
0	Release On Request
1	Release When Done

VAM *VME Arbiter Mode* RW
CS4 + $1053

This register permits to select the arbiter mode when board is in Slot1 mode

	D8	D9	D10	D11	D12	D13	D14	D15
Value	VAM1	VAM0	x	x	x	x	x	x
Default	0	1	x	x	x	x	x	x

With:

VAM1	VAM0	Arbiter Mode
0	0	SGL: Single Level, only level 3 arbitration
0	1	PRI: Priority, the level 3 is as the higher priority
1	0	RRS: Round-Robin: the levels rotates between lines
1	1	reserved



Please modify this register when no activity on the bus.
Modifying Arbiter Mode when activity in VME bus may cause erratic results.

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VMBMA *VME Master: A32 Base address for window A* RW
CS4 + $1055

VMBMB *VME Master: A32 Base address for window B* RW
CS4 + $1057

These register permit to complete the high order address for accesses in A32 mode.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	VA31	VA30	VA29	VA28	VA27	VA26	VA25
Default	x	0	0	0	0	0	0	0

With: VA31: VME address A31
..
VA25: VME address A25

VMAMA *VME Master: AM for window A* RW
CS4 + $105b

VMAMB *VME Master: AM for window B* RW
CS4 + $105d

These registers permit to complement the Address Modifiers (AM) for VME accesses and define the Data mode for VME access.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	AM2	AM1	AM0	x	x	x
Default	x	x	0	0	1	x	x	x

With: AM2: VME address modifier 2
..
AM0: VME address modifier 0

By default, the AM codes corresponds to non-privileged access.
For supervisor access, AM codes have to be modified from 0 0 1 to 1 0 1.

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VHIL *VME interrupt Handler: Interrupt Level* RO
CS4 + $1061

This register indicates the current VME interrupt level to acknowledge by reading the corresponding VHV register.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1
Default	x	x	x	x	x	x	x	x

With: IRQ1: VME interrupt request level 1
... ...
IRQ7: VME interrupt request level 7



This register always indicates the current VME IRQ Level, even masked interrupts.

VHM *VME interrupt Handler Mask* RW
CS4 + $1063

This register is used to mask incoming interrupt requests coming from VME bus.

	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	M7	M6	M5	M4	M3	M2	M1
Default	x	1	1	1	1	1	1	1

With:

Mx	Interrupt Mask
0	IRQx is enabled
1	IRQx is masked

When an IRQ is masked:
- no local IRQ is generated to the MPC8260.
- reading the corresponding VHV register does not acknowledge the VME IRQ

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VHV *VME Interrupter Vector* RO
CS4 + $1073 to CS4 + $107f

When accessed, this register acknowledges the corresponding VME interrupt as:

VME IRQ to acknowledge	VHV address
1	CS4 + $1072
2	CS4 + $1074
3	CS4 + $1076
4	CS4 + $1078
5	CS4 + $107a
6	CS4 + $107c
7	CS4 + $107e

Value:

	D8	D9	D10	D11	D12	D13	D14	D15
Value	V7	V6	V5	V4	V3	V2	V1	V0
Default	x	x	x	x	x	x	x	x

With: V0-V7: Vector



Reading this register initiates a Interrupt Acknowledge cycle only if corresponding interrupt is not masked.
Reading this register when no IRQ is pending, is not allowed

VINTER *VME Interrupter command register* WO
CS4 + $1067

This register generates the corresponding VME IRQ.

8260	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	x	x	x	x
Default	x	x	x	x	x	x	x	x

Writing any value to this register will generate an IRQ to the VME bus.
The IRQ level is defined by the VIVEC[ILx] bits described above in this chapter.
The IRQ is automatically cleared when the interrupt acknowledge cycle is completed.
For debug purposes, the SRESR register can be used to manually clear this interrupt.

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VIVEC *VME Interrupter Vector* RW
CS4 + $106d
VME slave + 7

This register contains IRQ level and the vector sent by the VME interrupter.

8260	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	IL2	IL1	IL0	Vec4	Vec3	Vec2	Vec1	Vec0
Default	0	0	0	0	0	0	0	0

With: IL2-IL0: IRQ level coded on 3 bits. IRQ level = 0 implies that no IRQ will be sent when writing the VINTER register
Vec4-Vec0: Low order bits of the vector sent by the interrupter during interrupt-acknowledge cycle. High order bits are IRQ level acknowledged coded on 3 bits.


Warning

This register is accessible from both VME bus and local processor.
The user must choose that this register is accessed by either VME either local processor, but never both at the same time.

VSMAIL *VME Slave Mailbox* WO
CS4 + $1065
VME slave + 1

This register implements a single mailbox.

8260	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	x	x	x	x	x	x	x	x
Default	x	x	x	x	x	x	x	x

When an external VME master writes any value in this register, and the VSBA24[MailOn] bit is set, an IRQ6 is sent to the MPC-8260.
To clear this interrupt, the MPC-8260 must write any value to this register.

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VSBA24 *VME Slave Base Window A24* RW
CS4 + $1069
VME slave + 3

This register sets the VME base address for the visible A24 memory window.

8260	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	WinA24On	MailOn	VME_rmw	x	A23	A22	A21	A20
Default	0	0	x	x	0	0	0	0

With:

A23	A22	A21	A20	VME Slave Base Address
0	0	0	0	$00'0000
0	0	0	1	$10'0000
0	0	1	0	$20'0000
0	0	1	1	$30'0000
0	1	0	0	$40'0000
0	1	0	1	$50'0000
0	1	1	0	$60'0000
0	1	1	1	$70'0000
1	0	0	0	$80'0000
1	0	0	1	$90'0000
1	0	1	0	$A0'0000
1	0	1	1	$B0'0000
1	1	0	0	$C0'0000
1	1	0	1	$D0'0000
1	1	1	0	$E0'0000
1	1	1	1	$F0'0000

WinA24On	Activation of the A24 Window
0	The VME A24 slave window is inactive
1	The VME A24 slave window is active

MailOn	Activation of the Mailbox function
0	An access to the Mailbox did not generates an IRQ
1	An access to the Mailbox generates an local IRQ

VME_rmw	Activation of the 'pseudo RMW' cycles
0	normal VME accesses
1	'pseudo-RMW' VME accesses: BBSY and AS will not be released



Warning

This register is accessible from both VME bus and local processor.
The user must choose that this register is accessed by either VME either local processor, but never both at the same time.



Warning

The 'pseudo-RMW' cycle is not time-limited. If the bus has not been released between either the VME bus timeout, either the local slave's timeout, it will create respectively either VME bus errors for the other VME masters, either local bus error on the slave. Thus please use the minimum VME cycles between the activation and the deactivation of this function.

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VSWA24 *VME Slave Window A24 management* RW
CS4 + $106b
VME slave + 5

This register contains the local offsets for the VME A24 window.

8260	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	x	SRA19	x	FLA22	FLA21	FLA20	FLA19	FLA18
Default	x	0	x	0	0	0	0	0

With: SRA19: corresponding high order local address for SRAM memory.
FLA18-FLA22: corresponding high order local addresses for Flash memory.


Warning

This register is accessible from both VME bus and local processor.
The user must choose that this register is accessed by either VME either local processor, but never both at the same time.

Conventions:

x: not used, undefined
WO: write only
RO: read only
RW: read and write

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8 Characteristics

Electrical characteristics

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY				
+5 V (VDD)	4.5 V	-	5.5	V
+12 V	10.8	-	13.2	V
-12 V	-13.2	-	-10.8	V
Input voltage	GND-0.3	-	VDD+0.3	V
Operating Power supply current				
Icc_{+5V} (without IP modules)	-	1800	-	mA
Icc_{+12V} (only used by IP modules and Flash protection)	-	TBD	-	mA
Icc_{-12V} (only used by IP modules)	-	---	-	mA

Environmental characteristics

PARAMETER	MAX
Operating	
Temperature	0° C to +70° C forced air cooling exit air
Altitude	5,000 m
Humidity (NC)	10% to 80%
Vibration	2 Gs RMS, 20–2000 Hz Random
Non-Operating	
Temperature	–40° C to +100° C
Altitude	15,000 m
Humidity (NC)	10% to 90%
Vibration	6 Gs RMS, 20–2000 Hz Random

Mechanical characteristics

PARAMETER	MAX
Height	233.4 mm (9.2 in.)
Depth	160.0 mm (6.3 in.)
Front Panel Height	261.8 mm (10.3 in.)
Width	19.8 mm (0.8 in.)
Max. Comp, Height	13.7 mm (0.54 in.)

General characteristics

PARAMETER	MAX
MTBF calculated with 90% confidence	160,000 hours

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Performance issues

The VSBC-6862 has been designed for providing efficient performance with peripheral connected around the PowerQUICC II processor.
The following table provides the respective wait states that should be expected for each access type.

Conditions: MPC-8260 @ 200 MHz

Access	Number of cycles
FLASH	
Read cycle single beat	TBD
SDRAM	
Read cycle single beat	TBD
Write cycle single beat	TBD
Read cycle burst (4 transfers)	TBD
Write cycle burst (4 transfers)	TBD
IP module, 8 MHz mode, memory space	
Read cycle single beat	TBD
Write cycle single beat	TBD
IP module, 8 MHz mode, other spaces	
Read cycle single beat	TBD
Write cycle single beat	TBD
Board registers	
Read cycle single beat	TBD
Write cycle single beat	TBD

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9 Physical board definition

9.1. PCB dimensions

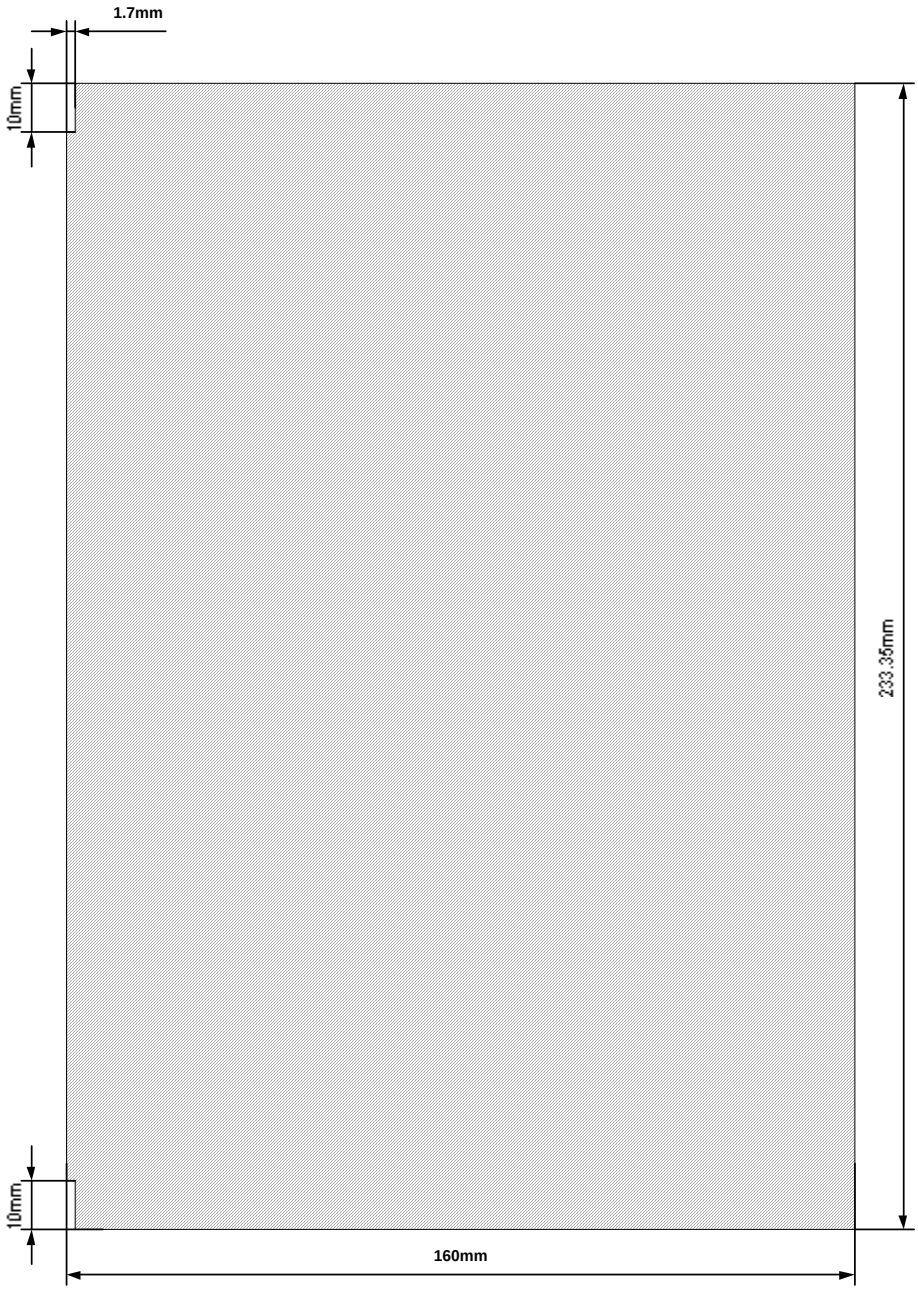


Figure 22: PCB dimensions

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9.2. Front panel

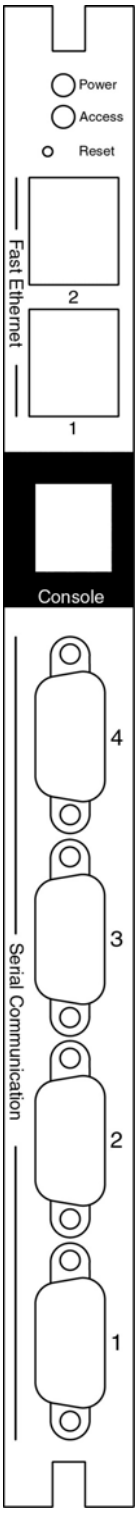


Figure 23: Front panel

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10 Software available

Thanks to ECRIN Automatismes, many software packages are already available for the VSBC-6862. ECRIN is our sister company and work together with ACTIS to provide full solution to our customers.
All software requests can be directly addressed at ECRIN. (see chapter Technical support)



10.1. Debug tools

Many debug tools are available for debugging.
These tools use the JTAG port of the 8260 to access low level resources.
Please refer to the Motorola's web page for the 8260 to find a list of third-party products.

However, a monitor is already installed on the VSBC-6862.
This monitor can also be used for debug purposes, see next chapter.

10.2. ECMON

The VSBC-6862 is provided with an pre-loaded monitor in Flash memory.
This monitor is a courtesy from ECRIN Automatismes, and this free version will not be supported by ECRIN Automatismes.
An extended version is also available at ECRIN Automatismes, which can provide more functions like auto-boot facilities.

This monitor will permit to directly load and execute user's programs without need of third-party tools.

The monitor provides the following main functions:

- memory read, write, fill
- serial load
- flash utilities
- real time device management

To access this monitor, connect a terminal to the front panel Console connector: P13.
The terminal must be set to the following parameters:

speed	9600 bit/s
data bits	8
stop bits	1
parity	none
handshake	none

When the VSBC-6862 boot, the following message will comes:

```
VSBC-6862 System Boot Vx.y
Copyright 2000 by ECRIN Automatismes.
```


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The boot time is less then 1 second.

Then, when typing the 'Return' key, the '**ECMon>**' prompt will be displayed.

The default radix for all commands is hexadecimal.
You can use an explicit prefix to specify the radix as:

hexadecimal	0x
decimal	0d
binary	0b
ASCII	'

The last command can be recalled typing the 'Control-A' sequence.
The command line can be erased typing the 'Control-X' sequence.

10.2.1. Command description

All current commands are described here in alphabetic order.
Some commands can be added or modified after releasing this manual and can be found and explained with the on-line ECMon's help menu.

env

Function : Create, modify or remove environment variable
Syntax : env [<name> [<value>]]
Options : <name> - name of environment variable
<value> - value of environment variable

eflash

Function : Erase flash memory
Syntax : eflash <address> [<count>]
Options : <address> - starting address
<count> - memory size to erase

help

Function: Display help
Syntax : help { <keyword> }
Options : <keyword> - to get help on specified command

Without parameter, displays the general help menu.
With the parameter command name, display the specific command help.

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i2c

Function : Read or write data from/to an I2C device
Syntax : i2c <device> <offset> <count> <address>
Options : <device> - I2C device address
<odd value> to read
<even value> to write
<offset> - starting I2C memory offset
<count> - number of data items to copy
<address> - local memory address

go

Function : Execute user program
Syntax : go <address>
Options : <address> - external routine entry

mcb, mcw, mcl

Function : Copy the contents of memory to another
Syntax : mcb <source> <count> <destination>
Options : <source> - starting source address
<count> - number of data items to copy
<destination> - starting destination address

mcb uses a byte-value
mcw uses a short-value
mcl uses a long value

mdb, mdw, mdl

Function : Displays the contents of memory (byte-value)
Syntax : mdb <address> [<count>]
Options : <address> - starting address
<count> - number of data items to display
(default is 0x0100)

mdb uses a byte-value
mdw uses a short-value
mdl uses a long value

mfb, mfw, mfl

Function : Fill the memory with a specific data (byte-value)
Syntax : mfb <address> <count> <value>
Options : <address> - starting address
<count> - number of data items to fill
<value> - value of specific data

mfb uses a byte-value
mfw uses a short-value
mfl uses a long value

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mmap

Function : Display memory map
Syntax : mmap

mmb, mmw, mml

Function : Modify the contents of memory (byte-value)
Syntax : mmb <address> [{ <value> | <keyword> }]
Options : <address> - starting address
<value> - data items
<keyword> - '+' to go on next address
- '-' to go on previous address
- '.' to exit

mmb uses a byte-value
mmw uses a short-value
mml uses a long value

mii

Function : Read or write a PHY register
Syntax : mii <device> <register> [<value>]
Options : <device> - Fast-Ethernet device
- '0' for port 1
- '10' for port 2
<register> - PHY register
<value> - value of PHY register

nload

Function : Load binary from TFTP server
Syntax : nload [<device>[<offset>[<filename><host>[<client>[<gateway>[<netmask>]]]]]]]
Options : <device> - Ethernet device
- '0' for port 1
- '10' for port 2
<offset> - loading offset
<filename> - file name to load
<host> - host IP address
<client> - client IP address
<gateway> - gateway IP address
<netmask> - network mask

nping

Function : Ping a host on the network
Syntax : nping <device> <host> [<client> [<gateway> [<netmask>]]]
Options : <device> - Ethernet device
- '0' for port 1
- '10' for port 2
<host> - host IP address
<client> - client IP address
<gateway> - gateway IP address
<netmask> - network mask

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pflash

Function : Program flash memory
Syntax : pflash <source> <count> <destination>
Options : <source> - starting source address
<count> - number of bytes to program
<destination> - starting destination address

reset

Function : Provide an hardware reset
Syntax : reset

sload

Function : Load binary from serial port
Syntax : sload [<device> [<offset>]]
Options : <device> - loading device and protocol
- '0' to download binary without protocol
- '1' to download Motorola S-Record (default)
<offset> - loading offset

time

Function : Get or set the time-keeper
Syntax : time [<date & time>]
Options : <date & time> - time-keeper value (YYYYMMDDHHMMSS)

vpd

Function : Display the Vital Product Data
Syntax : vpd

10.2.2. Advanced information

Preliminary information.

This chapter will describe the resources used for the monitor.
If the user will use ECMon with his application, he must care not to modify the following resources used internally by ECMon:

Mapping:	IMMR	0xFFF00000		
	internal DPRAM	0x0000-0100	SMC1 variables for console port	
	internal DPRAM	0x1000-1200	ECMon's variables	
	CS0	0xFE000000	Flash 0	First 128k used for ECMon
	CS1	0x00000000	SDRAM	
	CS2	0xFC000000	Flash 1	
	CS3	0xFA100000	RTC	
	CS4	0xFA000000	Internal registers & IP ID+IO	
	CS5	0xC0000000	IP mem	
	CS6	0xD0000000	VME master 1	
	CS7	0xE0000000	VME master 2	
	CS9	0xFB000000	SRAM	
Baud Rate Generator used for SMC1:		BRG7		

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10.2.3. Typical example

The following example will describe the procedure to use the second Flash memory bank as user's boot device:
Assuming the new software in this example is less than 64k. (=hexadecimal 10000)

sload 0 fb000000	Load the SRAM with the new software
(Send the file in ASCII mode with an text upload utility)	
eflash fc000000 10000	Erase the second Flash memory bank
pflash fb000000 10000 fc000000	Programm the second Flash bank with the values from SRAM

Then the user can invert the 'BootBnk' jumper and reset the board to boot on the new software.

In case of problem, the user can come back in the previous state inverting again the 'BootBnk' jumper and resetting the board.

If the Window's Hyperterminal is used to load the ASCII file to the VSBC-6862, please set the Line delay to 10ms in the Properties, Configuration, ASCII configuration menu.

10.3. VxWorks

VxWorks is now available for the VSBC-6862.
Please contact ECRIN Automatismes for more information.

10.4. Linux

Linux is available for the VSBC-6862.
Please contact ECRIN Automatismes for more information.

10.5. Other

For other software, ECRIN Automatismes can probably help you.
Please contact ECRIN Automatismes.

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11

Hardware available

One of the main advantage of the VSBC-6862 is his versatility. Through its IP and/or VME slots, the VSBC-6862 can be used in quantities of purposes.

Here follows the customization possibilites with ACTIS's modules:

11.1.List of ACTIS's IP modules

The VSBC-6862 can expand his functions by the mean of the IP modules.
Up to four IP modules can be plugged on this board.

A choice of these modules is available by ACTIS Computer, and the most used are described above.

Reference	Description
ADA-08	8 single ended (or 4 differential) channels, **12-bit A/D Converter** ±10 V, 140 KSample/sec, burst mode, 8 channels **12-bit D/A Converter** ± 10 V, 35 µs settling time, with calibration table, **two 8-bit TTL ports** with 4-bit handshaking, and **two 16-bit timers**
ADC-08	**8 channels** 12-bit, Analog/Digital Converter ±5V, ±10V, 0-10V, **140 KSample/sec, burst mod**e, level monitoring, watchdog
ADC-16	**16 channels** 12-bit, Analog/Digital Converter ±5V, ±10V, 0-10V, **programmable amplifier** x1, x10, x100, **140 KSample/sec**
DAC-08B	8 channels **14-bi**t, Digital/Analog Converter ±5V, ±10V, 0-10V, 35 µs settling time, **with calibration table**
CIO-32	Quad channels 8-bit port (with handshake) TTL Input/Output Interface (total 40 TTL I/O lines) and six 16-bit timers
INP-16	16 Isolated Digital Input (5 mA @ 12V, 10 mA @ 24V), three 16-bit timers, 2500 V isolation, flexible pattern-recognition, interrupt generation
LAN-10B	**LAN-10B** Ethernet™ Controller with on-board 64 KBytes SRAM buffer (sophisticated buffer management improve performance over traditional solutions) **including transition module with 10BASE-T (RJ45 for twisted pair), and AUI port**
LAN-12A	Arcnet ® Controller with 2 KBytes SRAM buffer, automatic ID selection, up to 2.5 Mbits/sec. Transition module for LAN-12A with coax and RJ-45 included

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LAN-15	MIL-STD-1553 Bus controller (BC), Remote terminal (RT), and Bus monitor (MT) **with 64K x 16 bit of RAM** (to support complex MT or BC applications), compatible with other IP using the DDC ACE controller
LAN-200	Fast Ethernet™ IEEE802.3u Controller with on-board 128 KBytes Fast SRAM buffer, 8 and 32 MHz compatible, DMA transferts supported, on-board 10BASE-T and 100BASE-TX transceivers. Price include LN-200 transition module
OUT-16	16 Isolated Digital Output (12-24V) up to 100 mA output current, three 16-bit timers, 2500 V isolation, differential output for active low or high signal
RDC-20/2x	Two channels resolver/synchro-resolver to digital converter, 10 to 16-bit resolution, 2 V RMS, 50 Hz to 10 KHz excitation, **Master/Vernie**r, Coarse/Fine, Gimbal assembly, **include transition module**
SCC-04AC	Quad **RS232** Serial Interface, Sync. up to 2 MBaud, Async. up to 38.4 KBaud, **8 Bytes Rx FIFO, 4 Bytes Tx FIFO, Z85230 enhanced controller, include TxClk & RxClk signals**
SCC-04B	Quad **RS422 and RS485** Serial Interface, Sync. up to 2 MBaud, Async. up to 38.4 KBaud, **8 Bytes Rx FIFO, 4 Bytes Tx FIFO, Z85230 enhanced controller**
SCC-04TTL	Quad TTL Serial Interface with Data, **Clock** and modem control signals. Sync. up to 2 MBaud, Async. up to 38.4 KBaud, **8 Bytes Rx FIFO, 4 Bytes Tx FIF**O, Z85230 enhanced controller
SCC-08A	Octal **RS232** Async Serial Interface (SC26C198) **up to 115.2 KBaud**, **16 Bytes FIFO** on each transmit & receive channel
SCC-08B	Octal **RS422 and RS485** Async Serial Interface (SC26C198) **up to 460.8 KBaud**, **16 Bytes FIFO** on each transmit & receive channel
UCC-08A	Octal **RS232** Synchronous up to **10 Mbit/sec**., Asynchrone Serial Interface **up to 115.2 KBit/sec**., **64 Bytes FIFO** on each transmit & receive channels
UCC-08B	Octal **RS422 and RS485** Synchronous up to **10 Mbit/sec**., Asynchrone Serial Interface **up to 2 Mbit/sec**., **64 Bytes FIFO** on each transmit & receive channels

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11.2.List of ACTIS's 6U transition modules

The IP modules provides many functions, some of these functions need special connectors or lot of I/O ports.
ACTIS provide transition modules for all its IP modules and cables to provide professional connectors on front panels.

A choice of ACTIS transition modules is described above.

Reference	Description
IO-32	Terminal Block with LED for 32 singles wires for 2 INP-16, OUT-16 (New version with Light Pipes), I/O connectors included.
IO-40	Terminal block for 40 single wires, and +5V/GND, for 2 ADC or 2 DAC, I/O connectors included.
IO-50	Universal Transition Module with terminal block for 50 singles wires (for all I/O IP modules), I/O connectors included.
SC-08D	Octal RJ-45 8-pin connector, with terminations for RS-422/485, for one SCC-08 A & B or one UCC-08 A & B
SC-08DB	Octal DB-25 connector, with jumpers for DTE & DCE mode and terminations for RS-422/485, compatible with one SCC-08 A & B or one UCC-08 A & B **WARNING !! require 8 TE**

11.3.List of ACTIS's 6U VME boards

The VSBC-6862 can communicate through the VME bus.
The following VME board can further expand the VSBC-6862 possibilities:

Reference	Description
VIPC-400	Slave Quad IP Module Carrier, supporting all IP spaces, 8 or 32MHz

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12
Technical support

Should you encounter any trouble during **installation** or **hardware** operation of your VSBC-6862, please contact our Technical support:

• Email : support@actis-computer.com

In order to solve your problem as quickly as possible, please check and note the following beforehand:

- VSBC-6862 serial number.
- Model name and number of PC Card and IP module.
- OS version such as OS-9, pSOS, VxWorks, etc.
- Software driver and application revisions.
- Date of purchase and name of your distributor.

For **software** support, please contact our sister company ECRIN Automatismes which supply BSP and IP driver for ACTIS Computer products:

• Phone : +33 476 92-2000 • Fax : +33 476 08-0318 • Email : support@ecrin.com

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13 Ordering information

VSBC-6862/200-128-16

VME board with MPC-8260 @ **200 MHz**
128 MBytes SDRAM, 16 MBytes Flash memory, and four serial ports

VSBC-6862/200-128-EK

Engineering Kit VSBC-6862, contains documentation, support CD-ROM, four IP cables, four multi-protocol serial cables.

CAB-RJ45-DB9

Adaptor cable with RJ-45 and DB-9 female in RS-232, DTE mode

CAB-V6862-SCC-01

Adaptor cable with DB-15 high density male and DB-25 male in RS-232/RS-422/RS-485/V.35, DCE mode

CAB-85B

85 cm adaptor cable between 50 pin high density IP carrier connector and standard 50 pin DIN 41651 connector on transition module.

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14
OEM Warranty

ACTIS Computer, warrants your VSBC-6862 board against any defect in material and workmanship, under normal use, for a period of three years from the date of purchase. In the event this product is found to be defective within the warranty period, ACTIS Computer will, at its option, repair or replace the defective single board computer.

This warranty is void if:

a) The board was operated or stored under condition of abnormal use or maintenance.
b) The board is repaired, modified or altered, unless such repair, modification or alteration is expressly authorized in writing by ACTIS Computer.
c) The board was subject to abuse neglect, lighting strike, electrical fault, improper packaging or accident.
d) The board was installed improperly.
e) The serial number of the board is defaced or missing.

ACTIS Computer will not, under circumstances, be liable for direct, special or consequential damages such as, but not limited to, damage or loss of property or equipment, loss of profits or revenues, cost of replacement goods, or expense or inconvenience caused by service interruptions. Under no circumstances will any person be entitled to any sum greater than the purchase price paid for the board.

To obtain warranty service, you should first contact the vendor from whom you purchased the ACTIS VSBC-6862 board. You may be asked to furnish proof of purchase to confirm the board is still under warranty.
All ACTIS VSBC-6862 board returned to ACTIS Computer or its authorized distributor must be securely packaged and shipped postage prepaid.

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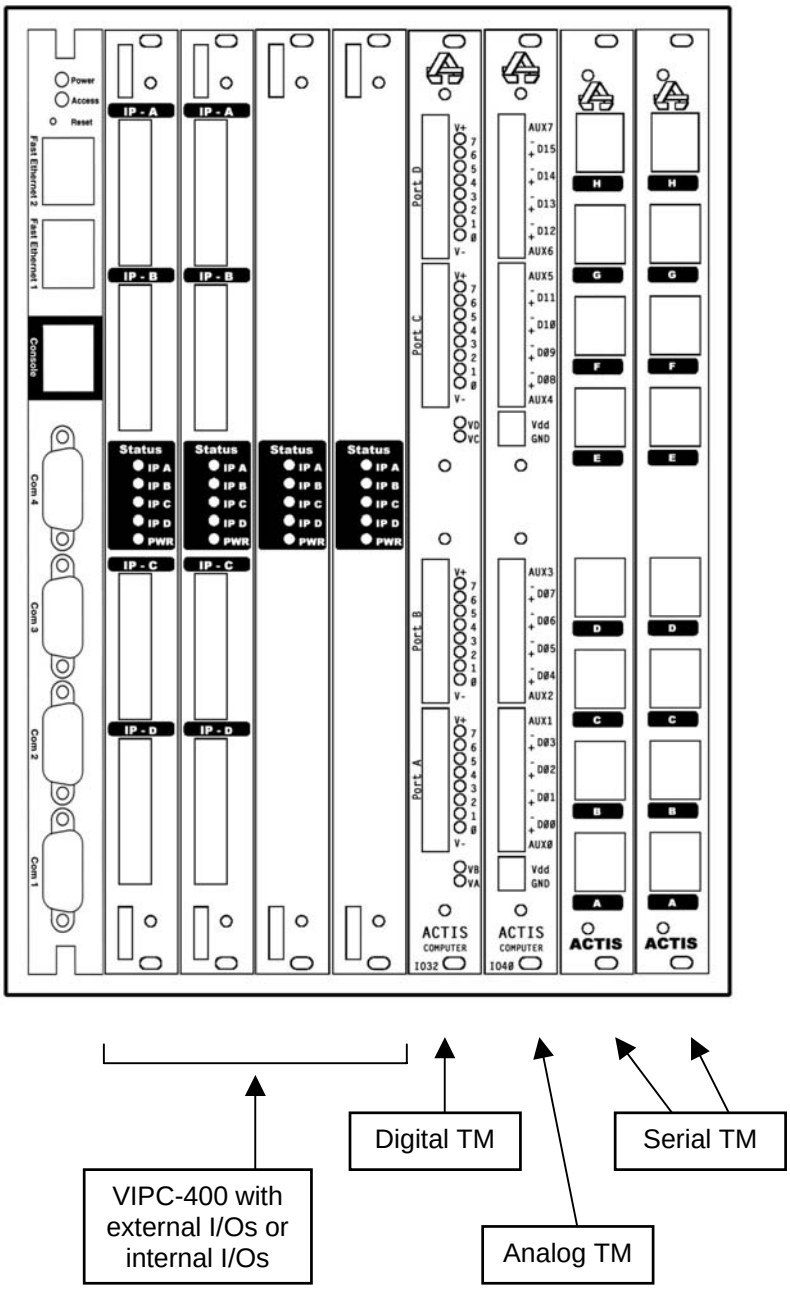
15 Appendix

15.1. Application examples with the VSBC-6862

15.1.1. Example A: Application with VME boards

This example represents the VSBC-6862 used in a standard VME rack with other VME boards and transition modules. In this configuration, the VSBC-6862 is VME master and can also be configured in system controller mode to arbiter the bus access for other masters.

Figure 24: Application example with VME boards

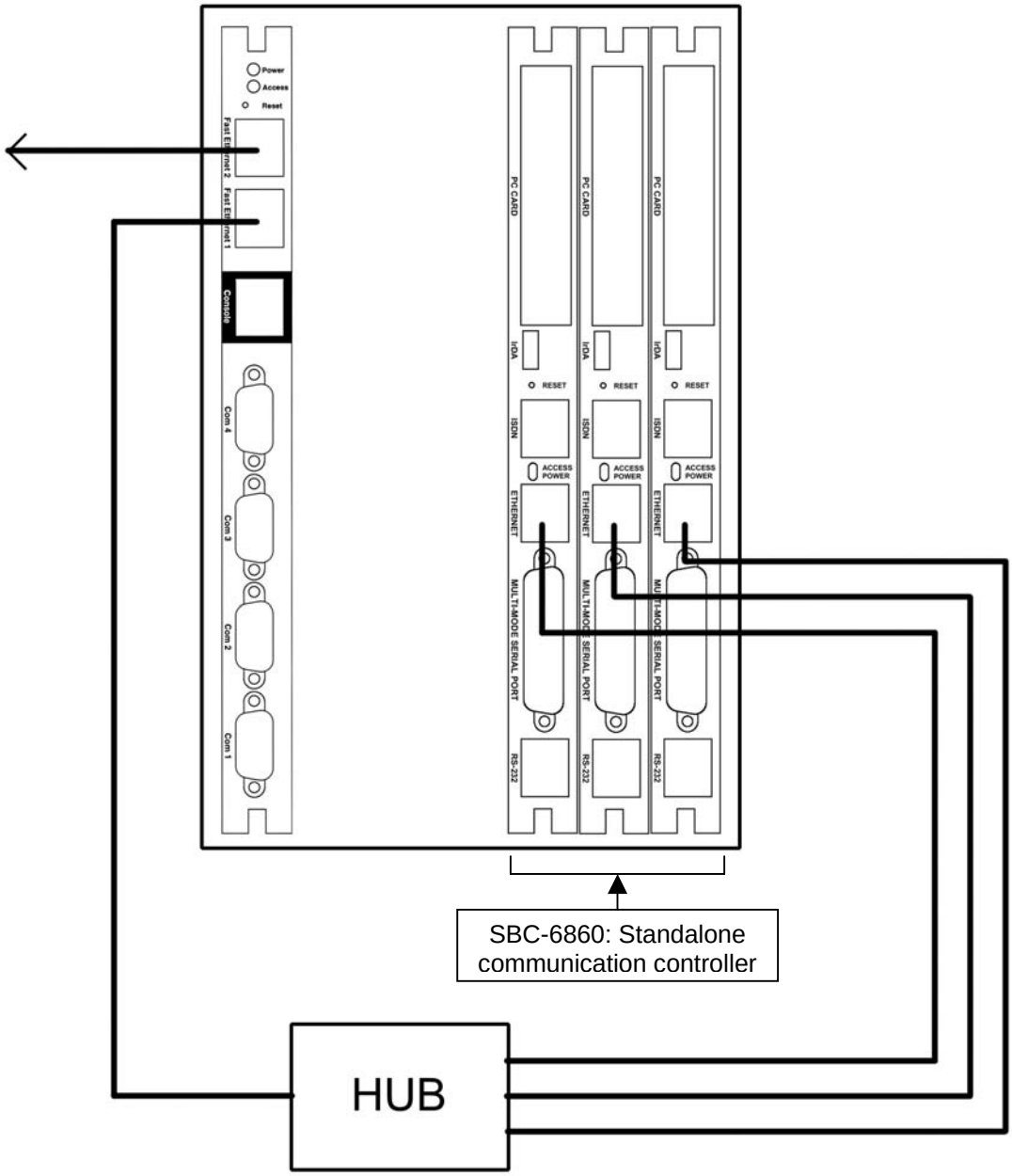


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15.1.2. Example B: Application with non-VME boards

The SBC-6860 is a single board computer, VME bus tolerant from ACTIS. This board provides two PC-Cards slots, one ISDN port, one multi-protocol serial port, two IP slots, and more...
In this example, the VSBC-6862 with its two Fast Ethernet ports can access other boards without usage of the VME bus, using a Fast Ethernet port to controls the specific peripherals of the SBC-6860, its second Fast Ethernet port can be used to connect other systems. Naturally, the VSBC-6862 can use the VME bus to access other VME boards.

Figure 25: Application example with non-VME boards

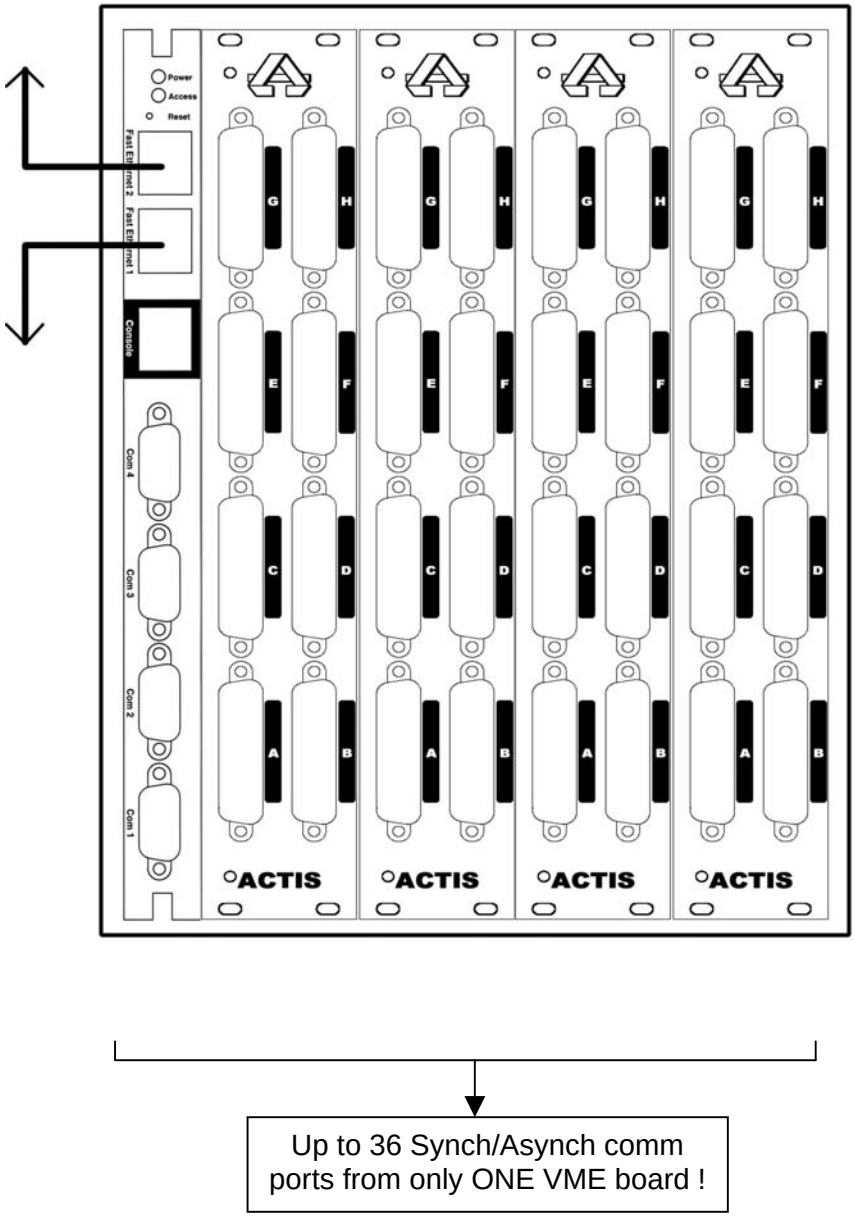


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15.1.3. Example C: Application in stand-alone

The VSBC-6862 can be used in stand-alone mode.
The following picture illustrates the VSBC-6862 equipped with four UCC-08A/B IP modules, which provides each eight synchronous or asynchronous serial ports. For more convenience, we added four SC-08DB transition modules to have standard DB-25 connections on front panel.
This single board system provides 32 synchronous or asynchronous serial ports, four multi-protocols communication ports, and two Fast Ethernet ports.

Figure 26: Application example in stand-alone



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