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USER'S GUIDE

VSBC-6872 series

VMEbus Single Board Computer with Freescale MPC8270 processor

Revision 1.4
3812



ACTIS Computer

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About this document

History

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0.9	Revised preliminary edition	Aug 12, 2004
1.0	First release	Sept 16, 2004
1.1	ECMon documentation added, minor changes and correction	May 4, 2005
1.2	Minor corrections	Oct 13, 2006
1.3	Update for board rev. C, P4 pin assignment	Aug 7, 2008

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Convention



This symbol mentions an important note or warning concerning proper functionality of the product described in this document.



This symbol indicates that detailed information are available on third-party literature.



This symbol emphasizes aspects the reader should read through carefully for his or her own advantage.

Hyperlink — This document provides external links to third-party web site for complementary documentation and information.

Link — This document provides some shortcut to related section for detailed information.

0x or $ — Placed in front of a number indicates a hexadecimal value.

NC — This notation is used to indicates a not connected pin (left open/floating).

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Photograph

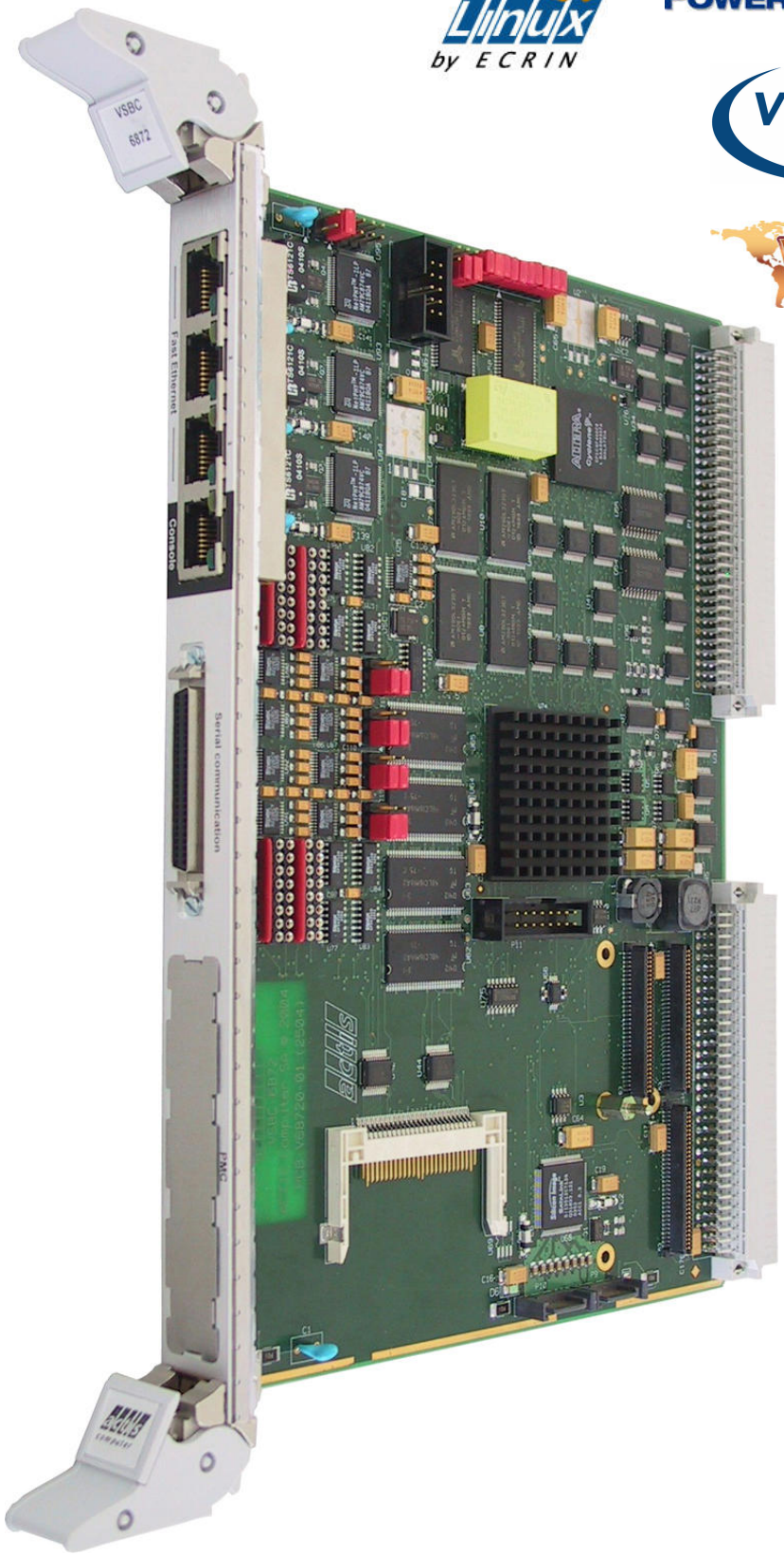


Figure 1 - VSBC-6872 photograph

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1 Introduction

The VSBC-6872 is an advanced VMEbus Single-Board Computer based on the Freescale MPC8270 PowerQUICC II processor. It is specifically designed to target embedded applications and features a complete A32/D32 VMEbus interface with System Controller and Master/Slave capabilities. The VME interface can be easily configured to fit a wide range of applications and to provide great flexibility at system level for integration.

The Freescale MPC8270 offers an integrated solution to deal with high-end applications. Its low power consumption level opens this system to a large range of network applications and system supervisions.

Three on-chip Fast Ethernet 10/100 Mbps controllers are available for standard network applications with CAT5 cables.

Four high-speed multi-protocol serial links are also available. The Communication Processor Module allows a management of several protocol types.

The memory controller supports SDRAM memory which offers a high-performance level for the system executive core.

The non-volatile storage is based on Flash devices, which supports boot capability. The Flash memory is organized in a two-bank structure. One bank of Flash, the on-board Real-Time Clock (RTC) and the SRAM memory are accessible from the VMEbus through A24 slave access.

The Freescale MPC8270 has an on-chip 32-bit/66MHz PCI bridge used for connecting a dual S-ATA controller and one PMC expansion module. The dual S-ATA controller can be used to connect mass storage peripherals.

A CompactFlash card interface operating in True IDE mode offers an additional data storage capability.

The VSBC-6872 represents a flexible configuration, with one PMC module which can be used for application extension. This PMC interface supports 32-bit modules, with a PCI clock frequency of 31.25 or 62.5 MHz. The VSBC-6872 can be customized through a wide range of PMC modules available from ACTIS Computer or third-party manufacturers. The PMC module typical applications are network controller, storage controller, acquisition system, etc.

Please refer to http://www.actis-computer.com/ for a complete list of available modules, or contact your local ACTIS Computer representative.

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1.1 Features

Processor

- Freescale MPC8270 PowerQUICC II processor
  - CPU - 450 MHz
  - CPM - 250 MHz
  - 60x bus - 100 MHz

Memory

- SDRAM 128-256 MByte
- Flash memory 16-32 MByte (2 swappable banks)
- SRAM 1-2 MByte
- Serial EEPROM 8 kbit
- CompactFlash card interface (True IDE mode)

Interfaces

- Three Fast Ethernet 10/100 Mbps
- Four high-speed serial links
- One RS-232 console port
- Dual S-ATA controller for hard disk drives
- Internal SPI and RS-232 (SMC2) ports

MPC8270 PCI bus

- PCI rev. 2.2 compliant
- 32-bit @ 31.25/62.5 MHz support
- 3.3 V environment

PMC mezzanine

- One PMC expansion slot
- Compatible with IEEE1386-1.2001 specification
- PCI 32-bit @ 31.25/62.5 MHz
- 3.3 V environment support
- User I/Os available on VMEbus P2 connector, ANSI/VITA 35-2000 compliant

VMEbus interface

- Master: A32/A24/A16/D32/D16/D8/RMW
- Slave: A24/A16/D32/D16/D8/RMW
- Requester: RWD, ROR, FAIR, programmable request level
- Arbiter: SGL, PRI, RRS, programmable timeout
- Handler: D8(O), IH(1-7)
- Interrupter: D8(O), ROAK, I(1-7)
- Bus Timer: BTO(16-112)
- Mailbox
- DMA Controller

Peripherals

- Real-time clock calendar, with 32 kByte battery backed-up SRAM

Software support

- ECMon monitor (included)
- Linux BSP (on request)
- VxWorks BSP (on request)

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1.2 VSBC-6872 Block Diagram

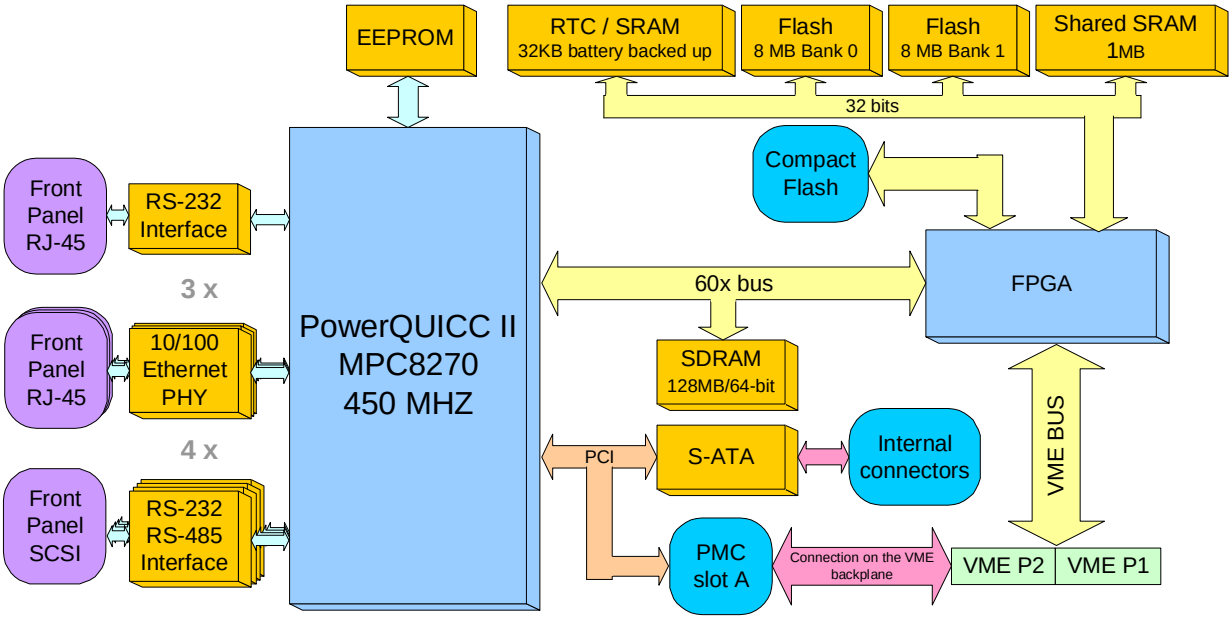


Figure 2 - Block diagram

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1.3 Component location

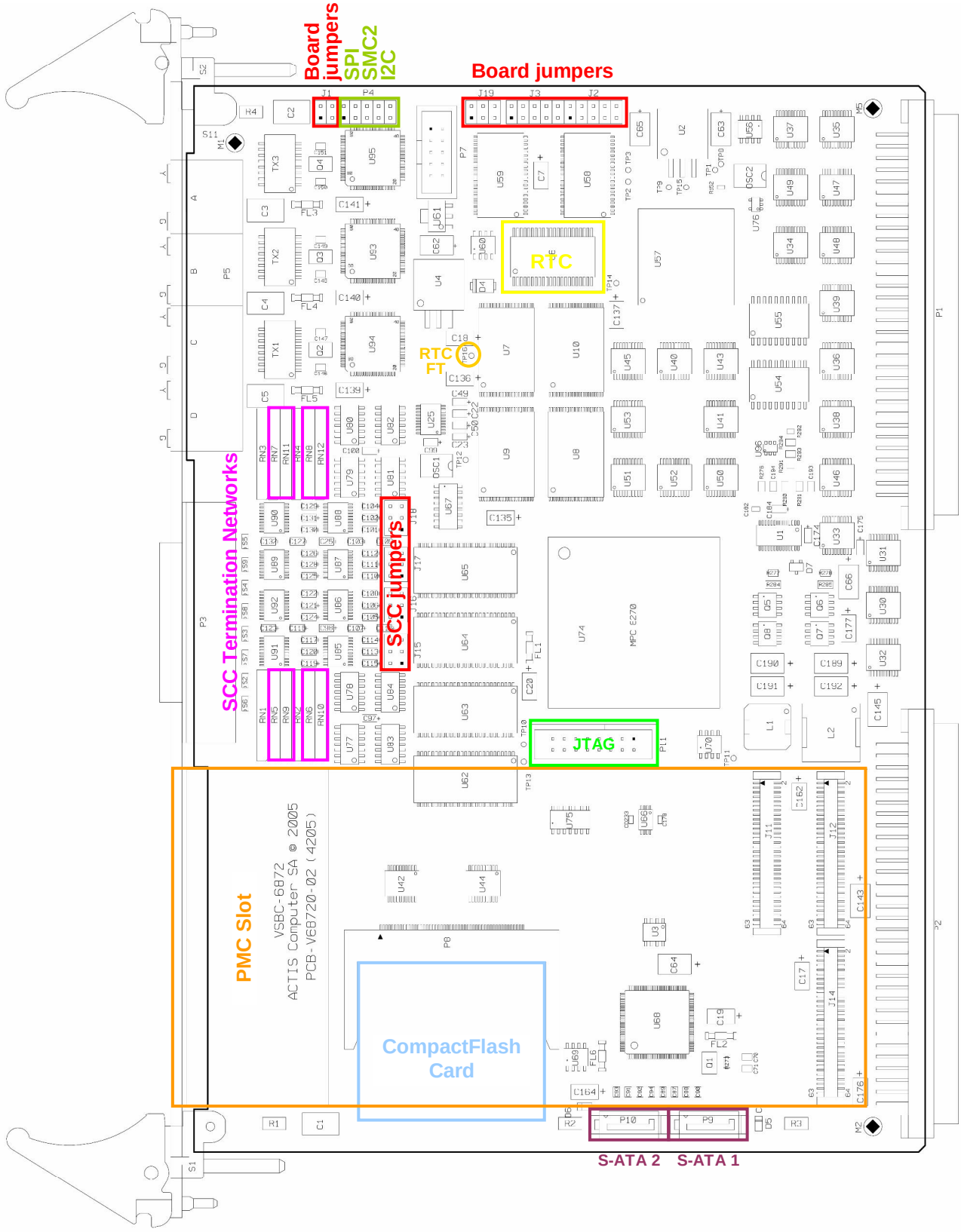


Figure 3 - Component location - top assembly

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2 Getting started

2.1 Unpacking instructions

If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.
Unpack the equipment from the shipping carton. Carefully check the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.





Avoid touching areas of integrated circuitry; static discharge can damage circuits.

2.2 Hardware Configuration

To produce the desired configuration and ensure proper operation of the VSBC-6872, you may need to carry out certain hardware modifications before installing the board.
The VSBC-6872 provides software control over most options: by setting bits in control registers after installing the board in a system, you can modify its configuration.



For detailed specification and register setting, please consult the Freescale literature:
"MPC8260 PowerQUICC II™ Family Reference Manual"
"MPC8280 PowerQUICC II™ Specification"
"MPC8280 Hardware Specifications"

Some options are not software programmable. Such options are controlled through installation or removal of jumpers or interface modules on the base board itself. For jumper configuration, please refer to 7.2 Board jumpers and 7.3 Serial Communication port jumpers.

2.3 Base board configuration

The Figure 3 shows the location of the connectors and jumpers on the VSBC-6872.

The VSBC-6872 is factory tested and shipped with the configurations described in the following sections. The board's factory-installed debug monitor operates properly with these factory settings.

2.4 Expansion module installation

The VSBC-6872 supports one PMC module. Please refer to 7.10.1 Installing a PMC for a detailed installation procedure.

2.5 Board installation

Before installing the VSBC-6872 into a VMEbus backplane, make sure that the SLOT1 jumper is set according to the slot location. If the VSBC-6872 is installed in slot 1 location, the System Controller must be enabled and then SLOT1 jumper has to be plugged in. For all other locations, the System Controller of the VSBC-6872 must be disabled and the SLOT1 jumper must be removed.

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2.6 ECMon monitor

The VSBC-6872 is provided with an installed board monitor utility. It features debugging capability and bootloader support with a user interface through a console port. It supports the primary board initialization for memory and peripheral bus controllers, and offers an easy to use board setup for board support package operation.

The ECMon debugger requires the use of the console port connected to a standard terminal. Please refer to the Figure 3 - Component location - top assembly section to find the console port P5[D] connector. Use the enclosed cable - part number CAB-RJ45-DB9 - which provides a direct connection to DB-9 female connector.

The terminal equipment need to have the following setting: data = 8-bit/char, stop bit = 1, parity=none, flow control=Xon/Xoff.

Terminal setting	
Baud rate	9600 bps
Data bit	8-bit/char
Stop bit	1
Parity	none
Flow control	Xon/Xoff

Table 1 - Console port setting

Please refer to 8.1 ECMon commands for a description of available commands.

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3 Functional description

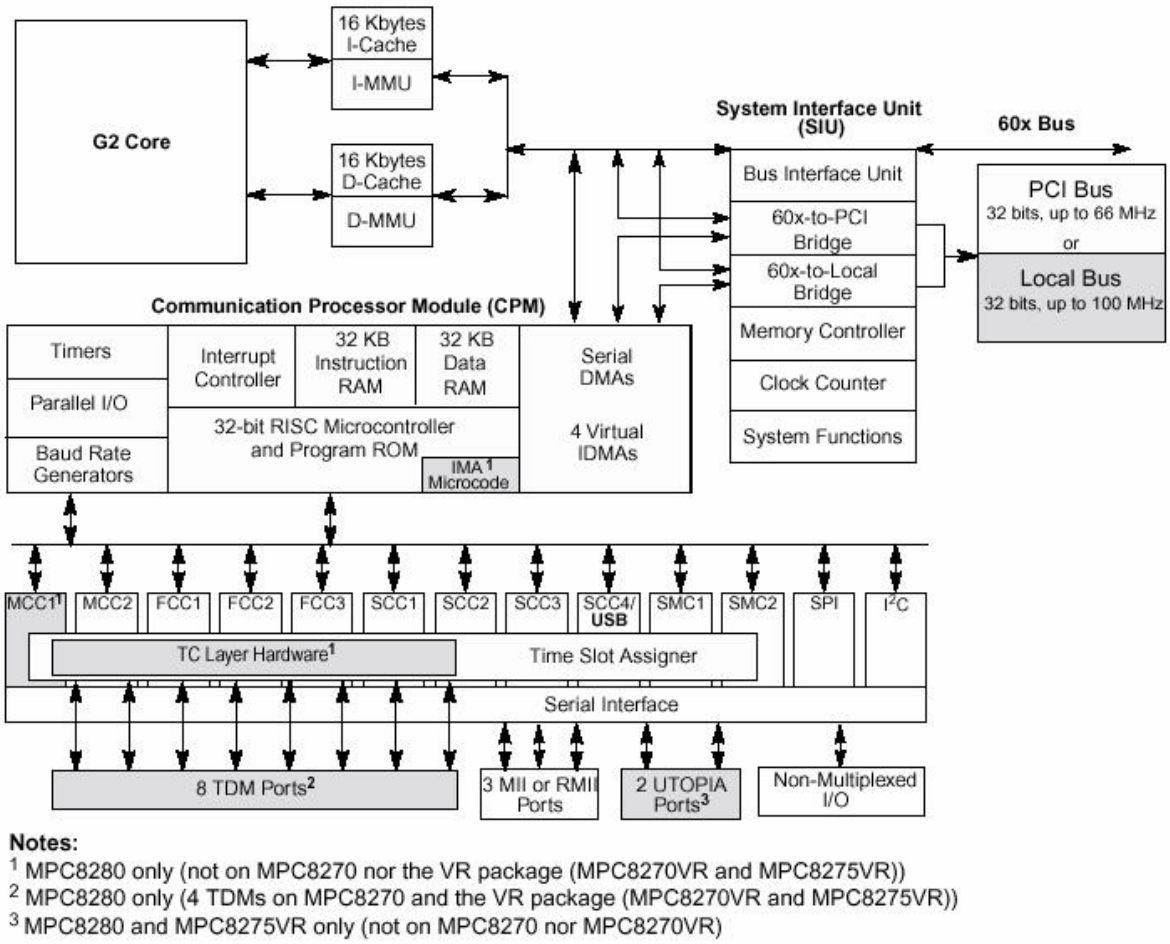
3.1 Freescale MPC8270 processor

The VSBC-6872 is based on the Freescale MPC8270 high-end PowerQUICC II processor which is specifically designed to address embedded applications. This processor architecture offers a very attractive design density by providing several on-chip peripheral controllers for a flexible Single Board Computer product.

This chip contains a RISC processor core, SDRAM controller, 32KB RAM CACHE, one PCI bus interface, three Ethernet interfaces, four multi protocol serial ports, one control for external memories and peripherals, DMA function, two standard serial ports, one I^2C interface, one SPI interface and general purpose I/Os.

The PowerQUICC II features two standard on-chip buses: the 60x Bus and the Peripheral PCI Bus. The 60x bus is used to access all the memories (SDRAM, flash, SRAM) and other devices with CPU access type (CompactFlash).

A Communication Processor Module manages the communication protocol of Ethernet ports and serial ports.



Notes:
[1] MPC8280 only (not on MPC8270 nor the VR package (MPC8270VR and MPC8275VR))
[2] MPC8280 only (4 TDMs on MPC8270 and the VR package (MPC8270VR and MPC8275VR))
[3] MPC8280 and MPC8275VR only (not on MPC8270 nor MPC8270VR)

Figure 4 - Freescale MPC8270 block diagram

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3.2 SDRAM controller

SDRAM memory is handled by the SDRAM timing state machine contained in the MPC8270. It is controlled by Chip Select 1.

The SDRAM state machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve maximum performance. This controller supports all SDRAM modes, such as pipelining and interleaving. The 64-bit wide data bus is directly connected to the 60x bus of the MPC8270 to achieve top performance.

The SDRAM organization depends on the ordered VSBC-6872 memory configuration, as follows:

SDRAM memory size	SDRAM devices organization
128 Mbyte	4 Meg x 16 x 4 banks
256 Mbyte	8 Meg x 16 x 4 banks

Table 2 - SDRAM device organization

SDRAM controller initialization (for 128-MByte)

PQII Base internal register : 0xFFF10000
W : Write

```
W     0xfff10184  0x3100      ;MPTPR
W     0xfff1019c  0x0f        ;PSRT
W     0xfff10190  0xab2e2462  ;PSDMR precharge all banks
W     0x200       0x12345678
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 1
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 2
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 3
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 4
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 5
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 6
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 7
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x8b2e2462  ;PSDMR CBR refresh 8
W     0x00000000  0xff        ;Access SDRAM
W     0xfff10190  0x9b0e2462  ;PSDMR mode set
W     0x118       0x12345678
W     0xfff10190  0xc32e2462  ;PSDMR enable refresh, normal operation
```

Table 3 - SDRAM initialization



For detailed specification and register setting, please consult the following literature:

1. *"Micron 256Mb SDRAM datasheet"*
2. *Freescale literature described in the hardware configuration chapter*

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3.3 Memory Management Unit

The MPC8270 processor integrates a Memory Management Unit (MMU) with a uniform, 4 gigabyte (GB) effective address (EA) space, and a 4GB (32-bit) real address (RA) space. The MPC8270 MMU performs address translation between effective and real addresses, as well as protection functions.
The MMU requires a valid setting of the Translation Lookaside Buffer (TLB) that controls the address translation, and storage attributes. Two 64-entry, fully-associative TLBs are used for instruction and data accesses.



For detailed specification and register setting, please consult the following literature:
Freescale literature described in the hardware configuration chapter

3.4 External Bus Controller

The MPC8270 External Bus Controller provides direct attachment for Flash type memory and peripheral devices.
To eliminate off-chip address decoding, the memory controller provides twelve programmable chip selects that enable system designers to locate memory and peripherals within the MPC8270 memory map. Chip select, data bus, and associated control signal timings are programmable.
For peripherals with variable timing requirements, the memory controller supports device-paced transfers with optional bus-timeout. System design is further simplified through dynamic bus sizing, which supports seamlessly attaching 8-, 16-, and 32-bit wide memories and peripherals.

For details about chip select assignment, please refer to 5.1 Peripheral Chip Select.



For detailed specification and register setting, please consult the following literature:
Freescale literature described in the hardware configuration chapter

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3.5 FLASH Memory

Two banks of 32-bit non-volatile FLASH memory are supported. Each bank is typically formed by two 32 to 64 Mbit devices, in accordance with the memory board configuration. These Flash devices are connected to the MPC8270 60x Bus which is managed by the memory controller.

These devices are compatible with Jedec-standard commands.

Each FLASH chip is split into two physical banks. This configuration provides simultaneous Read/Write operations, which offer the following advantages:

- Data can be continuously read from one bank while executing erase/program functions in the other bank.
- Zero latency between read and write operations

The FLASH memory devices are boot capable, on either the memory bank #0 or bank #1. This bank selection is done though the BOOTBANK (J3) setting. Each bank is driven by a specific chip select where this assignment can be cross-wired according to the BOOTBANK setting.

Flash bank #0 is accessible from the VMEbus through A24 slave access. Please refer to 3.15 VMEbus Interface for more information.

The first data in the flash memory is the Reset Word. This data initializes the MPC8270 after the Power-On Reset.

Default Reset Word (ECMon)

Address	Data
0xfe000000	0x0e
0xfe000008	0x87
0xfe000010	0xb6
0xfe000018	0x0e

Table 4 - MPC8270 reset word



For detailed specification and register setting, please consult the following literature:

1. *Fujitsu MBM29DL32XTE/BE datasheet*
2. *AMD Am29DL322D/323D/324D datasheet*
3. *Freescale literature described in the hardware configuration chapter*

3.6 SRAM Memory

The VSBC-6872 provides 1 MByte (2 MB option) of SRAM memory which uses a 32-bit data bus and is connected to the MPC8270 60x bus.

The SRAM memory is accessible from the VMEbus through A24 slave access for fast exchanges with external VME Masters. Please refer to 3.15 VMEbus Interface for more information.



For detailed specification and register setting, please consult the following literature:

1. *Samsung K6X4016T3F Family CMOS SRAM datasheet*
2. *Freescale literature described in the hardware configuration chapter*

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3.7 Real Time Clock

The VSBC-6872 provides a Real Time Clock device (RTC), which includes a battery backed-up 32 kByte SRAM. This RTC is a ST Microelectronics device with part number M48T37V.

The 32 kByte non-volatile SRAM provides flexible user data storage. This device supports an 8-bit bus interface, and has a direct connection to the MPC8270 60x Bus. It is accessible from the VMEbus through A24 slave access. Please refer to 3.15 VMEbus Interface for more information.

This RTC also provides Alarm, Battery Test, and Watchdog functions.

The RTC data are mapped in the SRAM memory map.

For detailed register description, please consult the ST Microelectronics literature "M48T37V datasheet"

Snaphat® Battery

The real-time clock device uses a detachable power source battery. This Snaphat® battery contains both the battery and the crystal and is designed to be snapped onto the RTC device.

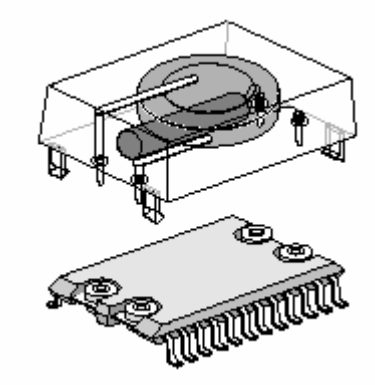


Figure 5 - RTC Snaphat® battery

The replacement battery pack is ST Microelectronics reference M4T28-BR12SH1

The VSBC-6872 is provided with an installed and calibrated Snaphat® battery. Therefore, for maintenance operation, an authorized operator can replace this Snaphat® battery by observing the following procedure.

1. Turn off the power supply
2. Remove carefully the Snaphat® battery. A DIP/IC extractor should be used.
3. Plug the new Snaphat® battery in respect with the correct orientation
4. Start a new calibration cycle for an accurate system clock precision

The RTC frequency test (FT) output can be measured on testpoint TP16. Refer to Figure 3 for location.

To avoid draining battery do NOT place SNAPHAT pins into conductive foam.

For detailed specification and register setting, please consult the following literature:
- *"ST Microelectronics M48T37V datasheet"*
- *"ST Microelectronics AN934 Timekeeper calibration application note"*

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3.8 CompactFlash card interface

A Type I CompactFlash card interface operating in True IDE mode is provided. It is connected to the MPC8270 60x bus and requires the use of a dedicated UPM configuration.
CompactFlash IORD# signal is connected to MPC8270 PGPL1 pin and IOWR# signal to PGPL2 pin.

UPM CompactFlash Initialization

	RAM Word #	RAM Word Value
RSS	0	0xcfff'fc00
	1	0x0fff'ff00
	2	0x0fff'fd00
	3	0x0ff3'fc80
	4	0x0ff3'fc80
	5	0x0ff3'fc04
	6	0x0fff'fd00
	7	0x3fff'fc01
WSS	24	0xcfff'fc00
	25	0x0fff'ff00
	26	0x0fff'fd00
	27	0x0ffc'fc80
	28	0x0ffc'fc80
	29	0x0ffc'fc00
	30	0x0fff'fe00
	31	0x3fff'fc05

Table 5 - UPM initialization for CompactFlash



For detailed specification and register setting, please consult the following literature:
- *1 "CompactFlash specification Rev : 2.0"*
- *2. Freescale literature described in the hardware configuration chapter*

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3.9 Fast Ethernet communication ports

The MPC8270 provides three Ethernet media access controllers that are generic implementations of the Ethernet Media Access Control (MAC) protocol complying with ANSI/IEEE Std 802.3 and IEEE 802.3u supplement. FCC supports half-duplex (CSMA/CD) and full-duplex operation for 10-Mbps and 100-Mbps operations.

The FCC are connected to on-board Fast Ethernet Physical devices (PHY), using MII interface bus, which provides the electrical physical layer for a direct interface to Unshielded Twisted Pair Cable 5 (UTP5) for 100Base-TX Fast Ethernet, or UTP5/UTP3 cable for 10Base-TX Ethernet.

Each FCC peripheral controls the PHY device, which is assigned to a front panel Ethernet port. The PHY device is configured by a set of MII registers accessed trough the serial management interface. Since all the PHY devices are connected to this serial management interface, each PHY has a unique PHY address to ensure the device selection.

The following table gives the relationship between the FCCs and the physical layer interfaces.

FCC #	FEC #	PHY Address
1	0	0x01
2	1	0x02
3	2	0x03

Table 6 - Fast Ethernet assignment



For detailed specification and register setting, please consult the following literature: "Freescale literature described in the hardware configuration chapter"

The PHY devices are based on AMD Am79C874 component.
For detailed register description, please consult the AMD Am79C874 datasheet.

3.10 SCC multi-protocol serial ports

The PowerQUICC II has four serial communications controllers (SCCs), which can be configured independently to implement different protocols for bridging functions, routers and gateways and to interface with a wide variety of standard WANs, LANs and proprietary networks. The choice of protocol is independent from the choice of interface. An SCC is described in terms of the protocol it runs. When an SCC is programmed to a certain protocol or mode, it implements functionality that corresponds to parts of the protocol's link layer (layer 2 of the OSI reference model).

Many SCC functions are common to protocols of the following controllers:

- UART
- HDLC and HDLC bus
- AppleTalk / Local Talk
- BISYNC
- Transparent
- Ethernet

Although the selected protocol usually applies both to the SCC transmitter and receiver, one half of an SCC can run transparent operations while the other runs a standard protocol (except Ethernet). Each Rx and Tx internal clock can be programmed with either an external or internal source.

Associated with each SCC is a digital phase-locked loop (DPLL) for external clock recovery, which supports NRZ, NRZI, FM0, FM1, Manchester and Differential Manchester. If the clock recovery function is not required (that is synchronous communication), then the DPLL can be disabled, in which case only NRZ and NRZI are supported.

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A SCC can support standard modem interface signals, RTS, CTS and CD. If required, software and additional parallel I/O lines can be used to support additional handshake signals.

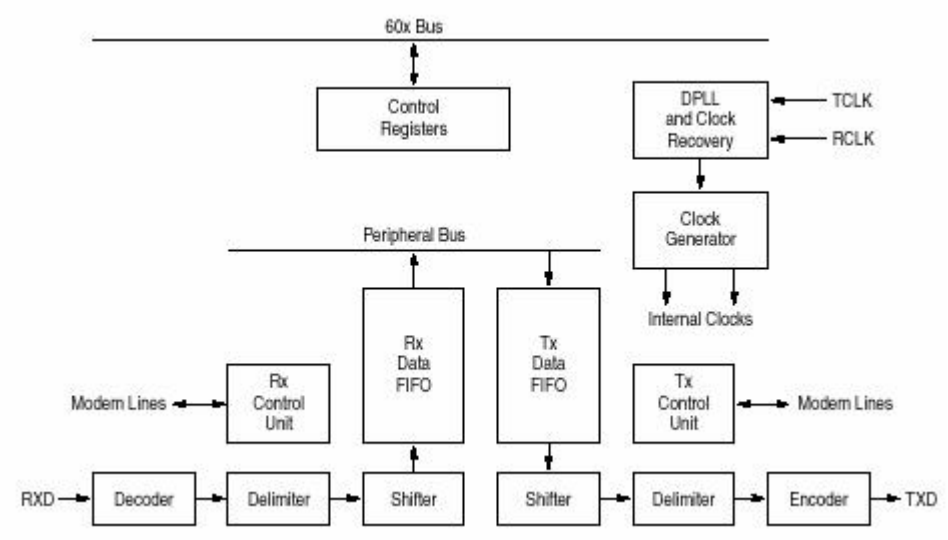


Figure 6 - SCC block diagram

The VSBC-6872 provides a configurable physical interface for each of the four serial communication ports. The physical interface mode can be selected as RS-232 or RS-422/RS-485/V.35 either by jumpers or by software through the SCCR register. Please refer to the SCCR register description and to 7.3 Serial Communication port jumpers for register setting and jumper configuration.

The VSBC-6872 provides removable resistor networks for each serial ports when configured in RS-485 mode. Each SCC requires two resistor networks as listed in Table 7 - SCC RS-485 removable resistor networks. These resistor networks are used for the serial communication network termination and must be installed only if the SCC is at one end of the RS-485 network.

SCC	Network Location	
1	RN8	RN12
2	RN7	RN11
3	RN6	RN10
4	RN5	RN9

Table 7 - SCC RS-485 removable resistor networks

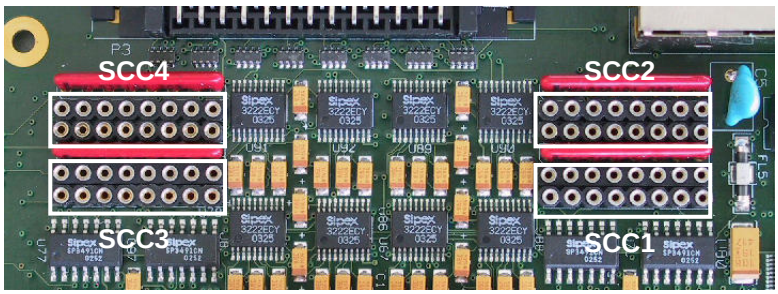


Figure 7 - SCC resistor networks location

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3.11 Interrupt controller

The MPC8270 Interrupt Controller supports up to eight external dedicated interrupt request sources. The interrupt request signals can also be connected on certain GPIO. These signals are defined as interrupt request function (Port C GPIO). For detailed information about the Interrupter controller setting, please refer to 5.4 Multiplexed General Purpose I/O ports and 5.3 Interrupt sources.

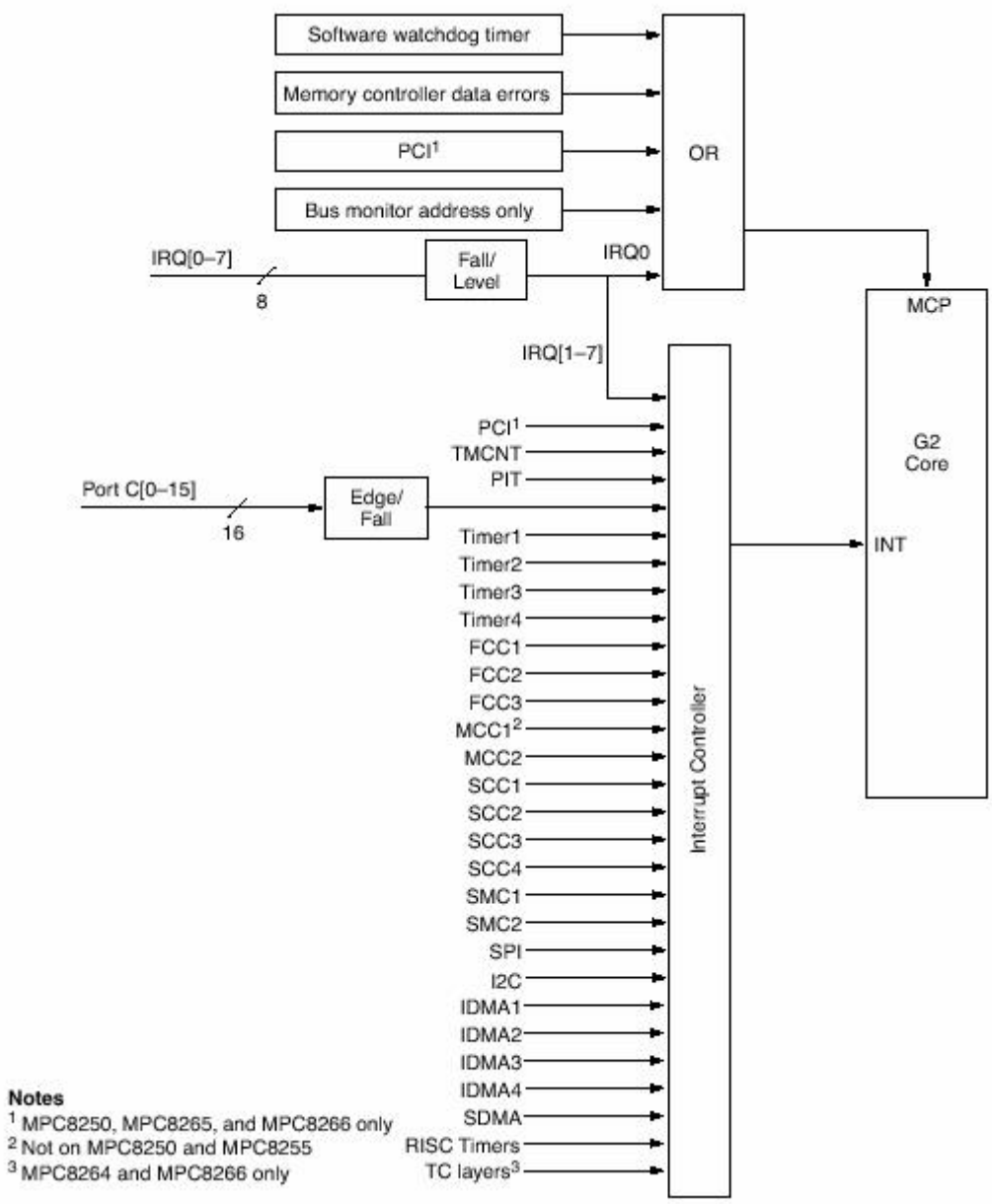


Figure 8 - MPC8270 interrupt controller

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3.12 Direct Memory Access Controller

The PowerQUICC II has two physical serial DMA (SDMA) channels.
The CPM implements two dedicated virtual SDMA channels for each FCC, MCC, SCC, SMC, SPI and I^2C – one for each transmitter and receiver.
An additional four virtual SDMA channels are assigned to the programmable independent DMA (IDMA) channels.

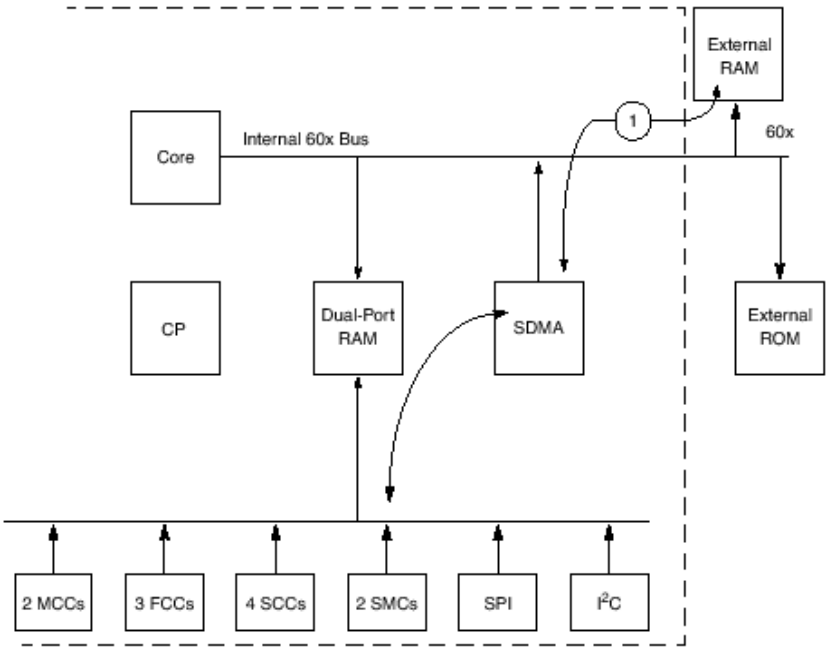


Figure 9 - DMA block diagram

For detailed specification and register setting, please consult the following literature: "Freescale literature described in the hardware configuration chapter"

3.13 I^2C serial interface bus

The MPC8270 processor has an on-chip I^2C serial bus controller compatible with the Philips specification. The I^2C bus has a two-wire, bi-directional, open-drain, low-speed serial interface. The serial clock and serial data lines are bi-directional, to support multiple bus masters and to mix high- and low-speed devices on the same bus.

The I^2C interface supports the following standard and enhanced features:

- up to 400-kHz operation
- 8-bit data transfers
- 7-bit addressing
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters

For detailed specification and register setting, please consult the following literature: "Freescale literature described in the hardware configuration chapter"

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3.13.1 VPD EEPROM (Vital Product Data)

This 8-kbit serial EEPROM is used to store a set of board specific parameters. These parameters provides the board configuration information (board revision, Ethernet addresses, SDRAM configuration, FLASH memory configuration, etc).

EEPROM address	0xad

Table 8 - VPD EEPROM address

The VPD memory structure is defined as follows.

Field	Offset	Size	Values
Magic Cookie	0x00	8	0x41 0x43 0x54 0x49 0x53 0x00 0x00 0x00 ("ACTIS")
Size of EEPROM	0x08	2	0x01 0x00
Reserved	0x0a	4	0x00 0x00 0x00 0x00
Date	0x0e	2	YY MM (BCD Format)
Options	0x10	240 max	XX

Table 9 - VPD serial EEPROM structure

The Option fields may have fixed or variable length. Each option begins with a tag octet, with a user-value defined between 0x80 to 0xfe (all other are reserved). The fixed-length type options, which do not include data, consist of only a tag octet. Only options 0x00 and 0xff are fixed-length type. All other options are variable-length type with a length octet following the tag octet. The value of the length octet does not include the two octets specifying the tag and length. The length octet is followed by "length" octets of data. In the case of some variable-length options the length field is a constant but must still be specified.

Option	Code	Length	Description
Pad	0x00	F, 1	The pad option can be used to cause subsequent fields to align on word boundaries
End	0xff	F, 1	The end option marks the end of valid information in the vendor field. Subsequent octets should be filled with pad options
Product Identifier (optional)	0x01	V	This option specifies the name of the product (ASCII terminated by a zero byte).
Serial Number (optional)	0x03	V	This option specifies the serial number of the product (ASCII terminated by a zero byte)
Revision (optional)	0x08	F, 4	This option specifies the firmware revision of the board
PCB Revision (optional)	0x09	F, 2	This option specifies the PCB revision
CPU Type (optional)	0x20	V	This option specifies the name of the processor (ASCII terminated by a zero byte)
CPU Clock Speed	0x21	F, 4	This option specifies the output clock speed in hertz (4 Bytes, MSB first)
Dynamic RAM	0x30	F, 4	This option specifies the dynamic RAM configuration (binary code which can prevent use of SDRAM)
Flash Memory (optional)	0x3c	F, 4	This option specifies the Flash memory configuration (binary code)
Ethernet Address #1 (optional, first Ethernet dev)	0x60	F, 6	This option specifies the first Ethernet address (6 Bytes, MSB first)
Ethernet Address #2 (optional, first Ethernet dev)	0x61	F, 6	This option specifies the second Ethernet address (6 Bytes, MSB first)
Ethernet Address #3 (optional, first Ethernet dev)	0x62	F, 6	This option specifies the third Ethernet address (6 Bytes, MSB first)

Table 10 - VPD options field



The optimized values are defined and stored by the factory. It is not recommended to change these parameters, since a wrong setting could affect the system operation.

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3.14 MPC8270 PCI bus

The local bus of the MPC8270 is set in PCI host mode by enabling its on-chip PCI bridge. It is PCI Specification Revision 2.2 compliant and is used on the VSBC-6872 to implement a single PMC slot and interconnect a dual S-ATA controller.

The following table gives the PCI devices present on the MPC8270 PCI bus.

Device Number	Vendor ID	Device ID	Function	MPC Interrupt
0x00	0x1057	0x18c0	MPC8270 PCI Bridge	N.A.
0x0b	0x1095	0x3512	Dual S-ATA Controller	INTA:IRQ7
0x0c	N.A.	N.A.	PMC slot	INTA:IRQ2, INTB:IRQ3, INTC:IRQ4, INTD:IRQ5

Table 11 - PCI bus devices

The MPC8270 PCI bus supports 32-bit at 31.25/62.5 MHz in 3.3V-only environment. The PCI bus clock frequency depends on the PMC capabilities. If a 33MHz-capable PMC is inserted, the PCI bus will run at 31.25 MHz otherwise it will run at 62.5 MHz.

Note that the PowerQUICC II's clocking architecture establishes a strict relation between clock frequencies of the core, CPM, 60x, and PCI. The MPC8270 of the VSBC-6872 is configured to achieve the best CPU and 60x bus performance.



For detailed specification and register setting, please consult the Freescale literature: "MPC8260 PowerQUICC II™ Family Reference Manual"

3.14.1 PMC expansion slot

The VSBC-6872 SBC supports a single PMC interface which offers a flexible extension for high performance peripheral. The PMC user I/Os are available on the VMEbus P2 connector according to the ANSI/VITA 35-2000 standard, 2.3 Mapping of Single PMC-P4 to VME-P2-Rows-A,C.
This mapping is reproduced here for your convenience:

PMC P4	VME P2	PMC P4	VME P2	PMC P4	VME P2	PMC P4	VME P2
1	1C	2	1A	33	17C	34	17A
3	2C	4	2A	35	18C	36	18A
5	3C	6	3A	37	19C	38	19A
7	4C	8	4A	39	20C	40	20A
9	5C	10	5A	41	21C	42	21A
11	6C	12	6A	43	22C	44	22A
13	7C	14	7A	45	23C	46	23A
15	8C	16	8A	47	24C	48	24A
17	9C	18	9A	49	25C	50	25A
19	10C	20	10A	51	26C	52	26A
21	11C	22	11A	53	27C	54	27A
23	12C	24	12A	55	28C	56	28A
25	13C	26	13A	57	29C	58	29A
27	14C	28	14A	59	30C	60	30A
29	15C	30	15A	61	31C	62	31A
31	16C	32	16A	63	32C	64	32A

Table 12 - PMC-P4 to VME-P2 mapping

3.14.2 Dual S-ATA Controller

The VSBC-6872 allows to connect two S-ATA hard disk drives via a dual S-ATA controller.

The S-ATA function is available in commercial temperature only.



For detailed specification and register setting, please contact Actis Computer.

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3.15 VMEbus Interface

3.15.1 60x-to-VME Bridge

An in-house designed 60x-to-VME Bridge is used to interface the MPC8270 with the VMEbus. The VMEbus interface of the bridge implements Master, Slave, Requester, Interrupter, Interrupt Handler, Arbiter, and Bus Timer modules. This bridge contains a set of configuration registers for controlling VME operations and board-specific features. A DMA controller is also included to perform SRAM-to-VME and VME-to-SRAM transfers without CPU utilization. Please refer to 4 Bridge Registers for detailed information.

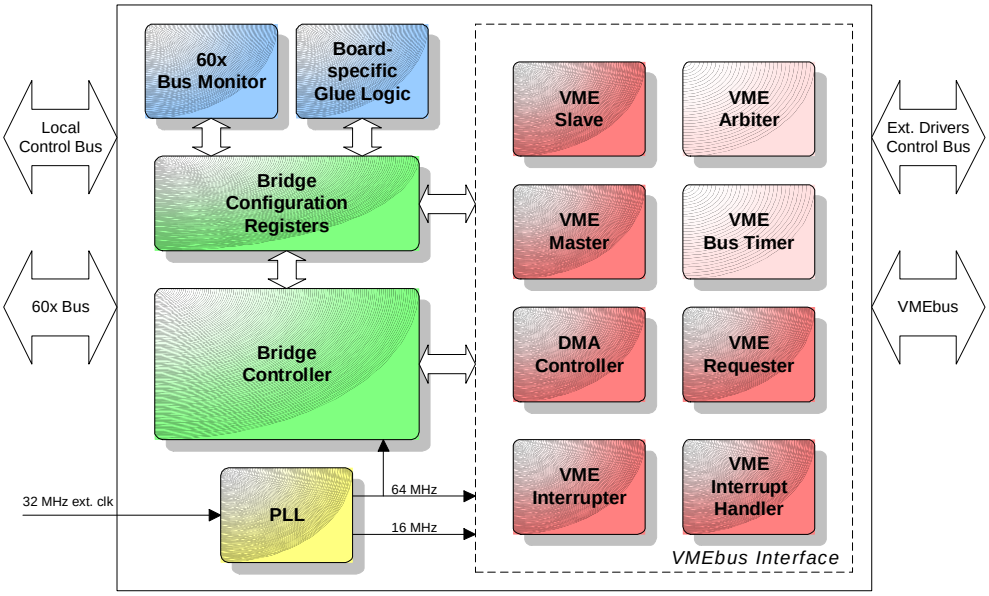


Figure 10 - 60x-to-VME Bridge block diagram

VME Arbiter and Bus Timer can be enabled or disabled to allow the board to function as a system controller board (slot 1) or as a peripheral board.

A configurable 60x Bus Monitor is also included in the bridge to replace the MPC8270 bus monitor and overcome its limited timeout period. Please refer to the BSCR register description for more information.

A dedicated UPM must be used to access the 60x-to-VME bridge (bridge registers and VME master). The UPM configuration must comply with the following description:

	RAM Word #	RAM Word Value
RSS	0	0xccfc'ec00
	1	0x00fc'fc40
	2	0x00fc'fc40
	3	0xf0fc'ec04
	4	0xf3fd'ec01
WSS	24	0xccfc'ec00
	25	0x00fc'fc40
	26	0x00fc'fc40
	27	0xf0fc'ec04
	28	0xf3fd'ec01
EXS	60	0xffff'ec01

Table 13 - UPM initialization for bridge access

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3.15.2 VMEbus Master

The VSBC-6872 is VME Master A32/A24/A16/D32/D16/D8/RMW

The VME master can use two windows to access the VMEbus. They are controlled by the UPM, with the chip selects CS6 and CS7. All VME Chip Selects take a CPU space of 64 MBytes.

The selection for A16, A24, and A32 modes are made by accessing different offsets in the chip select memory:

Offset	VME Zone	Size
0x000'0000-0x1ff'ffff	A32	32 MBytes
0x200'0000-0x2ff'ffff	A24	16 MBytes
0x300'0000-0x300'ffff	A16	64 kBytes

Table 14 - VME Master addressing space mapping

For A16 and A24 modes, all VME memory map is directly available.

For A32 mode, the VMBMA and VMBMB registers define the seven high order bits for A32 VME addresses. Thus, the VME 32 MBytes windows can be moved in all A32 memory space: 4 GBytes.

Depending on the offset accessed, the AM5 to AM3 are automatically set with the corresponding value to indicate the address mode used. The AM2 to AM0 bits are user defined in the VMAMA and VMAMB registers. Setting must be done according to the VMEbus specification.

The selection for D8, D16, and D32 are made dynamically with the software. A byte access generates automatically a VME D8 access, a word access a D16 access, and a long word access a D32 access.
It is possible to restrict the maximum size of the VME access modifying the Port Size field in the corresponding Base Register (BR[PS]) of the MPC8270.

☞ D16 and D32 accesses are only allowed on even addresses

The VME Master RMW cycle is controlled by VMBA[RMW]. Please refer to the VMBA register description for correct usage.

It is also possible to lock the VMEbus to get exclusive access of the bus. Please refer to 3.15.4 VMEbus Requester for more information.

3.15.3 VMEbus Slave

The VSBC-6872 is slave A24/A16/ D32/D16/D8/RMW.

The board contains an independent slave module. This module doesn't need the local processor initialized to be active.

From the VMEbus, the following zones are accessible:

- The VME slave registers
- The Flash memory bank 0
- The SRAM memory
- The Real-Time Clock device

Accessing one of these zones at the same time from the VMEbus and the host processor starts an internal arbitration between the two masters and keep the 'loosing' master in a wait state while the 'winning' master can access the zone.

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Note that an external VME access to one of these zones (VSBC-6872 slave access), doesn't block the host processor with the SDRAM, PMC module, or communication ports. For example, the MPC8270 can access the SDRAM while an external VME master accesses the local SRAM memory. Moreover, an external master can access the VSBC-6872 before it is initialized. All slave functions are independent of the MPC8270 state.

These zones are divided in three windows: one A16 window and two A24 windows.

A16 window
This window gives access to a subset of the bridge registers.
This windows occupies 2kBytes.
Its base address is defined with 5 jumpers (J2). Please refer to 7.2 Board jumpers for jumper configuration.

VME slave register memory map:

Offset	Name	Mode	Description	Access
0x01	VSMAIL	RW	VME Slave Mailbox	D8/D16
0x03	VSBA24	RW	VME Slave Base Window A24	D8/D16
0x05	VSWA24	RW	VME Slave Window A24 management	D8/D16
0x07	VIVEC	RW	VME Interrupter Vector	D8/D16
0x09	SRESR	WO	Software Reset Register	D8/D16
0x0b	XSAV24	RW	Extended SRAM Access from VME A24	D8/D16
0x0d	VIL	RW	VME Interrupter Interrupt Level	D8/D16

Table 15 - Bridge registers accessible from VMEbus

For more flexibility, these registers are also accessible from the MPC8270.

A24 windows
Two A24 windows are defined.
One is specified by the VSBA24 register and gives access to the Flash, SRAM, and RTC devices. It occupies 1 MByte and is enabled by setting VSBA24[WinA24On].

The Flash, SRAM or RTC are accessed depending on the offset in the VSBA24 window as:

VME Offset	Device	Size	Access
0x0'0000-0x7'ffff	SRAM memory	512 kBytes	D8/D16/D32
0x8'0000-0xb'ffff	Flash memory	256 kBytes	D16/D32
0xc'0000-0xc'7fff	RTC device	32 kBytes	D8

Table 16 - A24 Slave memory map

Except for the RTC device, this window does not include all memory map for Flash and SRAM memory. The VSWA24 register is used to complete the high order local addresses for these devices (Figure 11).

The Flash memory bank 0 is 8 MBytes, the VME slave window for Flash is 256 kBytes. 32 positions are needed to cover all Flash memory map. This is done using the VSWA24 register, bits FLA23-FLA18. These bits are the respective high order addresses sent to the local Flash memory. Note that the Flash memory is not accessible in D8 mode from VME. A D8 access will always select 16 bits on the Flash memory.

The SRAM memory is 1 MByte, the VME slave window for SRAM is 512 kBytes. 2 positions are needed to cover this memory map. This is done using the VSWA24 register, bit SRA19.

The second window is specified by the XSAV24 register and gives access to the whole SRAM memory (1 MB or 2 MB option). It occupies 1 or 2 MBytes and is enabled by setting XSAV24[EN] (Figure 12). The advantage of this window over the one defined by VSBA24 is that the whole SRAM is visible in a single VME window.

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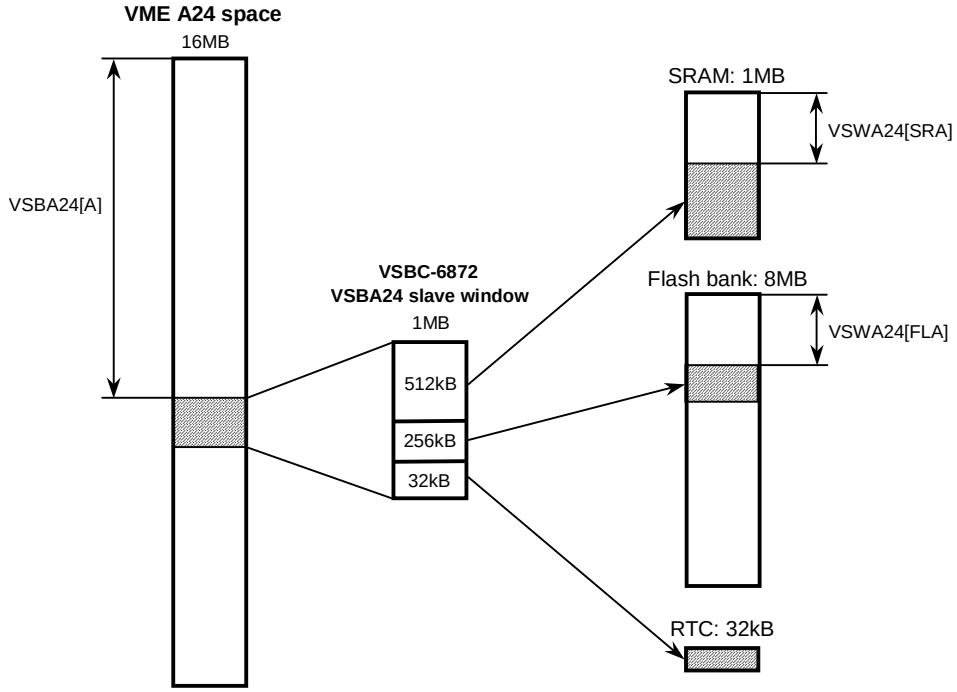


Figure 11 - VME Slave window defined by VSBA24

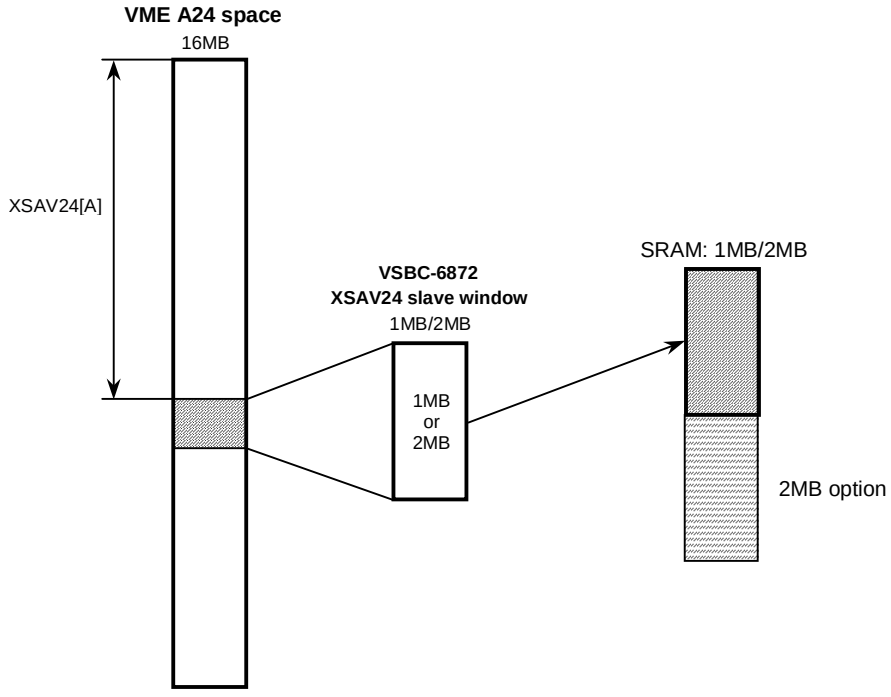


Figure 12 - VME Slave window defined by XSAV24

Note that the access to the shared memory can be locked by the host processor (giving it an exclusive local access). This is useful to keep memory coherency by avoiding an external VME access between two critical local accesses. Locking of the shared memory is achieved by setting BSCR[LOCK].

Please refer to the VSBA24, VSWA24, XSAV24, and BSCR registers description for more information.

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3.15.4 VMEbus Requester

The VMEbus Requester is: RWD, ROR, FAIR, with programmable request level.

The requester requests the VMEbus as soon as the VME Master or the VME Interrupt Handler wants to gain access of the bus. Its release mode (RWD or ROR) is defined in the VMBA register and its request mode (FAIR) in the XVCR register.

A lock function set by VSBA24[VME_lock] tells the requester not to release the VMEbus in order to provide the host processor with an exclusive VME access that may be required for a specific application.

Please refer to the VMBA, XVCR, and VSBA24 registers description for more information.

3.15.5 VMEbus Interrupter

The VSBC-6872 can send any interrupt level to the VMEbus with its interrupter I(1-7), D08(O), ROAK.
Before generating this interrupt, the interrupt level and the vector must be defined with the VIVEC register and/or VIL register.
The corresponding interrupt signal is asserted when writing any value to the VINTER register.

The interrupt is released at the end of the responding VME Interrupt Acknowledge (IACK) cycle.

Please refer to the VIVEC, VIL, and VINTER registers description for more information.

3.15.6 VMEbus Interrupt Handler

The VSBC-6872 is VME Interrupt Handler IH(1-7), D08(O)

This interrupt-handler is able to recognize all IRQ VME levels.
All levels can be masked with the VHM register.

When an IRQ is coming from the VME side, an IRQ1 is sent to the MPC8270.
The user can then read the IRQ levels active in the VHIL register.
Depending on the IRQ level to be acknowledged, the user can read the vector in the corresponding offset in the VHV register.
When reading the vector, a VME Interrupt Acknowledge (IACK) cycle is initiated.

Please refer to the VHM, VHIL, and VHV registers description for more information.

3.15.7 VMEbus Mailbox

The VSBC-6872 provides a single Mailbox system. From the VME side, it is composed of a single register: VSMAIL.
Before using this function, the VSBA24[MailOn] bit must be set to unmask the local IRQ.
When an external master writes to this register, an IRQ6 is sent to the host processor.
To clear this IRQ, the host processor must write any value to the VSMAIL register.

Please refer to the VSMAIL and VSBA24 registers description for more information.

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3.15.8 VMEbus System Controller

The VSBC-6872 provides System Controller capabilities that can be enabled or disabled with the SLOT1 jumper. Please refer to 7.2 Board jumpers for jumper configuration.

The VSBC-6872 System Controller provides the following functions:

- VMEbus Arbiter: SGL, PRI or RRS mode and programmable timeout.

  - In SGL mode: Single Level, the arbiter uses only the BusRequest3 signal from VME and activates only the BusGrant3 signal. The board with the higher relative priority is the nearest to the slot1.
  - In PRI mode: Prioritized, the arbiter uses the BusRequest3 as higher priority and BusRequest0 as lower priority. If a master with higher priority requests the bus, a BCLR is generated.
  - In RRS mode: Round Robin Select, the level of the priority of the request lines change in a circular manner. For example: If the Arbiter granted the bus to a Requester with level 2, the next most higher level is the level 1, with all other level shifted respectively in the level priority.

- VME Bus Timer: BTO(16 to 112), the timeout period can be programmed from 16µs to 112µs (in 16µs increment).

- IACK daisy-chain driver.

- 16 MHz system clock generator.

Please refer to the VAM and XVCR registers description for more information.

3.15.9 Bridge DMA Controller

The 60x-to-VME bridge includes a 1-channel DMA controller to perform SRAM-to-VME and VME-to-SRAM transfers without CPU utilization. A set of seven registers allows to configure and control DMA transfers. The SRAM and VME start addresses are specified in two 16-bit registers for each. Each address is split in high order and low order address registers. An 8-bit register specifies the data width and VME cycle type of transfer; the address modifier code is automatically selected based on this register setting. A 16-bit register specifies the length of transfer (the number of words to transfer) to transfer up to 256 kBytes in 4-byte (word) increment; it can be updated or not to reflect the progression of the DMA transaction. A control and status register allows to start the DMA transaction after all other registers have been set up. It is also possible to stop the transfer before completion. If enabled an interrupt is sent to the host processor at the end of the DMA transaction. A status bit can be read to check that the transaction completed without error.

Please refer to the DMASAH, DMASAL, DMAVAH, DMAVAL, DMAVSS, DMASIZ, and DMACSR registers description for more information.

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4 Bridge Registers

The bridge of the VSBC-6872 contains registers to configure and control the bridge VME modules and board specific features.
All these registers are 8-bit wide, unless otherwise noted and can be accessed from the MPC with Chip Select 4. A subset of these registers is also accessible from the VME through A16 addressing. The slave A16 base address can be hardware-defined by the user with 5 jumpers (J2). Please refer to 7.2 Board jumpers for detailed information.

The table below lists the bridge registers with their address offset:

Local Offset	VME offset	Register	Name	Page
0x1001	0x09	Software Reset Register	SRESR	38
0x1011	-	Switch Position Register	SWPR	38
0x1021	-	Board-Specific Configuration Register	BSCR	39
0x1025	-	Bridge Firmware Version Register	FVER	48
0x1051	-	VME Master Control Register	VMBA	40
0x1053	-	VME Arbiter Mode Register	VAM	40
0x1055	-	VME Master: A32 Base address for window A	VMBMA	41
0x1057	-	VME Master: A32 Base address for window B	VMBMB	41
0x105b	-	VME Master: Address Modifier for window A	VMAMA	41
0x105d	-	VME Master: Address Modifier for window B	VMAMB	42
0x1061	-	VME Interrupt Handler: Incoming Interrupt Requests	VHIL	42
0x1063	-	VME Interrupt Handler Mask Register	VHM	43
0x1065	0x01	VME Slave Mailbox Register	VSMAIL	45
0x1067	-	VME Interrupter Command Register	VINTER	44
0x1069	0x03	VME Slave Base Window A24 Register	VSBA24	46
0x106b	0x05	VME Slave Window management Register	VSWA24	47
0x106d	0x07	VME Interrupter Vector Register	VIVEC	44
0x1073-0x107f	-	VME interrupt Handler: Vector Register	VHV	43
0x1081	-	Extended VME Configuration Register	XVCR	47
0x1083	0x0d	VME Interrupter interrupt level Register	VIL	45
0x1085	-	Jumper Position Register	JMPR	48
0x1087	-	Serial Communication Controller Control Register	SCCR	49
0x1089	0x0b	Extended SRAM Access Control Register	XSAV24	50
0x1090	-	DMA SRAM Start Address High order bits Register	DMASAH	51
0x1092	-	DMA SRAM Start Address Low order bits Register	DMASAL	51
0x1094	-	DMA VME Start Address High order bits Register	DMAVAH	52
0x1096	-	DMA VME Start Address Low order bits Register	DMAVAL	52
0x1099	-	DMA VME Addressing Space and Data Size Register	DMAVSS	53
0x109a	-	DMA Transfer Size Register	DMASIZ	54
0x109d	-	DMA Control and Status Register	DMACSR	55

Table 17 - Bridge registers list

Local offset is the offset from MPC8270 CS4.
VME offset is the offset from A16 VME slave base address.

A detailed description of each register is given in the following pages.

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SRESR *Software Reset Register*

Address from MPC: CS4 + 0x1001
Address from VME: A16 base address + 0x09
Access type: Write Only

This register allows to generate an on-board Software or Power-On Reset.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	x	x	x	x	SRESET	PORESET	x	x
Reset	x	x	x	x	0	0	x	x

x: reserved

Name	Description
SRESET	Software Reset Writing a '1' generates a Software Reset
PORESET	Power-On Reset Writing a '1' generates a Power-On Reset

☞ These bits are automatically cleared after completion.

SWPR *Switch Position Register*

Address from MPC: CS4 + 0x1011
Address from VME: N/A
Access type: Read Only

This register gives the state of the VME SYSFAIL signal and of the user-configurable switch (3 jumpers).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	SYSFAIL	x	x	x	x	RC2	RC1	RC0
Reset	n/d	x	x	x	x	n/d	n/d	n/d

x: reserved, a zero is returned when read
n/d: not defined, is not determined by bridge at reset

Name	Description
SYSFAIL	VME SYSFAIL signal state
RC(2..0)	3-bit User code

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BSCR *Board-Specific Configuration Register*

Address from MPC: CS4 + 0x1021
Address from VME: N/A
Access type: Read/Write

This register allows the user to enable different board specific features.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	LOCK	WDEN	x	BMEN	BMT	BMVA
Reset	x	x	0	0	x	0	0	0

x: reserved, a zero is returned when read

Name	Description
LOCK	Locked access on shared memory 0: Normal operation, the Flash, RTC, and SRAM are shared 1: Access to memory (Flash, RTC, and SRAM) is locked by the MPC
WDEN	Watchdog Enable 0: RTC interrupt does not generate a Power-On Reset 1: RTC interrupt generates a Power-On Reset
BMEN	60x Bus Monitor Enable 0: Disabled 1: Enabled
BMT	60x Bus Monitor Timeout 0: 32 µs 1: 256 µs
BMVA	60x Bus Monitor on VME Master Access Enable Enables/disables the 60x bus monitor when the MPC accesses the VMEbus. 0: Disabled 1: Enabled



The LOCK function prevents access to the local shared memory from any VME Master as long as this bit is set to 1. If this function is kept active for a period of time longer than the VME Bus Timer timeout period, a VME Bus Error may be generated in case of a VME Master attempting to access the shared memory.
It is our recommendation to keep this function active for the shortest possible time.



The PowerQUICC II has a bus monitor for the 60x bus to ensure that each bus cycle is terminated within a reasonable period. The maximum timeout period is 2040 system bus clocks, that is 20.4 µs at 100 MHz. Since there is no guarantee to receive a VME bus grant within this time, the 60x-to-VME bridge includes a bus monitor that performs the same task with a timeout period extended to 32 or 256 µs. It can even be separately disabled on VME accesses. If you enable the 60x Bus Monitor of the bridge, make sure the Bus Monitor of the host processor is disabled (SYPCR[PBME] set to zero).

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VMBA *VME Master Control Register*

Address from MPC: CS4 + 0x1051
Address from VME: N/A
Access type: Read/Write

This register is used to configure the VME Requester (release mode and request level) and activate the RMW cycle (on master access).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	RM	RL1	RL0	x	x	x	x	RMW
Reset	1	1	1	x	x	x	x	0

x: reserved, a zero is returned when read

Name	Description
RM	Requester Release Mode 0: Release On Request (ROR) 1: Release When Done (RWD)
RL(1..0)	Requester Request Level 00: Bus Request 0 01: Bus Request 1 10: Bus Request 2 11: Bus Request 3
RMW	VME Read-Modify-Write Cycle Enables a single RMW cycle for a VME Master access 0: Normal Cycle 1: RMW Cycle

☞ For the RMW cycle to execute correctly on the VMEbus, the host processor must perform a Read cycle directly followed by a Write Cycle at the same location with the same Transfer Size. Before starting a RMW cycle, the host processor must set VMBA[RMW] to '1'. This bit is automatically cleared at the end of the cycle and must be set again for a new RMW cycle.
Note: during RMW cycles, all interrupts on the host CPU should be masked.

VAM *VME Arbiter Mode Register*

Address from MPC: CS4 + 0x1053
Address from VME: N/A
Access type: Read/Write

This register is used to configure the VME Arbiter mode. The arbiter is active when the board is configured as system controller (slot 1 jumper).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	VAM1	VAM0	x	x	x	x	x	x
Reset	0	1	x	x	x	x	x	x

x: reserved, a zero is returned when read

Name	Description
VAM(1..0)	VME Arbiter Mode 00: SGL: Single, uses Bus Request level 3 only 01: PRI: Priority, Bus Request level 3 has the highest priority 10: RRS: Round-Robin-Select 11: Reserved

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VMBMA *VME Master: A32 Base address for window A*

Address from MPC: CS4 + 0x1055
Address from VME: N/A
Access type: Read/Write

This register specifies the high-order address bits for VME Master A32 accesses (window A).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	VA31	VA30	VA29	VA28	VA27	VA26	VA25
Reset	x	0	0	0	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
VA(31..25)	VME Address bits A31..A25

VMBMB *VME Master: A32 Base address for window B*

Address from MPC: CS4 + 0x1057
Address from VME: N/A
Access type: Read/Write

This register specifies the high-order address bits for VME Master A32 accesses (window B).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	VA31	VA30	VA29	VA28	VA27	VA26	VA25
Reset	x	0	0	0	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
VA(31..25)	VME Address bits A31..A25

VMAMA *VME Master: AM for window A*

Address from MPC: CS4 + 0x105b
Address from VME: N/A
Access type: Read/Write

This register specifies the low-order bits of the VME Address Modifier (window A).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	AM2	AM1	AM0	x	x	x
Reset	x	x	0	0	1	x	x	x

x: reserved, a zero is returned when read

Name	Description
AM(2..0)	VME Address Modifier bits AM2..AM0

AM5..AM3 are automatically selected based on the VME addressing space (A32, A24, A16).

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VMAMB *VME Master: AM for window B*

Address from MPC: CS4 + 0x105d
Address from VME: N/A
Access type: Read/Write

This register specifies the low-order bits of the VME Address Modifier (window B).

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	AM2	AM1	AM0	x	x	x
Reset	x	x	0	0	1	x	x	x

x: reserved, a zero is returned when read

Name	Description
AM(2..0)	VME Address Modifier bits AM2..AM0

AM5..AM3 are automatically selected based on the VME addressing space (A32, A24, A16).

VHIL *VME Interrupt Handler: Incoming Interrupt Requests*

Address from MPC: CS4 + 0x1061
Address from VME: N/A
Access type: Read Only

This register indicates which VME interrupt request line is currently active.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1
Reset	x	n/d	n/d	n/d	n/d	n/d	n/d	n/d

x: reserved, a one is returned when read
n/d: not defined, is not determined by bridge at reset

Name	Description
IRQ(7..1)	VME Interrupt Request lines (active low)

☞ The Interrupt Handler Mask (see VHM register) is applied on this register.

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VHM *VME Interrupt Handler Mask Register*

Address from MPC: CS4 + 0x1063
Address from VME: N/A
Access type: Read/Write

This register is used to mask incoming interrupt requests coming from the VMEbus. It selects which IRQ lines are monitored by the VME Interrupt Handler.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	M7	M6	M5	M4	M3	M2	M1
Reset	x	1	1	1	1	1	1	1

x: reserved, a one is returned when read

Name	Description
Mx	Interrupt Mask 0: IRQx is enabled 1: IRQx is masked

VHV *VME Interrupt Handler: Vector Register*

Address from MPC: CS4 + 0x1073 to CS4 + 0x107f
Address from VME: N/A
Access type: Read Only

Reading this register starts a VME Interrupt Acknowledge (IACK) cycle controlled by the bridge Interrupt Handler. It then contains the status/ID returned by the acknowledged interrupter to the interrupt handler.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	V7	V6	V5	V4	V3	V2	V1	V0
Reset	n/d	n/d	n/d	n/d	n/d	n/d	n/d	n/d

n/d: not defined, is not determined by bridge at reset

Name	Description
V(7..0)	8-bit status/ID read during IACK cycle

The offset used to access this register determines the level of interrupt to acknowledge:

VHV offset	VME IRQ level to acknowledge
CS4 + 0x1073	1
CS4 + 0x1075	2
CS4 + 0x1077	3
CS4 + 0x1079	4
CS4 + 0x107b	5
CS4 + 0x107d	6
CS4 + 0x107f	7



An IACK cycle is started only when a VME interrupt is pending on the level corresponding to the VHV offset accessed. In the case there is no pending IRQ, no IACK cycle is started and value 0x00 is returned. Note that the VME interrupt must not be masked to be acknowledged (report to VHM register description).
Reading this register when there is no pending IRQ is not recommended.

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VINTER *VME Interrupter Command Register*

Address from MPC: CS4 + 0x1067
Address from VME: N/A
Access type: Read/Write

This register directs the VME Interrupter to generate an interrupt on the level programmed in VIVEC[IL] or VIL[IL].

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	x	x	x	x	VINTER
Reset	x	x	x	x	x	x	x	0

x: reserved, a zero is returned when read

Name	Description
VINTER	VME Interrupt Command Writing any value generates a VME interrupt, this bit is cleared at the completion of the VME Interrupt Acknowledge (IACK) cycle.

☞ It is our recommendation to set VINTER to one for starting the VME interrupt in order to check the IACK cycle completion by reading back a zero.

VIVEC *VME Interrupter Vector*

Address from MPC: CS4 + 0x106d
Address from VME: A16 base address + 0x07
Access type: Read/Write

This register specifies the status/ID sent by the VME Interrupter when responding to an IACK cycle. The three upper bits also specify the IRQ level of the interrupter.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	IL2/Vec7	IL1/Vec6	IL0/Vec5	Vec4	Vec3	Vec2	Vec1	Vec0
Reset	0	0	0	0	0	0	0	0

Name	Description
IL(2..0)	Interrupt Request Level of the VME Interrupter The IRQ level is coded on 3 bits from 1 to 7. If IL=000, no IRQ is sent when writing to the VINTER register.
Vec(7..0)	Interrupter status/ID

☞ The three upper bits of this register have a double functionality: they specify the IRQ level and they are part of the status/ID word. This functionality is kept for compatibility purpose. However if the user's application requires a full 8-bit status/ID independent of the IRQ level, it is possible to specify the IRQ level in the VIL register instead. It is our recommendation to do so in new software developments. See also VIL register description.

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VIL *VME Interrupter Interrupt Level Register*

Address from MPC: CS4 + 0x1083
Address from VME: A16 base address + 0x0d
Access type: Read/Write

This register specifies the IRQ level of the VME Interrupter.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	IL2	IL1	IL0	EN	x	x	x	x
Reset	0	0	0	0	x	x	x	x

x: reserved, a zero is returned when read

Name	Description
IL(2..0)	Interrupt Request Level of the VME Interrupter The IRQ level is coded on 3 bits from 1 to 7. If IL=000, no IRQ is sent when writing to the VINTER register.
EN	Register settings Enable 0: Interrupter IRQ level is specified in VIVEC register 1: Interrupter IRQ level is specified by IL in this register (VIVEC[IL] can take any values and is used only as part of the interrupter status/ID).



The Interrupter IRQ level can be defined either by VIVEC[IL] or by VIL[IL]. The state of VIL[EN] determines which one is used. Specifying IL in VIVEC is kept for compatibility reasons. If a full 8-bit status/ID independent of the IRQ level is required use VIVEC to specify the status/ID and VIL to configure the IRQ level. It is our recommendation to specify the Interrupter IRQ level in the VIL register. See also VIVEC register description.

VSMAIL *VME Slave Mailbox*

Address from MPC: CS4 + 0x1065
Address from VME: A16 base address + 0x01
Access type: Read/Write

This register implements a single mailbox.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Name	Description
D(7..0)	Mailbox data

When an external VME master writes any value in this register, and the VSBA24[MailOn] bit is set, a local interrupt is sent to the host processor (IRQ6).
To clear this interrupt, the host processor must write any value to this register.



The register content is only affected by a VME write access (i.e. host processor write access only clears MPC IRQ6 and does not change register's value).

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VSBA24 *VME Slave Base Window A24*

Address from MPC: CS4 + 0x1069
Address from VME: A16 base address + 0x03
Access type: Read/Write

This register specifies the VME Slave base address in A24 addressing space.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	WinA24On	MailOn	VME_lock	x	A23	A22	A21	A20
Reset	0	0	0	x	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
WinA24On	Activation of the VME Slave A24 Window 0: inactive 1: active
MailOn	Activation of the Mailbox function 0: inactive 1: active (IRQ sent to host processor when mailbox is accessed)
VME_lock	VME Lock Mode 0: normal VME access 1: VMEbus locked (BBSY* is kept asserted)
A(23..20)	VME Slave Base Address (A24 addressing space) 0000: 0x00'0000 0001: 0x10'0000 0010: 0x20'0000 0011: 0x30'0000 0100: 0x40'0000 0101: 0x50'0000 0110: 0x60'0000 0111: 0x70'0000 1000: 0x80'0000 1001: 0x90'0000 1010: 0xA0'0000 1011: 0xB0'0000 1100: 0xC0'0000 1101: 0xD0'0000 1110: 0xE0'0000 1111: 0xF0'0000

☞ The VME lock mode provides a lock mechanism of the VMEbus by signaling the VME requester to keep BBSY* asserted at the end of the current cycle. It gives the host processor an exclusive access to the VMEbus. VME_lock must be set back to '0' to release the bus. Abuse of this function may degrade system performance.
Note that VME_lock cannot be accessed in write mode from the VME.

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VSWA24 *VME Slave Window A24 management Register*

Address from MPC: CS4 + 0x106b
Address from VME: A16 base address + 0x05
Access type: Read/Write

This register contains the local offset for the SRAM and Flash devices (accessed through the VME Slave A24 window).

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	x	SRA19	FLA23	FLA22	FLA21	FLA20	FLA19	FLA18
Reset	x	0	0	0	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
SRA19	Corresponding high order local address bit for SRAM memory
FLA(23..18)	Corresponding high order local address bits for Flash memory

XVCR *Extended VME Configuration Register*

Address from MPC: CS4 + 0x1081
Address from VME: N/A
Access type: Read/Write

This register provides extended configuration capabilities for VME system adjustment.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	BTO2	BTO1	BTO0	x	ATO1	ATO0	x	FAIR
Reset	0	1	1	x	0	1	x	1

x: reserved, a zero is returned when read

Name	Description
BTO(2..0)	VME Bus Timer timeout period 000: 16 µs 001: 32 µs 010: 48 µs 011: 64 µs 100: 80 µs 101: 96 µs 110: 112 µs 111: disabled
ATO(1..0)	VME Arbiter timeout period 00: disabled 01: 16 µs 10: 24 µs 11: 32 µs
FAIR	VME Requester request mode 0: normal mode 1: FAIR mode

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FVER *Bridge Firmware Version Register*

Address from MPC: CS4 + 0x1025
Address from VME: N/A
Access type: Read Only

This register gives information on the Bridge firmware version.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	FVER7	FVER6	FVER5	FVER4	FVER3	FVER2	FVER1	FVER0
Reset	n/d	n/d	n/d	n/d	n/d	n/d	n/d	n/d

n/d: not determined by bridge at reset, Actis internal number

Name	Description
FVER(7..0)	Bridge firmware version

JMPR *Jumper Position Register*

Address from MPC: CS4 + 0x1085
Address from VME: N/A
Access type: Read Only

This register provides a software mean for reading the jumper configuration.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	SCON	BOOT	VSBA15	VSBA14	VSBA13	VSBA12	VSBA11
Reset	x	n/d	n/d	n/d	n/d	n/d	n/d	n/d

x: reserved, a zero is returned when read
n/d: not defined, is not determined by bridge at reset

Name	Description
SCON	VME System Controller jumper 0: enabled (board in slot 1) 1: disabled
BOOT	Flash Boot Bank selection jumper 0: Boot bank is Flash 1 1: Boot bank is Flash 0
VSBA(15..11)	A16 VME Slave Base Address jumpers

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SCCR *Serial Communication Controller Control Register*

Address from MPC: CS4 + 0x1087
Address from VME: N/A
Access type: Read/Write

This register is used to configure the 4 Serial Communication ports mode.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	MODE4	EN4	MODE3	EN3	MODE2	EN2	MODE1	EN1
Reset	0	0	0	0	0	0	0	0

Name	Description
MODE4	SCC4 Mode 0: RS-232 1: RS-422/RS-485/V.35
EN4	SCC4 Enable 0: disabled 1: enabled
MODE3	SCC3 Mode 0: RS-232 1: RS-422/RS-485/V.35
EN3	SCC3 Enable 0: disabled 1: enabled
MODE2	SCC2 Mode 0: RS-232 1: RS-422/RS-485/V.35
EN2	SCC2 Enable 0: disabled 1: enabled
MODE1	SCC1 Mode 0: RS-232 1: RS-422/RS-485/V.35
EN1	SCC1 Enable 0: disabled 1: enabled

There are two external jumpers for each Serial Communication port. One specifies the SCC mode (RS-232 or RS-422/RS-485/V.35) and the other determines whether the mode selection is taken from the jumper or from SCCR[MODE]. Please refer to 7.3 Serial Communication port jumpers for jumper configuration.

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XSAV24 *Extended SRAM Access from VME A24 Control Register*

Address from MPC: CS4 + 0x1089
Address from VME: A16 base address + 0x0b
Access type: Read/Write

This register specifies a single 1MB/2MB A24 window for accessing the whole SRAM memory.

8270	D8	D9	D10	D11	D12	D13	D14	D15
VME	D7	D6	D5	D4	D3	D2	D1	D0
Value	EN	SIZE	SRA20	x	A23	A22	A21	A20
Reset	0	0	0	x	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
EN	VME Slave A24 window for extended SRAM access Enable 0: disabled 1: enabled
SIZE	Size of VME Slave A24 window 0: 1MB 1: 2MB
SRA20	SRAM Address MSB (used for a 1MB window on 2MB SRAM) 0: lower SRAM memory 1: upper SRAM memory
A(23..20)	VME Slave A24 Base Address for extended SRAM access Note: if XSAV24[SIZE]=1, A20 is ignored. 1MB window 2MB window 0000: 0x00'0000 000x: 0x00'0000 0001: 0x10'0000 0010: 0x20'0000 001x: 0x20'0000 0011: 0x30'0000 0100: 0x40'0000 010x: 0x40'0000 0101: 0x50'0000 0110: 0x60'0000 011x: 0x60'0000 0111: 0x70'0000 1000: 0x80'0000 100x: 0x80'0000 1001: 0x90'0000 1010: 0xA0'0000 101x: 0xA0'0000 1011: 0xB0'0000 1100: 0xC0'0000 110x: 0xC0'0000 1101: 0xD0'0000 1110: 0xE0'0000 111x: 0xE0'0000 1111: 0xF0'0000

This register allows to share 1MB or 2MB (if mounted) of SRAM memory. The window defined by VSBA24 shares only 512kB of SRAM memory.



Since there are two different A24 Slave windows (specified by VSBA24 and XSAV24), it is important to be careful when defining them in order to avoid overlapping. An overlap of the slave windows may result in improper operation.

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DMASAH *DMA SRAM Start Address High order bits Register*

Address from MPC: CS4 + 0x1090
Address from VME: N/A
Access type: Read/Write

This register specifies the high order bits of the SRAM start address used by the DMA controller.
This is a 16-bit register.

8270	D0	D1	D2	D3	D4	D5	D6	D7
Value	x	x	x	x	x	x	x	x
Reset	x	x	x	x	x	x	x	x

x: reserved, a zero is returned when read

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	x	x	A11	A12	A13	A14	A15
Reset	x	x	x	0	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
A(11..15)	SRAM Start Address, high order bits

DMASAL register specifies the low order bits of the SRAM start address.

DMASAL *DMA SRAM Start Address Low order bits Register*

Address from MPC: CS4 + 0x1092
Address from VME: N/A
Access type: Read/Write

This register specifies the low order bits of the SRAM start address used by the DMA controller.
This is a 16-bit register.

8270	D0	D1	D2	D3	D4	D5	D6	D7
Value	A16	A17	A18	A19	A20	A21	A22	A23
Reset	0	0	0	0	0	0	0	0

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	A24	A25	A26	A27	A28	A29	x	x
Reset	0	0	0	0	0	0	x	x

x: reserved, a zero is returned when read

Name	Description
A(16..29)	SRAM Start Address, low order bits The SRAM start address must be aligned on a word (4-byte) boundary (that is, bits A(30..31) are zero)

DMASAH register specifies the high order bits of the SRAM start address.

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DMAVAH *DMA VME Start Address High order bits Register*

Address from MPC: CS4 + 0x1094
Address from VME: N/A
Access type: Read/Write

This register specifies the high order bits of the VME start address used by the DMA controller.
This is a 16-bit register.

8270	D0	D1	D2	D3	D4	D5	D6	D7
Value	A31	A30	A29	A28	A27	A26	A25	A24
Reset	0	0	0	0	0	0	0	0

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	A23	A22	A21	A20	A19	A18	A17	A16
Reset	0	0	0	0	0	0	0	0

Name	Description
A(31..16)	VME Start Address, high order bits



A(31..24) are used only for A32 addressing and are ignored for A24 and A16 addressing.
A(23..16) are used for A32 and A24 addressing and are ignored for A16 addressing.

DMAVAL register specifies the low order bits of the VME start address.

DMAVAL *DMA VME Start Address Low order bits Register*

Address from MPC: CS4 + 0x1096
Address from VME: N/A
Access type: Read/Write

This register specifies the low order bits of the VME start address used by the DMA controller.
This is a 16-bit register.

8270	D0	D1	D2	D3	D4	D5	D6	D7
Value	A15	A14	A13	A12	A11	A10	A9	A8
Reset	0	0	0	0	0	0	0	0

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	A7	A6	A5	A4	A3	A2	x	x
Reset	0	0	0	0	0	0	x	x

x: reserved, a zero is returned when read

Name	Description
A(15..2)	VME Start Address, low order bits The VME start address must be aligned on a word (4-byte) boundary (that is, bit A1 is zero)

DMAVAH register specifies the high order bits of the VME start address.

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DMAVSS *DMA VME Addressing Space and Data Size Register*

Address from MPC: CS4 + 0x1099
Address from VME: N/A
Access type: Read/Write

This register specifies which type of VME transfer is executed during a DMA transaction. It determines the Address Modifier code and the width of the data transfer.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	x	SIZE	SPACE1	SPACE0	x	SUP	x	PROGD
Reset	x	0	0	0	x	0	x	1

x: reserved, a zero is returned when read

Name	Description
SIZE	Transfer Data Size 0: 32-bit (D32) 1: 16-bit (D16)
SPACE(1..0)	VME Addressing Space 00: A32 01: reserved 10: A16 11: A24
SUP	Supervisory/Non-privileged Access 0: Non-privileged 1: Supervisory
PROGD	Program/Data Access 0: Program 1: Data

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DMASIZ *DMA Transfer Size Register*

Address from MPC: CS4 + 0x109a
Address from VME: N/A
Access type: Read/Write

This register specifies the number of words (4-byte) to be transferred during a DMA transaction. This is a 16-bit register.

8270	D0	D1	D2	D3	D4	D5	D6	D7
Value	D15	D14	D13	D12	D11	D10	D9	D8
Reset	0	0	0	0	0	0	0	0

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Name	Description
D(15..0)	DMA Transfer Size Number of words to be transferred (0x0001 transfers 4 bytes and 0x0000 transfers 256 Kbytes).

☞ If DMACSR[DSUEN] is set, the content of this register is updated during DMA transfer to reflect the state of the transaction. If the DMA transfer is stopped (either by user or due to an error), this register gives the number of words that remain to be transferred. When the DMA transfer completes successfully, this register contains the value 0x0000.
If DMACSR[DSUEN] is not set, the content of DMASIZ is unchanged.

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DMACSR *DMA Control and Status Register*

Address from MPC: CS4 + 0x109d
Address from VME: N/A
Access type: Read/Write

This register controls the DMA controller and reports error and done status.

8270	D8	D9	D10	D11	D12	D13	D14	D15
Value	IEN	DSUEN	x	x	IRQ	ERR	DIR	START
Reset	0	0	x	x	0	0	0	0

x: reserved, a zero is returned when read

Name	Description
IEN	IRQ Enable 0: disabled 1: enabled
DSUEN	DMA Size Register Update Enable 0: DMASIZ register is kept unchanged 1: DMASIZ register is updated during DMA transaction
IRQ	IRQ status 0: IRQ inactive 1: IRQ active, DMA transaction is done This bit and the IRQ are cleared by writing a '1'.
ERR	DMA Transfer Error 0: no error 1: an error occurred during DMA transaction This bit is cleared by writing a '1'. Also, starting a new DMA transfer automatically clears this bit.
DIR	Transfer Direction 0: from SRAM to VME 1: from VME to SRAM
START	DMA Start 0: DMA is done 1: DMA is in progress Writing a '1' starts a DMA transfer. A pending DMA transaction can be stopped by writing a '0'.



If DMACSR[IEN] is set, a local interrupt is sent to the host processor (IRQ1) when the DMA transfer is done and DMACSR[IRQ] is set. The interrupt is cleared when writing a '1' to DMACSR[IRQ].

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5 Board resources

5.1 Peripheral Chip Select

The MPC8270 provides several on-board peripheral devices, where the selection is done by chip select signals present on the 60x Bus Controller interface.
Each chip select is software programmable and provides the memory address range and timing related setting for the corresponding peripheral.
The following table gives the chip select association with the on-board peripherals and the ECMon default settings.

Chip select signal	Peripheral	BR(x)	OR(x)
CS0	Boot Device (Flash)	0xfe001901	0xff800cfc
CS1	SDRAM	0x00000041	0xf8002b00
CS2	Flash memory	0xfc001801	0xff800cfc
CS3	Real-Time Clock	0xfa100801	0xffff8cfc
CS4	Bridge Registers	0xfa001081	0xffff8104
CS5	not used	-	-
CS6	VME Master A	0xd0001081	0xfc000104
CS7	VME Master B	0xe0001881	0xfc000104
CS8	not used	-	-
CS9	SRAM	0xfb001801	0xfff00cfc
CS10	CompactFlash CS0	0xfa2010a1	0xffff8100
CS11	CompactFlash CS1	0xfa2090a1	0xffff8100

Table 18 - Chip Select assignment

5.2 Memory map

Since the peripheral selection is controlled by chip select signal, the VSBC-6872 supports a fully software programmable memory map. The VSBC-6872 is provided with pre-installed board monitor software called ECMon, this utility supports low-level hardware setting and provides user free setting board.

The following table gives the default memory map definition set by the ECMon board monitor.

Peripheral	Port size	Mode	CPU Address Range
MPC8270 Internal Memory	-	R/W	0xfff00000..0xfff2ffff
SDRAM Memory	64-bit	R/W	0x00000000..0x07ffffff
Boot Device (Flash)	32-bit	R/W	0xfe000000..0xfe7fffff
Flash Memory	32-bit	R/W	0xfc000000..0xfc7fffff
Real-Time Clock	8-bit	R/W	0xfa100000..0xfa107fff
Bridge Registers	16-bit	R/W	0xfa000000..0xfa007fff
CompactFlash CS0	16-bit	R/W	0xfa200000..0xfa207fff
CompactFlash CS1	16-bit	R/W	0xfa208000..0xfa20ffff
VME/A32 Master A	16-bit	R/W	0xd0000000..0xd1ffffff
VME/A24 Master A	16-bit	R/W	0xd2000000..0xd2ffffff
VME/A16 Master A	16-bit	R/W	0xd3000000..0xd300ffff
VME/A32 Master B	32-bit	R/W	0xe0000000..0xe1ffffff
VME/A24 Master B	32-bit	R/W	0xe2000000..0xe2ffffff
VME/A16 Master B	32-bit	R/W	0xe3000000..0xe300ffff
SRAM Memory	32-bit	R/W	0xfb000000..0xfb0fffff
PCI I/O Space	32-bit	R/W	0xfa800000..0xfabfffff
PCI I/O Memory Space	32-bit	R/W	0x80000000..0x87ffffff
PCI Prefetch Memory Space	32-bit	R/W	0x88000000..0x8fffffff

Table 19 - Memory map



This table represents the optimized programmed values. It is not recommended to change these parameters. Since some specific applications can require a different setting, this memory map setting need to be defined by experimented software engineers, for further assistance contact ACTIS Computer technical support.

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5.3 Interrupt sources

The following table provides the interrupt request signal assignment with their corresponding sources.

MPC IRQ#	Source
0	not used
1	Bridge DMA Controller/VME Interrupt Handler
2	PMC INTA
3	PMC INTB/JTAG probe
4	PMC INTC
5	PMC INTD
6	VME Mailbox
7	S-ATA Controller

Table 20 - Interrupt sources

The Fast Ethernet PHY transceivers use the following MPC I/O ports to send their interrupt:

MPC I/O port C #	Source
0	FCC1
1	FCC2
2	FCC3

Table 21 - FCC interrupt

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5.4 Multiplexed General Purpose I/O ports

The following tables give the pin assignment of MPC8270 I/O ports:

Port A	Description
0	not used
1	not used
2	not used
3	not used
4	not used
5	not used
6	not used
7	not used
8	SMC2_RXD
9	SMC2_TXD
10	not used
11	not used
12	not used
13	not used
14	FCC1_MII_RXD3
15	FCC1_MII_RXD2
16	FCC1_MII_RXD1
17	FCC1_MII_RXD0
18	FCC1_MII_TXD0
19	FCC1_MII_TXD1
20	FCC1_MII_TXD2
21	FCC1_MII_TXD3
22	FCC_MDIO
23	FCC_MDC
24	not used
25	not used
26	FCC1_MII_RX_ER
27	FCC1_MII_RX_DV
28	FCC1_MII_TX_EN
29	FCC1_MII_TX_ER
30	FCC1_MII_CRS
31	FCC1_MII_COL

Port B	Description
4	FCC3_MII_TXD3
5	FCC3_MII_TXD2
6	FCC3_MII_TXD1
7	FCC3_MII_TXD0
8	FCC3_MII_RXD0
9	FCC3_MII_RXD1
10	FCC3_MII_RXD2
11	FCC3_MII_RXD3
12	FCC3_MII_CRS
13	FCC3_MII_COL
14	FCC3_MII_TX_EN
15	FCC3_MII_TX_ER
16	FCC3_MII_RX_ER
17	FCC3_MII_RX_DV
18	FCC2_MII_RXD3
19	FCC2_MII_RXD2
20	FCC2_MII_RXD1
21	FCC2_MII_RXD0
22	FCC2_MII_TXD0
23	FCC2_MII_TXD1
24	FCC2_MII_TXD2
25	FCC2_MII_TXD3
26	FCC2_MII_CRS
27	FCC2_MII_COL
28	FCC2_MII_RX_ER
29	FCC2_MII_TX_EN
30	FCC2_MII_RX_DV
31	FCC2_MII_TX_ER

Table 22 - GPIO port A & B controller setting



'not used' I/Os must be configured as input

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Port C	Description
0	/FCC1_MII_IRQ
1	/FCC2_MII_IRQ
2	/FCC3_MII_IRQ
3	/IRQ_RTC
4	not used
5	not used
6	not used
7	/IRQ_CF
8	/SCC4_CD
9	/SCC4_CTS
10	/SCC3_CD
11	/SCC3_CTS
12	/SCC2_CD
13	/SCC2_CTS
14	/SCC1_CD
15	/SCC1_CTS
16	FCC3_MII_RXCLK
17	FCC2_MII_TXCLK
18	FCC2_MII_RXCLK
19	FCC3_MII_TXCLK
20	not used
21	/LED_AUX1
22	FCC1_MII_RXCLK
23	FCC1_MII_TXCLK
24	/LED_AUX0
25	SCC4_RXC
26	SCC3_RXC
27	SCC3_BRGO (SCC3_TXC)
28	SCC2_RXC
29	SCC1_RXC
30	/SCC4_DTR
31	SCC1_BRGO (SCC1_TXC)

Port D	Description
4	not used
5	not used
6	not used
7	RTC_WDI
8	SMC1_RXD
9	SMC1_TXD
10	SCC4_BRGO (SCC4_TXC)
11	/SCC1_DTR
12	/SCC2_DTR
13	/SCC3_DTR
14	I2C_SCL
15	I2C_SDA
16	SPI_MISO
17	SCC2_BRGO/SPI_MOSI
18	SPI_CLK
19	/SPI_SEL
20	/SCC4_RTS
21	SCC4_TXD
22	SCC4_RXD
23	/SCC3_RTS
24	SCC3_TXD
25	SCC3_RXD
26	/SCC2_RTS
27	SCC2_TXD
28	SCC2_RXD
29	/SCC1_RTS
30	SCC1_TXD
31	SCC1_RXD

Table 23 - GPIO port C & D controller setting



'not used' I/Os must be configured as input



Signals CD and DTR of the SCCs are not used/not routed to the serial port connector. CD is pulled-down to GND and DTR is left open.



*For detailed register description, please consult the Freescale literature "*MPC8260 PowerQUICC II™ Family Reference Manual*".*

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6 Technical Characteristics

DC electrical characteristics and operating conditions

$0 \leq T_A \leq 70$ °C; without PMC module installed

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY				
+5 V	4.875	5	5.25	V
+12 V	11.64	12	12.6	V
-12 V	–11.64	–12	–12.6	V
Icc_{+5V}		1.2	2.5	A
Icc_{+12V}	N/A	N/A	N/A	A
Icc_{-12V}	N/A	N/A	N/A	A

On-board peripherals

$0 \leq T_A \leq 70$ °C

PARAMETER	MIN	TYP	MAX	UNITS
MPC8270 processor *based on MPC8270ZUUPE device*				
60x CLK		100		MHz
MPC8270 CPU clock		450		MHz
MPC8270 CPM clock		250		MHz
PCI clock		62.5		MHZ

Environmental characteristics

PARAMETER	MAX
Operating	
Commercial temperature Industrial temperature	0°C to +70°C, forced air cooling -25°C to +85°C, forced air cooling
Airflow	10 CFM
Altitude	0 to 10,000 ft
Humidity (NC)	0% to 90%
Vibration	0.5G RMS 20-2000 Hz random
Shock	20G, 11 ms, ½ sine
Non-Operating	
Temperature	-40°C to +85°C

Mechanical characteristics

PARAMETER	MAX
Board Height	233.4 mm (9.2 in.)
Board Depth	160.0 mm (6.3 in.)
Front Panel Height	262 mm (10.3 in.)
Front Panel Width	20.2 mm (0.8 in.)
Max. Comp, Height	13.7 mm (0.54 in.)
Weight	0.35 kg

General characteristics

PARAMETER	MAX
MTBF calculated with 90% confidence Based on the Mil-Hdbk-217 FN2 specification, with the parameters: 1. Environment: GB, GC - Ground Benign, Controlled 2. Temperature: 30 °C	tbd

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7 Hardware description

7.1 Front panel connectors

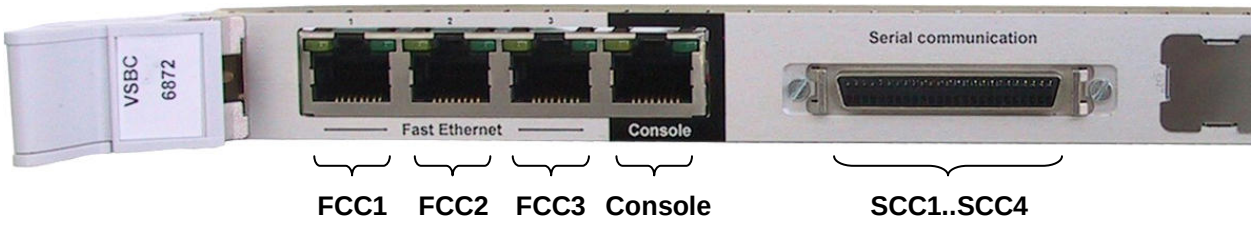


Figure 13 - Front panel connectors

7.1.1 Fast Ethernet port FCC1..FCC3

The MPC8270 processor supports up to three IEEE 802.3 Fast Ethernet ports. These network links are available with front connection on 8-pin RJ45 connectors.

See below the RJ45 8-pin connector pin assignment.

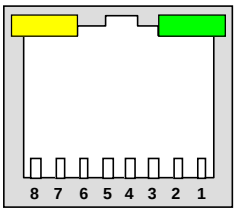


Figure 14 - Fast Ethernet port connector

Pin	Name	Direction	Description
1	TxD+	Output	Transmit data +
2	TxD-	Output	transmit data -
3	RxD+	Input	Receive data +
4	-	-	AC terminated
5	-	-	AC terminated
6	RxD-	Input	Receive data -
7	-	-	AC terminated
8	-	-	AC terminated

Table 24 - Fast Ethernet connector assignment

Both connectors provide two indicator LEDs which shows network activities as follows:

LED color	Description
Yellow	Collision
Green	Link and network activity

Table 25 - Network status LEDs

The Link LEDs are blinking during system reset.

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7.1.2 Console port

One RS-232 console is available for user interface. This serial port is handled by the MPC8270 SMC1 controller.

This serial link provides a front connector through a RJ45 8-pin connector, with the following pin assignment.

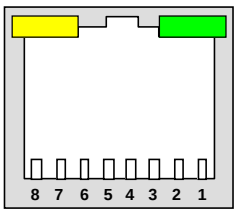


Figure 15 - Console port connector

Pin	Name	Direction	Description
1	NC		
2	NC		
3	GND	NA	Ground
4	TxD	Output	Transmit Data
5	RxD	Input	Receive Data
6	GND	NA	Ground
7	NC		
8	NC		

Table 26 - Console port pin assignment

This connector provides two user indicator LEDs.

LED color	Description
Yellow	User LED 0: - driven by GPIO PC24, on when low - toggled when slave access
Green	User LED 1: - driven by GPIO PC21, on when low - on at reset - toggled by SDRAM activity

Table 27 - User LEDs

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7.1.3 Multi-protocol serial ports SCC1..SCC4

A 50-pin SCSI connector (Ref. E-tec CSF-050-N900-01/21) is used for connecting the multi-protocol communication ports on the front panel. It groups together the four communication ports.
Here follows the connector pin assignment:

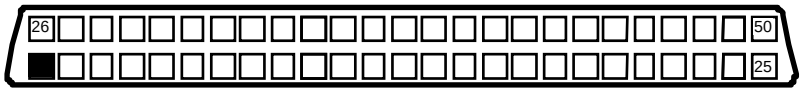


Figure 16 - Serial port connector

Pin	RS-232	RS-422/485 Half-duplex	RS-422/485 Full-duplex	Pin
1	GND	GND	GND	
	GND	GND	GND	26
2	-	TXCLK4-	TXCLK4-	
	-	RXCLK4-	RXCLK4-	27
3	CTS4	CTS4	CTS4	
	RXCLK4	RXCLK4+	RXCLK4+	28
4	RTS4	RTS4	RTS4	
	-	-	RXD4-	29
5	RXD4	-	RXD4+	
	TXCLK4	TXCLK4+	TXCLK4+	30
6	TXD4	TRXD4+	TXD4+	
	-	TRXD4-	TXD4-	31
7	GND	GND	GND	
	GND	GND	GND	32
8	-	TXCLK3-	TXCLK3-	
	-	RXCLK3-	RXCLK3-	33
9	CTS3	CTS3	CTS3	
	RXCLK3	RXCLK3+	RXCLK3+	34
10	RTS3	RTS3	RTS3	
	-	-	RXD3-	35
11	RXD3	-	RXD3+	
	TXCLK3	TXCLK3+	TXCLK3+	36
12	TXD3	TRXD3+	TXD3+	
	-	TRXD3-	TXD3-	37
13	GND	GND	GND	
	GND	GND	GND	38

Table 28 - Serial port pin assignment

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Pin	RS-232	RS-422/485 Half-duplex	RS-422/485 Full-duplex	Pin
14	-	TXCLK2-	TXCLK2-	
	-	RXCLK2-	RXCLK2-	39
15	CTS2	CTS2	CTS2	
	RXCLK2	RXCLK2+	RXCLK2+	40
16	RTS2	RTS2	RTS2	
	-	-	RXD2-	41
17	RXD2	-	RXD2+	
	TXCLK2	TXCLK2+	TXCLK2+	42
18	TXD2	TRXD2+	TXD2+	
	-	TRXD2-	TXD2-	43
19	GND	GND	GND	
	GND	GND	GND	44
20	-	TXCLK1-	TXCLK1-	
	-	RXCLK1-	RXCLK1-	45
21	CTS1	CTS1	CTS1	
	RXCLK1	RXCLK1+	RXCLK1+	46
22	RTS1	RTS1	RTS1	
	-	-	RXD1-	47
23	RXD1	-	RXD1+	
	TXCLK1	TXCLK1+	TXCLK1+	48
24	TXD1	TRXD1+	TXD1+	
	-	TRXD1-	TXD1-	49
25	GND	GND	GND	
	GND	GND	GND	50

Table 28 - Serial port pin assignment (cont'd)

Note that this pin assignment is compliant with Actis Computer's standard serial port on 50-pin SCSI connector specification.

☞ Signals CD and DTR of the SCCs are not present on the serial port connector.

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7.2 Board jumpers

A set of board jumpers allows the user to control the board operation and set the VME A16 Slave base address.

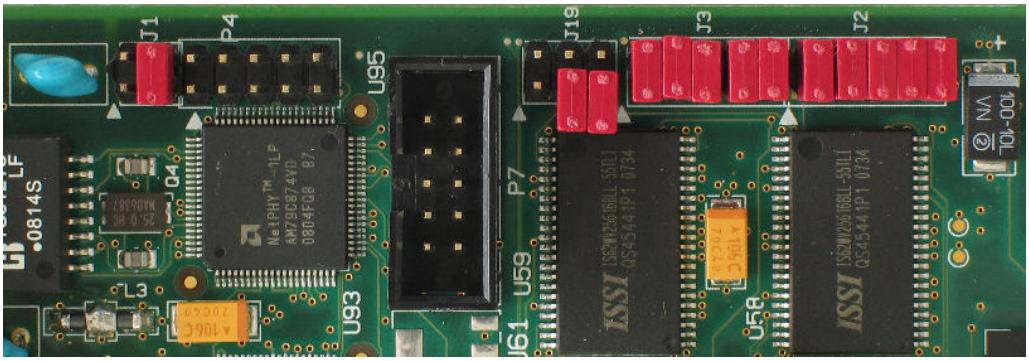


Figure 17 - Board jumpers

	Plugged in	Unplugged
J1		
▶ ❶ ② RSTCONF	MPC uses default config word	Config word read from boot device
③ ④ I2C_SDA	Normal operation	Reserved use
J19		
▶ ❶ ② Pos. 1-2	VME SYSRESET generates PORESET	SYSRESET not propagated to local reset
③ ④ Pos. 1-3	PORESET generates VME SYSRESET	Local reset not propagated to SYSRESET
⑤ ⑥ RESET	Power-On Reset asserted	Normal operation
J3		
▶ ❶ ② BOOTBANK	Boot device is Flash Bank 1	Boot device is Flash Bank 0
③ ④ SLOT1	VME System Controller enabled	VME System Controller disabled
⑤ ⑥ RC2	RC2=0	RC2=1
⑦ ⑧ RC1	RC1=0	RC1=1
⑨ ⑩ RC0	RC0=0	RC0=1
J2		
▶ ❶ ② VSBA15	VSBA15=0	VSBA15=1
③ ④ VSBA14	VSBA14=0	VSBA14=1
⑤ ⑥ VSBA13	VSBA13=0	VSBA13=1
⑦ ⑧ VSBA12	VSBA12=0	VSBA12=1
⑨ ⑩ VSBA11	VSBA11=0	VSBA11=1

- VME SYSRESET and PORESET jumpers (J19) cannot be plugged in both together.
- RC(2..0) is the 3-bit User Code.
- VSBA(15..11) defines the VME A16 Slave Base Address (access to bridge registers from the VMEbus).
- ◯◯ : indicates that a jumper is plugged-in in default configuration.

Table 29 - Board jumper configuration

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7.3 Serial Communication port jumpers

Each of the four serial communication ports has two jumpers for the physical interface mode configuration (RS-232 or RS-422/RS-485/V.35).

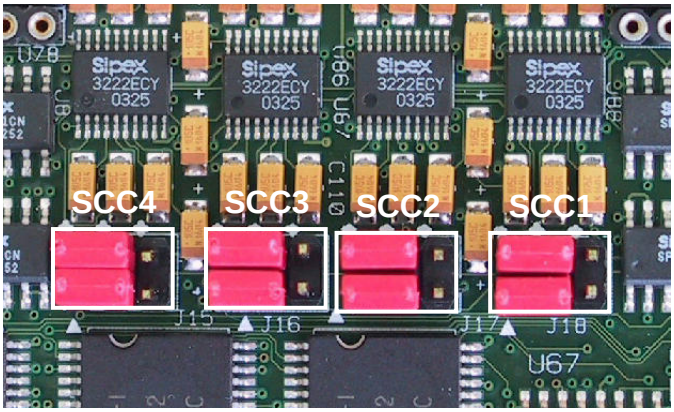


Figure 18 - Serial port jumpers

The following tables give the jumper location and configuration:

Jumper location	Serial Port
J15	SCC4
J16	SCC3
J17	SCC2
J18	SCC1

Table 30 - Serial port jumper location

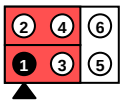
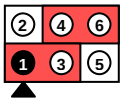
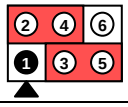
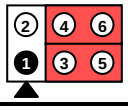
Jumper configuration	Serial Port Mode
	Determined by SCCR[MODE]. *Please refer to the SCCR Register description in the 'Bridge Registers' section.*
	Determined by SCCR[MODE]. *Please refer to the SCCR Register description in the 'Bridge Registers' section.*
	RS-422/RS-485/V.35 like
	RS-232

Table 31 - Serial port jumper configuration

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7.4 IEEE1149.1 Test Access Port, P11 Connector

The IEEE 1149.1 Test Access Port (TAP), commonly called the JTAG (Joint Test Action Group) debug port, is an architectural standard described in IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary Scan Architecture. The standard describes a method for accessing internal chip facilities using a four- or five-signal interface.
The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the IEEE 1149.1 specifications for vendor specific extensions, are compatible with standard JTAG hardware for boundary-scan system testing.

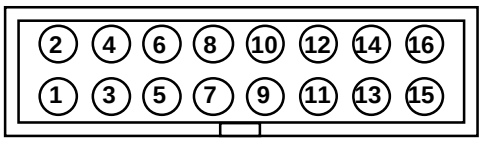


Figure 19 - Test Access Port connector

Pin	Signal	Description
1	TDO	Serial output data
2	NC	Not used
3	TDI	Serial input data
4	/TRST	Scan chain logic reset
5	/QREQ	Sleep mode
6	+3.3V	Power supply (pull–up resistor)
7	TCK	Serial clock
8	NC	Not used
9	TMS	Mode select
10	NC	Not used
11	/SRESET	Software Reset
12	GND	Ground
13	/HRESET	Hardware Reset
14	NC	Not used
15	/IRQ3	MPC8270 IRQ3 line
16	GND	Ground

Table 32 - IEEE1149.1 connector pin assignment

7.5 SPI/SMC2/I2C connector

The internal P4 connector is used to connect the MPC8270 SPI, SMC2, and I2C ports. The P4 pin assignment is given in the following table:

P4	Pinout
❶ ② SPI MISO	MISO on pin 1 and GND on pin 2
③ ④ SPI MOSI	MOSI on pin 3 and +3.3V on pin 4
⑤ ⑥ SPI SEL/CLK	SEL on pin 5 and CLK on pin 6
⑦ ⑧ SMC2 TX/RX	TX on pin 7 and RX on pin 8
⑨ ⑩ I2C SDA/SCL	SDA on pin 9 and SCL on pin 10

Table 33 - SPI/SMC2/I2C connector pin assignment

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7.6 S-ATA ports

The S-ATA port 1 and port 2 are respectively available on P9 and P10 connectors.

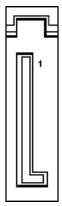


Figure 20 - S-ATA connector description

Pin	Name	Direction	Description
1	GND	-	Ground
2	TxP	Output	Transmit data +
3	TxN	Output	Transmit data -
4	GND	-	Ground
5	RxN	Input	Receive data -
6	RxP	Input	Receive data +
7	GND	-	Ground

Table 34 - S-ATA connector pin assignment

7.7 CompactFlash connector

The pin assignment of the CompactFlash connector is given in the following table:

Pin	Signal Name	Connected to
1	GND	GND
2	D03	MPC D(4)
3	D04	MPC D(3)
4	D05	MPC D(2)
5	D06	MPC D(1)
6	D07	MPC D(0)
7	-CS0	MPC CS10
8	A10	GND
9	-ATA SEL	GND
10	A09	GND
11	A08	GND
12	A07	GND
13	VCC	+3.3V
14	A06	GND
15	A05	GND
16	A04	GND
17	A03	GND
18	A02	MPC A(28)
19	A01	MPC A(29)
20	A00	MPC A(30)
21	D00	MPC D(7)
22	D01	MPC D(6)
23	D02	MPC D(5)
24	-IOCS16	no connect
25	-CD2	no connect

Pin	Signal Name	Connected to
26	-CD1	no connect
27	D11	MPC D(12)
28	D12	MPC D(11)
29	D13	MPC D(10)
30	D14	MPC D(9)
31	D15	MPC D(8)
32	-CS1	MPC CS11
33	-VS1	no connect
34	-IORD	MPC PGPL1
35	-IOWR	MPC PGPL2
36	-WE	pulled-up
37	INTRQ	MPC PC7
38	VCC	+3.3V
39	-CSEL	GND
40	-VS2	no connect
41	-RESET	PORESET
42	IORDY	no connect
43	reserved	no connect
44	reserved	pulled-up
45	-DASP	no connect
46	-PDIAG	no connect
47	D08	MPC D(15)
48	D09	MPC D(14)
49	D10	MPC D(13)
50	GND	GND

Table 35 - CompactFlash connector pin assignment

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7.8 VMEbus P1 connector

The VSBC-6872 implements a VMEbus interface on two 96-pin DIN-41612 connectors (P1 and P2). Here follows the pin assignment of these connectors:

Pin	a	b	c
1	D0	BBSY*	D8
2	D1	BCLR*	D9
3	D2	ACFAIL*	D10
4	D3	BG0IN*	D11
5	D4	BG0OUT*	D12
6	D5	BG1IN*	D13
7	D6	BG1OUT*	D14
8	D7	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	-	A17
22	IACKOUT*	-	A16
23	AM4	GND	A15
24	A7	IRQ7*	A14
25	A6	IRQ6*	A13
26	A5	IRQ5*	A12
27	A4	IRQ4*	A11
28	A3	IRQ3*	A10
29	A2	IRQ2*	A9
30	A1	IRQ1*	A8
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

Table 36 - VMEbus P1 connector pin assignment

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7.9 VMEbus P2 connector

Pin	a	b	c
1	PMC_IO2	+5 V	PMC_IO1
2	PMC_IO4	GND	PMC_IO3
3	PMC_IO6	-	PMC_IO5
4	PMC_IO8	A24	PMC_IO7
5	PMC_IO10	A25	PMC_IO9
6	PMC_IO12	A26	PMC_IO11
7	PMC_IO14	A27	PMC_IO13
8	PMC_IO16	A28	PMC_IO15
9	PMC_IO18	A29	PMC_IO17
10	PMC_IO20	A30	PMC_IO19
11	PMC_IO22	A31	PMC_IO21
12	PMC_IO24	GND	PMC_IO23
13	PMC_IO26	+5 V	PMC_IO25
14	PMC_IO28	D16	PMC_IO27
15	PMC_IO30	D17	PMC_IO29
16	PMC_IO32	D18	PMC_IO31
17	PMC_IO34	D19	PMC_IO33
18	PMC_IO36	D20	PMC_IO35
19	PMC_IO38	D21	PMC_IO37
20	PMC_IO40	D22	PMC_IO39
21	PMC_IO42	D23	PMC_IO41
22	PMC_IO44	GND	PMC_IO43
23	PMC_IO46	D24	PMC_IO45
24	PMC_IO48	D25	PMC_IO47
25	PMC_IO50	D26	PMC_IO49
26	PMC_IO52	D27	PMC_IO51
27	PMC_IO54	D28	PMC_IO53
28	PMC_IO56	D29	PMC_IO55
29	PMC_IO58	D30	PMC_IO57
30	PMC_IO60	D31	PMC_IO59
31	PMC_IO62	GND	PMC_IO61
32	PMC_IO64	+5 V	PMC_IO63

Table 37 - VMEbus P2 connector pin assignment

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7.10 PCI Mezzanine Card (PMC)

The VSBC-6872 supports a single PMC expansion slot which is compatible with the IEEE Std 1386.1-2001 specification. This interface bus is based on PCI Local Bus specification, Revision 2.2, 1998.
The PMC slot is connected to the MPC8270 PCI bus, which supports 32-bit devices with PCI clock at 31.25/62.5 MHz.

The signaling voltage key is set to 3.3 V.
Only 3.3V and universal compatible PMC must be used to avoid system conflict or hardware damage.

7.10.1 Installing a PMC

Performs the following procedure to install a PMC module.

- Turn off the system power supply
- Remove the bezel panel located on the PMC front side
- Plug carefully the PMC module in the PMC slot location.
- Verify that the EMC gasket is correctly positioned around the PMC front panel

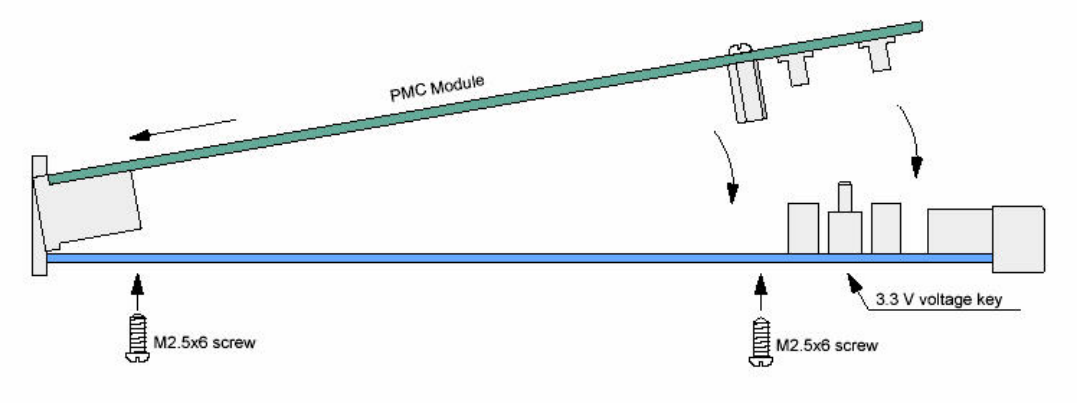


Figure 21 - PMC module installation

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7.11 PMC interface, J11 connector

The J11 and J12 connectors provide the 32-bit PCI interface signals.

Pin	Signal	Pin	Signal
1	<PULL-DOWN>	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	PRESENT#	8	5V
9	INTD#	10	NC
11	GND	12	NC
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	5V
19	3.3V	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	CBE3#
27	AD22	28	AD21
29	AD19	30	5V
31	3.3V	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	5V
39	GND	40	LOCK#
41	NC	42	NC
43	PAR	44	GND
45	3.3V	46	AD15
47	AD12	48	AD11
49	AD9	50	5V
51	GND	52	CBE0#
53	AD6	54	AD5
55	AD4	56	GND
57	3.3V	58	AD3
59	AD2	60	AD1
61	AD0	62	5V
63	GND	64	REQ64#

Table 38 - J11 connector pin assignment

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7.12 PMC interface, J12 connector

The J12 connector provides the additional PCI-32 interface signals as follows:

Pin	Signal	Pin	Signal
1	+12V	2	<PULL-DOWN>
3	<PULL-UP>	4	NC
5	<PULL-UP>	6	GND
7	GND	8	NC
9	NC	10	NC
11	<PULL-UP>	12	3.3V
13	#RESET	14	<PULL-DOWN>
15	3.3V	16	<PULL-DOWN>
17	NC	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V
25	AD12 (IDSEL)	26	AD23
27	3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	#CBE2
33	GND	34	NC
35	#TRDY	36	3.3V
37	GND	38	#STOP
39	#PERR	40	GND
41	3.3V	42	#SERR
43	#CBE1	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	3.3V
51	AD7	52	NC
53	3.3V	54	NC
55	NC	56	GND
57	NC	58	<PULL-UP>
59	GND	60	NC
61	<PULL-UP>	62	3.3V
63	GND	64	<PULL-UP>

Table 39 - J12 connector pin assignment

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7.13 PMC interface, J14 connector

The J14 connector contains the user I/Os of the PMC module. These I/Os are routed to the VMEbus P2 connector according to the ANSI/VITA 35-2000 standard. Please refer to 3.14.1 PMC expansion slot for PMC-P4 to VME-P2 mapping.

Pin	Signal	Pin	Signal
1	IO1	2	IO2
3	IO3	4	IO4
5	IO5	6	IO6
7	IO7	8	IO8
9	IO9	10	IO10
11	IO11	12	IO12
13	IO13	14	IO14
15	IO15	16	IO16
17	IO17	18	IO18
19	IO19	20	IO20
21	IO21	22	IO22
23	IO23	24	IO24
25	IO25	26	IO26
27	IO27	28	IO28
29	IO29	30	IO30
31	IO31	32	IO32
33	IO33	34	IO34
35	IO35	36	IO36
37	IO37	38	IO38
39	IO39	40	IO40
41	IO41	42	IO42
43	IO43	44	IO44
45	IO45	46	IO46
47	IO47	48	IO48
49	IO49	50	IO50
51	IO51	52	IO52
53	IO53	54	IO54
55	IO55	56	IO56
57	IO57	58	IO58
59	IO59	60	IO60
61	IO61	62	IO62
63	IO63	64	IO64

Table 40 - J14 connector pin assignment

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8 Software description

The VSBC-6872 contains a pre-installed debugger and bootloader utility called ECMon. This tool supports additional features as follows:

- Low-level board initialization
- Diskless system support
- Network file transfer (by using BootP/RARP and TFTP/NFS protocols)
- File system capability (FAT, EXT2, ISO9660, or ROM disk)
- Flexible file format support (Binary, Motorola S data and ELF)

ECMon supported commands are described in the following section.

The VSBC-6872 supports industry-standard Real-Time Operating Systems (RTOSs) such as VxWorks and Linux. Other BSP's are available on request.



For detailed BSP information, please consult the ACTIS Computer software department, or contact your local ACTIS Computer representative for up-to-date information about product availability literature

8.1 ECMon commands

8.1.1 Command line and syntax rules

The following table gives the command line syntax:

space or tab	must be used to separate keywords on the command line
;	can be used to separate multiple commands on a single line
#	can be used to put a comment at the end of the command line
@	followed by an environment variable, the parameter uses the value of the environment variable (currently, no space or tabulation is allowed)

To describe the command syntax, the following convention is used:

xxx	bold keyword should be directly used
<xxx>	keyword between '<' and '>' defines a parameter which must be replaced by a correct keyword
[<xxx>]	a parameter between '[' and ']' is optional
{ <xxx> }	a parameter between '{' and '}' is optional and can be repeated more than once

ECMon uses, by default, hexadecimal numbers for any parameters (except on some cases). To force another number base, a prefix must be inserted:

0x or $	for using a hexadecimal number (e.g.: 0x4A).
0b or %	for using a binary number (e.g.: 0b01001010).
0d or &	for using a decimal number (e.g.: 0d74).
'	for using a ascii number (e.g.: 'K)

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Note that to enter the decimal value 13 without prefix, the value 'D' must be used instead of '0D' because ECMon will interpret this one as the decimal prefix (such as the decimal value 11, use 'B' instead of '0B').

Additionally, for an internet address, ECMon accepts the standard internet notation (to replace a 32-bits word). In this case, the decimal number is used by default (e.g.: 192.52.109.0xF0).

If the AUTOBOOT feature is disabled, ECMon is waiting for a command from the serial console (no case sensitive). The following table gives shortcut keys for command line editing:

Keystroke	ASCII code	Function
Ctrl-X ESC	0x18 0x1B	Clear the entire command line (or abort a command if possible)
Ctrl-A	0x01	Recall the last command line
Ctrl-H (Backspace) DEL	0x08 0x7F	Delete the character on the left to the cursor
Ctrl-M (Carriage Return)	0x0D	Enable the current command line

Table 41 - ECMon command line editing shortcut keys

8.1.2 Command descriptions

The following table gives an overview of the ECMon commands.

Command	Description
crc	Compute the CRC32 from a memory space
dboot	Load binary and boot from a fixed-disk
dload	Load binary from a fixed-disk
dpart	Display the partition table on a fixed-disk
eflash	Erase flash memory
env	Create, modify or remove environment variable
go	Execute user program
help	Display help
i2c	Read or write data from/to an I2C device
kgdb	Call the KGDB module
mcb, mcw, mcl	Copy the content of memory to another
mdb, mdw, mdl	Display the content of memory
mfb, mfw, mfl	Fill the memory with a specific data
mii	Read or write a PHY register
mmb, mmw, mml	Modify the content of memory
mmap	Display memory map
nboot	Load binary and boot from TFTP server
nload	Load binary from TFTP server
nping	Ping a host on the network
nsave	Upload memory to a TFTP server
pci	Read or write a PCI configuration register
pflash	Program flash memory
rboot	Boot from ROM
reset	Provide an hardware reset
sboot	Load binary and boot from serial port
scsi	Display the information about a SCSI device
sload	Load binary from serial port
time	Get or set the time-keeper
vpd	Display the Vital Product Data

Table 42 - ECMon command overview

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crc *Compute the CRC32 from a memory space*

Syntax

crc <address> <count>

Parameters

address defines the starting address of the memory space

count defines the number of bytes to compute

Description

The crc command compute the CRC32 from a memory space.

See also

-

dboot *Load binary and boot from a fixed-disk*

Syntax

dboot [<device> [<offset> [<entry> [<filename> [<partition>]]]]]

Parameters

device defines address of the fixed-disk and the format of the file to be loaded. While <device> = AAAAAAAB

- AAAAAAA defines the fixed-disk address or the ROM disk base address (MSB)
- B defines the format of the file to be loaded
  - 0 for a binary file
  - 1 for a Motorola S1/S9 file
  - 2 for an ELF file (default)

offset defines the loading offset to the destination memory

entry defines the execution entry offset in the destination memory (default is 4)

filename defines the file name to be loaded (default is '/sysboot'). Additionally, the prefix 'fat:', 'ext2:' or 'iso9660:' can be used to override the partition information

partition defines the partition number to be used (default is 0)

Description

The dboot command should be used to download, from a fixed-disk, an external executable routine and to call the execution entry. If the partition number is not defined or is set to 0, this command uses the bootable partition. If the <entry> parameter is set with the value 0xFFFFFFFF, the execution entry is searched with the rboot command on the downloaded file.

See also

dpart, rboot, External Routine

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dload *Load binary from a fixed-disk*

Syntax

dload [<device> [<offset> [<filename> [<partition>]]]]

Parameters

device — defines address of the fixed-disk and the format of the file to be loaded. While <device> = AAAAAAAB

- AAAAAAA — defines the fixed-disk address or the ROM disk base address (MSB)
- B — defines the format of the file to be loaded
  - 0 for a binary file
  - 1 for a Motorola S1/S9 file
  - 2 for an ELF file (default)

offset — defines the loading offset to the destination memory

filename — defines the file name to be loaded (default is '/sysboot'). Additionally, the prefix 'fat:', 'ext2:' or 'iso9660:' can be used to override the partition information

partition — defines the partition number to be used (default is 0)

Description

The dload command is used to download, from a fixed-disk, an external executable routine or a Flash memory image. If the partition number is not defined or is set to 0, this command uses the bootable partition.

See also

dpart

dpart *Display the partition table on a fixed-disk*

Syntax

dpart <device>

Parameters

device — defines address of the fixed-disk while <device> = AAAAAAAB

- AAAAAAA — defines the fixed-disk address or the ROM disk base address (MSB)
- B — must be set to 0

Description

The dpart command should be used to show the partition table of a fixed-disk.

See also

-

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eflash *Erase flash memory*

Syntax

```
eflash <address> [ <size> ]
```

Parameters

address	defines the starting address of the flash memory to be erased
size	defines the size of the flash memory to be erased

Description

The eflash command should be used to erase the flash memory (before to use the pflash command). If the <size> parameter is ommited, the entire flash memory is erased starting at the address <address> (can be different to the flash memory base address).

See also

pflash

env *Create, modify or remove environment variable*

Syntax

```
env [ <name> [ <value> ] ]
env clear
env load
env save
```

Parameters

name	defines the name of the environment variable or the environment function
value	defines the value of the environment variable

Description

The env command allows several functions depending on the parameters passed:

<name>	<value>	Function
no	no	All the current environment variables are displayed
yes	no	The <name> environment variable is removed
yes	yes	The <name> environment variable is created or modified with <value>

Any environment variable name can be used except 'clear' (remove all current environment variables), 'save' (save all current environment variables in the non-volatile RAM), and 'load' (load current environment variables from the non-volatile RAM).
Please note :

- The 'BOOTARGS' environment variable is used during a call to an external routine.
- The 'AUTOBOOT' environment variable is used as the first command line after power-up.
- The 'AUTOWAIT' environment variable defines the timeout (number of seconds) for the AUTOBOOT condition (0 = disabled). After a power-up, ECMon uses these both environment variables to provide an autoboot feature (during the waiting time, while the keystroke 'carriage return' start the autoboot command, the keystroke 'escape' abort the autoboot command).
- If the <value> parameter must contain space or tabulation characters (such as for the 'AUTOBOOT' environment variable), the double-quote character must start and end the <value> data (e.g. *env AUTOBOOT "nboot 2 0 0 bootfile"*).
- The 'TERM' environment variable can be set to 'ansi' to provide an ANSI console.

See also

External Routine

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go — *Execute user program*

Syntax

go <address>

Parameters

address — defines the address of the external routine

Description

The go command is used to call an external routine at address <address>.

See also

External Routine

help — *Display help*

Syntax

help { <keyword> }

Parameters

keyword — specifies one or more keywords to get help about it

Description

Without <keyword> parameter, the help command displays all the available commands. To get help about a specific command, the help command must be called with the <keyword> parameter.

See also

-

i2c — *Read or write data from/to an I2C device*

Syntax

i2c <device> <offset> <count> <address>

Parameters

device — defines the I2C device address (odd value to read, even value to write)

offset — defines the starting I2C memory offset

count — defines the number of data items to copy

address — defines the local memory address

Description

The i2c command can be used to read or to write the content of a I2C device.

See also

-

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kgdb *Execute user program under KGDB*

Syntax

```
kgdb [ <device> [ <address> ] ]
```

Parameters

device	defines the serial port (0 for the console)
address	defines the address of the external routine

Description

The kgdb command is used to call KGDB which will control an external routine at address <address>.

See also

External Routine

mcb, mcw, mcl *Copy the content of memory to another*

Syntax

```
mcb <source> <size> <destination>
mcw <source> <size> <destination>
mcl <source> <size> <destination>
```

Parameters

source	defines the source address to be copied
size	defines the number of items to be copied in the destination memory
destination	defines the destination address to be modified

Description

The mcb, mcw and mcl commands should be used to transfert the content of a memory space to another (mcb uses a byte size, mcw uses a word size and mcl uses a long-word size).
Please note that:

- the <size> parameter defines the number of items (depend on the command used) and not the number of bytes.
- the bus error (or machine check error) is handled.

See also

pflash

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mdb, mdw, mdl Display the content of memory

Syntax

```
mdb <address> [ <count> ]
mdw <address> [ <count> ]
mdl <address> [ <count> ]
```

Parameters

address	defines the base address to be displayed
count	defines the number of items to be displayed

Description

The mdb, mdw and mdl commands can be used to show the content of a memory space (mdb uses a byte size, mdw uses a word size and mdl uses a long-word size).
Please note that:

- the <count> parameter defines the number of items (depend on the command used) and not the number of bytes.
- the bus error (or machine check error) is handled (the 'X' character is displayed).

See also

-

mfb, mfw, mfl Fill the memory with a specific data

Syntax

```
mfb <address> <count> <value>
mfw <address> <count> <value>
mfl <address> <count> <value>
```

Parameters

address	defines the destination address to be filled
count	defines the number of items to be filled in the destination memory
value	defines the data value to be used

Description

The mfb, mfw and mfl commands can be used to fill the content of a memory space (mfb uses a byte size, mfw uses a word size and mfl uses a long-word size).
Please note that:

- the <count> parameter defines the number of items (depend on the command used) and not the number of bytes.
- the bus error (or machine check error) is handled.

See also

-

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mii *Read or write a PHY register*

Syntax

```
mii <device> [ <address> [ <register> { <value> | <keyword> } ] ]
```

Parameters

device	defines the Ethernet port
address	defines the PHY address
register	defines the PHY register number
value	defines the PHY register value
keyword	defines the address's operator: '+' to go to the next address '-' to go to the previous address '.' to exit

Description

The mii command can be used to scan, dump, get or to set the PHY registers on the MII bus (Ethernet).

See also

-

mmb, mmw, mml *Modify the content of memory*

Syntax

```
mmb <address> [ { <value> | <keyword> } ]
mmw <address> [ { <value> | <keyword> } ]
mml <address> [ { <value> | <keyword> } ]
```

Parameters

address	defines the destination address to be modified
value	defines the value to be stored in the destination memory
keyword	defines the address's operator: '+' to go to the next address '-' to go to the previous address '.' to exit

Description

The mmb, mmw and mml commands can be used to modify the content of a memory space (mmb uses a byte size, mmw uses a word size and mml uses a long-word size).
Please note that the bus error (or machine check error) is handled (a 'X' character is displayed).

See also

-

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mmap *Display memory map*

Syntax

mmap

Description

The mmap command displays the memory map of the board.

See also

-

nboot *Load binary and boot from TFTP server*

Syntax

nboot [<device> [<offset> [<entry> [<filename> [<host> [<client> [<gateway> [<netmask>]]]]]]]]

Parameters

device	defines ethernet port and the format of the file to be loaded. While <device> = 0AAB AA defines the ethernet port B defines the format of the file to be loaded 0 for a binary file (default) 1 for a Motorola S1/S9 file 2 for an ELF file
offset	defines the loading offset to the destination memory
entry	defines the execution entry offset in the destination memory (default is 4)
filename	defines the file name to be loaded. Additionally, the prefix 'tftp:', or 'nfs:' can be used to use a specific file transfer protocol
host	defines the host's name (by using a DNS) or IP address
client	defines the client's IP address
gateway	defines the gateway's IP address
netmask	defines the network mask

Description

The nboot command should be used to download, from a TFTP server, an external executable routine and to call the execution entry. If the information is missing, this command requests a BootP/DHCP and a RARP server to retrieve the missing information (In case of a response from the RARP server, the file name is built from the client's IP address).
If the <entry> parameter is set with the value 0xFFFFFFFF, the execution entry is searched with the rboot command on the downloaded file.

See also

rboot, External Routine

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nload *Load binary from TFTP server*

Syntax

nload [<device> [<offset> [<filename> [<host> [<client> [<gateway> [<netmask>]]]]]]]

Parameters

device	defines ethernet port and the format of the file to be loaded. While <device> = 0AAB AA defines the ethernet port B defines the format of the file to be loaded 0 for a binary file (default) 1 for a Motorola S1/S9 file 2 for an ELF file
offset	defines the loading offset to the destination memory
filename	defines the file name to be loaded. Additionally, the prefix 'tftp:', or 'nfs:' can be used to use a specific file transfer protocol
host	defines the host's name (by using a DNS) or IP address
client	defines the client's IP address
gateway	defines the gateway's IP address
netmask	defines the network mask

Description

The nload command is used to download, from the console port, an external executable routine or a Flash memory image. If the client's IP address is missing, this command requests a BootP/DHCP or a RARP server to retrieve the missing information (In case of using the RARP server, the file name is built from the client's IP address).

See also

pflash

nping *Ping a host on the network*

Syntax

nping <device> <host> [<client> [<gateway> [<netmask>]]]

Parameters

device	defines the Ethernet port
host	defines the host's name (by using a DNS) or IP address to be checked
client	defines the client's IP address to be used
gateway	defines the gateway's IP address
netmask	defines the network mask

Description

The nping command should be used to check if a host is alive. If the client's IP address is missing, this command requests a BootP/DHCP and a RARP server to retrieve the missing information.

See also

-

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nsave *Upload memory to TFTP server*

Syntax

```
nsave <device> <address> <size> <filename> [ <host> [ <client> [
<gateway> [ <netmask> ] ] ] ]
```

Parameters

device	defines ethernet port and the format of the file to be loaded. While <device> = 0AAB AA defines the ethernet port B must be set to 0
address	defines the starting offset of the memory
size	defines the number of bytes to upload
filename	defines the file name to be used
host	defines the host's name (by using a DNS) or IP address
client	defines the client's IP address
gateway	defines the gateway's IP address
netmask	defines the network mask

Description

The nsave command is used to upload memory to a TFTP server. If the client's IP address is missing, this command requests a BootP/DHCP or a RARP server to retrieve the missing information (In case of using the RARP server, the file name is built from the client's IP address).

See also

pflash

pci *Read or write a PCI configuration register*

Syntax

```
pci [ <bus> [ <device> [ <function> [ <address> { <value> | <keyword> }
] ] ] ]
```

Parameters

bus	defines the PCI bus number
device	defines the PCI device number
function	defines the PCI function number
address	defines the address of the PCI configuration register
value	defines the value of the PCI configuration register
keyword	defines the address's operator: '+' to go to the next address '-' to go to the previous address '.' to exit

Description

The pci command can be used to scan, dump, get or to set the PCI configuration registers.

See also

-

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pflash *Program flash memory*

Syntax

pflash <source> <size> <destination>

Parameters

source	defines the image source address to be copied to the flash memory
size	defines the size of the source memory to be copied
destination	defines the starting address of the flash memory

Description

The pflash command is used to program the flash memory with an image defined by the <source> parameter.

See also

eflash

rboot *Boot from ROM*

Syntax

rboot <start> [<end>]

Parameters

start	defines the starting address
end	defines the ending address

Description

The rboot command should be used to boot from memory by searching for a specific data structure located in this memory aera. If the <end> parameter is specified while the specific data structure has not been found on the starting address, the rboot command continue to scan (by using 1K boundary) the memory until reaching the ending address.

```
struct _ecmon_romboot
{
    unsigned long _magic1; /* 0x00 : 'ECMO' */
#define ECMON_ROMBOOT_MAGIC1 0x45434D4F
    unsigned long _magic2; /* 0x04 : 'N_RB' */
#define ECMON_ROMBOOT_MAGIC2 0x4E5F5242
    unsigned long _entry; /* 0x08 : bootstrap entry */
    unsigned long _cs; /* 0x0C : checksum of this structure */
    char          _name[ 48 ]; /* 0x10 : name of bootstrap */
} /*__attribute__( ( packed ) )*/;
```

In case of a valid data structure has been found, the rboot command call the routine just after it (Normally, the called routine should not return).

See also

go, External Routine

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reset *Provide an hardware reset*

Syntax

reset

Description

The reset command provides an hardware reset (restart the firmware from the boot ROM).

See also

-

sboot *Load binary and boot from serial port*

Syntax

sboot [<device> [<offset> [<entry>]]]

Parameters

device — defines the serial port and the format of the file to be loaded. While <device> = 0AAB
- AA defines the serial port (0 for the console)
- B defines the format of the file to be loaded
  - 0 for a binary file
  - 1 for a Motorola S1/S9 file (default)
  - 2 for an ELF file

offset — defines the loading offset to the destination memory

entry — defines the execution entry offset in the file (default is 4)

Description

The sboot command should be used to download, from the console port, an external executable routine and to call the execution entry. If the <entry> parameter is set with the value 0xFFFFFFFF, the execution entry is searched with the rboot command on the downloaded file.

See also

rboot, External Routine

scsi *Display the information about a SCSI device*

Syntax

scsi <device>

Parameters

device — defines address of the SCSI device. While <device> = AAAAAAAB
- AAAAAAA defines the SCSI address of the device
- B must be set to 0

Description

The scsi command can be used to retrieve the information of a SCSI device (inquiry command).

See also

-

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sload *Load binary from serial port*

Syntax

sload [<device> [<offset>]]

Parameters

device defines the serial port and the format of the file to be loaded. While <device> = 0AAB
- AA defines the serial port (0 for the console)
- B defines the format of the file to be loaded
  - 0 for a binary file
  - 1 for a Motorola S1/S9 file (default)
  - 2 for an ELF file

offset defines the loading offset to the destination memory

Description

The sload command is used to download, from the console port, an external executable routine or a Flash memory image.

See also

pflash

time *Get or set the time-keeper*

Syntax

time [<date & time>]

Parameters

date & time defines the new time-keeper value (YYYYMMDDHHMMSS)

Description

The time command can be used to display the current date/time from the time-keeper or can be used to set the time-keeper with the <date & time> parameter.

See also

-

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vpd *Display the Vital Product Data*

Syntax

```
vpd
vpd load *
vpd save *
vpd modify [ { <tag> } ] *
```

* these command syntaxes are reserved for the board's manufacturer (do not use it)

Description

The vpd command should be used to show the content of Vital Product Data (normally, stored in an I2C device). The VPD structure is the form:

```
#define VPD_SIZE              256
#define VPD_MAGIC_COOKIE_SIZE 8
#define VPD_OPTIONS_SIZE      ( VPD_SIZE - 16 )
#define VPD_MAGIC_COOKIE      { 0x41, 0x43, 0x54, 0x49, 0x53, 0x00, 0x00 }

typedef struct
{
    unsigned char magic_cookie[ VPD_MAGIC_COOKIE_SIZE ]; /* 0x41435449530000 */
    unsigned char opt_size;                              /* VPD options size */
    unsigned char rsvd[ 5 ];
    unsigned char year;                                  /* year of VPD */
    unsigned char week;                                  /* week of VPD */
    unsigned char options[ VPD_OPTIONS_SIZE ];
} /*__attribute__ ((packed))*/ t_VPD;
```

All the tag's VPD are stored in the options field and contain all the board specific configuration (oscillator frequency, memory size, MAC address, etc.). A tag is represented by a unique byte value, followed by the size of the data and the data. The tag values are:

```
#define VPD_OPTIONS_PAD       0x00 /* Pad */
#define VPD_OPTIONS_END       0xFF /* End */
#define VPD_OPTIONS_PI        0x01 /* Product Identifier */
#define VPD_OPTIONS_SN        0x03 /* Serial Number */
#define VPD_OPTIONS_REV       0x08 /* Revision/Edition */
#define VPD_OPTIONS_DC        0x09 /* Date code */
#define VPD_OPTIONS_CPU_TYPE  0x20 /* CPU identifier */
#define VPD_OPTIONS_CPU_SPEED 0x21 /* CPU Clock Speed */
#define VPD_OPTIONS_EXTAL     0x22 /* Crystal Oscillator */
#define VPD_OPTIONS_EXTCLK    0x23 /* Off-Chip Oscillator Input */
#define VPD_OPTIONS_OSCCLK    0x24 /* Oscillator (SPLL Input) */
#define VPD_OPTIONS_RTCCLK    0x28 /* Time Keeper calibration */
#define VPD_OPTIONS_DRAM      0x30 /* DRAM Configuration */
#define VPD_OPTIONS_SRAM      0x34 /* SRAM Configuration #1 */
#define VPD_OPTIONS_SRAM2     0x35 /* SRAM Configuration #2 */
#define VPD_OPTIONS_ROM       0x38 /* ROM Configuration */
#define VPD_OPTIONS_FLASH     0x3C /* Flash Configuration #1 */
#define VPD_OPTIONS_FLASH2    0x3D /* Flash Configuration #2 */
#define VPD_OPTIONS_IP        0x40 /* IP Interface Configuration */
#define VPD_OPTIONS_PCMCIA    0x42 /* PCMCIA Interface Configuration */
#define VPD_OPTIONS_VME       0x44 /* VME Interface Configuration */
#define VPD_OPTIONS_VME2      0x45 /* VME Interface Configuration #2 */
#define VPD_OPTIONS_EA        0x60 /* Ethernet Address #1 */
#define VPD_OPTIONS_EA2       0x61 /* Ethernet Address #2 */
#define VPD_OPTIONS_EA3       0x62 /* Ethernet Address #3 */
#define VPD_OPTIONS_USER      0x80 /* Start of user's parameters */
```

For more information about the VPD structure, contact Actis Computer.

See also

-

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External Routine

Description

When an external routine must be executed, ECMon calls this external routine by using the following prototype:

```
struct _ecmon_jmptbl
{
    /* <<< ECMon V1.0 >>> */

    /* Serial functions */
    int (* _getc)( unsigned int port, unsigned long timeout );
    int (* _gets)( unsigned int port, char * str, unsigned long size );
    int (* _putc)( unsigned int port, int chr );
    int (* _puts)( unsigned int port, const char * fmt, ... );

    /* <<< ECMon V1.2 >>> */

    /* ECMon version (after serial functions for compatibility) */
    unsigned short _ecmon_version;
    unsigned short _board_version;

    /* <<< ECMon V2.0 >>> */
    /* <<< ECMon V2.1 >>> */
    /* <<< ECMon V2.2 >>> */
};

int external_routine
(
    const struct _ecmon_jumptbl * jumptbl, /* PPC - R3 */
    const char *                  bootargs /* PPC - R4 = getenv( "BOOTARGS" ) */
);
```

Normally, the called routine should not return (if not, the called routine must not corrupt the ECMon's configuration).

See also

env

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9 Web resources

This documentation is available for engineering and certified integrator companies which use the VSBC-6872 processor board. Additional technical information may be needed for specific software development, and third-party documentation must be used for a detailed description.

ACTIS Computer, VSBC-6872 (datasheet, application note)
http://support.actis-computer.com/

Freescale, PowerPC MPC8270
http://e-www.motorola.com/

Micron MT48LC16M16A2TG, SDRAM devices
http://www.micron.com/

Fujitsu MBM29DL323TE, FLASH memory
http://www.fma.fujitsu.com/

AMD AM79C874VC, Fast Ethernet PHY
http://www.amd.com/us-en/

Fairchild FM24C08, I2C EEPROM memory
http://www.fairchild.com/

STMicroelectronics M48T37V, real-time clock device
http://www.st.com/

Silicon Image Sil3512, S-ATA Drive Controller
Please contact, Actis Computer http://support.actis-computer.com/

VMEbus specification
http://www.vita.com/

PCI specification
http://www.pcisig.com/

PMC specification
http://www.vita.com/

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10 Ordering information

Part number	/	CPU speed option	SDRAM size option	Flash size option	-	Equipment version	Description
VSBC-6872							
							A*
							B
							Flash memory size
							E : 16 Mbyte *
							F : 32 Mbyte
							SDRAM memory size
							H : 128 Mbyte*
							J : 256 Mbyte
							CPU Frequency
							F : 450 MHz*

Example: VSBC-6872/FHE-A

* Standard product. For other configuration, please contact Actis Computer sales department.

Equipment version	T°range	One PMC slot	Three Fast Ethernet ports	Two S-ATA ports	Four multi – protocol serial links	One CompactFlash Socket	One Console Port	One RTC
A	0°C / +55°C	✔	✔	✔	✔	✔	✔	✔
B	-25°C / +71°C	✔	✔		✔	✔	✔	✔

Accessories and BSP software

The Actis Computer accessories allow a VSBC-6872 friendly use.

Part number	Description
CAB-RJ45-DB9	Console cable for standard male DB-9
CAB-PSCC04	SCSI 50-pin connector to four DB25 adaptor cables. Support RS-232, RS-422, RS-485 and V.35 interfaces.
BSP/VW/V6872	VxWorks Board Support Package
BSP/UX/V6872	Linux Board Support Package

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11 Sales department

If you need commercial information about the VSBC-6872 board, please contact our Sales Department as follows:

ACTIS Computer
North America Sales department : Email : usasales@actis-computer.com
Other countries Sales department :Email : sales@actis-computer.com

12 Technical Support

For up-to-date product information, including manuals, datasheets, application notes, PCN, etc, please consult our technical support web site http://www.actis-computer.com



12.1 Hardware and Software Assistance

If you encounter any installation trouble or any hardware or software related issues, please contact our technical support as follows:

ACTIS Computer
Technical support department : Email : support@actis-computer.com

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13 OEM Warranty

ACTIS Computer, warrants their product against any defect in material and workmanship, under normal use, for a period of two years from the date of purchase. In the event this product is found to be defective within the warranty period, ACTIS Computer will, at its option, repair or replace the defective single board computer.

This warranty is void if:

a) The board was operated or stored under condition of abnormal use or maintenance
b) The board is repaired, modified or altered, unless such repair, modification or alteration is expressly authorized in writing by ACTIS Computer
c) The board was subject to abuse neglect, lighting strike, electrical fault, improper packaging or accident
d) The board was installed improperly
e) The serial number of the board is defaced or missing
f) The board was not purchased from ACTIS Computer or from an authorized retailer

ACTIS Computer will not, under circumstances, be liable for direct, special or consequential damages such as, but not limited to, damage or loss of property or equipment, loss of profits or revenues, cost of replacement goods, or expense or inconvenience caused by service interruptions. Under no circumstances will any person be entitled to any sum greater than the purchase price paid for the board.

The warranty service is available y contacting your local ACTIS Computer representative, and provide your purchase order information to ensure warranty terms appliance. All board returned for repair or inspection operation need to be returned into their original box.

13.1 RMA request

To request a Return Merchandise Authorization (RMA) number, you need to contact your local ACTIS Computer representative.
ACTIS Computer will only accept product return from its agreed representative network, OEM customer need to contact its local representative to handle this procedure. ACTIS Computer will not accept product without RMA identification.

The RMA request procedure requires the following information:

- Customer information
- Product identification (quantity, reference, serial number)
- Purchase date
- Fault description

For further assistance, please get detailed information about our technical support team to the Hardware and Software Assistance section.

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