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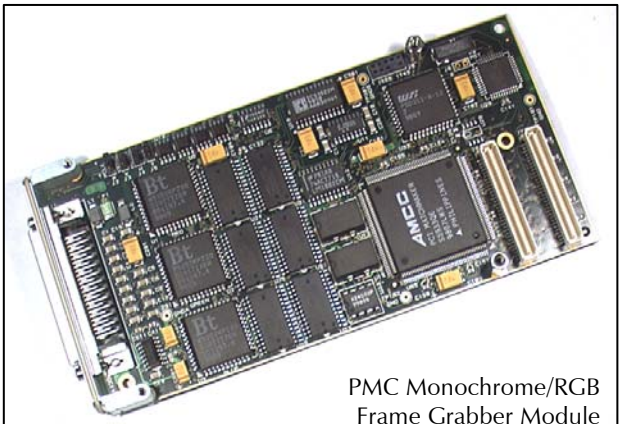
Find the *Active Silicon Snapper-PMC-8* at our website: ***Click HERE***

Active Silicon

SNAPPER-PMC-8/24

MONOCHROME • RGB • YCbCr • VIDEO DIGITIZER

- High quality analogue video acquisition board with square pixel sampling for CCIR, EIA (RS-170) standards, and non-standard video formats.
- Supports configurable RS-422 or TTL control, pixel clock and external trigger.
- Software programmable on-board sync generator.
- 8 bit Look Up Tables (LUTs).
- Software programmable black, white and clamp levels.
- On-board frame store with high speed readout, including PCI bus interface supporting 132 Mbytes/sec burst transfers. Support for master and slave operation.
- Hardware Region of Interest (ROI) and sub-sampling.
- On-board Data Mapper for hardware pixel mappings.
- Software Development Kit (SDK) for rapid integration.



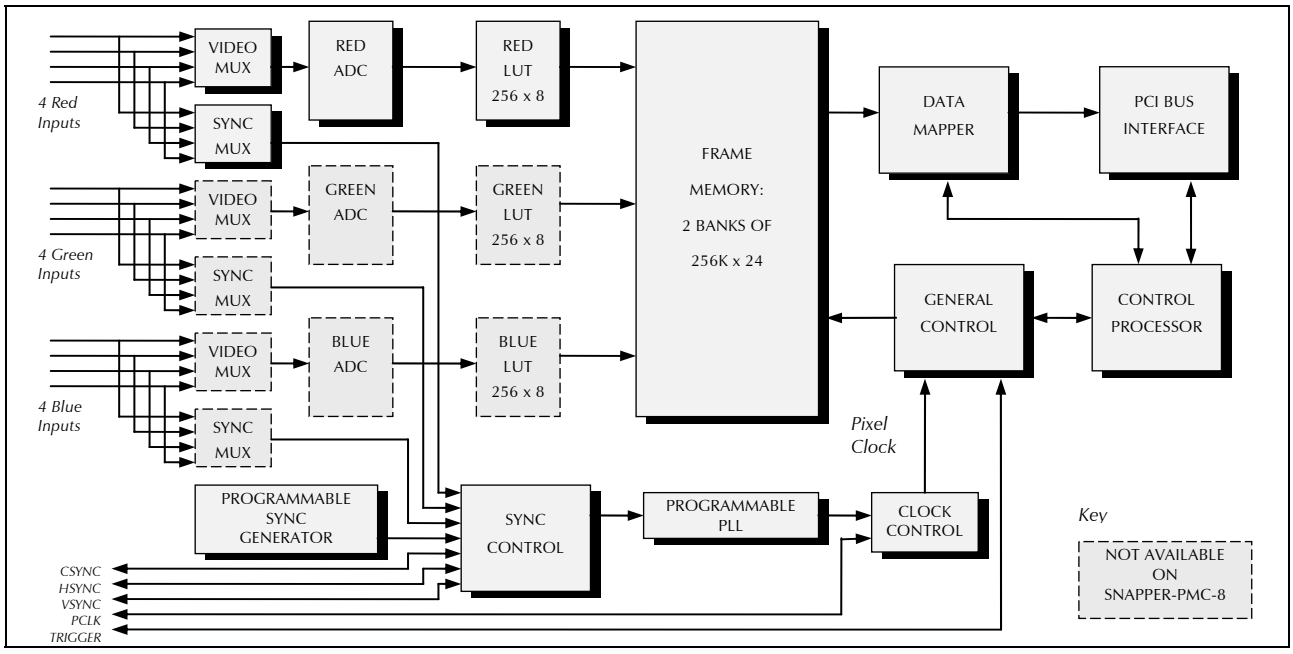
PMC Monochrome/RGB
Frame Grabber Module

OVERVIEW

Snapper-PMC-8/24 is high speed PCI board for the acquisition of standard CCIR or EIA/RS-170 video standards as well as slow scan and line scan cameras. The board is available in two variants, ***Snapper-PMC-24*** for RGB colour or monochrome video, and ***Snapper-PMC-8*** for monochrome only. Each channel is digitized via an 8 bit ADC, processed through an 8-bit programmable LUT (Look-Up Table), and then stored in on-board frame memory. Four software selectable inputs allow 4 RGB cameras or 12 mono cameras to be connected to a ***Snapper-PMC-24*** (or 4 mono cameras to a ***Snapper-PMC-8)***. A custom FPGA (field programmable gate array) then performs optional sub-sampling and region of interest generation for maximum flexibility and readout speed. The on-board frame buffer consists of two banks, each capable of holding 256K pixels. The frame memory architecture allows de-interlacing on readout. A programmable PLL (phase locked loop) and sync generator combined with the custom FPGA provides versatile sync and clock options for both input and output. An on-board hardware Data Mapper provides mapping and packing functions for the conversion of data, if required, to pixel formats suitable for immediate display. PMC (PCI Mezzanine Card) is a subset of the CMC (Common Mezzanine Card) IEEE standard P1386, that uses the industry standard PCI interface bus. ***Snapper-PMC-24*** is fully compliant with this standard.

The Software Developer's Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimised libraries, and is available for a variety of operating systems including Windows 3.1x/95/98/NT, MacOS 7/8, MS-DOS, Solaris 2, LynxOS and VxWorks. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A

Snapper-PMC-24 Block Diagram



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separate datasheet describes the SDK in detail.

CAMERA INTERFACE SPECIFICATION

Video Input: Each of the three ADCs has a four to one input multiplexer allowing each video channel to independently select one of four sources. Each video source is 75 Ohm terminated. The selection of any one of these video sources is under software control. On the ***Snapper-PCI-24*** this allows one of four RGB sources or three of twelve monochrome sources to be selected under software control. These three multiplexers have individual control, so if required the red input of channel 1 can be digitized at the same time as the green input of channel 3 and the blue input of channel 4. For the ***Snapper-PCI-8*** a maximum of four monochrome cameras can be supported. Video inputs are DC-restored to a programmable level. On the YCbCr version the RGB inputs can be redefined as YCbCr inputs, with the Cb and Cr inputs DC-restored to mid-level.

Sampling: By default CCIR video signals (European) are sampled at 14.75MHz and EIA video signals (USA and Japan) at 12.27MHz, resulting in square pixel sampling for both standards. These sampling frequencies are fully programmable under software control, which can be useful for zero aliasing with the internal pixel clock for CCD cameras. The video standard can be auto-sensed. Images are digitized in real-time - i.e. 40ms for full frame CCIR and 33ms for EIA. Maximum sampling rate is 20MHz.

Digital Video: As default standard RGB or monochrome video signals are digitized to 24 bits (8 bits for each of red, green and blue) with black level at 0 and peak white at 255. The control of black and white level can be fully adjusted under software control. In the software library an AGC function is provided to set the levels to the above default one or several others including CCIR 601 quantization levels. On the YCbCr version, the default levels are 16 to 235 for luminance and 44 to 212 for chrominance (75% colour bars). These quantization levels conform to CCIR Recommendation 601-2.

LUTs: The output of each ADC drives a 256 by 8 look up table (LUT). This allows functions such as gamma correction, brightness, contrast, and thresholding to be performed in real time in hardware. For the ***Snapper-PCI-24*** the three LUTs can be accessed individually, or all three can be written in parallel for speed.

Resolution: CCIR video images are digitized to a resolution of 768 x 576 and EIA (RS-170) video images to 640 x 480. These resolutions represent the full active picture area of the video signal. Non-standard cameras, such as line scan cameras can also be digitized in real-time at any resolution provided one frame or (one line) can fit into the frame store.

Sync: The sync source can be selected from one of the following:

- Any one of the video inputs (regardless of which of the inputs is being digitized).
- A separate 75 Ohm composite sync input *CSYNC* (which will accept negative going black level sync, or negative TTL level into 75 Ohms, or video including composite video).
- Separate horizontal sync and vertical sync inputs *HSYNC* and *VSYNC*. These are jumper selectable as either TTL or RS-422 (differential) levels. These inputs are individually programmable as negative or positive going.
- The on-board programmable sync generator.

The sync generator is fully programmable, with full register control of pulse widths and positions, interlaced / non-interlaced mode, and the presence / absence of double serration pulses. To ensure correct frequencies are generated the module is fitted with two crystal oscillators - one at 29.50MHz for CCIR use and one at 14.31818MHz for EIA use.
If *CSYNC*, *HSYNC* or *VSYNC* are not being used as inputs they can be individually driven as outputs. The output is in the same format as the corresponding input; i.e. *CSYNC* is black level (0.3V) into 75 Ohms, and *HSYNC* and *VSYNC* are either TTL or RS-422. *HSYNC* and *VSYNC* are individually programmable as negative or positive going. The *HSYNC* output can also be driven out as *CSYNC* with either TTL or RS-422 levels.
Note: Selection between TTL and RS-422 on *HSYNC* and *VSYNC* is achieved with jumpers. All other modes are controllable by software. *HSYNC* and *VSYNC* can be supplied to special order with 75 Ohm terminators fitted for use with sync sources which provide TTL levels into 75 Ohms, in which case the corresponding TTL outputs cannot be used.

Clock: The selected sync source drives the programmable phase locked loop (PLL), which normally provides the module's pixel clock. The PLL uses the latest monolithic frequency synthesizer technology, and allows control of pixels per line, phase detector gain, oscillator (VCO) gain, fast or slow loop filters, and a choice of four phases of clock (0°, 90°, 180° or 270°). The slow loop filter allows lock to poor sources such as video recorders. The PLL jitter is typically ±3ns, worst case ±7ns. Note that to achieve this performance a stable sync source, such as obtained using the separate *HSYNC* and *VSYNC* inputs, must be used. If a relatively poor sync source is used, such as composite video, typical jitter figures are around ±7ns to ±20ns.

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As an alternative to the PLL, the module's pixel clock can be provided by a pixel clock input 'PCLK'. This is jumper selectable as either TTL or RS-422 (differential), and either the positive or negative edge can be selected as the active edge. If PCLK is not being used as an input it can be driven as an output, with either the positive or negative edge selected as the active edge. The output is in the same format as the input; i.e. either TTL or RS-422. PCLK can be supplied to special order with a 75 Ohm terminator fitted for use with clock sources which provide TTL levels into 75 Ohms, in which case the corresponding TTL output cannot be used.
When PCLK is used, *HSYNC* and *VSYNC* inputs can function as line and frame enables.
Note: Selection between TTL and RS-422 on PCLK is achieved with jumpers. All other modes are controllable by software

Region of Interest: A region of interest (ROI) for acquisition and readout is software programmable. The horizontal start and length are controllable to a resolution of 8 pixels and the vertical start and length are controllable to a resolution of 2 lines. (The vertical start position must be less than 254 lines down the field.)

Sub-sampling: Sub-sampling can be performed in hardware and is software programmable. Sub-sampling can be by two or by four:
x2: Every 2nd pixel in the horizontal direction and only the first field of each frame.
x4: Every 4th pixel in the horizontal direction and every second line of the first field of each frame.

Frame Store: The video frame store consists of either 1 or 1.5 Mbytes of RAM configured as FIFO memory. The memory is arranged as two banks of 256K pixels - one bank for each video field. The two banks are accessed independently such that one field of data can be stored in the first memory bank whilst the previous field is read from the second. This allows data to be acquired at full video rates without missing fields. Alternatively the hardware can de-interlace captured video images on readout by switching banks on a line by line basis. (This de-interlacing method is hidden to the user in the software library).
Colour data is stored as full 24 bits. 8 bit Grayscale data is pre-packed to 16 bits in the Frame Store so that 2 data pixels can be read in a single PCI clock, thus doubling the read out rate. This data can be mapped to other pixel formats using the Data Mapper, (see the PCI Bus Interface section).

Trigger: A separate TTL / RS-422 trigger input 'TRIG' is provided for synchronization to external events - for example to synchronize to a strobed flash gun. The polarity of the trigger input is software programmable. Asynchronous reset cameras are fully supported in this mode.
If TRIG is not being used as an input it can be driven as an output under software control. The output is in the same format as the input; i.e. either TTL or RS-422. TRIG can be supplied to special order with a 75 Ohm terminator fitted for use with trigger sources which provide TTL levels into 75 Ohms, in which case the corresponding TTL output cannot be used.
Note: Selection between TTL and RS-422 is achieved with jumpers. All other modes are controllable by software.

Controls: Brightness, contrast and DC restoration level are performed in hardware under software control. These controls adjust the digitization levels for black level, white level and clamp level of the video signal. For example, this level of control allows a small range of the input video to be digitized to the maximum of 256 levels per ADC to provide contrast enhancement.

Interrupts: An interrupt signal is available and can be configured via software to interrupt on various events. Consult the "Snapper-24 Library – Programmer's Manual" for more details. Polled operation is also supported.

+12V Out: The raw +12V from the host machine power supply is output to provide power for the camera, if required. The output is protected by a resetable fuse, and is capable of sourcing 400mA.

Connectors: A 50 way mini D SCSI-2 style socket connects signals into the module.

Snapper-PMC-8: Snapper-PMC-8 is functionally identical to Snapper-PMC-24 with the following exceptions:

- Snapper-PMC-8 only has the Red channel ADC, and LUT fitted.
- Snapper-PMC-8 only has 1Mbyte of memory fitted, rather than 1.5MBytes..
- Snapper-PMC-8 has the Clamp Voltage level fixed at 0.17V, rather than being software

USA
Active Silicon
17 Wilson Street, Suite 13, Chelmsford
MA 01824 USA

Tel +1 978 244 0490
Fax +1 978 244 0491
info@activesilicon.com

Europe
Active Silicon Limited
Brunel Science Park, Kingston Lane, Uxbridge
Middlesex UB8 3PQ UK

Tel +44 (0) 1895 451972
Fax +44 (0) 1895 230131
info@activesilicon.com

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prior to PCI bus transfer).

Data Rates: Bus master DMA supports 132 Mbytes/sec data transfer rate. The PCI data is generated by the Data Mapper reading from the Frame Buffer memory. For 24 bit RGB data, 1 pixel is transferred on each PCI clock, whereas for grayscale data, 4 pixels are transferred on alternate PCI clocks.

Address Range and Interrupts: Automatically mapped to I/O space. Board requires 64 bytes of address space. Interrupts automatically selected by host operating system.

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	PCB: 149mm by 74mm. With connector (overall): 155mm by 74mm.
Approximate weight:	104g.
Mounting pillar height:	10mm.
IEEE Standard:	P1386 Draft 2.0, 4th April 1995 and P1386.1 Draft 2.0, April 1995.
Power consumption:	+5V @ 1.9 Amps, +12V @ 20mA, -12V @ 15mA.
Storage Temperature:	-15°C to +70°C.
Operating Temperature:	0°C to +55°C.
Relative Humidity:	10% to 90% non-condensing (operating and storage).
EMC Approvals:	CE mark for compliance with EN 55022:1994 (class B) and EN 50082-1:1992 in accordance with EU directive 89/336/EEC. FCC Class A.

Full mechanical drawings are available on request.

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
SNP-PMC-8 SNP-PMC-24	***Snapper-PMC-8*** monochrome frame capture board, or ***Snapper-PMC-24*** RGB frame capture board.
CBL-50MD-SNP CBL-50MD-SNP-8	***Snapper-PMC-8/24*** cable assembly. Both cables contain a trigger input/output and an analogue sync input/output. The CBL-50MD-SNP also contains a single set of RGB inputs whereas the CBL-50MD-SNP-8 contains four monochrome inputs. Other custom cables can be made to order. Please contact Active Silicon for more information.
-	Software Developer's Kit. For a full list of all supported operating systems, support contracts and other options, please refer to the SDK datasheet, or contact Active Silicon directly. Currently supported operating systems include Windows NT, Windows 95, Windows 98, Windows 3.1x, MS-DOS, Solaris 2, VxWorks, LynxOS and MacOS.

ORDERING NOTES

- Please contact Active Silicon for latest information on other Snappers, Bus Interface Boards, and supported OS.

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Additional Technical Information for Snapper-PMC-8/24

Connector Pinout

A 50 way mini D SCSI-2 style socket connects signals into the module.

Pin Number	Snapper-PMC-24
1	Digital Ground
2	Pixel Clock-
3	Digital Ground
4	Digital Ground
5	VSync-
6	HSync-
7	Trigger-
8	Digital Ground
9	Digital Ground
10	Analogue Ground
11	Analogue Ground
12	Red #3
13	Analogue Ground
14	***Red #1***
15	Analogue Ground
16	Green #3
17	Analogue Ground
18	***Green #1***
19	Analogue Ground
20	Blue #3
21	Analogue Ground
22	***Blue #1***
23	Analogue Ground
24	Analogue Ground
25	Analogue Ground

Pin Number	Snapper-PMC-24
26	+12V Out
27	Pixel Clock+
28	+12V Out
29	Digital Ground
30	VSync+
31	HSync+
32	***Trigger+***
33	***Digital Ground***
34	Analogue Ground
35	Analogue Ground
36	***CSync***
37	Analogue Ground
38	Red #4
39	Analogue Ground
40	Red #2
41	Analogue Ground
42	Green #4
43	Analogue Ground
44	Green #2
45	Analogue Ground
46	Blue #4
47	Analogue Ground
48	Blue #2
49	Analogue Ground
50	Analogue Ground

NOTES:

1. The signal names in ***bold italics*** are available on the standard cable, (Part number CBL-50MD-SNP).
2. Signals labelled as *Sig+* and *Sig-* are the two halves of the RS-422 signals and must be connected to twisted pair cabling.
3. When using the TTL level trigger, connect the input to *TRIGGER+*.

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