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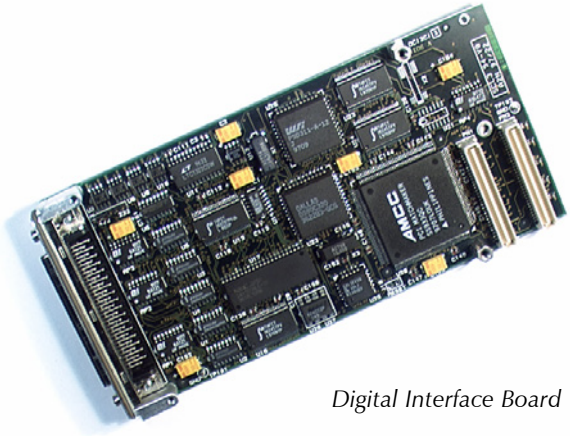
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16 BIT DIGITAL CAMERA INTERFACE

- Support for digital cameras, including Kodak Mega-plus 1.4, 1.4i, 1.6, 1.6i, 4.2 and XHF, Hamamatsu C4742 and C4880, Pulnix TM-1000, TM-1001, TM-9700, TM-9701, and all AIA compliant monochrome cameras.
- Support for digital line scan cameras, including two-tap - for example the Dalsa and Basler ranges.
- Maximum acquisition rate of 25 Msamples/sec or 20 Msamples/sec with hardware region of interest (ROI) and sub-sampling.
- Camera interface provided by reconfigurable FPGA.
- Module fitted with 68 way connector for direct connection to AIA compliant monochrome cameras. Cables are available to connect to other cameras.
- PMC IEEE standard P1386 compliant.
- Software Development Kit (SDK) for rapid integration.



Digital Interface Board

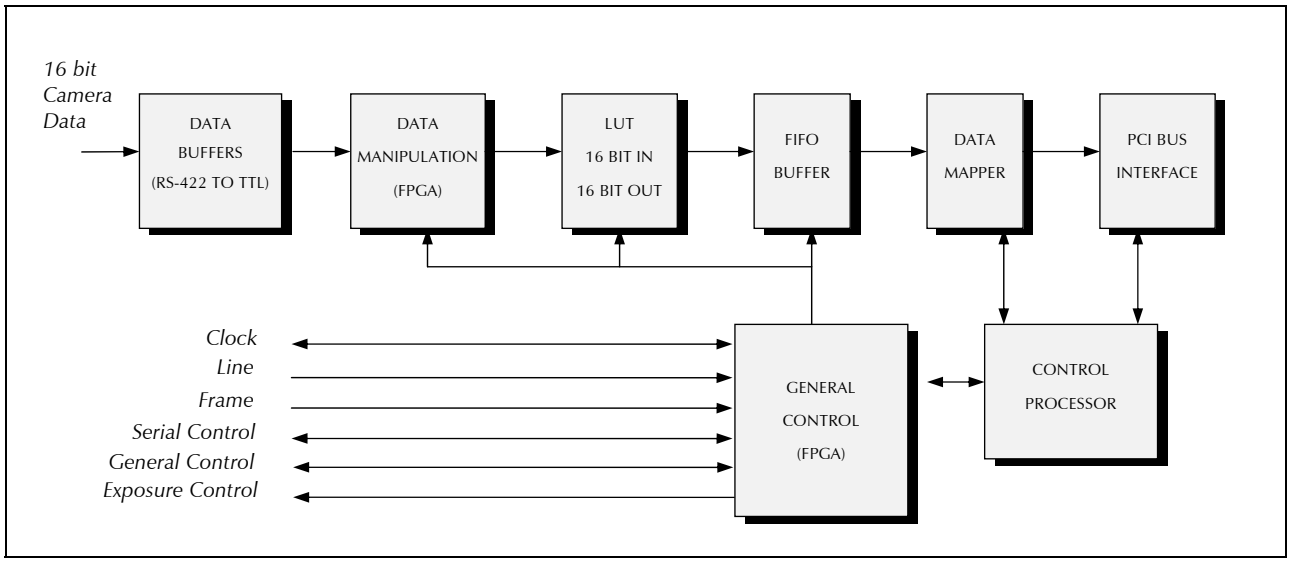
OVERVIEW

Snapper-PMC-DIG16 is a compact module for the acquisition of digital data from a variety of sources including digital frame capture cameras and digital line scan cameras. The module is based around a custom FPGA (field programmable gate array) which is loaded under software control during initialisation. This allows the many variants of digital cameras to be accommodated without the need for hardware modifications. This FPGA also performs optional sub-sampling and region of interest generation for maximum flexibility and frame update rate. The data from the FPGA is fed through a fully programmable 16 bit in/16 bit out LUT which provides support for MSB and LSB data alignment, dynamic range cropping, gamma correction and binary thresholding. Dynamic range cropping is used to reduce a camera's output to eight bits per pixel for faster DMA transfer to host memory. The LUT output is then stored in a FIFO buffer.

An on-board hardware Data Mapper provides mapping and packing functions for the conversion of data, if required, to pixel formats suitable for immediate display. This formatted data is then transferred across the PCI bus to host memory.

The Software Developer's Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimised libraries, and is available for a variety of operating systems including Windows 3.1x/95/98/NT, MacOS 7/8, MS-DOS, Solaris 2, LynxOS and VxWorks. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A separate datasheet describes the SDK in detail.

Snapper-PMC-DIG16 *Block Diagram*



SPECIFICATION

Data Input: Up to 16 bit digital data in RS-422 (differential) format. For cameras which generate less than 16 bit data, unused inputs can be masked under software control. Video data can be LSB or MSB aligned.

LUT: A 16 bit in, 16 bit out (i.e. 65536 by 16) LUT allows arbitrary mappings between input data from the camera and output data to the Bus Interface Board. This allows functions such as gamma correction, brightness, contrast and thresholding to be performed in real time in hardware. The LUT is also used to provide barrel roll functions which means that if required the MSB from the camera can always be mapped to the MSB of the output data regardless of the number of valid data bits from the camera. To speed up LUT access only part of the LUT needs to be written if the camera has less than 16 valid bits - for example only 256 out of 65536 entries need to be written if an 8 bit camera is connected.
For two tap cameras, the full LUT can be used to manipulate the two 8 bit data paths independently.

FIFO: A 16384 by 32 bit FIFO provides buffering between the camera and the Bus Interface Board. Note that this is not a frame store – ***Snapper-PMC-DIG16*** supports high speed DMA across the PCI bus and therefore the amount of data acquired is limited only by the amount of available memory in the host.

Output Format: Data (either 8 bit or 16 bit) is packed into 32 bit words before being written to the FIFO. On reading from the FIFO, the data can be mapped using the Data Mapper to other pixels formats, for example 16 bit RGB data, for fast display to a 65k colour display.

Clock: The module's pixel clock is normally provided by a pixel clock input *STROBE*. This is an RS-422 (differential) signal, and either the positive or negative edge can be selected as the active edge. The maximum clock rate is 20 MHz, that is camera data can be stored at a rate of 20 Msamples/sec resulting in a maximum bandwidth of 40 Mbytes/sec for 16 bit cameras. If ROI functions are not needed the maximum clock rate increases to 25 MHz.
Alternatively *STROBE* can be driven as an RS-422 output, with either the positive or negative edge selected as the active edge. The output clock rate can be one of the following: 250 kHz, 500 kHz, or 1, 2, 2.5, 3.125, 4, 5, 6.25, 8, 10, 12.5, 16, 20, 25, 33, 40 or 50MHz.
For use with cameras which must receive a clock and which also return a clock it is possible to drive a clock out on a general purpose I/O line and receive clock on *STROBE*.

Region of Interest: A region of interest (ROI) for acquisition and readout is software programmable. Area scan ROIs can be captured up to a maximum size of 8192 by 8192, with the start of the ROI being up to 8192 lines after the start of the frame enable, and up to 8192 pixels after the start of the line enable. Line scan ROIs can be up to 65535 pixels across. Horizontal co-ordinates are controllable to a resolution of 1 pixel, and vertical ROI co-ordinates are controllable to a resolution of 1 line.

Sub-sampling: Sub-sampling can be performed in hardware and is software programmable. Sub-sampling can be by one, two, four, or eight. For example, with a non-interlaced camera, sub-sampling by two will acquire every other pixel and every other line.

Readout Time: 32 bit data is read from the FIFO at full PCI clock rates. This means that, for example, if the PCI clock is running at a typical 33 MHz, the readout rate from the FIFO through the Data Mapper into the PCI bus interface will be 132 Mbytes/sec - equivalent to the maximum PCI bus data rate.

Line and Frame Enables: The line and frame signals are normally provided by the inputs *LINE_EN* and *FRAME_EN*. These are RS-422 (differential) signals, and can be either active high or active low. These signals connect via buffers to the FPGA so cameras which do not use conventional line or frame enables can be supported via custom FPGA configuration files. (Consult Active Silicon for further details). For line scan cameras these signals are redefined to allow a programmable line start signal to be driven out to the camera, as well as *LINE_EN* being received from the camera.

Control Lines: These comprise four general purpose I/O lines, four general purpose output lines, two TTL inputs, and one comms port:

General Purpose I/O Lines *(IO_A, IO_B, IO_C, IO_D):* These are all RS-422 (differential) signals. The SDK library allows direct software control of these lines which can be individually selected as inputs whose value can be read, output high, or output low. Where these lines are used by a supported camera, higher level functions are supplied in the SDK providing functions such as for exposure mode control.
General Purpose Output Lines *(OUT_A, OUT_B, OUT_C, OUT_D):* These are all RS-422 (differential) signals , although they can also be used as complementary TTL level outputs. The SDK library allows direct software control of these lines which can be individually selected as output high or output low. Where these lines are used by a supported camera, higher level functions are supplied in the SDK providing functions such as "Shutter On". One of these lines (*OUT_A*) can be used to provide exposure time - see 'Exposure Pulse' below.
TTL Inputs *(TTL_TRIG1, TTL_TRIG2):* These two TTL level inputs can be used for triggers, as alternatives to the general purpose RS-422 I/O lines.
Comms Port*:* A standard asynchronous bi-directional communications port allows serial control of

cameras. It can be configured at either RS-422 or RS-232 levels with transmit and receive data. Data format is configurable to be 7 or 8 data bits, 1 or 2 stop bits, and either odd, even, mark, space or no parity. Standard baud rates from 600 to 19200 are supported, as well some as faster rates such as 28800 and 57600. Non-standard rates are available to special order. (Consult Active Silicon for further details).

Exposure Pulse: The general purpose line *OUT_A* can generate a programmable hardware timed pulse which can be used to provide exposure time control etc. The maximum width and resolution of this pulse is up to a 24 hour pulse with a resolution of several microseconds for short pulses or several milliseconds for long pulses.

Interrupts: An interrupt signal is available and can be configured via software to interrupt on "acquisition complete". Polled operation is also supported.

Connectors: A 68 way high density socket.

PCI BUS INTERFACE SPECIFICATION (INCLUDING DATA MAPPER)

Interface: PCI (Peripheral Component Interconnect) Bus to PCI Local Bus Specification Revision 2.1 using 5V signalling environment.

Data Mapper: 8 or 16 bit data can be mapped to 32 bit RGBX, XBGR, BGRX, XRGB or to 16 bit RGB as RGB16 or RGB15. (All data formats are automatically packed to 32 bits prior to PCI bus transfer).

Data Rates: Bus master DMA supports 132 Mbytes/sec data transfer rate. The PCI data is generated by the Data Mapper reading from the 32 bit wide FIFO memory. PCI data can be read on every clock, and is therefore capable of bursting at the full 132Mbytes/sec transfer rate.

Address Range and Interrupts: Automatically mapped to I/O space. Board requires 64 bytes of address space. Interrupts automatically selected by host operating system.

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	PCB: 149mm by 74mm. With connector (overall): 156mm by 74mm.
Approximate weight:	90g.
Maximum component height:	4.8mm.
Mounting pillar height:	10mm.
Snapper connectors:	Two 58 way, 0.1" pitch connectors, each arranged as two rows of 29.
Power consumption:	+5V @ 0.8 Amp.
Storage Temperature:	-15°C to +70°C.
Operating Temperature:	0°C to +55°C.
Relative Humidity:	10% to 90% non-condensing (operating and storage).
EMC Approvals:	CE mark for compliance with EN 55022:1994 (class B) and EN 50082-1:1992 in accordance with EU directive 89/336/EEC. FCC Class A.

Full mechanical drawings are available on request.

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
SNP-PMC-DIG16	***Snapper-DIG16*** 16 bit digital camera interface module with a PMC interface
SNP-PMC-DIG16-50M	LVDS variant of the above (maximum pixel clock rate of 50MHz)
CBL-68-AIA-A-6M	6m long cable for AIA compliant cameras.
CBL-68-AIA-A-3M-NC	3m long cable with single connector - for use with custom cameras.
CBL-68-37D-A-3M	3m long cable for Kodak Megaplus 1.4, 4.2, and Hamamatsu C4742.
CBL-68-44D-A-3M	3m long cable for Basler L120
CBL-68-PULNIX1000-ADP	Short adapter cable for connection to Pulnix TM1000, TM1001, TM9700, TM9701 cameras via Pulnix cable 30DG-02.
CBL-68-XILLIX1400-3M	3m long cable for Xillix Micro Imager 1400 (10 and 12 bit versions).
CBL-68-HAM-A-2M	2m long cable suitable for most Hamamatsu cameras, including the C4880 and C4742-95, with separate BNC trigger input and output.
CBL-68-DALSA-CLC-A-3M	3m long cable for connection to the Dalsa CLC series line scan cameras with one or two output channels (OS1, OS2).
-	Software Developer's Kit. For a full list of all supported operating systems, support contracts and other options, please refer to the SDK datasheet, or contact Active Silicon directly. Currently supported operating systems include Windows NT, Windows 95, Windows 98, Windows 3.1x, MS-DOS, Solaris 2, VxWorks, LynxOS and MacOS.

ORDERING NOTES

- Please contact Active Silicon for latest information on other Snappers, Bus Interface Boards, and supported operating systems.

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Additional Technical Information for Snapper-PMC-DIG16

Connector Pinout

A 68 way D type socket connects signals into the module.

Pin Number	Snapper-PMC-DIG16	Pin Number	Snapper-PMC-DIG16
1	GND	35	GND
2	MSB+	36	MSB-
3	MSB-1+	37	MSB-1-
4	MSB-2+	38	MSB-2-
5	MSB-3+	39	MSB-3-
6	MSB-4+	40	MSB-4-
7	MSB-5+	41	MSB-5-
8	MSB-6+	42	MSB-6-
9	MSB-7+	43	MSB-7-
10	MSB-8+	44	MSB-8-
11	MSB-9+	45	MSB-9-
12	GND	46	GND
13	MSB-10+	47	MSB-10-
14	MSB-11+	48	MSB-11-
15	MSB-12+	49	MSB-12-
16	MSB-13+	50	MSB-13-
17	TTL_TRIG1	51	N/C
18	TTL_TRIG2	52	N/C
19	MSB-14+	53	MSB-14-
20	MSB-15+	54	MSB-15-
21	IO_A+	55	IO_A-
22	CAM_SER_OUT+	56	CAM_SER_OUT-
23	CAM_SER_IN+	57	CAM_SER_IN-
24	IO_B+	58	IO_B-
25	FRAME_EN+	59	FRAME_EN-
26	LINE_EN+	60	LINE_EN-
27	IO_C+	61	IO_C-
28	IO_D+	62	IO_D-
29	STROBE+	63	STROBE-
30	OUT_A+	64	OUT_A-
31	OUT_B+	65	OUT_B-
32	OUT_C+	66	OUT_C-
33	OUT_D+	67	OUT_D-
34	GND	68	GND

NOTES:

1. Suitable cable connector: Honda PCS-XE68MA or equivalent with hood PCS-68LKAU2N or equivalent.
2. Connector fitted to ***Snapper-PMC-DIG16***: Honda PCS-XE68LFDTUN.

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