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USER DOCUMENTATION
FOR

5800 Series
Data Acquisition Boards

A2-12041 R1.07

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NOTES

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1. INTRODUCTION

1.1 CHOICE OF MODELS

The 5800 is part of an extensive line of data acquisition boards for the PC which includes boards optimized for use with windows, very low cost boards, sensor specific DIRECT CONNECT boards, isolated digital I/O boards, boards for DSP applications, PCMCIA cards, and more.

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Summary Of Models:

Windows Optimized	Model
12 bit, 100kHz, Low Cost	5508LF
12 bit, 333kHz	5801MF
12 bit, 333kHz, High Gain	5802MF
16 bit, 100kHz	5803HR
16 bit, 100kHz, High Gain	5804HR

Very Low Cost	Model
12 bit, 100kHz Lowest Cost	5508LC
12 bit, Multifunction	5500MF
12 bit, Multifunction	5516DMA
12 bit, Multifunction	5525MF
16 bit, Lowest Cost	5500HR

Sensor Specific	Model
Thermocouple Inputs	5508TC
RTD Inputs	5508RTD
Strain Gage Inputs	5508BG
Isolated Inputs	5508SCi

Digital Series	Model
Counter/Timers	5609CTR
120/240 VAC Detect	5608ACI (4000 Vrms isolation)
24/48 VDC Detect	5616DCI (4000 Vrms isolation)
Contact Closure Detect	5616CCI
120/240 VAC Switching	5608ACO (4000 Vrms isolation)
Relay Switching	5608ACO (4000 Vrms isolation)
24/48 VDC Switching	5616DCO (4000 Vrms isolation)
TTL Input/Output	5632TTL

C40 DSP Applications	Model
12 bit, 333kHz	5401DMF
12 bit, 333kHz, High Gain	5402DMF
16 bit, 100kHz	5403DHR
16 bit, 100kHz, High Gain	5404DHR

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1.2 SOFTWARE COMPATIBILITY

The 5800 Series boards are compatible with ADAC's ADLIB WIN (a full-feature Windows driver library). This library provides functions to set all of the software programmable modes of operation, and include examples to acquire and output data.

In addition, drivers are available for PC data acquisition packages such as TestPoint.

1.3 PRODUCT DESCRIPTION 5800 SERIES

The 5800 Series are high performance data acquisition boards for the PC ISA bus. The 5801MF and 5802MF have 16 single-ended or 8 differential analog inputs multiplexed to a 12 bit A/D converter with maximum throughput of 333 kHz. The 5803HR and 5804HR have 16 single-ended or 8 differential analog inputs multiplexed to a 16 bit A/D converter with maximum throughput of 100 kHz. Both boards feature a 1024 word FIFO and dual 16-bit DMA for optimum performance in a Windows environment. The boards also have 40 lines of TTL level digital I/O and two optional 16 bit D/A voltage outputs. Board connections on the 5800 are terminated in a 50 pin "D" connector at the rear of the PC. Two auxiliary IDC header connectors are located at the rear of the board to access the 32 lines of auxiliary digital I/O.

The 5800 Series cards have no hardware jumpers; all user options are set via software. The only exception is a hardware switch for base address selection.

1.3.1 Models

The 5800 Series of data acquisition boards includes four models. The following table describes the main differences between each model.

Product Name	ADC Resolution	Programmable Gains
5801MF	12-bit	1, 2, 4, 8
5802MF	12-bit	1, 10, 100, 500
5803HR	16-bit	1, 2, 4, 8
5804HR	16-bit	1, 10, 100, 500

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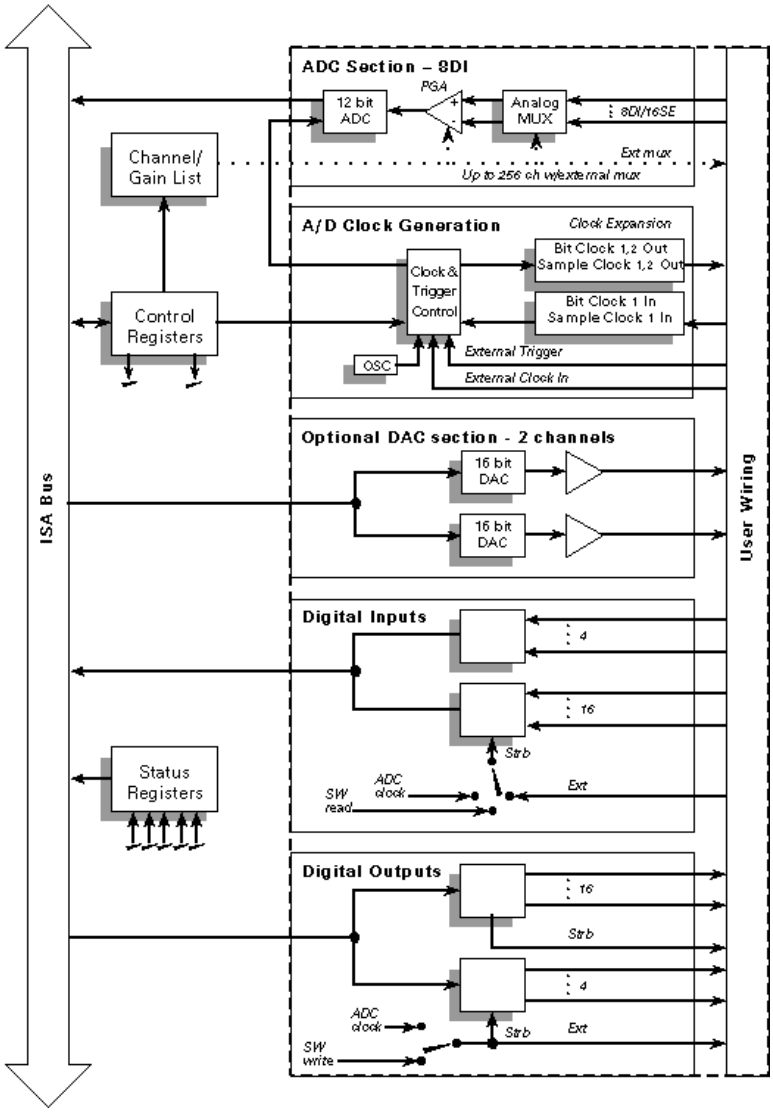


Figure 1.1 5801MF/5802MF Block Diagram

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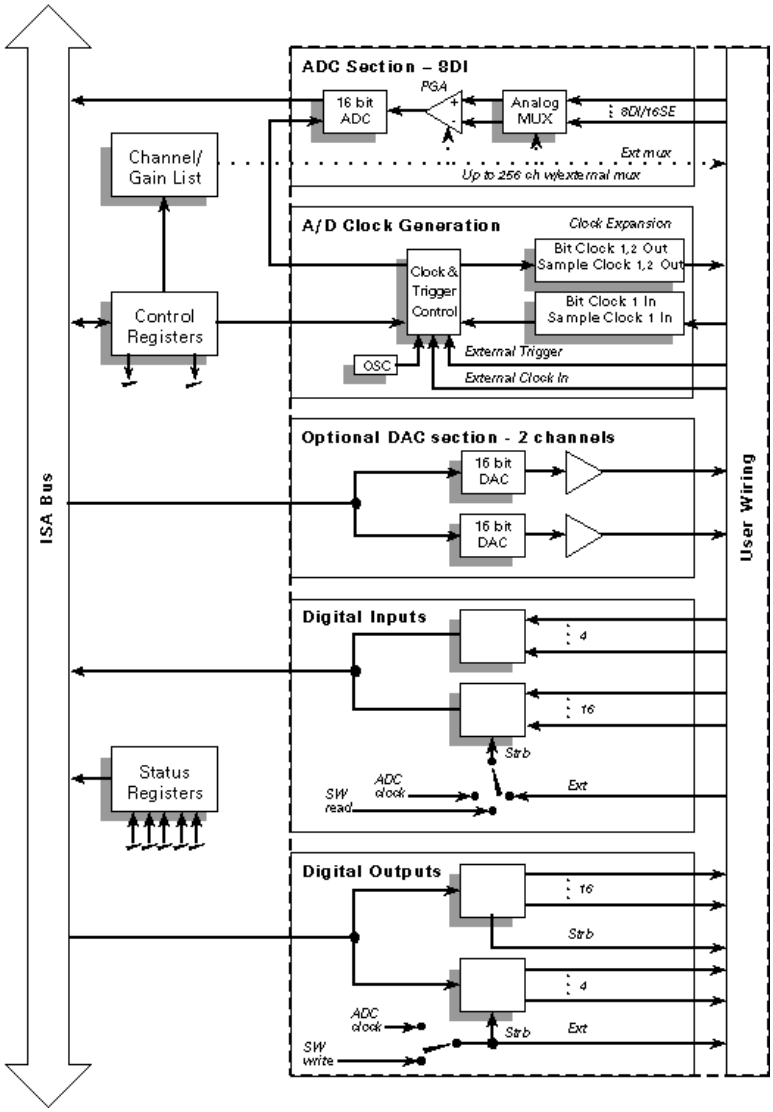


Figure 1.2 5803HR/5804HR Block Diagram

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1.3.2 Analog Inputs

Each of the 5800 Models supports 16 single-ended or 8 differential analog inputs (expandable to 64) multiplexed to a 12 or 16 bit A/D converter. The input multiplexer is supported by a 256 element channel gain RAM which allows the board to select gain on a per channel basis and to access channels in any order. The 12-bit ADCs have maximum throughput of 333 kHz and a programmable input range of ±10 V or 0-10 V. The 16-bit ADCs have throughput of 100 kHz and an input range of ±10 V. An on-board Counter/Timer circuit provides a trio of counters dedicated to A/D clocking functions.

1.3.3 Analog Outputs

The 5800 Series may be equipped with two optional, DC accurate, 16-bit resolution, DACs. The output range of the DACs is programmable to either ±10 V or 0 to +10 V. Boards with 16-bit ADCs (5803HR & 5804HR) are provided with DACs which are accurate to 15-bits, while the DACs provided on boards with 12-bit ADCs (5801MF & 5802MF) are 14-bit accurate.

1.3.4 Digital I/O

All boards have 40 lines of TTL level digital I/O. Eight of these lines (4 in and 4 out) are brought out via the main 50 pin connector, user accessible at the back of the PC. Two 40 pin headers on the 5800 Series (internal to the PC) provide access to an additional 16 digital inputs and 16 digital outputs. These digital I/O lines may be brought to the back of the computer with optional adapter connectors which are compatible with ADAC's line of isolated digital I/O panels.

1.3.5 ISA Interface

For maximum performance in a Windows environment, the 5800 boards feature a 1024 word FIFO and dual 16-bit DMA.

The 5800 Series also supports interrupt capability. Interrupts may be used to flag process completion, as well as, a full complement of error conditions.

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1.4 CE COMPLIANCE

The 5800 Series meets the essential health and safety requirements, is in conformity with the relevant EC Directives as listed using the relevant section of the following EC standards and other normative documents;

EN 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurement and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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2. GETTING STARTED

2.1 UNPACKING AND HANDLING

The 5800 is shipped in an anti-static conductive bag. Care must be taken to ensure the board does not come in contact with any static electrical charges. While unpacking the 5800 and any associated products, be certain that the board remains inside the anti-static bag.

***IMPORTANT**: The possibility of static discharge through the 5800 components must be avoided at all times. Touch the metal ground of your system before removing the 5800 from the anti-static bag, and always touch the bag before touching the board. Try to handle the board by the edges.*

2.2 HARDWARE INSTALLATION

The 5800 card may be installed in any one of the peripheral connectors on the backplane of the PC. While unpacking or installing the 5800, follow the installation steps carefully. The 5800 uses static sensitive devices and must be handled accordingly.

1) **TURN OFF ALL POWER TO THE SYSTEM**. Before removing the cover of the PC, make sure that the power is disconnected. Serious damage may result to the system if the power is not OFF before installing any cards.

2) **REMOVE THE COVER**. Remove the screws on the rear of the PC to remove the cover. For more detailed instructions refer to your computer "Installation and Setup" Manual.

3) **REMOVE SPARE SLOT COVER**. Remove the metal cover from the back of an empty slot in the PC. Make sure you save the screw for the next step.

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4) **INSTALLING THE 5800**. Pick up the 5800 and again touch the metal ground of the system before allowing the board to directly contact any conductive parts of the system. Next, insert the rear of the 5800 into the PC card guide and slide it down into the card edge connector. Make sure that the card is seated squarely, and screw down the rear connector bracket using the slot cover screw.

5) **REPLACE SYSTEM COVER**. Slide the cover back on the system replacing all of the screws. Reconnect power cord and any other peripherals that may have been disconnected. If any questions arise, refer to your computer manual.

6) **EXTERNAL CONNECTION**. Refer to Section 3.3 *EXTERNAL CONNECTIONS* for information on wiring to the optional screw termination panel. Attach G58 cable to the 50 pin connector of the 5800 which is projecting out the back of the computer.

***NOTE**: Computer power should always be turned OFF when attaching or removing the screw terminal panel or cable.*

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3. HARDWARE CONFIGURATION

3.1 CONFIGURING THE 5800 SERIES

The 5800 Series contains virtually no hardware jumpers; most board configuration elements are software selectable. The two exceptions are the board address switches, and the ADC input range selection jumpers.

3.1.1 Direct View

Each 5800 board is supplied with a free copy of DIRECT VIEW for Windows (DVW) board tutorial software. DVW is a unique package that guides the user through board installation, configuration, and field wiring connections. The fastest, and easiest way to configure the 5800 is with DVW. In addition, DVW contains a data acquisition section that confirms proper operation of the 5800 card in the host PC, as well as, this complete user manual as an interactive Help System.

We strongly recommend using DVW for configuring, installing, and connecting to your 5800 card.

3.2 BOARD SETTINGS

The following chart indicates the factory default settings of the 5800, including the power-up states of all the software controlled configuration items.

Should the user wish to change the base address, or disable the PC ISA interface, the Summary of Configuration Switches on the following pages list each switch with a short description of its function. The diagram in Figure 3.1 indicates location of these switches. Following the summary is a more detailed explanation of switch functions.

A list of adjustment potentiometers is also provided. Note that these potentiometers are set at the factory, and only should be altered if it becomes necessary to recalibrate the board.

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FACTORY DEFAULT/POWER-UP CONFIGURATION		
DESCRIPTION	**SETTING**	**SWITCHES**
PC INTERFACE		
ISA Control	ENABLED	SW8 CLOSED/ON
Base Address	120_H	SW1, SW3, SW4 OPEN/OFF SW2, SW5 CLOSED/ON
Bus Address Width	20_H	---
Interrupt Level	DISABLED	S/W Selectable (CONTROL2)
DMA Channel	DISABLED	S/W Selectable (CONTROL2)
ADC CONFIGURATION		
Input Multiplexer	8 Channels Differential	S/W Selectable (CONTROL3)
Data Coding	Two's Complement	S/W Selectable (CONTROL3)
Input Range	±10 V	JP1, JP2 in Bipolar Position
DAC CONFIGURATION		
Data Coding	Two's Complement	S/W Selectable (CONTROL6)
Output Range	±10 V	S/W Selectable (CONTROL6)
NOTE: Input range for 16-bit ADCs is fixed at ±10 V		

Fuse #	Power Line	Fuse Value
F2	±15 V to J8	Pico Fuse 125mA 125 V
F3	±15 V to J8	Pico Fuse 125mA 125 V
F4	+5 V to J8	Pico Fuse 3.0A 125 V
F1	+5 V to J1, J2	Pico Fuse 3.0A 125 V

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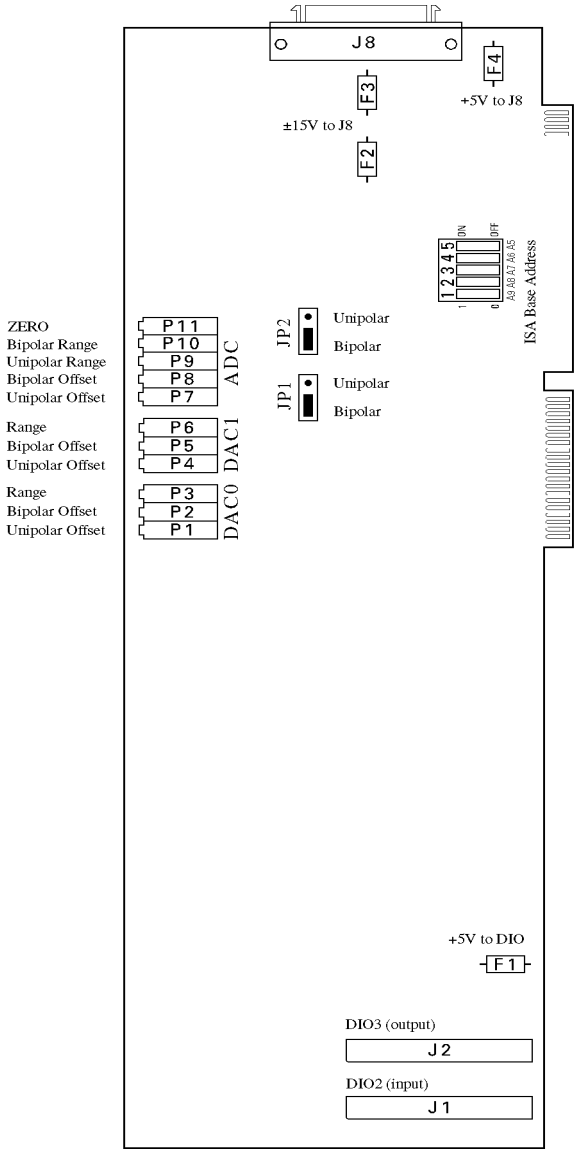


Figure 3.1 Component Placement 5801MF/5802MF
(Factory Default Configuration Shown)

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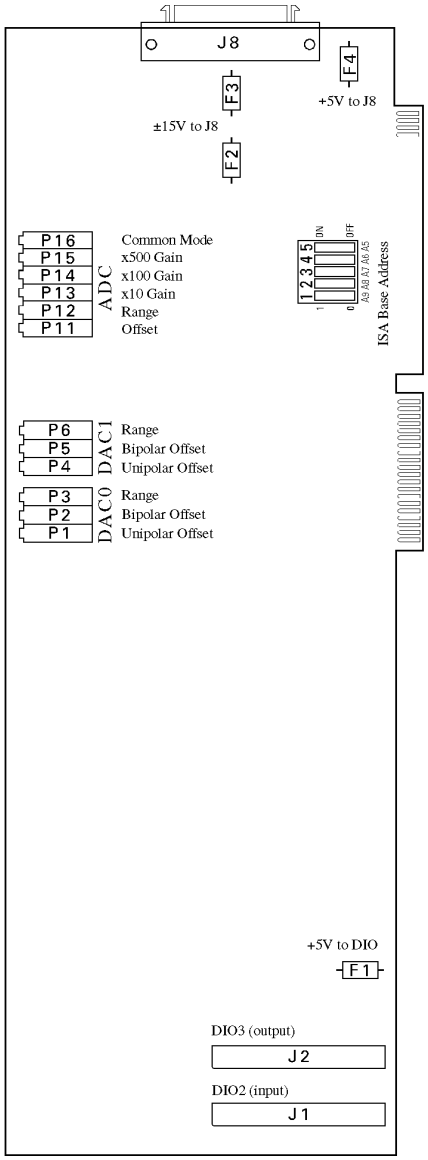


Figure 3.2 Component Placement 5803HR/5804HR

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3.2.1 Summary Of Configuration Switches

SWITCHES	DESCRIPTION	SETTING	COMMENT
SW1-SW5	Base Address	*SW1-0	Address Bit A9
	Selection	*SW2-1	Address Bit A8
		*SW3-0	Address Bit A7
		*SW4-0	Address Bit A6
	DEFAULT = 120_H	*SW5-1	Address Bit A5

*Indicates Factory Default Settings
0 = Open/Off 1 = Closed/On

Table 3.1 Configuration Switch Summary

Potentiometer	Description
DAC0	
P1	Unipolar Offset Adjust
P2	Bipolar Offset Adjust
P3	Range Adjust
DAC1	
P4	Unipolar Offset Adjust
P5	Bipolar Offset Adjust
P6	Range Adjust
12-bit ADC	
P7	Unipolar Offset Adjust
P8	Bipolar Offset Adjust
P9	Unipolar Range Adjust
P10	Bipolar Range Adjust
16-bit ADC	
P11	Offset Adjust
P12	Range Adjust
Programmable Gain	
P13	X2 / X10 Adjust
P14	X4 / X100 Adjust
P15	X8 / X500 Adjust

Table 3.2 Adjustment Potentiometers

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3.2.2 Base I/O Address

The 5800 Series board is factory configured for a Base Address of 120_H which will locate the on-board registers at addresses 120_H through $13F_H$. Unused register space is reserved for program compatibility with other boards. The 5800 occupies thirty-two consecutive address locations in the PC I/O Address Map. The address space used by this board must not be used by any other board in your system. If your board is not functioning, you may have another board in your system with the same address. Either remove that board, or change the base address the 5800 board. Note that if you wish to install more than one 5800 in your system, the base address of all the boards except one **MUST BE CHANGED** from the factory default.

3.2.2.1 Selecting A New Base Address

If you find it necessary to change the default base address of your 5800 Series board, you must first select a new address which is unused by any other board. The tables in Appendix C indicate which addresses are normally "occupied" in a standard PC ISA or compatible computer. Address ranges in **BOLD** text reflect potential "safe" addresses for "add-in" boards; shaded ranges are not recommended. If you have any additional "add-in" boards, check their manuals to determine what address space they occupy. Address 100_H through $1EF_H$ is normally only occupied by "add-in-boards". See Section 3.2.2.2 *Configuring A New Base Address* for additional information.

For easy reference indicate the new address you have chosen here:

5800 Series Board Base Address: _____

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3.2.2.2 Configuring A New Base Address

Use the following worksheet to determine the new jumper configuration.

Write in the 3 digit (HEX) address you wish to use in the spaces on line 1 (the chosen base address must be a multiple of 20_H.) Using the HEX to Binary conversion chart, fill in the binary equivalent in the boxes below each digit line 2). On line 3), write the word "ON" below each binary digit which is a "1". Line 3 indicates which of switches SW1 through SW6 must be ON.

Hex	Binary	Hex	Binary	Hex	Binary	Hex	Binary
0	0000	4	0100	8	1000	C	1100
1	0001	5	0101	9	1001	D	1101
2	0010	6	0110	A	1010	E	1110
3	0011	7	0111	B	1011	F	1111

Table 3.3 Hexadecimal to Binary Conversion

1) HEX ADDRESS
Default *1* *2* *0*

2) BINARY ADDR.
Default *0 0 0 1* *0 0 1 0* *0 0 0 0*

3) Switch Setting
Switch S1 S2 S3 S4 S5
Default *0 1* *0 0 1*

1 = ON or CLOSED
0 = OFF or OPEN

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3.2.3 Interrupt Level

The 5800 may be programmed to interrupt the HOST CPU at any one of six interrupt priority levels. Priority levels may not be shared.

3.2.3.1 Selecting An Interrupt Level

If you plan to use interrupts you must first select an interrupt level which is unused in your PC by any other board. Appendix C lists the standard interrupt levels used in a PC. Be sure to check your user manuals to be certain the interrupt level you select is not in use by any other "add-in" boards. The 5800 may be programmed to interrupt on any of the following interrupt levels:

IRQ3, IRQ5, IRQ7, IRQ10, IRQ11, IRQ15

3.2.4 DMA Channel

The 5800 may be pre programmed to automatically transfer data from the ADC to system memory using either single channel or dual channel DMA on any of three possible channels. DMA channels may not be shared.

3.2.4.1 Selecting A New DMA Channel

If you plan to use DMA you must first select a DMA channel(s) which is unused in your PC by any other board. Appendix C lists the standard DMA channels used in a PC. Be sure to check your user manuals to be certain the DMA channel you select is not in use by any other "add-in" boards. The 5800 may be programmed to run DMA transfers over any 1 or 2 of the following channels:

DMA5, DMA6, DMA7

3.2.5 Analog Input Configuration

The analog inputs are impedance buffered, and drive a unity gain differential amplifier that can be referenced in a number of ways allowing the following programmable input configurations: Single-Ended, Pseudo-Differential and Fully-Differential. For selecting the best configuration for your application see the section later in this chapter on "*Connecting User Wiring"*.

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The input configuration is programmed through register CONTROL3 (bits S/D and PDEN). See Section 4.4 *H/W REGISTERS* for specifics on programming each of these modes. Note that these modes also apply to expansion channels.

3.2.6 ADC Range

The input range of the ADC is selected via hardware jumpers. The 5801MF and the 5802MF may be configured for either ±10 V bipolar or 0-10 V unipolar operation. The 5803MF and the 5804MF are set at the factory to ±10 V bipolar range only. The following table illustrates which jumpers must be installed for each configuration.

5801MF and 5802MF Range Selection

JP1	JP2	ADC Input Range
BIP	BIP	±10 V Bipolar
UNI	UNI	0-10 V Unipolar

Note that you must also configure the input data coding by writing to CONTROL3 (bit U/B). See Section 4.4 *H/W REGISTERS* for specifics on programming each of these modes.

The ranges above are the limits at the A/D converter itself. The programmable gain circuitry must also be taken into account in defining the usable error free input range. The various 5800 Series boards provide a wide range of programmable ranges and resolutions.

The following tables indicate the maximum resolution under different conditions. Note that resolution is not accuracy. Resolution defines the minimum definable voltage increment. Absolute DC accuracy and relative accuracy define exactly how close the reading will be to the actual voltage input. Refer to Section 5 *SPECIFICATIONS* for accuracy specifications.

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Programmable Gain	Full Scale Range	Microvolt Resolution
x1	± 10.00 V	4.88 mV/bit
x2	± 5.00 V	2.44 mV/bit
x4	± 2.50 V	1.22 mV/bit
x8	± 1.25 V	0.61 mV/bit

Table 3.4 5801MF Bipolar Input Range/Resolution

Programmable Gain	Full Scale Range	Microvolt Resolution
x1	0 to 10.00 V	2.44 mV/bit
x2	0 to 5.00 V	1.22 mV/bit
x4	0 to 2.50 V	0.61 mV/bit
x8	0 to 1.25 V	0.31 mV/bit

Table 3.5 5801MF Unipolar Input Range/Resolution

Programmable Gain	Full Scale Range	Microvolt Resolution
x1	± 10.00 V	4.88 mV/bit
x10	± 1.00 V	488 µV/bit
x100	±100 mV	49 µV/bit
x500	± 20 mV	9.8 µV/bit

Table 3.6 5802MF Bipolar Input Range/Resolution

Programmable Gain	Full Scale Range	Microvolt Resolution
x1	0 to 10.00 V	2.44 mV/bit
x10	0 to 1.00 V	244 µV/bit
x100	0 to 100 mV	24 µV/bit
x500	0 to 20 mV	4.9 µV/bit

Table 3.7 5802MF Unipolar Input Range/Resolution

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Programmable Gain	Full Scale Range	Microvolt Resolution
x1	± 10.00 V	305 µV/bit
x2	± 5.00 V	152 µV/bit
x4	± 2.50 V	76 µV/bit
x8	± 1.25 V	38 µV/bit

Table 3.8 5803HR Bipolar Input Range/Resolution

Programmable Gain	Full Scale Range	Microvolt Resolution
x1	± 10.00 V	305 µV/bit
x10	± 1.00 V	31 µV/bit
x100	± 100 mV	3.1 µV/bit
x500	± 20 mV	0.6 µV/bit

Table 3.9 5804HR Bipolar Input Range/Resolution

3.2.7 DAC Range

The output range of the optional DACs is programmable to either ±10V or 0 to 10V. The range is programmed through register CONTROL6 (bit U/B). See Section 4.4 *H/W REGISTERS* for specifics on programming of this mode.

The following table indicates the maximum resolution for each available range. Note that resolution is not accuracy. Resolution defines the minimum definable voltage increment. Absolute DC accuracy and relative accuracy define exactly how close the actual voltage output will be to the expected output. Refer to Section 5 *SPECIFICATIONS* for accuracy specifications.

Range Configuration	Full Scale Range	Microvolt Resolution
BIPOLAR	± 10.00 V	305 µV/bit
UNIPOLAR	0 to 10.00 V	152 µV/bit

Table 3.10 5800 Series Output Range/Resolution

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3.3 EXTERNAL CONNECTIONS

WARNING! *Never connect or disconnect cables or screw terminal panels to the 5800 card while the host PC power is on. Always turn the PC's power OFF before attaching a cable or panel to the 5800.*

The 5800 card brings out ±15 V and +5 V to the main I/O connector J8, and +5V to the auxiliary digital I/O connectors J1 and J2. These power lines are individually fused to protect the 5800 card. Connecting or disconnecting cables or screw terminal panels (as well as any user connections to these power lines) may blow a fuse, or worse, cause damage the 5800 card. If you are getting incorrect data readings on your 5800 card, check all fuses to make sure they have not blown. Replacement fuses can be obtained from ADAC, or from most electronics stores (such as Radio Shack in the USA). Fuse values on the 5800 card are as follows:

Fuse #	Power Line	Fuse Value
F2	-15 V to J8	Pico Fuse 125mA 125 V
F3	+15 V to J8	Pico Fuse 125mA 125 V
F4	+5 V to J8	Pico Fuse 3.0A 125 V
F1	+5 V to J1, J2	Pico Fuse 3.0A 125 V

3.3.1 Connecting User Wiring

Incorrect connection of user wiring is one of the most common problems experienced by users of data acquisition boards. To ensure proper results, you must first determine what type of signal source you are measuring (Ground Referenced Source or Floating Source), and then choose the appropriate input configuration on your data acquisition card (Differential, Pseudo-Differential, or Single-Ended).

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3.3.1.1 Signal Types

Floating Sources

A Floating Source is a signal that has no connection to the building's power ground. Examples of Floating Sources are Thermocouples, batteries and battery powered devices, and signals from optically isolated devices. When connecting Floating Sources to a data acquisition card, the ground reference of the signal must be tied to the analog ground (AGND) in order to establish a common reference point.

Ground Referenced Sources

A Ground Referenced Source is one which is connected to the same common ground as the host PC, and therefore has the same ground as the data acquisition card. An example is equipment that plugs into the same building power source as the host PC.

***NOTE**: Due to differences in a building's power system, the Ground Referenced Source and the data acquisition board's ground may not be at the same voltage level. This difference is referred to as a Common Mode Voltage. Common Mode Voltage can be eliminated by using either Pseudo-Differential (PD) or Full-Differential (DI) input configurations on the data acquisition board.*

Signal Level

In addition to the grounding of source signals, the maximum voltage level of the signal should be taken into account when choosing the optimum input configuration on the data acquisition board. When working with signals with a maximum level below 1 V (Low Level), care must be taken to minimize possible affects caused by noise in the environment. The addition of noise will have less effect on signals in the 1-10 V range (High Level), and therefore High Level signals can use more types of input configurations.

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3.3.1.2 Choosing A/D Input Configuration

Once you have determined what type of input signal source you have, and the voltage level, you then need to select the proper/optimum input configuration on your data acquisition card:

Single-Ended

Applications with a Floating Source are typically wired to a data acquisition board configured for Single-Ended (SE) configuration. Since only one wire from each input signal is connected to a multiplexed input of the A/D, the Single-Ended configuration provides a larger number of inputs per board than Differential (see below) configuration. Grounded Signal Sources can be wired in Single-Ended configuration only when signal leads are less than 12 feet AND when all signals share a common ground (the signals must be local to one another).

With the Single-Ended configuration, the input signals are tied to the Channel Hi side of an analog input, and all signal low sides are tied to the SGND ground on the data acquisition card.

Single-Ended configuration should only be used when:

- There is no Common Mode Voltage
- Ground isolation is not required
- Signal leads are less than 12 feet.

Note that of all three possible input configurations, Single-Ended offers the least amount of noise rejection. Because of this, Low Level signals should only be wired in Single-Ended configuration when you are certain that their is little or no noise being introduced to the signal from the system, or the environment. We do not recommend using Single-Ended configuration with Low Level signals.

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Figure 3.3 shows proper wiring for Single-Ended configuration.

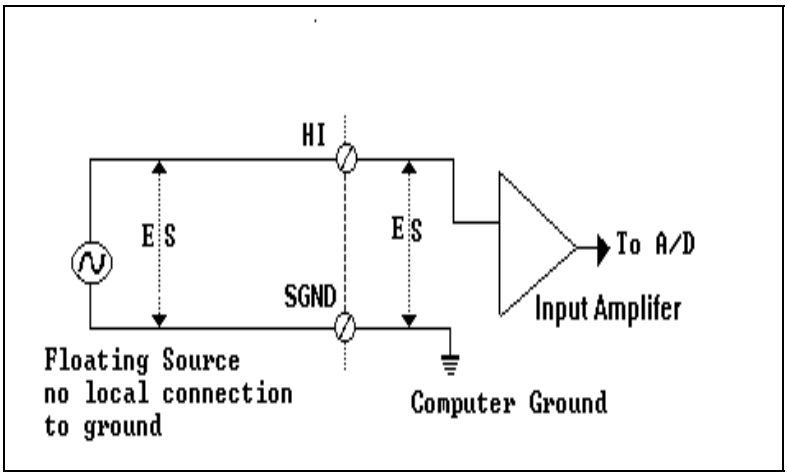


Figure 3.3 Single-Ended Configuration

Pseudo-Differential (PD)

For multiple signal sources that share a common ground (signals must be local to one another), the Pseudo-Differential mode may be the most desirable. The Pseudo-Differential configuration is similar to Single-Ended, but the analog low side of each signal is isolated from analog ground (AGND) by a 10 megohm resistor and a capacitor. All input returns are tied to together to PDIN. Pseudo-Differential configuration allows the system to reject any common-mode voltage difference that may exist.

Pseudo Differential configuration should be used when:

- Common Mode Voltage exists
- Common Mode Noise does not exist
- Each Source has a local ground
- Input signals are greater than 1 V (High Level)
- Signal leads are longer than 12 feet

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Figure 3.4 shows proper wiring for Pseudo-Differential configuration.

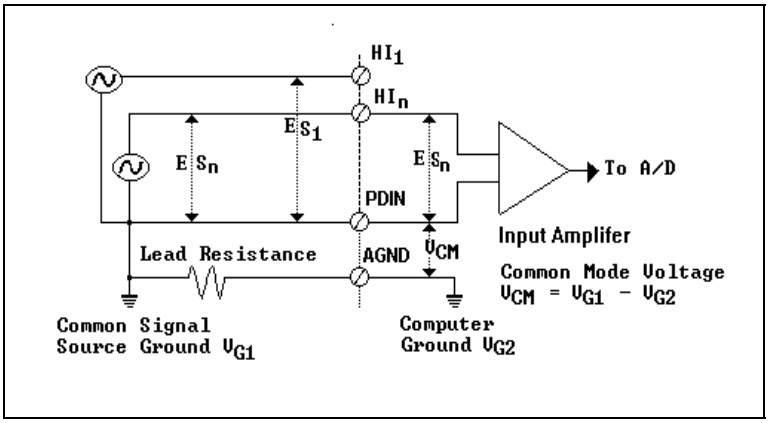


Figure 3.4 Pseudo-Differential Configuration

Fully-Differential (DIFF)

In installations where each Ground Referenced Source signal has a local ground (signal located remote from one another), the Fully-Differential configuration must be used. Since the Fully-Differential configuration only responds to the difference in a signal between its high and low voltages, any Common Mode Voltage will be canceled out. In addition, Fully-Differential configuration provides the best performance of the three configurations in an electrically noisy environment.

The Fully-Differential configuration should be used when any of the following exists:

- Each source has a local ground
- Signal sources are remote from one another
- Common Mode Voltage exists
- Common Mode Noise exists
- Signal sources are low-level (less than 1V)
- Signal source leads are longer that 12 feet

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Fully-Differential for Grounded Signal Sources

See Figure 3.5 for an example of connecting Grounded Signal Sources in Fully Differential configuration.

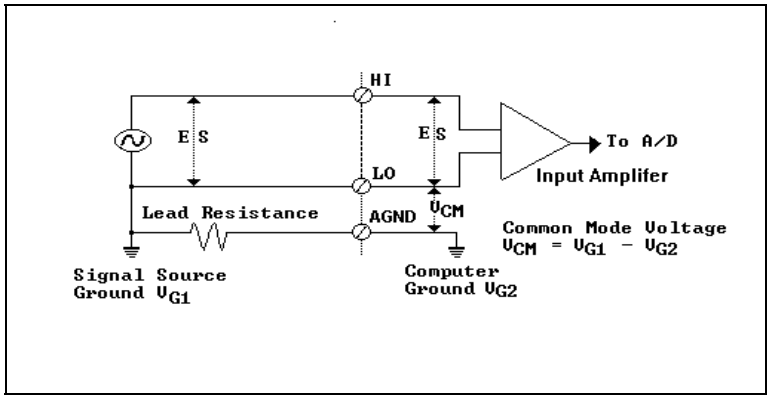


Figure 3.5 Fully-Differential Configuration for Grounded Sources

Fully-Differential for Floating Signal Sources

Floating Signal Sources are typically wired to a data acquisition board in Single-Ended configuration, however, when the Floating Source signal leads pass through an electrically noisy environment, Fully-Differential configuration will give the best performance. When wiring Floating Signal sources in Fully-Differential configuration, a resistor must be connected from the low side of the sources to analog ground (AGND). These resistors create a return path to AGND for the bias currents of the instrumentation amplifier. If a return path is not provided, the bias current will build up stray capacitance, resulting in drift and possible saturation of the amplifier.

If the input signal is DC coupled a 10K ohm to 100K ohm resistor must be connected from the input signal's return to the data acquisition board's AGND.

For AC coupled input signals a 10K ohm to 100K ohm resistor must be connected from both input signal high and input signal low to AGND.

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Figure 3.6 shows how to properly wire a Floating Source Signal in Fully-Differential configuration.

In the case where there is a combination of Ground Referenced Sources and Floating Sources, the Fully-Differential mode should be used.

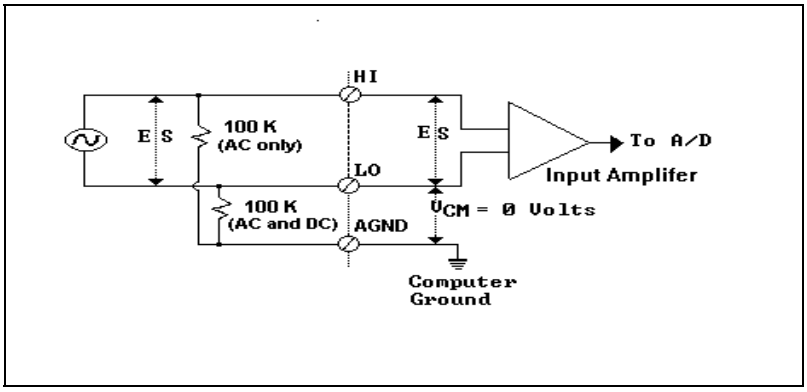


Figure 3.6 Fully Differential Configuration for Floating Sources

3.3.2 Main I/O Connector (J8)

The main board connector is a 50 pin SCSI-II type connector. This connector carries all the analog I/O connections as well as some digital I/O connections (4 in and 4 out).

The 5800 input channels may be connected directly to any High Level voltage source. If long leads are run from transducer to system, it is very important that the leads be shielded to protect against pickup of power frequency and other noise.

ADAC has available a line of screw terminal panels which can be used to ease field wiring to the 5800. Any of these panels may be connected to the 5800 with a standard SCSI-II cable (which can be ordered through us as a G58 cable). Our line of terminal panels includes:

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TB5800-16 - This panel provides access to the 16 analog channels, as well as the optional DACS, DIO ports 0 and 1, and various clocking and triggering signals.

TB5800-64 - This panel provides access to the same signals as the TB5800-16. In addition, a bank of input multiplexers expands the number of available analog input channels to 64.

TB5800-TC - This panel provides access to the same signals as the TB5800-16. In addition, the board includes circuitry which enables the user to directly connect up to 16 thermocouples to the panel. The panel amplifies the signals (×200) and provides cold junction compensation for any of a variety of thermocouple types. These 16 inputs are all multiplexed into analog input channel 0. Note that digital output bits 2 and 3 are not available on this panel as they are used to select the compensation rate.

3.3.2.1 Signal Definitions

The following is a description of each of the signals available at the 50-pin SCSI-II connector at the front edge of the board.

ANALOG INPUT CHANNELS

These channel signals are over-voltage protected to 20 V above or below the ±15 V power supply. The channel inputs can withstand input voltages of up to ±20 volts when the power to the system is off.

TB5800-16

CH0..CH7 - These signals can be the positive half of the associated differential input channel pair, or single-ended/pseudo-differential input channels 0 through 7.

CH8..CH15 - These signals can be the negative half of differential input channels 0 through 7, or single-ended/pseudo-differential input channels 8 through 15.

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TB5800-64

CH0..CH31 - These signals can be the positive half of the associated differential input channel pairs, or single-ended/psuedo-differential input channels 0 through 31.

CH32..CH63 - These signals can be the negative half of the differential input channels 0 through 31 or single-ended/pseudo-differential input channels 32 through 63.

TB5800-TC

CH1..CH7 - These signals can be the positive half of the associated differential input channel pairs, 16 through 22, or single-ended channels 16 through 22.

CH9..CH15 - These signals can be the negative half of the differential input channel pairs, 16 through 22 or single-ended channels 23 through 29.

TC0..TC15+ - These signals are the positive half of the associated thermocouple input channel pairs.

TC0..TC15- - These signals are the negative half of the thermocouple input channels TC0 through TC15.

NOTE - *Although the* ***TB5800-TC*** *channel numbers for the high level inputs are labeled CH1 through CH7 and CH9 through CH15 on the terminal board itself, the actual channel numbers selected when using software drivers written and controlled by ADAC are CH16 to CH29. See the above* ***TB5800-TC*** *signal descriptions for channel number association details.*

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ANALOG OUTPUTS

DAC1, DAC0 - These signals are the voltage output signals from the optional DACs. Since the DAC outputs are also fed back to an on-board multiplexer, the DACS can be used to drive the ADC for diagnostic purposes.

***NOTE**: If DACs are not installed, these signals are still connected to the internal ADC multiplexers. Care should be taken with these signals because they are NOT input protected like the Analog Input channels. Under no circumstances should these lines be connected to an active voltage source when the board is not powered.*

RTN1, RTN0 - These signals are the return lines for the voltage outputs. These inputs are essentially tied to AGND (Analog Ground) on the board.

DIGITAL I/O LINES

DI3..DI0 - These signals are the four TTL level digital input lines of DIO0. These lines are not clocked.

DO3..DO0 - These signals are the four TTL level digital output lines of DIO1. These lines are not clocked, however when this port is written to, the DOSTB line may be used to latch the data externally. Note that DO2 and DO3 are used to select the thermocouple compensation rate when the TB5800-TC is used.

DOSTB - This signal generates an active high TTL level pulse when the DO lines are updated. The DO lines are updated as this signal goes high and can be considered valid at the trailing (falling) edge.

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TERMINAL PANEL CONTROL

These signals are used to control the various optional terminal panels. The function of some signals may vary slightly depending on the panel used.

MUX7..MUX3 - These signals are used to control the external multiplexers on active panels. These lines directly reflect the current state of the Channel RAM bits of the same name.

CJEN - This signal reflects the CJEN bit in the G/C RAM. This signal is used by the TB5800-TC terminal panel to enable and disable cold junction compensation. Note that DO2 and DO3 are used to select the thermocouple compensation rate when this panel is used

RSVD - This signal is reserved for use with future terminal panels. This signal is a TTL level output future use.

CLOCK AND TRIGGERS

XPCLK - This is the External Pacer clock input. This input recognizes TTL level signals and is edge sensitive. The active edge is programmable via CONTROL3.

TGIN - This is the External Trigger/Gate input. This input recognizes TTL level signals and is used to start or stop the ADC acquisition process. This input may be programmed for rising or falling edge or level sensitivity via CONTROL1.

TGOUT - This TTL level output reflects the activity on the TGIN signal after it has been conditioned. This signal may be used to carry the gate function to other boards. This signal is always active high.

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GROUND LINES

SGND - This signal is the reference ground used for A/D conversions. If you are measuring from a fully floating source in differential mode, it would be beneficial to tie one of the channel inputs to this point. This signal should not be used for sinking large amounts of current. This signal also acts as the common reference line when the board is configured for single-ended inputs.

PDIN - This signal is the common return line used when the board is configured for pseudo differential input mode.

AGND - This signal is the power return for the ±15 V power supply lines. It is distinguished from the DGND line because it generally helps separate the potentially high frequency digital ground noise from the analog circuits which are powered by ±15 V.

DGND - This signal is the +5 V power return line. It is generally more noisy than AGND and is a good logic low reference point.

POWER LINES

+15V, -15V - This power is only intended to power the optional terminal panels with active circuitry on them. These voltages are supplied by one of the on-board DC/DC converters. Approximately ±30mA is available on these lines. Both lines are fused @ 125mA.

+5V - This signal is sourced directly from the PC Bus. Take great care when using this power. These lines are fused @ 3 Amps.

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3.3.2.2 J8 Pin Assignments

SIGNAL NAME	J8 PIN	SIGNAL NAME	J8 PIN
PDIN	1	CH0	26
CH8	2	CH1	27
CH9	3	CH2	28
CH10	4	CH3	29
CH11	5	CH4	30
CH12	6	CH5	31
CH13	7	CH6	32
CH14	8	CH7	33
CH 15	9	SGND	34
RTN0	10	DAC0	35
RTN1	11	DAC1	36
+15V (fused)	12	-15V (fused)	37
AGND	13	AGND	38
DGND	14	CJEN	39
DI1	15	DI0	40
DI3	16	DI2	41
DO1	17	DO0	42
DO3	18	DO2	43
DOSTB	19	XPCLK	44
TGOUT	20	RSVD	45
MUX3	21	TGIN	46
MUX5	22	MUX4	47
MUX7	23	MUX6	48
+5V (fused)	24	+5V (fused)	49
DGND	25	DGND	50
n/c = no connection			

Table 3.11 J8 Pin Assignments

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3.3.2.3 TB5800-16 Connections

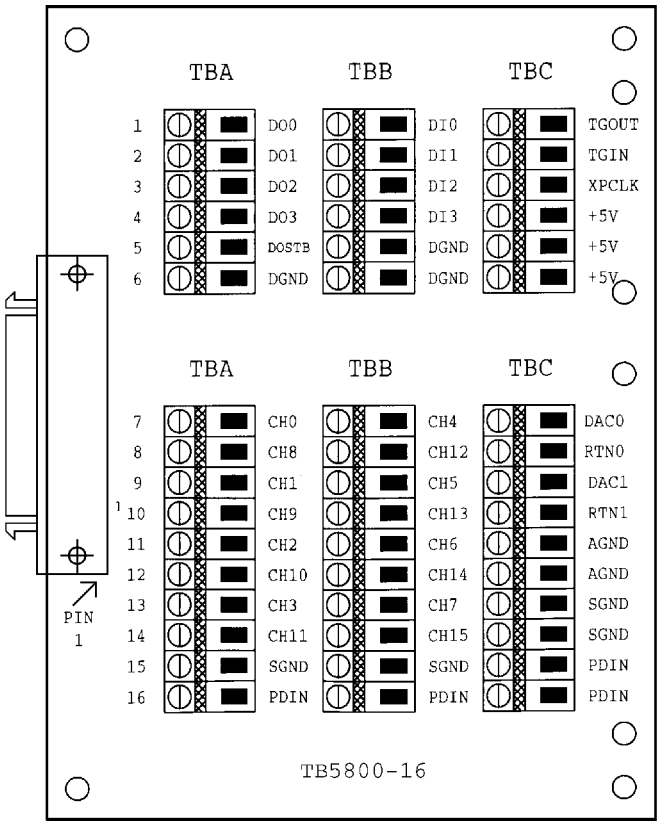


Figure 3.7 TB5800-16 CONNECTIONS FOR 5800

See the DIRECT VIEW for WINDOWS software for examples of proper connection of user wiring.

NOTE: Always turn computer power OFF before connecting or disconnecting a screw terminal panel or cable to the 5800 card.

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3.3.2.4 TB5800-64 Connections

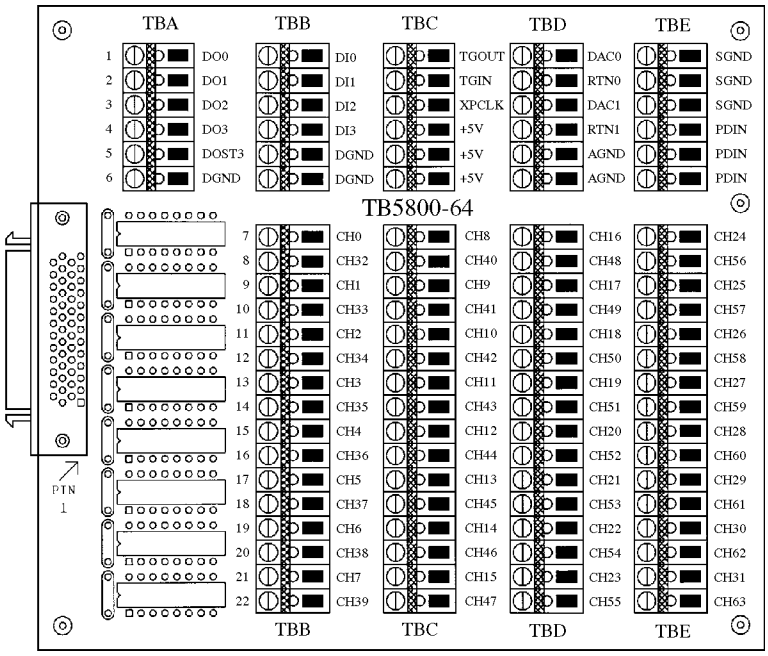


Figure 3.8 TB5800-64 CONNECTIONS FOR 5800

See the DIRECT VIEW for WINDOWS software for examples of proper connection of user wiring.

NOTE: Always turn computer power OFF before connecting or disconnecting a screw terminal panel or cable to the 5800 card.

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3.3.2.5 TB5800-TC Connections

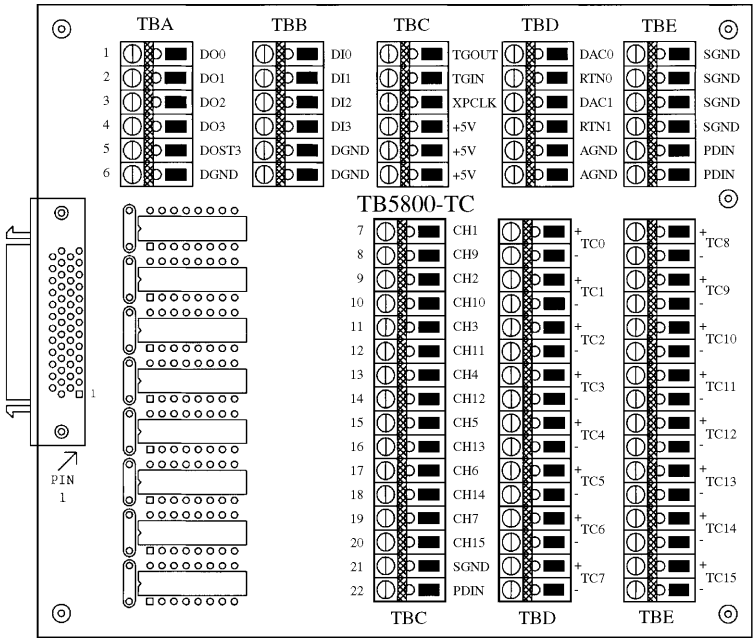


Figure 3.9 TB5800-TC CONNECTIONS FOR 5800

See the DIRECT VIEW for WINDOWS software for examples of proper connection of user wiring.

NOTE: Always turn computer power OFF before connecting or disconnecting a screw terminal panel or cable to the 5800 card.

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3.3.3 Auxiliary Digital I/O Connectors (J1, J2)

The 5400 also provides two auxiliary 40 pin headers on the back of the board. These provide access to the two 16-bit DIO ports (DIO2 and DIO3). A special cable assembly (G16) is available to bring each of these headers to a 37-pin D-type connector mounted at the back of the PC.

Two G16 cables are required to bring all the DIO signals to the back of the PC. Each G16 cable requires an empty slot in the back or your PC to install.

ADAC has available a line of screw terminal panels which can be used to ease field wiring to the 5400. Any of these panels may be connected directly to the 37-pin D-type connector (G16 Cable), or a G37 cable may be used to connect from the back of the PC to a remotely mounted panel. Our line of terminal panels includes:

Standard Panels -

DC-37 - This panel provides access to the 16 DIO lines associated with DIO2 or DIO3 as well as the associated STROBE signal.

4000VRMS Isolated Panels

ACI-EX - This panel allows the user to detect up to 8 separate A/C voltage lines.

ACO-EX - This panel provides 8 high voltage relays which are controlled by the digital output port.

DCI-EX - This panel may be used to detect high level DC voltages on up to 16 points.

DCO-EX - This panel may be used to switch up to 16 level DC voltages.

Each of these panels is described in detail in Appendix A of this manual.

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3.3.3.1 Signal Definitions

The following is a description of each of the signals available at the 40-pin DIO headers.

DI0..DI15 - These signals are the 16 TTL level digital input lines of DIO2. These lines can be strobed in (STBIN2) depending on how the board is programmed.

DO0..DO15 - These signals are the 16 TTL level digital output lines of DIO3. These lines may be clocked. When these lines are updated, a strobe pulse (STBOUT3) is generated (polarity programmable) which can be used to latch data into another device.

STBIN2 - This TTL level input signal may be used to strobe data into DIO2. The active edge of this signal is programmable.

STBOUT3 - This TTL level output signal will generate a pulse whenever the DO0..DO15 are updated. The polarity of this pulse is programmable.

DGND - This signal is the +5 V power return line. It may also be used as a reverence ground for TTL signals.

+5V - This signal is sourced directly from the PC Bus. Take great care when using this power. These lines are fused @ 3 Amps.

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3.3.3.2 J1 and J2 Pin Assignments

SIGNAL NAME J1/J2	J1/J2 PIN	G16 PIN (37-pin D)
DGND	1	1
+5V (fused)	2	20
DGND	3	2
D0	4	21
DGND	5	3
D1	6	22
DGND	7	4
D2	8	23
DGND	9	5
D3	10	24
DGND	11	6
D4	12	25
DGND	13	7
D5	14	26
DGND	15	8
D6	16	27
DGND	17	9
D7	18	28
DGND	19	10
D8	20	29
DGND	21	11
D9	22	30
DGND	23	12
D10	24	31
DGND	25	13
D11	26	32
DGND	27	14
D12	28	33
DGND	29	15
D13	30	34
DGND	31	16
D14	32	35
DGND	33	17
D15	34	36
DGND	35	18
STBIN2 / STBOUT3	36	37
DGND	37	19
n/c	38	n/c
n/c	39	n/c
n/c	40	n/c
n/c = no connection		

Table 3.12 J1 and J2 Pin Assignments

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3.3.3.3 Installing a G16 Cable

The following figure illustrates how a G16 cable is installed.

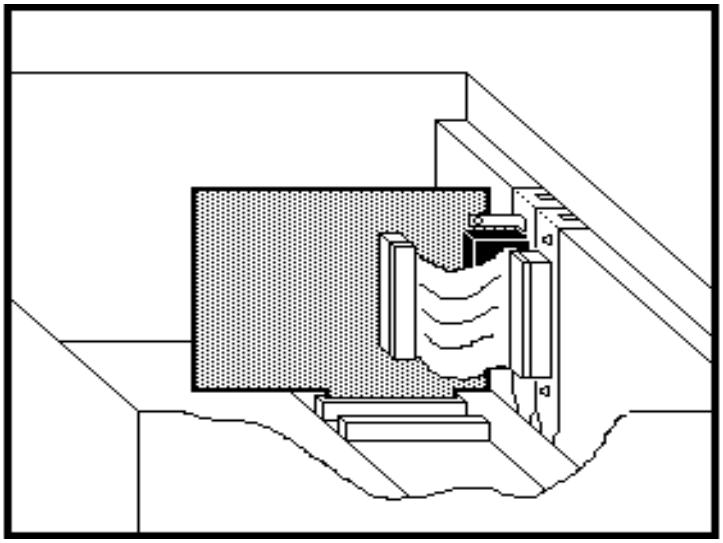


Figure 3.10 G16 Cable Installation

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3.3.3.4 DC-37 Connections

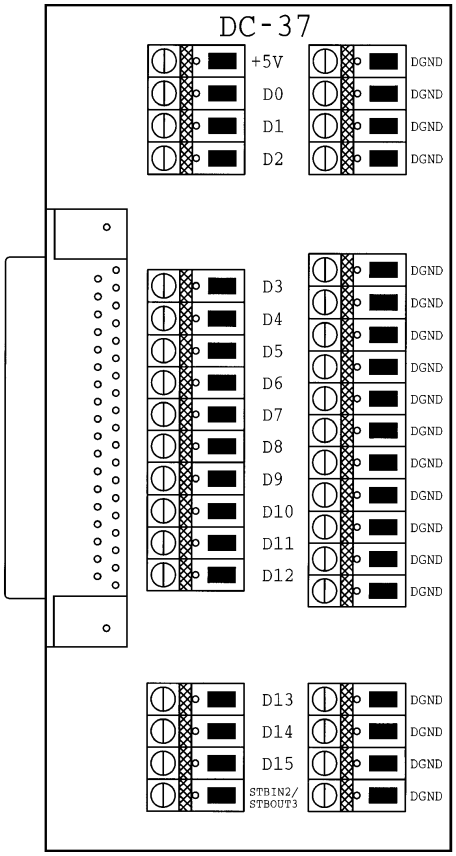


Figure 3.11 DC-37 CONNECTIONS FOR 5800

***NOTE**: Always turn computer power OFF before connecting or disconnecting a screw terminal panel or cable to the 5800 card.*

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4. OPERATING THE 5800

4.1 5800 DEVICE DRIVERS

The simplest method of operating the 5800 is by using a program package such as TestPoint or LabVIEW. These packages can be incorporated to do a wide range of display, data logging and control functions. For those who prefer to write their own programs, the 5800 may be purchased with ADLIB Series of driver packages. These packages provide easy to use software calls to perform most available board functions

4.1.1 LabVIEW

The 5800 is fully supported by the ADAC-LVi data acquisition VIs for LabVIEW. Please refer to the ADAC-LVi manual for details on using ADAC cards with LabVIEW. Note that the ADAC-LVi data acquisition VIs and the user manual can be downloaded from ADAC's web site at www.adac.com.

4.1.2 TestPoint

When using the 5800 with TestPoint, refer to the ADAC driver manual for information specific to the 5800. The driver manual exists as a Help system, and is shipped with the TestPoint software.

After the initial installation of the TestPoint software, click on the Help question mark labeled "ADAC" in the TestPoint program group. Information on operating the 5800, as well as other ADAC plug-in boards, is detailed in this Help system.

4.1.3 Windows Drivers

ADLIB Drivers provide the custom programmer with high level, callable subroutine libraries that access to all of the I/O functions on data acquisition boards.

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Windows 3.1, Windows 98/95 and Windows NT

ADLIB WIN is set of sophisticated, high level, dynamically linked library (DLL) data acquisition subroutines for programmers involved in the developing of process and/or data acquisition applications. ADLIB WIN is both a Microsoft C interface library (C, Visual C++) and a Visual Basic interface library for Windows 3.1, Windows 98/95 and Windows NT. The functions supplied with ADLIB WIN provide an easy to use interface to the line of PC data acquisition products, shielding the programmer from the complexity of low level DAQ board programming and complicated DMA and interrupt handling mechanisms of the PC and the Windows environment. ADLIB WIN supports DMA, Interrupt and Software Polled data transfer methods for acquiring data. ADLIB WIN has full support for analog high level (10 V) and analog low level (mV) inputs. Routines for thermocouple inputs are included.

4.2 THEORY OF OPERATION

4.2.1 Process Definitions

In order to best understand how to operate the various board functions, it is important to first understand the language which will be used to describe the process. The following is a list of pertinent terms and their definitions as this document will be using them.

ADC

Analog to Digital Converter. This is the circuitry which samples the voltage present at one of the inputs and translates that reading to a number which is representative of that voltage. The number supplied by the ADC is referred to as the ADC DATA or RAW DATA and its units are bits or binary digits.

DAC

Digital to Analog Converter. This is the circuitry which translates a binary data word to a specific voltage level. The optional DACs on the 5800 Series boards are specified for DC accuracy and not well suited to waveform generation. The DACs on these boards cannot be clocked, the outputs are updated as soon as they receive new data.

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Channel

Analog Input. This term is used to refer to any of the 64 addressable connections to the ADC. 16 available (or with the optional TB5800-64 multiplexer panel, 64 available) multiplexed connections to the ADC. The 5800 Series has 16 channels. By using a TB5800-64 multiplexer panel the maximum number of channels may be increased to 64.

ADC Data- also Raw Data

This is essentially the unscaled number returned by the ADC. For a 12 bit converter this number will be either in the range of - 2048..+2047 for two's complement data coding (which is standard for bipolar inputs) or in the range of 0..+4095 for straight binary data coding (which is standard for unipolar inputs.). This number is typically multiplied by some scale factor to convert the number to more useful engineering units. For example: 10V input uses a scale factor of .004883V/bit. An ADC reading of 1024 when multiplied by .004883 V results in 5.000 V.

A/D Conversion

This is the process of sampling a single input or transducer's voltage and generating a representative data value

Acquisition

This term is used to refer to a series of A/D conversions. This series may consist of sampling a single channel several times or sampling several channels sequentially one or more times. An acquisition has a clearly defined Starting point and Ending point. Thus an acquisition may be STARTED and STOPPED.

ADC Clock

This is the signal or impetus which initiates an A/D conversion. To CLOCK the ADC is to start an A/D conversion. The term clock is used for this process because typically a clock signal consists of a series of pulses which are periodic or evenly timed. If A/D conversions are evenly spaced it is then possible to digitally reconstruct the input waveform without distorting its component frequencies.

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PACER Clock

This is a timed periodic signal which may either directly clock the ADC or initiate a burst of conversions. Thus the PACER clock can be the ADC clock source, but not exclusively.

BURST Clock

This is also a timed periodic signal which may be used to directly clock the ADC. When the Burst clock is used, this signal defines the time between individual conversions. This signal is not, however, continuous. It lasts for a predefined number of pulses and then stops. The duration of this signal is called the burst clock; the period of individual pulses is the burst rate. Bursts are initiated by the pacer clock.

ADC Trigger

This is the signal or impetus which initiates or terminates an Acquisition. Essentially the Trigger Starts or Stops the PACER Clock.

G/C RAM

This is the term used for the on-board channel/gain lookup table. The length of this table can be anywhere from 1 element to 256 elements. When an ACQUISITION is in process, the board will sequentially go through this list to determine the channel and gain setting for the next conversion. Thus channels may be sampled in any order and at any gain. Note, however, that for maximum performance, it is recommended that channels with like gains should be grouped together in the sample sequence.

Polled -

This is an acquisition mode in which all aspects of the data collection is handled directly. Specifically, once an A/D conversion is initiated, the software must POLL the status register testing for a DATA available flag to set. The data is then read from the board. This mode requires the most software overhead, although on a fast machine, this mode also provides the highest speed potential.

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Interrupt -

This is an Acquisition Mode best suited to slower acquisition rates. The board may be programmed to interrupt the CPU when a condition occurs (for example new data is available). This allows the software to perform some other task between conversions, rather than wait exclusively for the next piece of data. The CPU is relatively slow to respond to interrupts, however, so the merits must be balanced against the disadvantages when using this mode.

DMA

This is the most self-sufficient of the Acquisition Modes available over the host bus. DMA is short for Direct Memory Access. In this mode, data from each conversion is automatically transferred directly from the board to some prespecified block of system memory. Essentially, DMA allows the acquisition process to run in the background with almost no software overhead at all.

FIFO

Short for First In First Out, a FIFO is a standard feature on the 5800. A FIFO is a specialized form of memory where essentially the data from each conversion is stored in a memory queue. Data is then read from the queue in the same order it was stored. This allows multiple conversions to be performed before the data is moved off board. This is particularly useful in maximizing speed potential of data transfer when operating under Windows.

4.2.2 Analog Input Channel Selection

A 4-bit code in G/C RAM Register controls the on-board multiplexers which select one of 16 single ended input channels, or 1 of 8 differential inputs channels. These bits provide access to the Channel/Gain RAM. Writing a 0000_H to the G/C RAM register will select input Channel 0. Writing a 0001_H to this register will select input Channel 1 and so on.

When using an active multiplexer terminal panel (such as a TB5800-64 or TB5800-TC). Channel selection is a little more complex. The 4 lowest bits of the G/C RAM select 1 of 16 (or 1 of 8) channel groups. One or more of these channels is connected to an additional multiplexer. The external multiplexers are controlled by the next 4 bits of the G/C RAM. The TB5800-TC has a 16 input multiplexer

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connected to channel 0. The TB5800-64 has eight 1 of 8 multiplexers connected to channels 0 through 3 and channels 8 through 11.

For example, the fourth TC channel would be addressed at 0030_H. Channel group 0, mux input 3 (of 0..15). The second channel (of 0..7) of the fourth group (of 0..15) on the -64 panel would be addressed at 0013_H.

4.2.3 Programmable Gain Selection

A 2-bit code in G/C RAM Register controls the on-board gain circuitry which allows the selection of 1 of 4 possible gains. The gain is set at the same time as the channel. Available gains are x1,x2,x4,x8 or x1,x10,x100,x500 depending on model.

4.2.4 G/C RAM Control

The G/C RAM is a list of Gain and Channel selection combinations which acts like a circular buffer of 1 to 256 elements. When A/D conversions are initiated, this list determines which channel will be sampled next. The G/C RAM is controlled by two registers. These are the G/C RAM register and the SADDR register.

The RAM address pointer is decremented by 1 through the RAM after each conversion until it points to address 0. The next conversion will then reset the RAM address pointer to the starting address stored in the SADDR register. Reading the G/C RAM register returns the contents of the RAM element currently being pointed to (the channel and gain combination currently selected for the next conversion. Writing to the G/C RAM register will update the currently selected RAM element and decrement the RAM address pointer.

To set up a Gain/Channel List, write the number of elements (minus 1) to the SADDR register. Then write each list element to the G/C RAM register. After the last element is written, the G/C RAM address pointer will again be pointing to the first element. The List is ready for conversions.

To configure the G/C RAM for a single channel. Write 00_H to the SADDR register, and treat the G/C RAM register as a simple R/W register. Each time the G/C RAM is updated, an on-board timing circuit measures out the minimum time for settling to the new Channel/Gain setting. This settling time can be monitored by polling the READY flag

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of the STATUS2 register. If a conversion is initiated before this flag clears, an error flag will set.

NOTE: *It is strongly recommended that you do not try to update the G/C RAM while conversions are in process (enabled) since the RAM address pointer will be changing at the start of each conversion asynchronous to program accesses to this register.*

4.2.5 Cold Junction Compensation Selection

This only applies to the TB5800-TC analog input panel which allows direct connection to up to 16 thermocouple devices. One aspect of this panel is to introduce an offset voltage to compensate for the thermocouple junction formed when the thermocouple wire is connected to the tin plated copper screw terminals. The compensation circuit takes panel temperature and thermocouple type into account. Hence it is necessary to "inform" the panel which type of thermocouple is being used.

The panel uses DIO1 bits 2 and 3 to select the compensation rate. The CJEN bit of the G/CRAM Register to enable and disable the compensation circuitry. The result is as follows. Only one thermocouple type may be selected at a time, but compensation may be enabled or disabled on a per channel basis through the G/CRAM.

Compensation rates are programmable for the following types of thermocouples:

Thermocouple	Compensation Rate
Type J	51.7 µV/°C
Type K or Type T	40.6 µV/°C
Type E	60.9 µV/°C
Type R or Type S	6.0 µV/°C
Type B or Millivolt Input	0.0 µV/°C

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4.2.6 Clocking The ADC

The source of the ADC clock may be any of the following:

1) Software command
2) Counter/Timer A2
3) External event (XPCLK)
4) Burst Clock

Once an ADC clock is received, the Analog input is immediately sampled. Converted data will become available within 10 microseconds of the clock (max) (3 microseconds for 12-bit boards). Any attempt to clock the ADC while an A/D conversion is currently running will result in a Clock Error. This condition is indicated by the CERR flag of STATUS 2. The following are a number of possible clocking schemes.

At a minimum, to perform analog acquisitions, conversions must be enabled (CVEN = 1, STATUS1), the FIFO must be enabled (FFEN = 1, CONTROL1).

4.2.6.1 Software Generated Single Clock

A single A/D conversion may be initiated by writing to the ACQDATA register while the convert command is selected (SELECT = 00_H). The 5800 will sample the voltage present on the channel selected by G/C RAM. Always wait for the READY flag (STATUS2) to clear before issuing a CONVERT command.

4.2.6.2 Counter/Timer Clocking

A series of A/D conversions may be controlled by on-board combination of Timer A1 and Timer A2. These timers may be programmed to generate a periodic clock rate as high as 333 kHz or as slow as 4 samples per hour. Timer A1 is clocked by a MHz signal and Timer A2 is clocked by Timer A1.

Once the clock rate is programmed, Timer A2 must be selected as the clock source by writing 001 to bits S2,S1,S0 in CONTROL3. Refer to Section 4.2.7 Starting (Triggering) An Acquisition for information on triggering (starting) a clocked acquisition.

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4.2.6.3 External Event Clocking

Conversions may also be caused by an external event. XPCLK is an edge sensitive TTL input which can be programmed to cause conversions. Writing 010 to bits S2,S1,S0 in CONTROL3 will enable a rising edge at XPCLK to generate conversions. Writing 011 these bits will enable a falling edge at XPCLK to generate conversions.

4.2.6.4 Burst Clocking

This mode uses the Burst clock to initiate conversions. The burst rate is defined by programming the BRATE register. The duration of the burst is defined by writing to the BLENGTH register. If burst mode is enabled by setting the BMDE bit (CONTROL3), each burst will be started by any of the three previously mentioned clock sources (see Sections 4.2.6.1 *Software Generated Single Clock*, 4.2.6.2 *Counter/Timer Clocking* and 4.2.6.3 *External Event Clocking*). Simply program the board as if to use one of the above clock sources, and in addition, set the BMDE bit.

4.2.6.5 Maximum Clock Rate

The maximum rate which the ADC should be clocked and retain optimal accuracy will vary depending on several factors. These include ADC resolution (12 or 16 bits), gain setting, and sampling mode.

The first limiting factor is the ADC chip itself. Boards with 12 bit ADC chips (5801MF and 5802MF) are capable of performing analog to digital conversions at up to 333 kilo-samples per second. Models with 16 bit ADC chips (5803HR and 5804HR) will sample at rates up to 100 kilo-samples per second. These limits may not be exceeded. If the sample clock is run faster, some of the clock pulses will be ignored by the circuitry, and the clock error flag (CERR) in STATUS2 will set.

The second factor involves the front end circuitry. The bandwidth of the front end will vary depending on the gain setting (and the required resolution). The bandwidth will limit the maximum signal frequency the board can pass. Essentially, when sampling a single channel repeatedly, the ADC may be operated up to its maximum speed, but the front end will filter out any frequency components of the input signal which exceed the bandwidth of the system.

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When changing channels, even if the input signal is static, the front end is required to respond to a changing input each time the channel is changed. The net effect is that the maximum sampling speed of the ADC is limited to the bandwidth of the front end when changing channels.

Each time a conversion is initiated, the ADC goes into hold mode and the front end begins to settle on the next channel. At this point a timer is started. The duration of the timer is determined by the gain setting. If a new conversion is begun before the timer completes its cycle, the CERR flag will set indicating the front end has not settled sufficiently and the accuracy of the data may be compromised. The timer cannot, however, determine whether the channel has actually changed or not. For example, if the front end bandwidth is 33 kHz but only a single channel is sampled at 100 kHz, the CERR flag will set even though the data is accurate.

The following table indicates the bandwidth and sampling rates for each of the models and gains, and at what sample rate the error flag will set. Use this table as a guide in determining sampling rates and correct error flag interpretation.

Product	Gain	Front End Bandwidth (minimum)	Max Sample Rate *	Error Flag sets if rate above
5801MF	×1,×2,×4,×8	166 kHz	333 kHz	333 kHz
5802MF	×1,×10	166 kHz	333 kHz	333 kHz
	×100,×500	16 kHz	33 kHz	33 kHz
5803HR	×1,×2	50 kHz	100 kHz	100 kHz
	×4,×8	25 kHz	50 kHz	50 kHz
5804HR	×1	50 kHz	100 kHz	100 kHz
	×10	25 kHz	50 kHz	100 kHz
	×100	5 kHz	10 kHz	1 kHz
	×500	500 Hz	1 kHz	1 kHz
5801MF + TB5800-TC High Level Inputs	×1,×2,×4,×8	166 kHz	333 kHz	333 kHz
5801MF + TB5800-TC TC Inputs	×1,×2,×4,×8	5 kHz	10 kHz	333 kHz

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** **NOTE**: Max Sample Rate applies only if input channel is changing. For single channel acquisition, max sample rate = the max rate of the ADC itself (100kHz or 333kHz)*

4.2.7 Starting (Triggering) An Acquisition

There are several methods which can be used to initiate an acquisition. All of these are achieved by triggering or gating the ADC clocks mentioned previously in Section 4.2.6 *Clocking The ADC*. Note that a trigger is an edge active event and gate is a level controlled enable.

1) Software gate
2) External gate (TGIN)
3) External Trigger (TGIN)

4.2.7.1 Software Gate

To start the ADC clock with software, select CGEN control (CGSL = 0, CONTROL1). This will allow CGEN (also in CONTROL1) to be used to enable and disable Timer A1 and Timer A2. Configured this way, CGEN drives the gate inputs of Timer A1 and Timer A2 directly. CGEN may not be used to enable the external clock input (XPCLK). This allows Timer A1 and Timer A2 to be used for other purposes if an external ADC clock is selected.

Use CVEN (STATUS1) to gate external clocks.

CGEN has no effect on the slave expansion clock input.

4.2.7.2 External Gate

An ADC clock may be "switched On" (and Off) with the external trig/gat input (TGIN). Set CGSL = 1 to select the external control, set TGSL = 1 to select level sensitive control, and use TGPL to select active high or active low control. (All bits are in CONTROL1). If the on-board timers drive the ADC, the external gate input drives the GATE input of the timers after being polarity conditioned. The ADC clock will be enabled as long as the gate input is in the active state.

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4.2.7.3 External Trigger

The external gate/trig input (TGIN) may also be configured as an edge sensitive enable for the ADC clock. Set CGSL = 1 to select the external control, set TGSL = 0 to select edge sensitive control, and use TGPL to select rising or falling edge control. (All bits are in CONTROL1). External triggers are ignored until the ADC is enabled (CVEN = 1, STATUS1). Once the ADC is enabled, the next active edge signal on TGIN will enable the ADC Clock source. To disable the clock, refer to Section 4.2.8 *Stopping An Acquisition (CLOCK).*

***NOTE**: The TRIG flag (STATUS2) will set when a valid trigger is received. This flag must be cleared by writing a 0. Once a valid trigger has been received, triggers must be re-armed before a new trigger can be received. To reset the trigger circuitry, simply disable conversions (CVEN = 0, STATUS1).*

4.2.8 Stopping An Acquisition (CLOCK)

The current acquisition will halt under several circumstances. The most basic method is to simply disable the ADC by setting CVEN = 0. This will effectively shut off the ADC and re-prime the trigger inputs.

1) Software gate
2) External gate (TGIN)
3) External Trigger (TGIN)
4) FIFO Overflow

4.2.8.1 Software Gate

To stop the ADC clock when operating in software gated mode, simply set CGEN = 0 (CONTROL1). Refer to *Section 4.2.7.1 Software Gate* for additional information on this mode.

4.2.8.2 External Gate

An ADC clock may also be "switched off" with the external trig/gat input (TGIN). Refer to *Section 4.2.7.2 External Gate* for additional information about this mode.

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4.2.8.3 External Trigger

The external gate/trig input (TGIN) may also be used to stop an acquisition. In this mode, referred to as about trigger mode, the ADC is disabled after a certain number of conversions are performed following a trigger. How many conversions may be any number from 2 to 65,000. The conversions are counted by Timer A0. Timer A0 is loaded with a number (n). Once triggered, timer A0 will decrement after each conversion. When the timer counts to 0 (n + 1 conversions), the CVEN flag (conversion enable) is automatically cleared. If the timer is loaded with a value of 1, the ADC will be stopped after two valid clocks (writing a value of 0 is not allowed).

To configure the board for about trigger mode, set ATEN = 1, and TGSL = 0 (CONTROL1), and set the trigger polarity (TGPL, CONTROL1). CGSL, the local/external trigger select is ignored (trigger source is always external in about trigger mode).

If TGEN = 0, conversions are enabled as soon as the ADC is enabled (CVEN = 1, STATUS1). The next valid trigger will enable Timer A0 to count conversions.

If TGEN = 1, conversions will begin after the next valid trigger. Timer A0 will be enabled to count conversions after the second valid trigger is received.

4.2.8.4 FIFO Overflow

The 5800 Series boards will also automatically halt the conversion clock if the OVF flag sets (STATUS1). This is to prevent loss of data. The OVF flag will set if the ADC FIFO becomes full. This feature cannot be disabled.

4.2.9 ADC Data Transfer

ADC data is transferred off board via the ADCFIFO register. This register requires 16 bit access from the ISA bus to address Base + 00_H. Writing the appropriate value to the SELECT register is necessary to access the ADCFIFO. The data in this register is used for two types of data transfer mode. These are POLLED, INTERRUPT and DMA.

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4.2.9.1 ADCFIFO Register

This register accesses a 1024 Word FIFO. When the FIFO is enabled, at the end of each conversion the sample data from the ADC is latched into the FIFO and stored until it is read. If the FIFO becomes full, no further data will be stored until some is read out or the FIFO is reset. This register may be read directly (ISA read), or the data can be moved automatically to memory via DMA.

The FIFO has several status/control flags associated with it. These are:

- **FFEN** (CONTROL1) - Enables/Resets FIFO.
- **FNE** (STATUS1) - Indicates FIFO is not empty.
- **FHF** (STATUS1) - Indicates FIFO is half full.
- **OVF** (STATUS1) - Indicates FIFO is full.

The data read from the FIFO will return 2's complement encoded 12 or 16 bit data (zero volts = 0, negative voltage = negative value, positive voltage = positive value). The data can be treated as a 16 bit signed integer. The upper 4 bits of DIO0 can be used to quickly determine whether the board supports a 12-bit or 16-bit ADC.

***NOTE**: When the FIFO is empty (FNE = 0) or disabled (FFEN = 0), reading the ADCFIFO register will return the BOARD ID.*

4.2.9.2 Software Polled Acquisition Mode

This mode is the most CPU intensive acquisition mode, but on a fast machine, one can achieve higher data rates over the ISA bus than with DMA if the code is very efficient.

Basically, the G/C List, and clock and trigger modes are set up and initiated. The FNE flag in STATUS1 is polled until data becomes available. When data is available it is read from the FIFO. Be careful when sampling multiple channels. If you get out of sync, the board does not provide a way to determine which channel the data belongs to.

4.2.9.3 Interrupt Driven Mode

Interrupt mode is more efficient than polled mode especially if a slower sampling speeds are used because the overhead of polling status flags is removed. In this mode, program control is automatically transferred to a

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predetermined memory location as a result of any of several individually selectable events. The interrupt level used is programmable by writing to CONTROL2. Interrupts are enabled when a level is selected. Refer to Section 3.2.3.1 *Selecting An Interrupt Level*.

Interrupt On FIFO Not Empty

The CPU is interrupted whenever new data is available. This mode is selected by setting FIMD = 0 (CONTROL2) and disabling DMA by clearing the DLn bits in CONTROL2.

***NOTE** that an interrupt is generated only when FNE goes from 0 to 1. Therefore the entire contents of the FIFO should be read during the interrupt service routine so that the FNE will go low. If this is not done, no further interrupts of this type will be generated.*

Interrupt On FIFO Half Full

The CPU is interrupted whenever the FIFO becomes more than half full. This mode is selected by setting FIMD = 1 (CONTROL2) and disabling DMA by clearing the DLn bits in CONTROL2.

***NOTE** that an interrupt is generated only when FHF goes from 0 to 1. Therefore, enough of the contents of the FIFO must be read during the interrupt service routine so that the FNF will go low. If this is not done, no further interrupts of this type will be generated.*

Interrupt On TERMINAL COUNT

The CPU is interrupted after all selected DMA transfers are performed. This interrupt may be cleared by clearing the DMATC flag (MODE bit 6).

SPECIAL NOTE: Programmable Interrupts

The 5800 supports software programmable interrupts. However, the implementation is not as normally described by ISA definitions or IBM manuals. Standard implementation dictates that an interrupt will present a rising edge to the interrupt controller and remain until the interrupt is serviced. This implies that the interrupt was inactive (low) before the interrupt is generated and after it is serviced.

In our implementation, the idle state of the interrupt line is undriven. Since the standard interrupt controller circuits have pullups, this means the selected interrupt line will be seen as high by the interrupt

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controller. When an interrupt must occur, the signal is driven low momentarily and then released (generating the required rising edge, and subsequent high level state). With this system, interrupt lines may be shared between similar boards.

***NOTE** that the flag associated with the interrupt condition should be cleared by the interrupt service routine (this is not automatic in all cases). It is the act of the flag changing state that causes the interrupt pulse, so the flag must be cleared to reset the interrupt circuitry.*

4.2.9.4 DMA Transfer Mode

This mode requires the least software overhead of the ISA transfers, allowing the highest potential conversion speeds. In this mode, ADC data is automatically transferred to some predetermined location in memory by the DMA controller as soon as it becomes available. As many as 32,000 samples may be taken before software intervention is necessary. This mode can use any of the clocking methods, however, the overhead required for software clocking may defeat the purpose of using DMA.

Transfers will begin as soon as three conditions are met:

1) The DMA controller is programmed
2) A DMA channel is selected
3) The FIFO is not empty.

Be careful to empty the FIFO before enabling DMA, or any leftover data in the FIFO will end up getting transferred also (unless of course that is desirable). Also, because of the programmable nature of the DMA circuitry, unselected DMA requests will look to the DMA controller like active requests (the undriven lines float high). Thus it is necessary to enable DMA on the board **before** enabling the DMA controller chip. This will drive the selected request line low (inactive).

DMA can be programmed to use a single channel, or toggle between two channels following each terminal count. Note that when using dual channel mode, the terminal count flag (DMATC in STATUS1) must be cleared before the terminal count occurs on the next channel. Disabling DMA will reset the channel pointer to the primary channel. Refer to *Section 3.2.4.1 Selecting A New DMA Channel*.

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Interrupts which are useful in DMA transfer mode include the following. Interrupt on DMATC is enabled automatically when interrupts and DMA are enabled. Essentially, an interrupt is sent when the DMA transfer is complete. Another useful interrupt is the interrupt on Timer A0 terminal count. This is used with About Trigger Mode (see Section 4.2.8.3 *External Trigger*). Here the CPU is interrupted when the clock is stopped by Timer A0 counting down to zero (A0TC in STATUS1). This interrupt is also always enabled. One more useful interrupt is Interrupt on ADC Overflow (OVF in STATUS1). When an Overflow error occurs (the FIFO gets full) the ADC is automatically disabled. This may be a good time for program intervention. This mode is also always enabled.

If an overflow error is generated during a DMA transfer it is an indication that the PC bus is overloaded. Essentially this means that another board in the system is using up too much of the available bus transfer bandwidth. If this is the case, concurrent bus accesses must be stopped, or the conversion frequency must be slowed down.

4.2.9.5 Maximum Conversion Rate With DMA

The maximum acquisition rate of the ADC may be limited by the maximum DMA transfer rate of the machine rather than the conversion time of the ADC. The slower of the two will obviously set the limits of the system.

Typically, a DMA transfer cycle takes about 5 microseconds. However, a single transfer can take as long as 11 microseconds or more depending on system overhead (these numbers are based on the DMA controller running at 8 MHz, which is generally the case on most of the faster machines out.) Even if no other DMA channel is used, the memory refresh cycles will periodically push off DMA cycles. Effectively, this means that in a system with simple double buffered system, the ADC clock cannot run much faster than about 90 kHz and not lose data. This is improved upon with the addition of FIFOs. With FIFO's, the periodic slow transfers will simply cause the data to queue up in the FIFO.

Even higher data rates are, of course, possible if less than 1000 samples are to be taken (this is the depth of the FIFO). This FIFO is also invaluable when more than a single DMA block is to be filled. The FIFO can absorb the data while the CPU is resetting the DMA controller between complete DMA acquisition blocks.

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4.2.10 DAC Data Transfer

The optional on-board DACs are updated when they are written to. There is no clocking mechanism available. Data written to DAC0 is stored in a holding register. When DAC1 is written to, both DACs are updated simultaneously. The DAC DATA registers each require 16 bit access from the ISA bus to address Base + 00_H. Writing the appropriate value to the SELECT register will determine which of these registers is read.

4.2.10.1 DAC Data Registers

This register set provides access to the on-board DACs from the ISA bus. There are no flags to indicate the DAC outputs have settled. If the DACs are written to before their outputs have fully settled, the outputs will simply begin slewing to the new level.

The data written to the DACs may either be written as a two's complement 16 bit word for bipolar applications, or 16-bit unsigned if configured for unipolar operation. CONTROL6 is used to configure the DACs. The default condition of the DACs is bipolar with offset binary coding. At powerup, the DACs are preloaded to output 0 volts.

4.2.11 Digital Acquisition

The 5800 Series boards support 40 bits of digital I/O. All lines are TTL level, all input ports are terminated to +5V with 4.7KΩ resistors, and all output ports power up driving low. The DIO ports operate with positive logic. A "0" represents a TTL low, and a "1" represents a TTL high.

4.2.11.1 DIO0 4 bit Input Port

These signals are available at the main 50 pin I/O connector. They are accessed via the DIO0 register. This register is not latched. Any read access to this register will return the state of the 4 input bits.

4.2.11.2 DIO1 4 bit Output Port

These signals are also available at the main 50 pin I/O connector and are accessed via the DIO1 register. This register is latched when written to. There is a strobe signal (DOSTB) associated with the 4 output bits. This signal is normally low, but it will go high for 100ns when the port is written to. The falling edge of this signal can be used to externally latch this data.

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NOTE *that when the TB5800-TC Thermocouple interface panel is used, bits 2 and 3 of this port are no longer available. Instead these bits are used to select the Cold Junction Compensation rate of the thermocouple panel.*

4.2.11.3 DIO2 16 bit Input Port

The 16 bit input port on the 5800 Series boards is accessible through a 40 pin header on the board. The signals on this connector can be brought out to the back of the PC (at the cost of a slot) using an optional G16 cable. This cable is terminated with a 37-pin D-type connector which is compatible with a DC-37 screw terminal panel, as well as the DCI-EX and ACI-EX high voltage isolation panels.

This input port has a strobed holding register. Input data is latched into this register as a result of one of two sources. These are an external edge sensitive TTL input (active edge is selectable) available on the 40-pin header, or the output of Timer A2. The strobe source is selected using the D2SS1 and D2SS0 bits in CONTROL7. The input strobe can also be disable so that each access to the holding register (DIO2) will return the current state of the actual port. Note that DIO2 must be accessed as a 16-bit read on the ISA bus.

There are two flags associated with this port. Both are located in STATUS2. The STB2 flag will set when an input strobe is received. If strobes are disabled, this bit will remain set (indicating there is always new data). This flag can be cleared by writing to it, but it will also clear when the DIO2 register is read. The D2ERR flag will set if new data is strobed into the port before the previous data was read. Both of these flags can be programmed to generate a CPU interrupt (S2IEN and D2IEN in CONTROL7).

4.2.11.4 DIO3 16 bit Output Port

The 16 bit output port on the 5800 Series boards is also accessible through a 40 pin header on the board. The signals on this connector can be brought out to the back of the PC (at the cost of a slot) using an optional G16 cable. This cable is terminated with a 37-pin D-type connector which is compatible with a DC-37 screw terminal panel, as well as the DCO-EX and ACO-EX high voltage isolation panels.

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This output port has a pre-register. Output data can be stored in this register until it is strobed out onto the port. The data can either be strobed out automatically after each write to DIO3 or strobed out on the falling edge of Timer A2 out. Bit D3SS1 of CONTROL7 is used to program the mode. Note that DIO3 must be accessed as a 16-bit write on the ISA bus.

When the output port is updated an external strobe output will pulse for 100ns. The trailing edge of this pulse may be used to externally latch the output data. The pulse may be either active high of active low (bit D3SS0 of CONTROL7).

There are two flags associated with this port. Both are located in STATUS4. The STB3 flag will set when an the pre-register is strobed out onto the port. If strobes are disabled, this bit will remain set (indicating pre-register has been strobed out). This flag can be cleared by writing to it, but it will also clear when the DIO3 register is written to. The D3ERR flag will set if a strobe occurs before the pre-register is loaded. Both of these flags can be programmed to generate a CPU interrupt (S3IEN and D3IEN in CONTROL7).

4.3 PROGRAM EXAMPLES

The following sections will illustrate the basic sequence of steps necessary to program the board in any of the modes available. These are pseudo-code examples which should be relatively easy to translate into your language of choice.

4.3.1 Board Reset

In order to guarantee a clean acquisition, it is a good idea to reset the board prior to any acquisition. The following steps will bring the board to a known idle state. This of course will stop any acquisition currently in process, so do not use this method to start an ADC acquisition if some other process is still running.

write 00_H to STATUS2	*Put board in reset state*
write 80_H to STATUS2	*Release reset*
wait for READY = 1	*(*STATUS2*)*

(necessary if a conversion may already be in process)

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If there is a prior conversion still in process, the READY flag will not set until this conversion has completed. On 16-bit boards, the ADC will perform a self calibration each time the board is reset. This calibration will take about 50 milliseconds to complete. The READY flag will set after the calibration process is done.

The ACQDATA register (Base + 00_H) should return the board ID at this point.

4.3.2 Single Sample Acquisition

This acquisition mode is the most basic mode of the board. It does not involve timed acquisition. This procedure will simply sample the voltage at any channel.

RESET BOARD
or

write 00_H to CONTROL1	*disable triggers*
write 00_H to CONTROL3	*disable clocks*
write 40_H to STATUS1	*disable ADC*
write 00_H to SADDR	*single element RAM list*
write 01_H to CONTROL1	*enable FIFO*
write $C0_H$ to STATUS1	*enable ADC (*CVEN *= 1)*

repeat:

write 01_H to SELECT	*select* G/C RAM
select gain/channel	*(*ACQDATA*)*
wait for READY = 1	*(*STATUS2*)*
write 00_H to SELECT	*select* ADC FIFO
write 00_H to ACQDATA	*start conversion*
wait for FNE = 1	*(*STATUS1*)*
read ADC data	*(*ACQDATA*)*

If you sample the same channel each time, it is only necessary to repeat the last 3 steps.

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4.3.3 Clocked Acquisition

This acquisition mode uses Timers A1 and A2 to generate the ADC clocks. Timer A1 is fed by a 5 MHz clock and Timer A2 is fed by Timer A1. To calculate the Timer data to generate a specific frequency divide 5,000,000 by the desired frequency in Hz. The resultant integer must be equal to the product of the numbers written to the Timers. If the result is less than 2^{17} set Timer A1 data = 0002_H and set Timer A2 data = result ÷ 2. If the result is larger, pick two numbers whose product is the result.

RESET BOARD	
or	
write 00_H to CONTROL1	*disable triggers*
write 00_H to CONTROL3	*disable clocks*
write 40_H to STATUS1	*disable ADC*
write 00_H to SADDR	*single element RAM list*
write 74_H to TCONTROLA	*Timer A1 = mode 2*
write low byte Timer A1 data	*(*TIMERA1*)*
write high byte Timer A1 data	*(*TIMERA1*)*
write $B4_H$ to TCONTROLA	*Timer A2 = mode 2*
write low byte Timer A2 data	*(*TIMERA2*)*
write high byte Timer A2 data	*(*TIMERA2*)*
write 01_H to SELECT	*select* G/C RAM
select gain/channel	*(*ACQDATA*)*
wait for READY = 1	*(*STATUS2*)*
write 00_H to SELECT	*select* ADC FIFO
write 01_H to CONTROL3	*Bipolar, DI, Timer A2 = clock*
write $C0_H$ to STATUS1	*enable ADC (*CVEN *= 1)*
write 05_H to CONTROL1	*enable FIFO, gate Timers on*
repeat:	
wait for FNE = 1	*(*STATUS1*)*
read ADC data	*(*ACQDATA*)*
write 40_H to STATUS1	*disable ADC (Stop Acquisition)*

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If the CERR (clock error) flag sets (STATUS2), the clock rate has exceeded the speed limit of the ADC. If the OVF (overflow) flag sets (STATUS1) the ADC sample rate has exceeded the data bandwidth of your machine/software.

4.3.4 Multiple Channel Burst Acquisition

This acquisition mode uses the burst clock to generate ADC clocks. The board will sample each channel in the G/C list, wait for a new clock from Timer A2 and repeat the process. The burst rate must be >= the Timer A2 rate × # of channels (burst length). To determine the burst rate data value, divide 1,000,000 by the desired rate and subtract 1.

For this example, the Timer A2 rate is 10kHz, the burst rate is 100kHz, and 8 channels are samples. The following table is how the G/C list will be configured. Notice that channels with like gain settings are grouped together in the list.

List Element	Channel	Gain
1	0	×1
2	2	×1
3	5	×1
4	3	×2
5	1	×4
6	4	×4
7	6	×8
8	7	×8

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RESET BOARD
or

write 00_H to CONTROL1	*disable triggers*
write 00_H to CONTROL3	*disable clocks*
write 40_H to STATUS1	*disable ADC*
write 74_H to TCONTROLA	*Timer A1 = mode 2*
write 02_H to TIMERA1	*Timer A1 data= 2*
write 00_H to TIMERA1	*(2.5MHz)*
write $B4_H$ to TCONTROLA	*Timer A2 = mode 2*
write FA_H to TIMERA2	*Timer A2 data= 250*
write 00_H to TIMERA2	*(10 kHz)*
write 07_H to BLENGTH	*Burst length = 8 samples*
write 09_H to BRATE	*Burst rate = 100 kHz*
write 07_H to SADDR	*8 element RAM list*
write 01_H to SELECT	*select* G/C RAM
write 0000_H to ACQDATA	*G/C list element #1*
write 0002_H to ACQDATA	*G/C list element #2*
write 0005_H to ACQDATA	*G/C list element #3*
write 0103_H to ACQDATA	*G/C list element #4*
write 0201_H to ACQDATA	*G/C list element #5*
write 0204_H to ACQDATA	*G/C list element #6*
write 0306_H to ACQDATA	*G/C list element #7*
write 0308_H to ACQDATA	*G/C list element #8*
wait for READY = 1	*(*STATUS2*)*
write 00_H to SELECT	*select* ADC FIFO
write 05_H to CONTROL3	*Bipolar, DI, Burst Mode*
write $C0_H$ to STATUS1	*enable ADC (*CVEN *= 1)*
write 05_H to CONTROL1	*enable FIFO, gate Timers on*
repeat:	
wait for FNE = 1	*(*STATUS1*)*
read ADC data	*(*ACQDATA*)*
write 40_H to STATUS1	*disable ADC (Stop Acquisition)*

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If the BERR (burst error) flag sets (STATUS2), the burst rate is less than the pacer rate × burst length. The first piece of data will be data from the first channel in the G/C list (list element #1). Keep careful track of what channel you are reading data from.

4.3.5 Programming Tips

There are several different enable signals in the control register. The difference between these bits is subtle but important.

CVEN - This flag located in the STATUS1 register enables the ADC to do conversions. This flag also re-arms trigger inputs. This enable will NOT stop or disable clocks, it will only cause the ADC to ignore any clocks. If you are running in a mode where a trigger is used to start the clock, set this bit last to start the acquisition.

FFEN - This flag located in the CONTROL1 register clears and enables the FIFO. If this bit is cleared, all data currently stored in the FIFO will be lost. This bit MUST be set to sample ADC data over the ISA bus.

CGEN - This flag located in the CONTROL1 register gates Timers A1 and A2. If you are using the on-board timers, and starting them with software, always set this bit last to start the acquisition.

TGEN - This flag located in the CONTROL1 register gates the external trigger/gate. If you are using the external trigger input as a gate, always set this bit last to start the acquisition.

4.3.6 Programming The DACs

This simple program shows how to update the optional DAC voltage outputs. The actual voltage will not change until the DAC1 data register is updated is updated.

write 02_H to SELECT	*select DAC 0 data register*
write DAC0 data	*(*ACQDATA*)*
write 03_H to SELECT	*select DAC 1 data register*
write DAC1 data	*(*ACQDATA*)*

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4.4 H/W REGISTERS

The 5800 register map is designed as a superset of the DAS–1800 Series register map. All Registers on the DAS-1800 are 8 bit access only except the ones mapped to Base + 00_H. The 5800 contains several H/W Registers not available on the DAS-1800. The 5800 has additional DATA Registers and an additional CONTROL Register. With few exceptions, the DATA registers are 16 bit access only and the CONTROL/STATUS registers are 8 bit access only.

4.4.1 Register Summary

ADDRESS (Base + n)	REGISTER	R/W	FUNCTION
00_H,01_H	ACQDATA	R/W	Acquisition Data Port
02_H	SELECT	R/W	Acquisition Port Select
03_H	DIO0	R	Digital Port 0 / Board ID
	DIO1	W	Digital Port 1
04_H	CONTROL1	R/W	ADC Trigger/Gate/FIFO
05_H	CONTROL2	R/W	ADC Interrupt/DMA
06_H	CONTROL3	R/W	ADC Configuration
07_H	STATUS1	R/W	Int/FIFO/TimerA/ADC
08_H	BLENGTH	R/W	Burst Length Register
09_H	BRATE	R/W	Burst Rate Register
$0A_H$	SADDR	R/W	RAM Address Register
$0B_H$	STATUS2	R/W	ADC/ERROR
$0C_H$	TIMERA0	R/W	Timer A0 Status/Data
$0D_H$	TIMERA1	R/W	Timer A1 Status/Data
$0E_H$	TIMERA2	R/W	Timer A2 Status/Data
$0F_H$	TCONTROLA	W	Timer A Control Register
10_H,11_H	DIO2	R	Digital Port 2
12_H,13_H	DIO3	R/W	Digital Port 3
16_H	CONTROL6	R/W	DAC Configuration
$1A_H$	CONTROL7	R/W	Digital I/O Strobe
$1B_H$	STATUS4	R/W	DIO Port 3 / Error

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The following registers are all accessed through the ACQDATA register at Base + 00_H. To access a particular register, write the indicated value to the SELECT register (Base + 02_H)

SELECT	REGISTER	R/W	FUNCTION
0	BOARD ID	R	Identification Word
0	ADCFIFO	R	ADC FIFO Data
0	CONVERT	W	A/D Convert Command
1	G/C RAM	R/W	Gain and Channel List
2	ADCDATA	R	ADC Latched Data
2	DAC0DATA	W	DAC0 Data Register
3	CHAN	R	Latched Channel
3	DAC1DATA	W	DAC1 Data Register

4.4.2 ACQDATA Base + 00_H Acquisition Data Registers (16-bit) (Read/Write)

ACQDATA is a special register through which both DACs, the ADC, and the Gain/Channel RAM may be accessed. These are all 16-bit access only registers. Any I/O read or write to this address will access the register selected in the SELECT register located at Base + 02_H

This address is used for the following functions:

- Board ID
- Data from the ADC FIFO
- A/D Convert Command
- Data to/from the gain/channel RAM
- Data to DAC0
- Data to DAC1

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4.4.2.1 Board ID (Read)

This register is accessible only when the ADC FIFO is disabled (FFEN = 0) or empty (FNE = 0). This is the case at power-up and this register may be read immediately after power-up or reset to determine which board or board options are currently installed. Bit assignments for the BOARD ID are as follows:

15	14	13	12	11	10	9	8
PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4

7	6	5	4	3	2	1	0
PD3	PD2	PD1	PD0	VER3	VER2	VER1	VER0

At power-up the board will return the board ID at address Base + 00_H.

The bit names are defined and used as follows:

- **PD11** through **PD0** define the product being accessed. These bits will read back as follows for 5800 Series:

PD_N	Product
01_H	5801MF Gain = 1,2,4,8
02_H	5802MF Gain = 1,10,100,500
03_H	5803HR Gain = 1,2,4,8
04_H	5804HR Gain = 1,10,100,500

- **VER3** through **VER0** define the installed options on the board. These bits are fixed at the factory to one of the following:

VER_N	DACs
01_H	
02_H	•

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4.4.2.2 ADC FIFO (Read)

This register may be accessed by writing 00_H to the SELECT register. It provides 16 bit read only access to the ADC FIFO. For boards with a 12-bit ADC, the data is right justified. Data will be returned in two's complement format for 12 or 16-bit boards configured for bipolar mode. This allows data to be treated directly as 16 bit signed integers. Unipolar data is returned as direct binary with leading zeros. 12-bit data may be interpreted as a signed or unsigned 16-bit integer.

Bit 6 of STATUS1, FNE (FIFO Not Empty), indicates whether there is any data currently in the FIFO. FIFO half full and FIFO overflow flags are also available in the same register.

Bit 0 of CONTROL1 is used to enable and disable the FIFO, as well as, to reset the FIFO. The FIFO must be enabled before it can be loaded with ADC Data. Disabling the FIFO also clears its contents.

Bit 7 of CONTROL3, U/B is used to select the appropriate input data coding for the jumpered input configuration: Unipolar data is returned as a straight binary number. Bipolar data is returned as a 16 bit two's complement number (signed integer).

Bit assignments for 12-bit bipolar ADC data are as follows:

15	14	13	12	11	10	9	8
AD11	AD11	AD11	AD11	AD11	AD10	AD9	AD8

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Bit assignments for 12-bit unipolar ADC data are as follows:

15	14	13	12	11	10	9	8
0	0	0	0	AD11	AD10	AD9	AD8

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

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Bit assignments for 16-bit ADC data are as follows:

15	14	13	12	11	10	9	8
AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

The FIFO powers up empty and disabled.

The bit names are defined and used as follows:

- **0** = Always reads as zero
- **AD15** through **AD0** are ADC data bits, AD0 is LSB and AD11 or AD15 is MSB.

4.4.2.3 A/D Convert Command (Write)

This register may be used to initiate an A/D Conversion. A Write to Base + 00_H will initiate a conversion. For SW conversions to operate, bits 2, 1 and 0 of the SELECT register must be set = 0. Also, A/D conversions must be enabled (STATUS1, CVEN = 1). When the clock source is set to the clock bus (CONTROL3, S2 = 1), SW convert is disabled on all but the clock bus source board. Issuing a convert command from the clock bus source board will result in a conversion on all boards connected to the bus.

The following steps should be followed to cause SW conversions:

- Select software convert only in CONTROL3 by setting S2, S1 and S0 bits = 0
- Enable A/D Conversions by setting the CVEN bit of STATUS1 = 1. (Refer to the section on STATUS1 for information on controlling the bits in STATUS1)
- Wait for READY = 1 (STATUS2)
- Select A/D Conversions by writing 00_H to the SELECT register
- Repeat the following steps as desired
- Write any value to ACQDATA
- Wait for READY = 1 (STATUS2)

Data may be read after each conversion or after a series of conversions from the ADC FIFO register.

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Bit assignments for the CONVERT command are as follows:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

The bit names are defined and used as follows:

- **X** = Don't care what is written

The convert command is selected, but disabled at Power-up.

4.4.2.4 Gain/Channel RAM (Read/Write)

This register may be accessed by writing 01_H to the SELECT register. It provides 16-bit read/write access to the ADC Gain/Channel RAM which is used to select the channel number and gain setting for the next A/D conversion.

Reading this register will return the currently selected gain/channel combination. Writing to this register will update the currently selected RAM location. Each write to this register will also decrement the current RAM address. Hence, successive writes to this register will set adjacent RAM locations. The current RAM location may be set by writing to the SADDR (Starting Address) Register.

***NOTE**: Shortly after the start of each ADC conversion (after the ADC S&H has gone into HOLD) the current RAM address will also decrement. Therefore, it is a good idea to disable conversions when updating the gain/channel list.*

***NOTE** also that each time the gain/channel RAM address is changed, the gain and/or channel setting is assumed to have changed. The front end circuitry (multiplexers and gain amp) must settle to the new settings. Therefore after each change an internal timer marks out the required settling time for the new settings. This settling period is indicated by the READY flag in STATUS2 going low for the duration of the settling time. If an ADC clock is received during this time, the clock error flag (CERR) will set.*

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Bit assignments for Gain/Channel RAM data are as follows:

15	14	13	12	11	10	9	8
X	X	X	X	TEST	CJEN	GN1	GN0

7	6	5	4	3	2	1	0
MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

The contents of the Gain/Channel RAM is undefined at power-up.

The bit names are defined and used as follows:

- **X** = don't care
- **TEST -** This is a special diagnostic bit. When this bit is set, the MUX selection is ignored and the ADC is connected to on-board DAC #0. This feature is only available when the optional DACs are installed.
- **CJEN -** This bit is read/write. It is used to enable cold junction compensation on the TB5800-TC terminal panel. When this bit is set (1) The compensation rate selected by bits 2 and 3 in DIO1 will be applied to the selected input channel. When this this bit is clear (0), the compensation is disabled for that channel.

  CJEN = 0: Cold Junction Compensation disabled
  CJEN = 1: Cold Junction Compensation enabled
- **GN1** and **GN0** select the ADC gain settings as follows:

Gain Code		Gain Value			
GN1	**GN0**	**5801MF**	**5802MF**	**5803HR**	**5804HR**
0	0	x1	x1	x1	x1
0	1	x2	x10	x2	x10
1	0	x4	x100	x4	x100
1	1	X8	X500	X8	X500

- will **MUX3** through **MUX0** control the on-board analog input multiplexers. Use these bits to select one of 16 channels in single ended mode or 1 of 8 in differential mode. Bit 11 (TEST) must be set = 0 for these bits to select the analog input channels.

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If one of the available expansion multiplexer panels (TB5800 Series) are used, these bits will select the external multiplexer bank.

- **MUX7** through **MUX4** are only used when one of the available TB5800 Series expansion panels is employed. Then these bits select the individual channel in a multiplexer bank.

4.4.2.5 DAC0 and DAC1 Data (Write)

This register may be accessed by writing 02_H or 03_H to the SELECT register. It provides 16 bit write only access to the two optional on-board DACs. Data format is normally offset binary for all DAC configurations (0000_H represents negative full scale, $0FFF_H$ or $FFFF_H$ represents positive full scale). DACs which are programmed to operate in bipolar mode may also be programmed to accept two's complement data (see CONTROL6 bit 6).

To select DAC0 DATA, 02_H must be written to the SELECT register.

To select DAC1 DATA, 03_H must be written to the SELECT register.

The outputs of DAC0 and DAC1 are both updated when DAC1 DATA is written to.

Bit assignments for 16-bit DAC data are as follows:

15	14	13	12	11	10	9	8
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

The bit names are defined and used as follows:

- **X** = Don't care what is written
- **DA15** through **DA0** are DAC data bits, DA0 is LSB and DA15 is MSB.

Both DACs will power up driving out 0 Volts.

The software reset bit (STATUS2 bit 7) has no affect on the DACs.

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4.4.3 SELECT Base + 02_H Acquisition Port Select (8-bit) (Read/Write)

This register is used to control the function of the ACQDATA register The values written to this register define which acquisition function may be accessed at address Base + 00_H.

Bit assignments for the SELECT register are as follows:

7	6	5	4	3	2	1	0
rsvd	0	0	0	0	TEST	APS1	APS0

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **rsvd -** This write only bit is reserved for factory testing. Always write 0 to this bit.
- **0 -** These bits are not used and will always return 0.
- **TEST** - This bit is used to enable a special factory test mode for the board. Always set this bit to 0.

  TEST = 0: Test Mode OFF, Normal operation.
  TEST = 1: Test Mode ON.

- **APS1** and **APS0** select the function of the ACQDATA register as follows:

APS1	APS0	R/W	Function
0	0	R W	ADC FIFO Data Convert Command
0	1	R/W	Gain/Channel RAM
1	0	R W	ADC Data Latch DAC0 DATA
1	1	R W	ADC Channel Latch DAC1 DATA

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4.4.4 DIO0, DIO1 Base + 03_H Digital I/O Ports (8-bit) (Read/Write)

This register is used to access the two 4-bit digital ports DIO0 and DIO1. In addition, this port contains board ID information.

4.4.4.1 DIO0 (Read Only)

This 8-bit register provides access to the 4 input bits of digital port 0, and provides limited board ID information.

Bit assignments for the DIO0 register are as follows:

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	D3	D2	D1	D0

The bit names are defined and used as follows:

- Indicates which version of the 5800 family is being accessed as **ID3** through **ID0** represent the product ID. The value returned follows:

ID3-ID0	PRODUCT
6_H	580xHR
7_H	580xMF
C_H	USI = 2 (DAS-1600)

- **D3** through **D0** represent each of the four input lines of digital port 0. These lines are not latched and represent the state of the input lines at the time of the read.

4.4.4.2 DIO1 (Write Only)

This 8-bit register provides access to the 4 output bits of digital port 1.

Bit assignments for the DIO1 register are as follows:

7	6	5	4	3	2	1	0
X	X	X	X	D3	D2	D1	D0

These lines power-up driving out logic 0.

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The bit names are defined and used as follows:

- **X** = don't care, value
- **D3** through **D0** represent each of the four output lines of digital port 1. These lines are updated when this port is written. The current state of these lines can NOT be read back unless these lines are connected to the four digital input lines of DIO0. Writing a "1" to a given bit will output a TTL /CMOS "high level" on the associated digital output line. Writing a "0" will output a TTL/CMOS "low level".

***NOTE**: D3 and D2 are used to select the cold junction compensation rate on the TB5800-TC terminal panel as follows. The CJEN bit of the GCRAM register must be set (1) also to enable compensation:*

D3	D2	Thermocouple	Compensation Rate
0	0	Type J	51.7 µV/°C
0	1	Type K or Type T	40.6 µV/°C
1	0	Type E	60.9 µV/°C
1	1	Type R or Type S	6.0 µV/°C
*	*	Type B or Millivolt Input	0.0 µV/°C

** To select Type B or no compensation, clear (0) CJEN in the CGRAM register for the specified channel.*

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4.4.5 CONTROL1 Base + 04_H FIFO/Trigger/Timer Control (8-bit) (Read/Write)

This register is used to control the trigger, gate and FIFO enable functions of the ADC.

Bit assignments for the CONTROL1 register are as follows:

7	6	5	4	3	2	1	0
ATEN	TGPL	TGSL	TGEN	CGSL	CGEN	RSVD	FFEN

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **ATEN -** This bit is used to enable *About Trigger* mode. In *About Trigger* mode, once conversions have been started (by a valid hardware of software trigger), the next valid hardware trigger condition on the TGIN input enables Timer A0. Timer A0 then decrements each time a new A/D Conversion occurs. Once Timer A0 counts to 0, conversions are disabled.

  ATEN = 0: *About Trigger* mode disabled
  ATEN = 1: *About Trigger* mode enabled

- **TGPL -** This bit selects the input polarity of the TGIN input.

  TGPL = 0: TGIN is falling edge or low level active
  TGPL = 1: TGIN is rising edge or high level active

- **TGSL -** This bit selects the input mode of the TGIN input. When edge sensitive mode is used, the trigger may be re-armed to detect a new trigger by clearing CVEN (STATUS1).

  TGSL = 0: TGIN is edge sensitive (*TRIGGER* mode).
  TGSL = 1: TGIN is level sensitive (*GATE* mode).

- **TGEN -** This bit is used to enable/disable the TGIN input. Note that this bit will not disable the "second" trigger in *About Trigger* mode which starts Timer A0 counting conversions.

  TGEN = 0: TGIN input ignored (disabled).
  TGEN = 1: TGIN input enabled.

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- **CGSL -** This bit selects the source of the gate inputs to Timer A1 and Timer A2 (the internal Pacer clocks). Refer to Intel 82C54 specification for information on the functions of the gate inputs of Timer A1 and Timer A2.

  CGSL = 0: CGEN bit gates Timer A1 and Timer A2.
  CGSL = 1: TGIN input gates Timer A1 and Timer A2.

- **CGEN** - This bit is a software gate for Timer A1 and Timer A2. Note that this bit only functions if CGSL = 0.

  CGEN = 0: Timer A1 and A2 gated off (when CGSL = 0).
  CGEN = 1: Timer A1 and A2 gated on (when CGSL = 0).

- **RSVD -** The function of this bit has not yet been defined. This bit is reserved for future product enhancements. Always set this bit = 0.

  RSVD = 0: undefined
  RSVD = 1: undefined

- **FFEN -** This bit enables and disables or resets the on-board ADC FIFO. When the FIFO is reset, all data in the FIFO is lost. The FIFO must be enabled to run A/D conversions.

  FFEN = 0: ADC FIFO reset (disabled).
  FFEN = 1: ADC FIFO enabled.

FIFO/Trigger/Timer Control. The following tables help to illustrate how the above register should be programmed for a given Trigger/Gate mode.

Function (Internal ADC Pacer)	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X*	0	0	0 / 1	CVEN
External Gate	0	1	1	1	X	TGIN
External Post Trigger	0	0	1	1	X	TGIN
External Pre Trigger or External About trigger	1	0	**	0	1	TGIN

* X = don't care

** With TGEN = 0, the first external trigger will enable Timer A0 to count conversions. With TGEN = 1, the first trigger enables Timer A2 to clock the ADC, and the second trigger enables Timer A0 to count conversions.

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Function (External ADC Pacer)	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X*	0	0	***	CGEN
External Gate	0	1	1	0	***	TGIN
External Post Trigger	0	0	1	0	***	TGIN
External Pre Trigger or External About trigger	1	0	**	0	***	TGIN

* X = don't care

** With TGEN = 0, the first external trigger will enable Timer A0 to count conversions. With TGEN = 1, the first trigger enables Timer A2 to clock the ADC, and the second trigger enables Timer A0 to count conversions.

*** Timers A1/A2 are available for "alternate use". CGEN will gate the timers on and off.

4.4.6 CONTROL2 Base + 05_H DMA/Interrupt Control (8-bit) (Read/Write)

This register controls the various DMA and Interrupt functions associated with the ADC function.

Bit assignments for the CONTROL2 register are as follows:

7	6	5	4	3	2	1	0
TIEN	FIMD	IL2	IL1	IL0	DL2	DL1	DL0

This register powers up with all bits = 0.

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The bit names are defined and used as follows:

- **TIEN -** This bit enables interrupts on Timer A2 terminal count. If this bit is set and an interrupt level is selected, the Timer A2 terminal count flag (A2TC) in the STATUS1 register will generate an interrupt when it sets.

  TIEN = 0: Timer A2 terminal count interrupt disabled.
  TIEN = 1: Timer A2 terminal count interrupt enabled if interrupts enabled.

- **FIMD -** This bit selects the FIFO interrupt mode. There are two types of interrupt which may be caused by the FIFO. These are FIFO Half Full (FHF) and FIFO Not Empty (FNE). Each of these conditions are represented by flags in the STATUS1 register. The state of this bit determines which of these two flags, when set, will generate an interrupt. Note that if DMA Is selected (see DL2-DL0) neither of these conditions will generate an interrupt. Instead, the DMA Terminal Count flag (DMATC) will cause an interrupt.

  FIMD = 0: Interrupt on FIFO Not Empty selected.
  FIMD = 1: Interrupt on FIFO (more than) Half Full is selected.

- **IL2, IL1, IL0 -** These bits serve two functions. First, they select the interrupt level for the board. Second they enable interrupts. Essentially, selecting an interrupt level also enables interrupts to be generated. An interrupt is generated whenever the INT flag in the STATUS1 register is set.

  The 5800 Series boards use an open collector low level pulse rather than the typical totem pole implementation. In our implementation, clearing or disabling the interrupt before it is serviced is not possible. This implementation also allows for shared interrupts among boards which implement this interrupt mechanism.

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The following table indicates these bits are used to select an interrupt level:

IL2	IL1	IL0	Interrupt Level A
0	0	0	Interrupt A disabled
0	0	1	Level 3
0	1	0	Level 5
0	1	1	Level 7
1	0	0	Interrupt A disabled
1	0	1	Level 10
1	1	0	Level 11
1	1	1	Level 15

- **DL2, DL1, DL0 -** These bits are used to both select the DMA Channel and to enable DMA. Once enabled, whenever the FIFO not empty flag sets, a DMA Request is issued. The request will remain active until the FIFO is emptied or a DMA Terminal Count is received.

  When dual DMA is used, the first requests are generated on the higher priority level (lower number) and continue on that level until a DMA Terminal Count is detected. At this point requests on the first channel are discontinued and requests are generated on the second DMA channel until a terminal count is detected on that channel. Presumably while transfers were occurring on the second channel, the DMA controller was being reprogrammed for a new starting address on the first level. The DMATC flag (STATUS1 bit 1) must be cleared from the previous transfer before the current transfer completes. Transfers will not begin on a new DMA channel unless the DMATC flag from the prior transfer has been cleared.

  When a the second terminal count is received, requests again resume on the first level.

  When DMA is disabled the active DMA Channel is automatically reset to the higher priority (first) channel in the dual DMA sequence.

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The following table indicates these bits are used to select a DMA channel:

DL2	DL1	DL0	DMA Channel
0	0	0	DMA disabled
0	0	1	Channel 5
0	1	0	Channel 6
0	1	1	Channel 7
1	0	0	DMA disabled
1	0	1	DUAL DMA Channel 5 and Channel 6
1	1	0	Dual DMA Channel 6 and Channel 7
1	1	1	Dual DMA Channel 5 and Channel 7

4.4.7 CONTROL3 Base + 06_H ADC Config/Clock Control (8-bit) (Read/Write)

This register controls the ADC input configuration, as well as, the on-board PACER Clock Modes.

Bit assignments for the CONTROL3 register are as follows:

7	6	5	4	3	2	1	0
U/B	S/D	rsvd	rsvd	PDEN	BMDE	S1	S0

This register powers up with all bits = 0.

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The bit names are defined and used as follows:

- **U/B -** This bit selects the data coding (Unipolar or Bipolar) of the ADC (where applicable). This bit should always be set to match the jumpered ADC input configuration.

  U/B = 0: Sets ADC to return two's complement in Bipolar mode.
  U/B = 1: Sets ADC to return straight binary in Unipolar mode.

- **S/D -** This bit selects the input multiplexer configuration (Differential or Single-ended) of the ADC. The options are 8 Fully-differential inputs (each channel has a high and a low input) or 16 Single-ended inputs (each channel has a high input and all channels share a common low input).

  Note that with a TB5800-64 terminal panel, the maximum number of channels increases to 32 Differential or 64 Differential.

  S/D = 0: ADC multiplexer set to 8 Differential inputs.
  S/D = 1: ADC multiplexer set to 16 Single-ended inputs.

- **rsvd -** This bit is R/W but it is reserved for future applications. This bit should always be set = 0.

  rsvd = 0: Always write 0 to this bit.

- **PDEN -** This bit enables Pseudo Differential Mode when the input multiplexers are configured for Single Ended Operation. Pseudo Differential mode connects the PDIN common return directly to the low side of the input instrumentation amplifier. This mode is recommended when the common reference point is tied to some ground other than board Analog Ground.

  PDEN = 0: User common tied to Analog Ground (Single-ended)
  PDEN = 1: User common tied to Instrument Amp Low (Pseudo-Differential)

- **BMDE -** This mode is used to enable ADC Burst Mode.

  BMDE = 0: Burst mode is disabled.
  BMDE = 1: Burst Mode is enabled.

- **S1, S0** - These bits select the source of the ADC Pacer Clock.

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The following table indicates these bits are used to select a Pacer Source:

S1	S0	ADC Pacer Clock Source
0	0	Software Convert only.
0	1	Internal Pacer Clock (Timer A2 Out falling edge)
1	0	External Pacer Clock (XCLK rising edge)
1	1	External Pacer Clock (XCLK falling edge)

4.4.8 STATUS1 Base + 07_H Int/FIFO/Timer A Status (8-bit) (Read/Write)

This register provides status flags which report the condition of various on-board processes. These bits are each set by a specific condition and may be cleared by writing a "0". Writing a "1" has no effect. The exceptions to this are FHF and FNE which cannot be directly controlled at all in software, and CVEN, which may be set and cleared only if bit 6 is set.

Bit assignments for the STATUS1 register are as follows:

7	6	5	4	3	2	1	0
CVEN	FNE	FHF	OVF	A0TC	A2TC	DMATC	INT

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **CVEN -** This bit is used to enable A/D Conversions. This bit is the master control for the ADC. No conversions can happen unless this bit is set. To set this bit, write a 1 to bits 6 and 7 simultaneously. To clear this bit write a 1 to bit 6 and a 0 to bit 7 simultaneously.

  This bit is reset (0) by hardware if a FIFO Overflow occurs, or in *About Trigger* mode when Timer A0 Terminal Count occurs.

  CVEN = 0: A/D Conversions are disabled.
  CVEN = 1: A/D Conversions are enabled.

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set CVEN: Write "1" to bits 7 and 6 of Status.
clear CVEN: ATEN = 1 and Timer A0 Reaches Terminal Count, or FIFO becomes full (OVF = 1), or write "1" to bit 6 and write "0" to bit 7.

- **FNE -** This bit indicates that the ADC FIFO is Not Empty. This bit cannot be set or cleared directly. It can be cleared indirectly by reading the FIFO until it is empty, or by resetting the FIFO (CONTROL1, FFEN = 0). This bit can generate an interrupt (see INT).

  FNE = 0: ADC FIFO is empty (no DATA).
  FNE = 1: ADC FIFO contains data.

- **FHF -** This bit indicates that the ADC FIFO is Half Full or more. This bit cannot be set or cleared directly. It can be cleared indirectly by reading the FIFO until it is less than half full (512 words), or by resetting the FIFO (CONTROL1, FFEN = 0). This bit can generate an interrupt (see INT).

  FHF = 0: ADC FIFO contains less than 512 words of DATA.
  FHF = 1: ADC FIFO contains 512 words of DATA or more.

- **OVF -** This bit indicates that the ADC FIFO has filled to capacity (1024 Words). To prevent data loss, when this flag sets, conversions are disabled (CVEN → 0) automatically. This bit can generate an interrupt (see INT).

  OVF = 0: no error
  OVF = 1: ADC FIFO is full.

  set OVF: ADC FIFO becomes full
  clear OVF: Write "0" to bit 4 of STATUS1.

- **A0TC -** This flag indicates a Timer A0 terminal count has occurred (or more specifically the output of Timer A0 has generated a rising edge. This flag will only set if *About Trigger* mode is enabled (ATEN = 1). Timer A0 should be set to 8254 mode 0 for this flag to operate correctly. This flag will generate an interrupt if it sets and interrupts are selected.

  A0TC = 0: Timer A0 Terminal Count has not occurred.
  A0TC = 1 Timer A0 Terminal Count has occurred.

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set A0TC: ATEN = 1 and Timer A0 generates a TC
clear A0TC: Write "0" to bit 3 of STATUS1.

- **A2TC -** This flag indicates a Timer A2 terminal count has occurred (or more specifically the output of Timer A2 has generated a rising edge. This flag will only set if Interrupts on Timer A2 terminal count are enabled (TIEN = 1). Timer A2 should be set to 8254 mode 2 for this flag to operate correctly. This flag will generate an interrupt if it sets and interrupts are selected.

  A2TC = 0: Timer A2 Terminal Count has not occurred.
  A2TC = 1: Timer A2 Terminal Count has occurred.

  set A2TC: TIEN = 1 and Timer A2 generates a TC
  clear A2TC: Write "0" to bit 2 of STATUS1.

- **DMATC -** This flag indicates that the DMA controller on the ISA host has generated a terminal count pulse for one of the currently selected DMA channels. This flag will generate an interrupt if interrupts are selected.

  DMATC = 0: No DMA terminal count has occurred.
  DMATC = 1: DMA Terminal Count occurred.

  set DMATC: ISA Host generates TC for selected DMA Channel
  clear DMATC: Write "0" to bit 1 of STATUS1.

- **INT -** This flag indicates that an interrupt has been generated by this board to the ISA Host. An interrupt must be selected for this bit to function.

  INT = 0: No interrupt has been generated
  INT = 1: An interrupt was generated

  set INT: (see below)
  clear INT: Write "0" to bit 0 of STATUS1

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The following is a list of all available interrupt sources and what is necessary to enable these interrupts in addition to selecting an interrupt level:

Interrupt Condition	STATUS flag	Selected by Enabled by	Special Conditions
FIFO not Empty	FNE→1	FIMD = 0	DMA disabled
FIFO Half Full	FHF→1	FIMD = 1	DMA disabled
ADC FIFO Overflow	OVF	FFEN = 1	none
Timer A0 Terminal Count	A0TC	always	8254 Mode 0
Timer A2 Terminal Count	A2TC	TIEN = 1	8254 Mode 0
DMA Terminal Count	DMATC	always	DMA enabled
Digital Port 2 Overflow	D2ERR	D2IEN = 1	none
Digital Port 2 Strobe	STB2	S2IEN = 1	none
Digital Port 3 Underflow	D3ERR	D3IEN = 1	none
Digital Port 3 Strobe	STB3	S3IEN = 1	none

4.4.9 BLENGTH Base + 08_H Burst Length Register (8-bit) (Read/Write)

This register is used to set the number of samples to take in each burst when burst mode is enabled.

Bit assignments for the BURST register are as follows:

7	6	5	4	3	2	1	0
BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **BL7** through **BL0** select the number of samples per burst as follows: # Samples per Burst = BLn+ 1 = 1 to 256

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4.4.10 BRATE Base + 09_H Burst Rate Register (8-bit) (Read/Write)

This register is used to set the speed of the burst clock when burst mode is enabled. In Burst mode sampling, the burst clock sets the time between samples within a burst and the Pacer clock sets the time between bursts.

Bit assignments for the BURST register are as follows:

7	6	5	4	3	2	1	0
0	0	BR5	BR4	BR3	BR2	BR1	BR0

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **0 -** These bits are not used.
- **BR5** through **BR0** select the burst clock rate as follows:

  Burst Clock Frequency (Hz) = 1MHz ÷ (BR_N + 1)

4.4.11 SADDR Base + $0A_H$ Gain/Channel Starting Address (8-bit) (Read/Write)

This register is used to control and configure the Gain/Channel RAM. Writing to this address performs a dual function. It sets the Starting Address value of the G/C RAM and it sets the value of the G/C RAM address pointer.

To fill a specific location in the G/C RAM write the desired address to this location and then write the desired value to the G/C RAM data register. Note that each time the G/C RAM is written to, the G/C address pointer decrements by one. Thus to fill the G/C RAM set this register to the highest necessary value and then write all the data to the G/C RAM data register.

To view a specific location in the G/C RAM, write the designated RAM address to this register and then read the G/C RAM DATA register. The G/C RAM address pointer does not change when the G/C RAM data register is read.

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After each A/D conversion completes, the G/C RAM address counter is decremented and the new gain and channel data is used for the next conversion. Once the G/C RAM address counter reaches Zero, the next address will be the Starting address written to this register.

To perform conversions on a single channel set the SADDR register to 00_H and set the G/C RAM DATA register to the desired channel.

Bit assignments for the SADDR register are as follows:

7	6	5	4	3	2	1	0
SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **SA7** through **SA0** sets the C/G RAM Starting address and the C/G RAM address counter to any value in the range 0 to 255.

4.4.12 STATUS2 Base + $0B_H$ Error/Trigger/Reset Status (8-bit) (Read/Write)

This register provides access to the auxiliary error flags associated with the ADC function and the digital input functions. Additionally this register reports status of several board conditions. Each of these flags are set automatically by a specific condition except the RESET control bit. With the exception of the READY and RESET flags, all bits can be cleared by writing a "0" the associated bit position.

Bit assignments for the STATUS2 register are as follows:

7	6	5	4	3	2	1	0
RESET	STB2	GATE	READY	D2ERR	0	BERR	CERR

This register powers up with all bits = 0 except RESET and STB2.

The bit names are defined and used as follows:

- **RESET -** This bit may be used to reset all on-board registers. When a 0 is written to this bit all on-board functions are stopped and all registers are reset. This bit must then be set = 1 to allow the board to be programmed.

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On 16 bit boards, the ADC will perform a self calibration each time the board is reset. This calibration will take about 50 milliseconds to complete. The READY flag will set after the calibration process is done

RESET = 0: Board is held in reset state.
RESET = 1: Board is not held in reset state.

write 0: Reset all board registers to power-up state.
write 1: Enable registers for programming.

- **STB2 -** This bit indicates that new data has been strobed into Digital Port 2. This bit may be cleared either by reading the digital Port 2 or by writing a 0 to this flag. Note that when software only strobes are selected, this flag will always read 1 (new data is always available).

  STB2 = 0: No data at digital port 2.
  STB2 = 1: New data strobed into digital port 2.

  set STB2: Strobe received on digital port 2.
  clear STB2: Write "0" to bit 6 of STATUS2 or read DIO2.

- **GATE -** This flag indicates the state of theADC pacer clock gating function. Whenever gate/trigger function is selected, this bit will reflect whether the selected clock source is gated ON or OFF.

  Note: If the clock bus is the selected source, this flag is only useful on the clock master board. Ignore this bit on the slave board.

  GATE = 0: Selected Pacer source is gated OFF.
  GATE = 1: Selected Pacer source is gated ON.

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- **READY -** This bit indicates that the board is ready for a new clock. This flag will clear if conversions are disabled (CVEN = 0), if the front end is settling following a gain/channel change, if the ADC is in the midst of a conversion, or if burst mode is enabled and the burst is still in process. This flag cannot be changed by writing to it directly. This flag is most useful in conjunction with the CONVERT command. The CONVERT command should not be used until this flag is active.

  READY = 0: The ADC is busy: doing conversion, or burst of conversions , or front end is settling, or ADC is disabled.
  READY = 1: The ADC is ready to receive a new clock.

- **D2ERR -** This flag indicates an input overflow has occurred on Digital Port 2. This flag will set if a Digital Port 2 strobe is received while the STB2 flag is still set indicating the data from a prior strobe was overwritten.

  D2ERR = 0: no error
  D2ERR = 1: Digital Port 2 Overflow error occurred.

  set D2ERR: Digital Port 2 was strobed before old data was read.
  clear D2ERR: Write "0" to bit 3 of STATUS2.

- **0 -** This bit always returns 0.

- **BERR -** This flag indicates a burst error has occurred. A burst error will be flagged if a PACER clock is received while a burst of conversions is still running. If this flag set either the PACER clock rate must be decreased, the BURST Rate must be increased, or the BURST Length must be decreased.

  BERR = 0: no error
  BERR = 1: A Burst Error occurred.

  set BERR: Burst trigger received before previous Burst completed.
  clear BERR: Write "0" to bit 1 of STATUS2.

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- **CERR -** This flag indicates a clocking error has occurred. A clock error will be flagged if an ADC clock is received while the ADC is in the process of a conversion or too soon after the gain/channel setting was updated. Essentially this flag will set if a clock is received while the READY flag is not set and conversions are enabled.

  CERR = 0: no error.
  CERR = 1: A clock error has occurred.

  set CERR: An ADC clock is received when ADC Is not ready.
  clear CERR: Write "0" to bit 0 of STATUS2.

4.4.13 Counter/Timer A Base + $0C_H$ through Base + $0F_H$ (8-bit) (Read/Write)

This register set access an Intel 82C54 timer/counter chip. This device comprises four consecutive bytes of the register map, starting at Base + $0C_H$. Refer to Appendix B or the Intel data sheet for information on programming this device.

The Timer chip A consists of three 16-bit down counters. Each of these counters is dedicated to a specific function as follows:

Timer	Function	Base Clock	Interrupt	Interrupt Status
A0	Conversion Counter	ADC Conversion Clock	YES	A0TC
A1	Base Clock for Timer A2	5 MHz	NO	
A2	ADC Pacer Clock	Timer A1 OUT	YES	A2TC

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4.4.14 DIO2 Base + 10_H Digital Port 2 (INPUT) (16-bit) (Read)

This register is used to access the 16-bit Digital Input Port. This register may only be accessed as a 16-bit access. Digital Port 2 is available at the auxiliary DIO connector.

Input data is strobed into a holding latch by one of several modes. The strobe source is selected in CONTROL7. Once a strobe is received, the STB2 flag in STATUS2 is set. The latched data is accessed by reading this register. After the register is read, the STB2 flag clears until the next strobe.

Note that if software strobes are selected, no strobes are generated and the STB2 flag will always remain set. Each access to this register will return the current state of the digital input lines (instead of the holding register).

Bit assignments for the DIO2 register are as follows:

15	14	13	12	11	10	9	8
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

7	6	5	4	3	2	1	0
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

The bit names are defined and used as follows:

- **DI15** through **DI0** represent the contents of the digital input holding register. These bits reflect the logic levels currently present on the 16 lines of digital Input Port 2. These lines are all pulled to +5V by a 10 kΩ resistor. Any unconnected lines will read back "1".

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4.4.15 DIO3 Base + 12_H Digital Port 3 (OUTPUT) (16-bit) (Read/Write)

This register is used to access the 16-bit Digital Output Port. This register may written to as a 16-bit access. Digital Port 3 is available at the auxiliary DIO connector.

Output data is stored in a holding register until strobed onto the Port Lines by one of several modes. The strobe source is selected in CONTROL7. Once a strobe is received, the STB3 flag in STATUS4 is set. The data in the holding register may be accessed by reading this register. After this register is written to, the STB3 flag clears until the next strobe.

Note that if software strobes are selected, writing this register automatically generates a strobe for the byte or word accessed. STB3 will always remain set in this case.

Bit assignments for the DIO3 register are as follows:

15	14	13	12	11	10	9	8
DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

7	6	5	4	3	2	1	0
DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

The bit names are defined and used as follows:

- **DO15** through **DO0** represent the contents of the digital output holding register. If STB3 is high, these bits reflect the logic levels which are currently being driven out on the 16 lines of digital Output Port 1. Writing a "1" to any bit will cause the associated output line to drive out a TTL/CMOS high level. Writing a "0" to any bit will cause the associated output line to drive out a TTL/CMOS low level. Reading these bits will return the value currently in the digital output holding register.
  These bits (and their associated lines) power up driving out TTL/CMOS low level.

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4.4.16 CONTROL6 Base + 16_H DAC Config (8-bit) (Read/Write)

This register controls the DAC input configuration as well as the on-board Pacer clock modes.

Bit assignments for the CONTROL6 register are as follows:

7	6	5	4	3	2	1	0
U/B	2C	0	0	0	0	0	0

This register powers up with all bits = 0.

The bit names are defined and used as follows:

- **U/B -** This bit selects the output offset configuration (Unipolar or Bipolar) of both DACs.

  U/B = 0: Sets the DAC outputs to Bipolar (±10V FSR).
  U/B = 1: Sets the DAC outputs to Unipolar (0 to 10V FSR).

- **2C -** This bit selects the data coding for both DAC0 and DAC1. When set the data coding is two's complement (valid only for Bipolar mode). When this bit is clear, the data coding is straight binary for unipolar operation and offset binary for bipolar operation.

  2C = 0: DAC data coding is straight or offset binary.
  2C = 1: DAC data coding is 2's complement.

- **0 -** These bits are not used.

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4.4.17 CONTROL7 Base + $1A_H$ Digital I/O Strobe Control (8-bit) (Read/Write)

This register is used to control the strobe functions of the Digital I/O Ports.

Bit assignments for the CONTROL7 register are as follows:

7	6	5	4	3	2	1	0
S3IEN	D3IEN	D3SS1	D3SS0	S2IEN	D2IEN	D2SS1	D2SS0

This register powers up with all bits = 0.

The bit names are defined and used as follows

- **S3IEN -** This bit is used to enable an interrupt when data is strobed out onto DIO3. An interrupt will be sent whenever interrupts are enabled and STB3 = 1 (STATUS4).

  S3IEN = 0: Interrupt on STB3 Strobe disabled
  S3IEN = 1: Interrupt on STB3 Strobe enabled

- **D3IEN -** This bit is used to enable an interrupt when a data error occurs on DIO3. An interrupt will be sent whenever interrupts are enabled and D3ERR = 1 (STATUS4).

  D3IEN = 0: Interrupt on D3ERR Error disabled
  D3IEN = 1: Interrupt on D3ERR Error enabled

- **D3SS1 -** This bit selects the source for DIO3 strobe. When software only strobe is selected, the data is automatically strobed onto the output lines when the DIO3 register is written to. In this case STB3 (STATUS4) will remain set.

The following table shows how these bits are used:

D3SS1	Description
0	Software Strobe Only
1	ADC pacer (falling edge Timer A2 out)

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- **D3SS0 -** This bit selects the active edge of the strobe output for DIO3. The active edge is the trailing edge of the data strobe. The data is output on the leading edge and guaranteed valid on the active (trailing edge). The following table shows how these bits are used:

D3SS0	Description
0	Rising active edge Port 3 strobe output
1	Falling active edge Port 3 strobe output

- **S2IEN -** This bit is used to enable an interrupt when data is strobed into DIO2. An interrupt will be sent whenever interrupts are enabled and STB2 = 1 (STATUS2).

  S2IEN = 0: Interrupt on STB2 Strobe disabled
  S2IEN = 1: Interrupt on STB2 Strobe enabled

- **D2IEN -** This bit is used to enable an interrupt when a data error occurs on DIO2. An interrupt will be sent whenever interrupts are enabled and D2ERR = 1 (STATUS2).

  D2IEN = 0: Interrupt on D2ERR disabled
  D2IEN = 1: Interrupt on D2ERR enabled

- **D2SS1, D2SS0 -** These bits select the source for DIO2 strobe. When software only strobe is selected, reading the DIO2 data register will return the current state of input lines. In this case the STB2 strobe flag will always remain set.

The following table shows the function of these bits:

D2SS1	D2SS0	Description
0	0	Software Strobe Only
0	1	ADC pacer (falling edge Timer A2 out)
1	0	Rising edge Port 2 external strobe input
1	1	Falling edge Port 2 external strobe input

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4.4.18 STATUS4 Base + $1B_H$ DIO Port 3 / Error Status (8-bit) (Read/Write)

This register provides access to the status and error flags associated with the digital output functions. Each of these flags are set automatically by a specific condition. All bits can be cleared by writing a "0" to the associated bit position.

Bit assignments for the STATUS4 register are as follows:

7	6	5	4	3	2	1	0
0	STB3	0	0	D3ERR	0	0	0

This register powers up with all bits = 0 except STB3.

The bit names are defined and used as follows:

- **0 -** These bits are not used.
- **STB3 -** This bit indicates that data in DIO3 has been strobed onto its output lines. This bit may be cleared either writing to digital port 3 or by writing a 0 to this flag. Note that when software only strobes are selected, this flag will always read 1 (port always ready for new data).

  STB3 = 0: Data has not been strobed out DIO3.
  STB3 = 1: Data has been strobed onto DIO3.

  set STB3: Strobe received on DIO3.
  clear STB3: Write "0" to bit 6 of STATUS4 or write DIO3 register.

- **D3ERR -** This flag indicates an output underflow has occurred on Digital Port 3. This flag will set if a Digital Port 3 strobe is received while the STB3 flag is still set indicating that the DIO3 holding register was not updated before a new strobe occurred.

  D3ERR = 0: no error
  D3ERR = 1: DIO3 Underflow error occurred.

  set D3ERR: DIO3 was strobed before new data was written.
  clear D3ERR: Write "0" to bit 3 of STATUS4 or write to DIO3 register.

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5. SPECIFICATIONS

5.1 GENERAL (ALL MODELS)

Function	High level or wide range 8/16 channel multiplexed analog to digital converter with programmable gain, DMA, interrupts, and on-board ADC Counter/Timer. Also 40 lines Digital I/O and 2 optional 16-bit DACs. Full size, AT height, for PC compatibles
Bus Interface	The 5800 is designed to plug directly into any 16-bit ISA bus slot.

5.2 5801MF & 5802MF

5.2.1 Analog Inputs (5801MF and 5802MF)

Input Configuration	Software Selectable 8 Fully Differential 16 Single Ended 16 Pseudo Differential
Input Expansion	Up to 64 channels
Resolution	12 bit (2.4mV/bit on 0 to 10 V range)
Acquisition Rate:	
Single channel	
Any Gain	333 kHz max
Changing Channels	
Gain = ×1, ×2, ×4, ×8, ×10	333 kHz max
Gain = ×100, ×500	33 kHz max
A/D Full Scale Ranges (Jumper Selectable)	±10 V, 0 to 10 V

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Gain (Software Selectable)	
5801MF	×1, ×2, ×4, ×8
5802MF	×1, ×10, ×100, ×500
Input Range ADC Full Scale Range plus Input Gain:	
5801MF	±10 V, ±5 V, ±2.5 V, ±1.25 V, 0–10 V, 0–5 V, 0–2.5 V, 0–1.25 V
5802MF	±10 V, ±1 V, ±100 mV, ±20 mV, 0–10 V, 0–1 V, 0–100 mV, 0–20 mV
Differential Linearity	±3/4 LSB, no missing codes
Linearity:	±1/2 LSB
Gain Error:	Manually adjustable to Zero
Gain Drift:	±8 ppm/°C
Zero Error:	Manually adjustable to Zero
Zero Drift:	±2 ppm/°C
Signal to Noise and distortion: (S/N+D)	69 dB min @ gain = ×1
Total Harmonic Distortion:	80dB (typical) @ gain = ×1, measured to 5^{TH} harmonic
Full Power Bandwidth	200 kHz
Input Impedance:	
Shunt Res. to Ground	10 MΩ to ground
Shunt Capacitance	5 pF
Series Resistance	1 kΩ series

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Overvoltage Protection:	±35 V (powered) ±20 V (unpowered)
Acceptable Operating Limit Signal plus Common Mode	±12 V
Output Coding (Software Selectable) Unipolar Bipolar	 straight binary offset binary two's complement
Gain/Channel Selection	256 Element RAM
Data Format: Host (ISA)	 16-bit right justified
Data Storage:	1024 Word FIFO
Data Transfer Methods:	16-bit ISA bus access 16-bit DMA (ISA) 16-bit Dual DMA (ISA)

5.2.2 A/D Trigger (5801MF and 5802MF):

Clock Sources (Software Selectable):	- software - programmable pacer, 82C54 - user defined external TTL
Trigger Sources (Software Selectable):	- software - pacer 82C54 (Burst mode) - external (TTL)
Triggering Modes (Software Selectable)	- software gate - external gate - periodic burst - pre-trigger (sample until trigger) - post-trigger (sample after trigger) - around trigger (sample before and after trigger)

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5.2.3 D/A Outputs (5801MF and 5802MF):

Number of Outputs	2 (opt.)
Resolution	16 bit (0.15 mV/bit on 0 to 10V range)
D/A Full Scale Range (Software Selectable)	±10V, 0 to 10V
Settling Time to 0.0008%	13 µsec for 20V step 2.5 µsec for 1 bit step
Differential Linearity	±2 LSB @ 25° C monotonic 0 to 50° C
Linearity	± 2 LSB
Gain Error	Manually adjustable to Zero
Gain Drift	±25ppm of FSR/° C
Zero Error	Manually adjustable to Zero
Zero Drift Bipolar Unipolar	 ± 12ppm of FSR/° C ± 5ppm of FSR/° C
Data Coding (Software Selectable)	straight binary offset binary 2's complement
Data Format	16-bit Right justified on ISA bus
Data Storage	Single Word Latch
Data Transfer Methods	16-bit ISA bus access
DAC Clock Update Source	Update on write
Output Current	±5mA
Output Impedance (DC)	0.05

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Signal to Noise Ratio	83 dB
Total Harmonic Distortion	not specified – DACs for DC level only
Absolute Accuracy (DC)	±0.6 mV @ 25°C

5.3 5803HR & 5804HR

5.3.1 Analog Inputs (5803HR and 5804HR)

Number of Inputs	16 Single-ended 16 pseudo-differential 8 differential
A/D Expansion	Up to 64 channels external
Resolution	16 bit
Acquisition Rate:	
Single channel	
Any Gain	100 kHz max
Changing Channels	
Gain = ×1,×2	100 kHz max
Gain = ×4,×8,×10	50 kHz max
Gain = ×100	10 kHz max
Gain = ×500	1 kHz max
A/D Full Scale Ranges	±10 V
Programmable Gain (Software Selectable)	
High level (5803HR)	x1, x2, x4, x8
Low level (5804HR)	x1, x10, x100, x500
Full Scale Input Ranges (A/D Full Scale Range Plus Input Gain)	
5803HR	±10 V, ±5 V, ±2.5 V, ±1.25 V
5804HR	±10 V, ±1 V, ±0.1 V, ±20 mV
Differential Linearity	no missing codes
Linearity	± 1.5 LSB

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Gain Error	Adjustable to Zero
Gain Drift	±5 ppm/° C 0.0015% FSR
Zero Error	Adjustable to Zero
Zero Drift	0.0015% FSR
Signal to Noise and Distortion	(S/N+D) 87 dB min @ gain = 1, 83 ksps
Total Harmonic Distortion	97 dB (typical) @ gain = 1, measured to 5th harmonic
Full Power Bandwidth	200 kHz
Input Impedance	
Shunt Res. to Ground	10 M
Shunt Capacitance	5 pf
Series Resistance	300
Overvoltage Protection	±35 V (powered) ±20 V (unpowered)
Acceptable Operating Limit (Signal Plus Common Mode)	±12V
Output Coding (Software Selectable)	
Unipolar	straight binary
Bipolar	offset binary 2's complement
Gain/Channel Selection	256 element RAM
Data Format	16-bit Right justified on ISA bus
Data Storage	1024 Word FIFO to ISA
Data Transfer Methods	- 16-bit ISA bus access - 16-bit DMA (ISA) - 16-bit Dual DMA (ISA)

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5.3.2 A/D Trigger (5803HR and 5804HR):

Clock Sources (Software Selectable)	- software - programmable pacer, 82C54 - user defined external TTL
Trigger Sources (Software Selectable)	- software - pacer 82C54 (Burst mode) - external (TTL)
Triggering Modes (Software Selectable)	- software gate - external gate - periodic burst - pre-trigger (sample until trigger) - post-trigger (sample after trigger) - around trigger (sample before and after trigger)

5.3.3 D/A Outputs (5803HR and 5804HR):

Number of Outputs	2 (opt.)
Resolution	16 bit (0.15 mV/bit on 0 to 10V range)
D/A Full Scale Range (Software Selectable)	±10V, 0 to 10V
Settling Time to 0.0008%	13 µsec for 20V step 2.5 µsec for 1 bit step
Differential Linearity	±1 LSB, monotonic
Linearity	± 1 LSB
Gain Error	Manually adjustable to Zero
Gain Drift	±15ppm of FSR/° C
Zero Error	Manually adjustable to Zero
Zero Drift	
Bipolar	± 5ppm of FSR/° C
Unipolar	± 3ppm of FSR/° C

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Data Coding: (Software Selectable)	straight binary offset binary 2's complement
Data Format	16-bit right justified on ISA bus
Data Storage	Single Word Latch
Data Transfer Methods	- 16-bit ISA bus access
DAC Clock Update Source	Update on write
Output Current	±5mA
Capacitive Load	1000 pf max.
Signal to Noise Ratio	83 dB
Total Harmonic Distortion	not specified – DACs for DC level only
Absolute Accuracy (DC	± 0.3mV @ 25° C

5.4 DIGITAL INPUTS (ALL MODELS)

Number of Input lines	4 accessible from main I/O connector 16 accessible from auxiliary I/O connector
High Level Input Voltage Low Level Input Voltage	2 V min. 0.8V max.
High Level Input Current Low Level Input Current	20µA max (VIN= 2.4V) 200µA max (VIN= 0.4V)
Data Coding	positive logic
Data Storage	single word latch
Data Transfer Methods	- 8-bit ISA bus access - 16-bit ISA bus access
Clock Sources (Software Selectable)	- software read by ISA host - Timer A2 (ADC clock) - external (edge selectable)

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5.5 DIGITAL OUTPUTS (ALL MODELS)

Number of Output lines	4 accessible from main I/O connector 16 accessible from auxiliary I/O connector
High Level Output Voltage Low Level Output Voltage	2.4 V (15mA sourcing) 0.5 V (48mA sinking)
Data Coding	positive logic
Data Storage	single word latch
Data Transfer Methods	- 8-bit AT bus access - 16-bit AT bus access
Clock Source	software write
Output Strobe	TTL pulse

5.6 PHYSICAL & ENVIRONMENTAL (ALL MODELS)

Size	4.8”x 13.35”
Main I/O Connector	50-Pin “High Density D” (SCSI type 2 or 3)
Auxiliary Digital I/O Connector	Two 40 pin IDC headers
Temp. Range of Operation	0° C – 55° C
Power Requirements	+5V @ 2.2 Amps
CE Conformity	EN 55022 Class B EN 50082-1 IEC 801-2 IEC 801-3 IEC 801-4

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5.7 TERMINAL PANELS

The following specifications augment and/or replace the specifications defined for a particular product in the 5800 Series. Some terminal panels provide additional active circuitry which affects the specifications of the host board.

Specifications listed below replace those defined for the host board when a specific terminal panel is employed. It can be assumed that any specification not listed below remains unchanged when the particular panel is used.

5.8 TB5800-16

This panel simply brings each of the signals present on the 50-pin SCSI II connector out to a screw terminal mounted on the panel. There is no active circuitry on the board, and none of the specifications of the host board are affected by its use.

Size:	4.00”x 5.28”
Connector:	50-Pin “High Density D” (SCSI type 2 or 3)
Temp. Range of Operation:	0° C – 55° C
Power Requirements:	none

5.9 TB5800-64

This panel contains supplementary multiplexers which increase the total number of available analog inputs.

Input Configuration: (Software Selectable)	32 Fully-Differential 64 Single-Ended 64 Pseudo-Differential
Size:	5.80”x 5.28”
Connector:	50-Pin “High Density D” (SCSI type 2 or 3)
Temp. Range of Operation:	0° C – 55° C
Power Requirements:	40mA @ +5V in addition to host requirements

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5.10 TB5800-TC

This panel contains supplementary multiplexers which increase the total number of available analog inputs.

5.10.1 Host Board: 5801MF / 5401DMF

Input Configuration:	
High Level	
(Software Selectable)	7 Fully-Differential 14 Single-Ended
Low Level / Thermocouple	16 Fully-Differential
Acquisition Rate:	
Single channel	
Any Gain	333 kHz max
Changing Channels	
High Level	
Gain = ×1,×2,×4,×8	333 kHz max
Low Level / Thermocouple	
Gain = ×1,×2,×4,×8	10 kHz max

5.10.2 Low Level / Thermocouple Channels

A/D Full Scale Ranges: (Jumper Selectable)	±50mV, 0 to 50mV
Input Range: ADC Full Scale Range plus Input Gain	±50mV, ±25mV, ±12.5mV, ±6.25mV, 0–50mV, 0–25mV, 0–12.5mV, 0–6.25mV
Gain Error:	Manually adjustable to Zero
Gain Drift:	0.1% of reading over full temp range
Zero Error:	Manually adjustable to Zero
Zero Drift:	±100 ppm/°C

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Cold Juncton Compensation Error:	0.1° C
Cold Juncton Compensation Drift:	±1° C over full temp range
Open Thermocouple Detection:	+ Full Scale Reading

5.10.3 Physical / Environmental

Size:	5.80”x 5.28”
Connector:	50-Pin “High Density D” (SCSI type 2 or 3)
Temp. Range of Operation:	0° C – 55° C
Power Requirements:	340 mA @ +5V in addition to host requirements

5.10.4 Low Level Input Channels

Thermocouple Type	Compensation Rate
J	51.7 µV / °C
K,T	40.6 µV / °C
E	60.9 µV / °C
R,S	6.0 µV / °C

Table 5.1
Cold Junction Compensation Rates

Programmable Gain	Full Scale Range	Resolution 12 bit	Resolution 16 bit
×1	± 50 mV	24.4 µV / bit	1.53 µV / bit
×2	± 25 mV	12.2 µV / bit	0.76 µV / bit
×4	± 12.5 mV	6.1 µV / bit	0.38 µV / bit
×8	± 6.25 mV	3.0 µV / bit	0.19 µV / bit

Table 5.2
Low Level Millivolt Input

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Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 30 °C	Resolution 16 bit @ 30 °C
×1	-210 to 760	0.47 °C / bit	0.030 °C / bit
×2	-210 to 450	0.24 °C / bit	0.015 °C / bit
×4	-210 to 230	0.12 °C / bit	0.007 °C / bit
×8	-142 to 120	0.06 °C / bit	0.004 °C / bit

Table 5.3
Low Level Input Type J Thermocouple

Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 30 °C	Resolution 16 bit @ 30 °C
×1	-270 to 1,230	0.60 °C / bit	0.037 °C / bit
×2	-270 to 600	0.30 °C / bit	0.019 °C / bit
×4	-270 to 300	0.15 °C / bit	0.009 °C / bit
×8	-230 to 150	0.07 °C / bit	0.004 °C / bit

Table 5.4
Low Level Input Type K Thermocouple

Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 30 °C	Resolution 16 bit @ 30 °C
×1	*	*	*
×2	-270 to 400	0.29 °C / bit	0.018 °C / bit
×4	-270 to 250	0.14 °C / bit	0.009 °C / bit
×8	-230 to 140	0.07 °C / bit	0.004 °C / bit

Table 5.5
Low Level Input Type T Thermocouple

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Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 30 °C	Resolution 16 bit @ 30 °C
×1	-270 to 660	0.39 °C / bit	0.024 °C / bit
×2	-270 to 350	0.19 °C / bit	0.012 °C / bit
×4	-270 to 180	0.10 °C / bit	0.006 °C / bit
×8	-120 to 100	0.05 °C / bit	0.003 °C / bit

Table 5.6
Low Level Input Type E Thermocouple

Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 600 °C	Resolution 16 bit @ 600 °C
×1	*	*	*
×2	*	*	*
×4	0 to 890	0.54 °C / bit	0.033 °C / bit
×8	0 to 660	0.27 °C / bit	0.017 °C / bit

Table 5.7
Low Level Input Type R Thermocouple

Programmable Gain	Full Scale Range °C	Resolution 12 bit @ 600 °C	Resolution 16 bit @ 600 °C
×1	*	*	*
×2	0 to 1,760	1.20 °C / bit	0.075 °C / bit
×4	0 to 1,250	0.60 °C / bit	0.037 °C / bit
×8	0 to 690	0.30 °C / bit	0.019 °C / bit

Table 5.8
Low Level Input Type S Thermocouple

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E.5 TRICKS WITH THE TB5800-TC E-6

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A. ISOLATED DIGITAL I/O PANELS

A.1 PRODUCT OVERVIEW DIO SERIES

The DIO series of signal conditioning terminal panels incorporate high voltage isolation circuitry strategically located outside the PC to protect the sensitive computer circuitry from potentially harmful voltages and currents. Isolation panels are available in four varieties: ACI-EX, DCI-EX, ACO-EX and DCO-EX. All four panels provide 4000 VRMS isolation between the screw terminals and the PC.

ADAC's data acquisition boards with auxiliary digital I/O can support a single input panel and a single output panel. Note that any digital lines not supported by the signal conditioning panel will not be available if the panel is used. For example, the DIO panels do not support strobes, and the ACO panels only support 8 of the 16 DIO lines on each auxiliary digital I/O connector located on the data acquisition board.

A.2 INSTALLATION

A.2.1 Panel installation

The G16 cable installs inside the PC to connect each of the board's auxiliary digital I/O connectors to the rear of the PC. Two G16 cables are required to bring all the board's auxiliary DIO signals to the back of the PC. Each G16 cable requires an empty slot in the back or your PC to install. The DIO panel may then be connected directly to the 37-pin D-type connector, or a G37 cable may be used to remotely connect the panel to the PC. The following figure illustrates how a G16 cable is installed.

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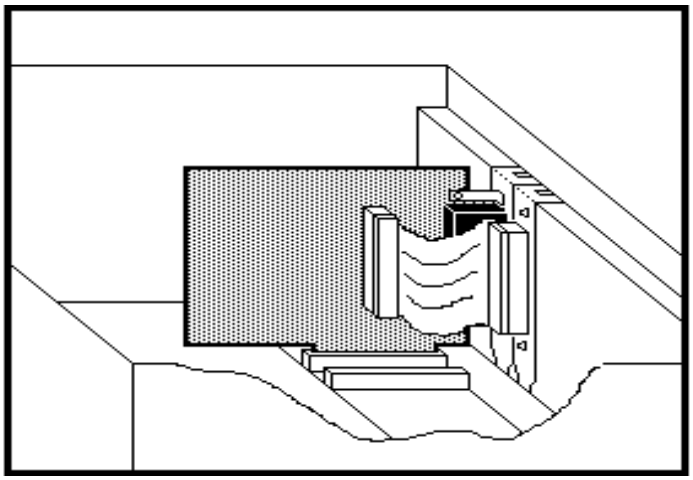


Figure A.1 G16 Cable Installation

It is important to note that input panels should only be connected to the data acquisition board's input port (DIO2) and output panels should only be connected to the data acquisition board's output port (DIO3). The following table indicates which panels are compatible with which ports.

Compatibility Chart				
Digital I/O Port (Board Connector)	**ACI-EX**	**DCI-EX**	**ACO-EX**	**DCO-EX**
DIO2 (J1)	•	•		
DIO3 (J2)			•	•

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A.3 ACI-EX

The ACI-EX is an 8 channel AC input voltage detection panel. This product is offered in two versions: The ACI-EX-120 to detect the presence of 90-150 VAC levels, and the ACI-EX-240 to detect the presence of 180-300 VAC levels.

The terminal panel provides 4000 VRMS optical isolation between AC voltages connected to the screw terminals, and the mating connector to the board inside the PC. Removable shield panels surround the terminal board to isolate the high voltage input signals from any adjacent panels or cables attached to the back of your PC.

Each AC input channel consists of an optical diode bridge which in turn drives an optical transistor. AC voltages are translated into TTL level pulse train which must be conditioned via software. The ACI panel operates with negative logic, meaning that the presence of AC voltages at the terminals is indicated by a "0" in the associated port bit.

The following diagram is representative of each of the eight input circuits on an ACI-EX panel.

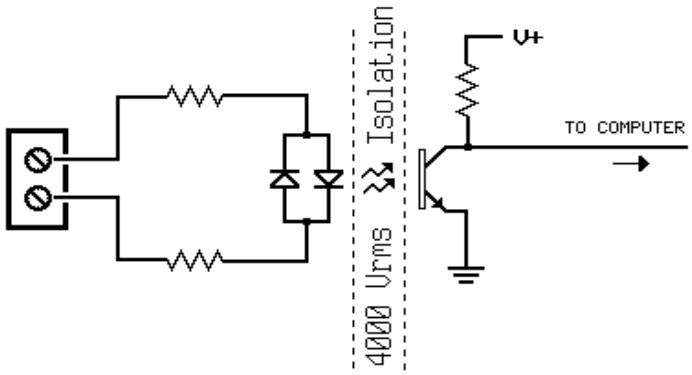


Figure A.2 Input Circuit Equivalent (1 of 8)

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A.3.1 Connecting To The ACI-EX

This panel allows measurement of 8 separate points, the inputs on each panel are numbered either 0 to 7. These numbers correspond to D0 through D7 in the auxiliary DIO port data bits (D8 through D15 on the port become unavailable). Each measurement point is represented as a single bit in one of the DIO port registers. The presence of AC voltages is represented by a "0" in the associated bit position. Note that an ACI-EX may only be connected to DIO2 (J1).

Each input point has a pair of (2) associated terminals. The polarity of these terminals is immaterial. To measure AC signals at a particular terminal pair, connect the HOT lead of your measurement source to one terminal and connect the COMMON or return of your source to the other terminal.

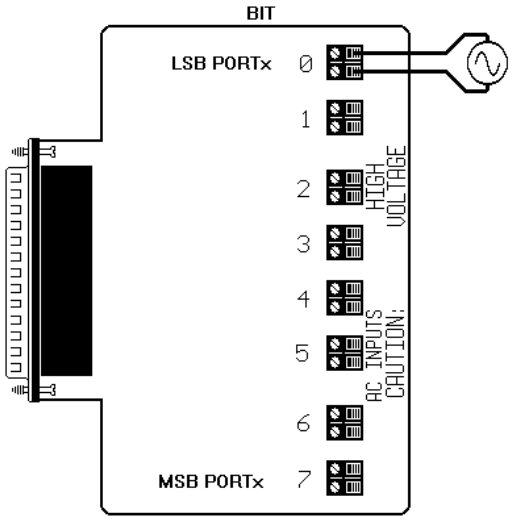


Figure A.3 AC Input Panel Connections

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A.4 ACO-EX

The ACO-EX is an 8 channel AC switching panel. This product may be used to switch AC or DC levels up to 240 VAC or 60 VDC.

The terminal panel includes 8 independent relays which provide 4000 VRMS mechanical isolation between AC voltages connected to the screw terminals, and the mating connector to the board inside the PC. Removable shield panels surround the terminal board to isolate the high voltage input signals from any adjacent panels or cables attached to the back of your PC.

Each AC output channel consists of a current switch which in turn activates a relay. The ACO panel operates with positive logic, meaning that relays are closed or turned ON by writing a "1" to the associated port bit. The following diagram is representative of each of the eight relay circuits on an ACO-EX panel:

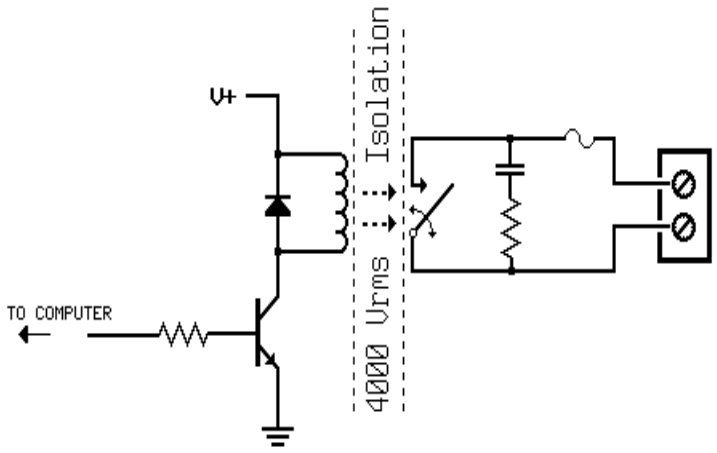


Figure A.4 AC Output Circuit Equivalent (1 of 8)

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A.4.1 Connecting to the ACO-EX

This panel provides 8 mechanical relay switches, the inputs on each panel are numbered either 0 to 7. These numbers correspond to D0 through D7 in the auxiliary DIO port data bits (D8 through D15 on the port become unavailable). Each relay is controlled by a single bit in one of the DIO port registers. If a "0" is written to a bit, the associated relay will turn OFF (OPEN). If a "1" is written to a bit, the associated relay will turn ON (CLOSE). An ACO-EX may only be connected to DIO3 (J2).

Each input point has a pair of (2) associated terminals. The polarity of these terminals is immaterial. Each terminal is connected to one lead of a relay. To switch AC signals at a particular terminal pair, connect the HOT lead of your AC Source to one terminal and connect the load you wish to switch to the other terminal. The COMMON or return of your source should be tied to the return side of your load.

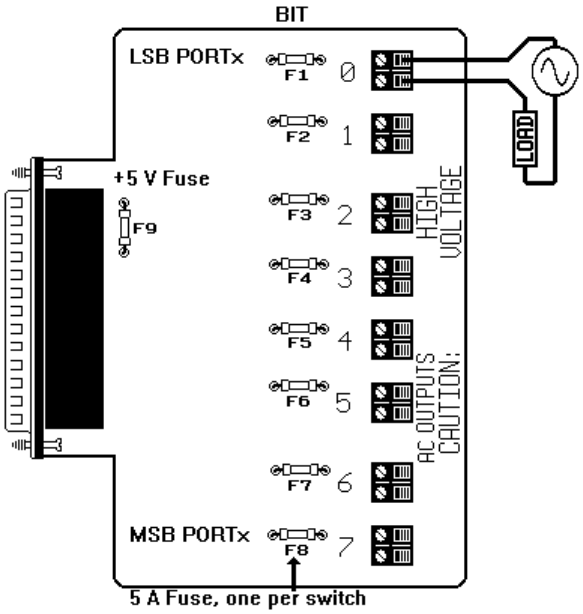


Figure A.5 AC Output Panel Connections

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A.5 DCI-EX

The DCI-EX is a 16 channel DC input voltage detection panel. This product is offered in two versions: the DCI-EX-24 to detect the presence of 15 - 40 VDC levels, and the DCI-EX-48 to detect the presence of 30 - 60 VDC levels.

The terminal panel provides 4000 VRMS optical isolation between DC voltages connected to the screw terminals and the mating connector to the board inside the PC.

Each DC input channel consists of an optical diode which in turn drives an optical transistor. DC voltages are translated into a TTL level signal which is presented to the I/O module. The DCI panel operates with negative logic, meaning that presence of DC voltages at the terminals is indicated by a "0" in the associated port bit. The following diagram is representative of each of the sixteen input circuits on a DCI-EX:

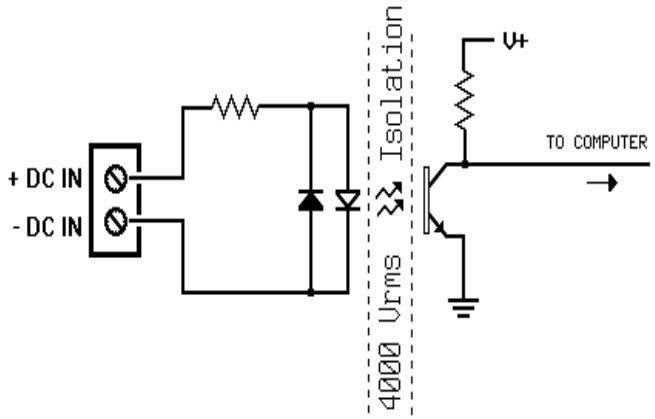


Figure A.6 DC Input Circuit Equivalent (1 of 16)

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A.5.1 Connecting To The DCI-EX

This panel allows measurement of 16 separate points. The inputs on each panel are numbered 0 to 15, corresponding to D0 through D15 in the auxiliary DIO port data bits. Each measurement point is represented as a single bit in one of the DIO port registers. The presence of the specified DC voltages is represented by a "0" in the associated bit position. A DCI-EX may only be connected to DIO2 (J1).

Each input point has a pair of (2) associated terminals. The polarity of these terminals is important. To measure DC signals at a particular terminal pair, connect the HOT (+) lead of your measurement source to the top terminal and connect the COMMON (-) or return of your source to the bottom terminal.

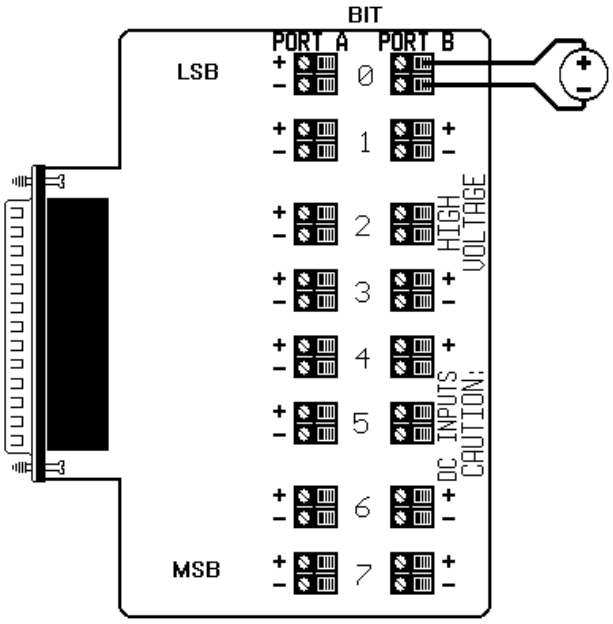


Figure A.7 DC Input Panel Connections

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A.6 DCO-EX

The DCO-EX is a 16 channel DC switching panel. This product may be used to switch DC levels up to 60 VDC, and may source up to 400 mA.

The terminal panel provides 4000 VRMS optical isolation between DC voltages connected to the screw terminals, and the mating connector to the board inside the PC.

Each DC output channel consists of an optical diode which in turn drives an optical transistor in a Darlington configuration. The DCO panel operates with positive logic, meaning that the output switches are closed or turned ON by writing a "1" to the associated port bit. The following diagram is representative of each of the sixteen transistor switch circuits on a DCO-EX expander panel.

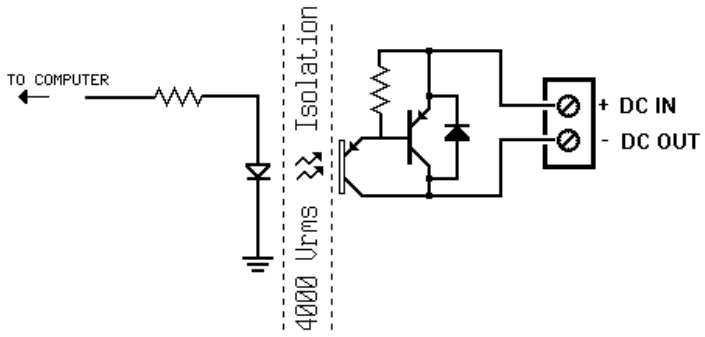


Figure A.8 DC Output Circuit Equivalent (1 of 16)

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A.6.1 Connecting To The DCO-EX

This panel provides 16 optically isolated switches. The inputs on each panel are numbered 0 to 15, corresponding to D0 through D15 in the auxiliary DIO port data bits. Each switch is controlled by a single bit in one of the DIO port registers. If a "0" is written to a bit, the associated switch will turn OFF (OPEN). If a "1" is written to a bit, the associated switch will turn ON (CLOSE). A DCO-EX may only be connected to DIO3 (J2).

Each input point has a pair of (2) associated terminals. The polarity of these terminals is important. To switch DC voltages at a particular terminal pair, connect the HOT (+) lead of your DC source to the top terminal and connect the load you wish to switch to the bottom terminal. The COMMON (-) or return of your source should be tied to the return side of your load.

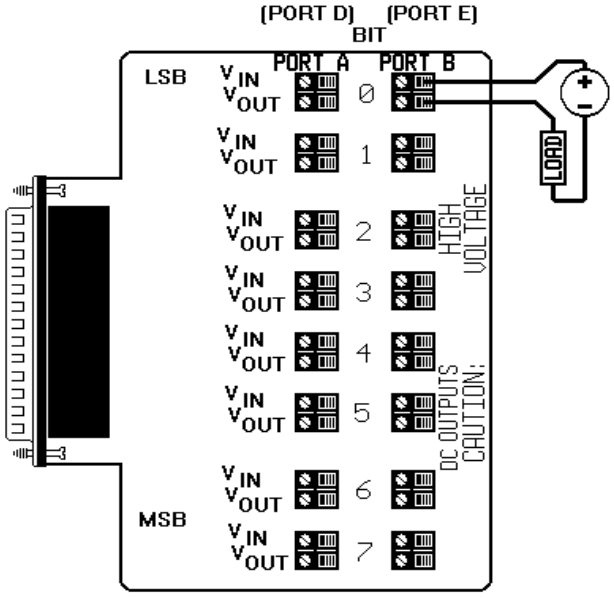


Figure A.9 DC Output Panel Connections

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A.7 SPECIFICATIONS

ACI-EX	
General :	
Bits	8
Type	AC Detection 120VAC or 240VAC
Port Direction	Input
Debounce	Must be performed in software
Input Characteristics:	
Minimum Voltage Detected	
120 V Option	90VAC
240 V Option	180VAC
Maximum Voltage for no Detect	
120 V Option	60VAC
240 V Option	120VAC
Detect Presence:	12.5 msec
Detect Absence:	12.5 msec
Isolation:	
Type	Optical
4000V RMS	Any terminal to computer
1500V RMS	Channel to channel

ACO-EX	
General :	
Bits	8
Type	RELAY, AC/DC Switching
Port Direction	Output
Output Characteristics:	
LOGIC LEVEL	INPUT LEVEL
0 =>>	Switch Opened
1 =>>	Switch Closed
Maximum Switch Voltage	250VAC, 60V DC
Maximum Switch Current	5A
Maximum Switch Power	
Resistive Load	AC: 550VA, DC 120W
Inductive Load	AC: 220VA, DC 48W

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Rated Load	
Resistive Load	AC: 110V 5A, DC: 24V 5A
Inductive Load	AC: 110V 2A, DC: 24V 2A
Minimum Applicable Load (Reference Value)	5V DC, 1 mA
Contact Resistance	50 mΩ max
Operate Time	7 msec max
Release Time	4 msec max
Bounce Time	6 msec max

Isolation:

Type	Mechanical
4000V RMS	Any terminal to computer
1500V RMS	Channel to channel

DCI-EX

General:

Bits	16
Type	DC Detection 24V DC or 48V DC
Port Direction	Input

Input Characteristics:

	-24 Option	**-48 Option**
Maximum Operating Voltage:	40V DC	60V DC
Minimum Voltage Detected:	15V DC	30V DC
Maximum Voltage for no Detect:	2.5V DC	4.5V DC
Typical Threshold:	8V DC	17V DC
Detect Presence:	2 µsec	2 µsec
Detect Absence:	20 µsec	20 µsec

ISOLATION

Optical	
4000V RMS	Any terminal to computer
750V RMS	Channel to channel

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DCO-EX

General:

Bits	16
Type	DC Switch
Port Direction	Output

Output Characteristics:

LOGIC LEVEL	**INPUT LEVEL**
0 =>>	Switch Opened
1 =>>	Switch Closed
Maximum Switch Voltage	60V DC
Maximum Switch Current	400 mA
Voltage Drop Through Switch	1.2 V max
Operate Time	2 µsec
Release Time	20 µsec

ISOLATION:

Type	Optical
4000V RMS	Any terminal to computer
750V RMS	Channel to Channel

PHYSICAL & ENVIRONMENTAL (all models)

Size of Terminal Panels:	5.40" x 4.50" x 0.75"
Connector	37 pin standard "D" sub-miniature socket brought to outside of PC. Mates with ITT/Cannon DC-37P or equivalent on mating screw terminal panel.
Screw Terminals	Clamping terminals accept 14-22 AWG (all models) wire.
Temperature Range of Operation	0 to 55 °C.
Power Consumption	add 325 mA for AC Output Panel, add 625 mA for DC Output Panel.

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B. PROGRAMMABLE INTERVAL TIMER (PIT)

B.1 THEORY OF OPERATION

The Programmable Interval Timer (PIT) utilizes an Intel 8254 type integrated circuit which provides three independent 16 bit counters, each of which can be programmed to operate in one of six modes. The function of each counter is set by writing a control word specifying the mode, count loading sequence, and selection of binary or BCD (binary coded decimal) counting.

B.1.1 Counter Control

The counter chip is accessed via four registers. One register is dedicated to each of the three counters (0, 1, and 2) and the fourth register is a universal control register (TCTRL) used to program all counter functions.

Each counter is programmed by writing a control word to TCTRL followed by writing the initial count value to the individual counter register. Bits 6 and 7 of TCTRL (SC0 and SC1) determine which counter the control word is directed at. Bits 4 and 5 (RL0 and RL1) control the Read/Load Mode of the specified counter (high byte, low byte etc.). Bits 1, 2, and 3 set the mode for the specified counter (modes 0 through 5). The final bit (BCD, bit 0) determines whether the counter will operate in Binary or BCD counting mode.

The counter is not activated until after the initial counter value is written (one or two bytes dependent on RL0 and RL1, bits 4 and 5 of the CSR). The counter will count down from the initial count to zero (terminal count). Writing an initial count of 0 will be interpreted as the maximum initial count of 216 for binary counting or 104 for BCD counting.

After power-up, the mode, count value, and output of the counters are undefined until programmed. It is not necessary to program unused counters.

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B.1.2 Counter Status

There are several types of status information which can be made available by reading the counter registers. This includes present count status, counter output level, load status, and programmed mode. All information pertaining to a given counter is accessed through its counter register (TIMER0..2). To determine which information is desired, a special control word must be written to the control register. The following is a breakdown of the available status modes for each of the counters.

B.1.2.1 Direct Read

A Direct Read to one of the three counter registers will return the current count of that counter. The clock line to the selected counter must be inhibited during a read to avoid false values due to reading a changing count. The current mode of the counter will determine how many, and which bytes of the counter will be made accessible.

B.1.2.2 Counter Latch Command

If it is not desirable to disable the clock input, the current state of a given counter can be latched by writing a control word, and then read back through the counter register. To latch the current count, write to the control register with the following format: Bits 6 and 7 (SC0 and SC1) select the desired counter, and bits 4 and 5 (RL0 and RL1) = 00. All other bits will be ignored. The counter is then read to access the latched information. Once read, the counter will automatically revert to Direct Read Mode (above). If multiple Counter Latch Commands are written, only the first is effective. Subsequent Counter Latch Commands are ignored until the counter register is read.

B.1.2.3 Read Back Command

This command makes available all information about a given counter. The format of this command written to the control register is as follows. Bits 6 and 7 (SC0 and SC1) = 11. If bit 5 is set, the specified counter(s) will latch the current count status. If bit 4 is set the programmed mode of the counter is latched. (Both bits may be set). Setting bits 3, 2, and 1 determine which counter(s) (counters 2, 1, and 0 respectively) will be affected by the command. Bit 0 is ignored. To retrieve the status information, simply read the counter register(s).

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The format of the status word is as follows. Bit 7 indicates state of counter output. Bit 6 if set, indicates counter has not been loaded yet, if clear, count is available to be read. Bits 5 through 0 indicate the mode originally programmed into the counter (RL1, RL0, M2, M1, M0, BCD respectively).

As with multiple COUNTER LATCH commands, only the first status latch command to a counter will be effective; others are ignored unless there is an intervening read. When both count and status are latched for a counter (regardless of which was latched first), the first read to that counter will return the status followed by the latched count in one or two reads (depending on how the counter was programmed). Additional reads will return an unlatched count (See Direct Read Section B.1.2).

B.1.3 Pit Operating Modes

This Section defines the six possible modes of operation for the PIT.

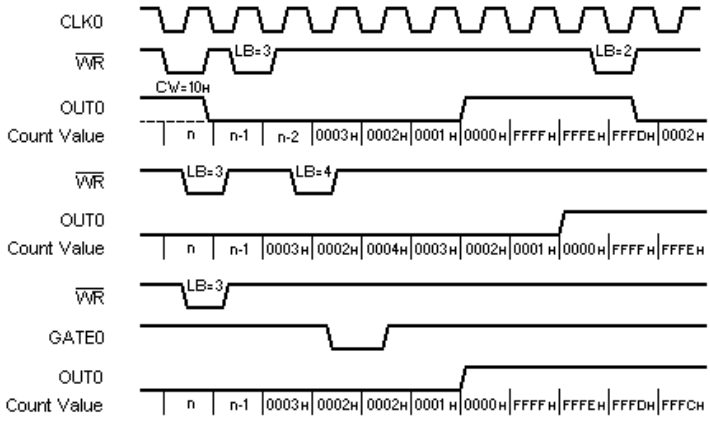
In the following descriptions, a clock pulse is defined as a rising edge, followed by a falling edge, of the counter clock input.

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MODE 0 - STOP ON TERMINAL COUNT (USED FOR EVENT COUNTING)

After the control word is written, the output will go low and remain low until the terminal count is reached. Terminal Count occurs N + 1 (N = Value loaded into count register) clock pulses after the control word and initial count are written. The first clock pulse after set-up loads the counter and does not decrement the count. Therefore, if a value of 9 is written to the count register after writing the Mode Zero control word, that counter's output will remain low for 10 clock pulses before going high at terminal count. Writing the first byte of a new count will disable counting and set the output low. Writing the second byte or a single byte load (or a new control word), restarts the sequence.

Pulling the gate enable line low will suspend counting. If a new count of N is written while the gate is low, it is loaded into the counter on the next clock pulse. When the gate subsequently goes high, Terminal Count is reached after N clock pulses (Not N+1).

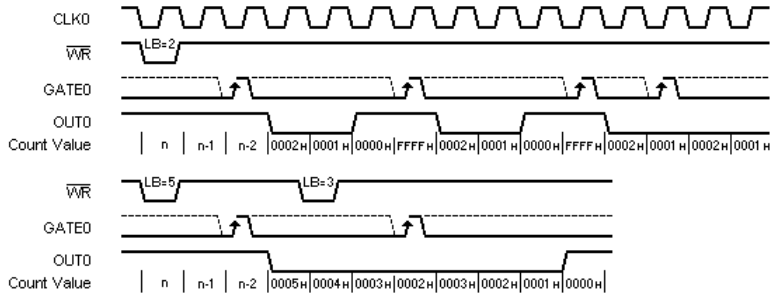


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MODE 1 - HARDWARE RETRIGGERABLE ONE SHOT

After the control word and initial count (N) are written, the counter is armed, and the output is high. A rising edge of the gate enable line triggers the counter, and the output goes low on the falling edge of the next clock pulse. The output will stay low for N clock pulses unless retriggered. When retriggered, timing begins again on the next clock pulse at the original count value. The gate input is used only to trigger the counter and has no direct effect on the output.

A new count can be written to the counter during a one-shot pulse (output low) without affecting the pulse duration. However, the next trigger (gate rising edge) will restart timing at the new count value.

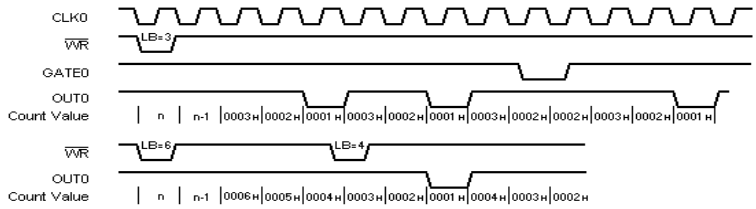


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MODE 2 - RATE GENERATOR (USED AS ADC CLOCK)

Mode 2 is similar to a divide by N counter. After the control word and initial count (N) are written, the next clock pulse loads the counter. The output is initially high, goes low for one clock period after N-1 additional clock pulses, and repeats every N clock pulses. Bringing the gate enable low disables counting; a low output is immediately reset high. The rising edge of the gate input restarts the sequence from a count of N at the next clock pulse. Thus, the counter can be synchronized to an external event by either hardware (the gate input) or software (by writing the control word and initial count).

Writing a new count has no affect on the counting sequence until the new count is loaded into the counter at the end of the sequence, or at the next clock pulse following a rising edge of the gate input. For this operating mode, N=1 is not permitted.

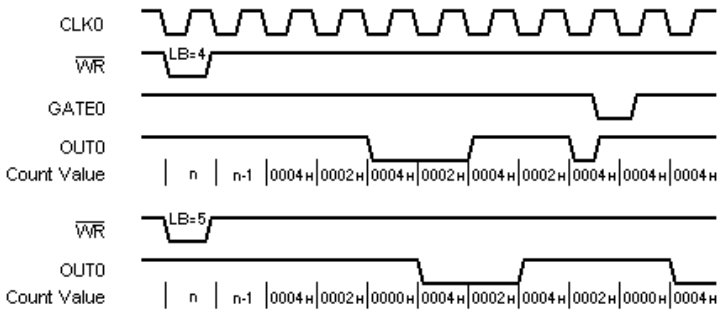


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MODE 3 - SQUARE WAVE GENERATOR

Mode 3 is identical to Mode 2 except for duty cycle of the output. For an even count input (N) the output will be high for (N/2) clock pulses and low for (N/2) clock pulses. For an odd initial count the output will be high for (N+1)/2) clock pulses and low for ((N-1)/2) clock pulses. When using an odd count, the output will be high for one clock pulse longer than it is low.

A new count will be loaded into the counter at the end of the current half cycle, or at the next clock pulse following a rising edge of the gate input.

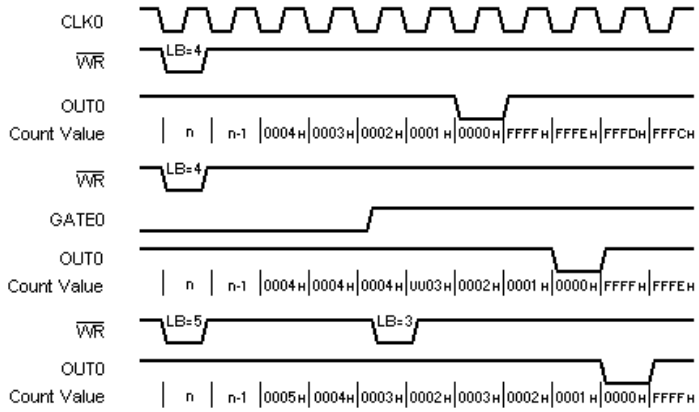


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MODE 4 - SOFTWARE TRIGGERED STROBE

Mode 4 is identical to Mode 0 except that the output remains high during counting, goes low N+1 clock pulses after the initial count (N) is written, remains low for the duration of one clock pulse, and returns high.

Pulling the gate enable line low will suspend counting, but has no effect on the output. Unlike Mode 0, writing the first byte of a new count has no effect on the output or on counting in process. Writing the second byte or a single byte load, permits the new count to be loaded on the next clock pulse, and the output will strobe low after N additional clock pulses (or a total of N+1 clock pulses after writing the second byte).

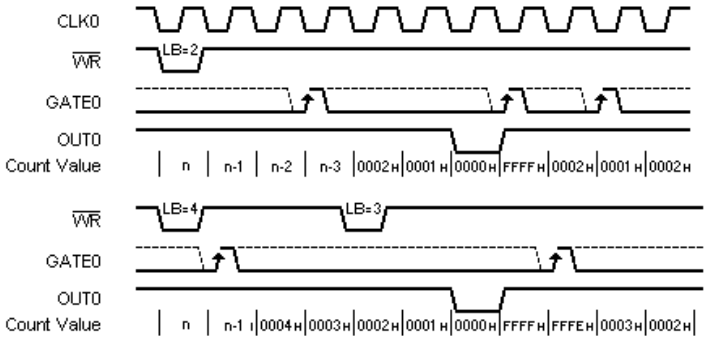


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MODE 5 - HARDWARE TRIGGERED STROBE, RETRIGGERABLE

Mode 5 is similar to Mode 4 except the gate enable input is used to trigger the counter. After writing the control word and initial count (N), the counter is armed, and the output is high. A rising edge of the gate input triggers the counter. The next clock pulse loads the counter, but does not decrement the count. After an additional N clock pulses (N+1 total), the output will go low for the duration of one clock pulse, and then return high. The counter is retriggerable; the output will not strobe low until N+1 clock pulses after the most recent trigger (gate rising edge).

Writing a new count has no effect on the counting sequence until followed by a gate trigger. Counting will then continue from the new count, with the output strobing low N + 1 clock pulses later (new value of N), unless retriggered.



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B.2 8254 REGISTER DESCRIPTIONS

B.2.1 TIMER0 (Read/Write) CTR Base Counter/Timer 0 Status & Data

This Register accesses data and status registers of Counter/Timer 0. The definition of these bits will vary depending on programming. If programmed for multiple functions, the first access will return the STATUS BYTE (if programmed), the next access will return the COUNTER LOW BYTE LATCHED (if programmed), and the last access will return the COUNTER HIGH BYTE LATCHED (if programmed). Once the latched status is read, this register returns the current state of the high and/or low byte of the counter (low byte first).

COUNTER 0 HIGH BYTE							
D07	D06	D05	D04	D03	D02	D01	D00
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8

Bit 7-0 CT15 - CT8 - High byte Counter Data (R/W)

Depending on how the PIT Control Register has been programmed, these bits can have several definitions. If programmed to access the high byte data, writing to these bits will set the starting count of the high byte of the counter. The control word must first be written to the control register followed by the high byte count to this register. If programmed to access the low byte only, these bits are automatically loaded with 00 Hex. Reading these bits will return either the current count of the high byte, or a previously latched count.

power up: undefined

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COUNTER 0 LOW BYTE							
D07	D06	D05	D04	D03	D02	D01	D00
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Bit 7-0 CT7 - CT0 - Low Byte Counter Data (R/W)

If programmed to access the Low Byte Data, writing to these bits will set the starting count of the low byte of the counter. The control word must first be written to the control register followed by the high byte count to this register. If programmed to access the high byte only, these bits are automatically loaded with 00 Hex. Reading these bits will return either the current count of the low byte, or a previously latched count.

power up: undefined

STATUS BYTE COUNTER 0							
D07	D06	D05	D04	D03	D02	D01	D00
OUT	NULL	RL1	RL0	M2	M1	M0	BCD

Bit 7 OUT - Counter Output Status (R/O)

This bit returns the status of the output for the counter. If set, the output is high, if clear, the output is low.

SET:	OUT = high
CLR:	OUT = low
power up:	undefined

Bit 6 NULL - Count Data Status (R/O)

This bit returns the status of the count data in the counter data registers. If set, this indicates a control word or new count has been written to the counter, but not yet loaded (NULL COUNT). If clear, count data is available.

SET:	Null Count
CLR:	Count Valid
power up:	undefined

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Bit 5-0 RL1,RL0,M2,M1,M0 - Mode Status (R/O)

These bits return the Programmed Mode of the register. They read-back the values programmed into the counter via the Register Control Word. Refer to Section B.2.4 for an explanation of these bits.

power up: undefined

B.2.2 TIMER1 CTR Base +1H (Read/Write)

Counter 1 Data/Status Register. (See Section B.2.1)

B.2.3 TIMER2 CTR Base +2H (Read/Write)

Counter 2 Data/Status Register. (See Section B.2.1)

B.2.4 TCTRL CTR Base +3H (Write Only)

This register controls all functions of the counter, including Count Mode, and Read-Back Mode. It has a basic bit definition supplemented by two special commands. The following describes all three formats.

PIT CONTROL WORD							
D07	D06	D05	D04	D03	D02	D01	D00
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Bit 7-6 SC1-SC0 - Counter Select (W/O)

These bits select which Counter is being addressed by the current control word according to the following:

SC1	SC0	PIT COUNTER SELECTED
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	READ-BACK Command

power up: undefined

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Bit 5-4 RL1-RL0 - Read/Load Mode Select (W/O)

These bits select which the Read/Load Mode for the selected counter (SC1,SC0) according to the following:

RL1	RL0	READ/LOAD MODE SELECTED
0	0	Counter Latch Command
0	1	Read/Load High Byte Only
1	0	Read/Load Low Byte Only
1	1	Read/Load Low Byte followed by High Byte

power up: undefined

Bit 3-1 M2, M1, M0 - Count Mode Select (W/O)

These bits select which Counter Mode will be assigned to the selected counter (SC1,SC0) according to the following (refer to Section B.1.2.3 for a discussion on Count Modes).

M2	M1	M0	COUNT MODE SELECTED
0	0	0	Mode 0 (Event Counter)
0	0	1	Mode 1 (H/W Triggered One shot)
0	1	0	Mode 2 (Rate Generator)
0	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (S/W Triggered Strobe)
1	0	1	Mode 5 (H/W Triggered Strobe)

power up: undefined

Bit 0 BCD - Count Format (W/O)

This bit defines the counting format of the selected counter (SC1,SC0). When Clear the counter counts as a 16 bit binary counter. When set, the counter counts in binary coded decimal (BCD, 4 Decades).

SET:	BCD Count (4 decades)
CLR:	Binary Count (16 bits)
power up:	undefined

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COUNTER LATCH COMMAND							
D07	D06	D05	D04	D03	D02	D01	D00
SC1	SC0	0	0	X	X	X	X

Bit 7-6 SC1, SC0 - Counter Select (W/O)

These bits select which Counter is being addressed by the current control word according to the following:

SC1	SC0	PIT COUNTER SELECTED
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	READ-BACK Command (See below)

power up: undefined

Bit 5-4 (0) - Always 0 for Counter Latch Command (W/O)

These bits distinguish the COUNTER LATCH Command from a normal CONTROL WORD. The addressed counter latches its current count in a special holding register. The stored data may be accessed by reading the selected counter's data register (see Section B.2.1). Once written to a given counter, all subsequent Counter Latch Commands are ignored until the latched counter data is read.

power up: undefined

Bit 4-0 Ignored

READ-BACK COMMAND							
D07	D06	D05	D04	D03	D02	D01	D00
1	1	COUNT/	STAT/	CT2	CT1	CT0	X

Bit 7-6 (1) - Always 1 for READ-BACK COMMAND (W/O)

These bits distinguish the READ-BACK Command from a normal CONTROL WORD.

power up: undefined

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Bit 5 COUNT/ - Latch Counter(s) (W/O)

When this bit is clear, a LATCH COUNTER Command is addressed to the counter(s) selected by bits 3-1 of this command word. Refer to LATCH COUNTER Command above for more information.

power up: undefined

Bit 4 STAT/ - Latch Status (W/O)

When this bit is clear, a LATCH STATUS Command is addressed to the counter(s) selected by bits 3-1 of this command word. The stored status data may be accessed by reading the selected counter's data register (see Section B.2.1). If multiple latch commands are issued to a given counter, the Status data byte is the first byte read.

power up: undefined

Bit 3-1 CNT2, CNT1, CNT0 - Counter Select (W/O)

These bits select which counter(s) the command is addressed to. Any combination of counters may be selected. Each bit, when set, selects the counter. CNT2 selects Counter 2, CNT1 selects Counter 1, and CNT0 selects Counter 0.

SET:	Address command to selected counter
CLR:	No action on selected counter
power up:	undefined

Bit 0 (X)

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C. PC CONFIGURATION MAPS

C.1 STANDARD PC I/O MAPS

PC/AT/386+	
I/O ADDRESS (HEX)	**DESCRIPTION**
000-0FF	Do not use
100-1EF	Uncommitted
1F0-1F8	Fixed Disk Controller
1F8-1FF	Rsvd by IBM
200-20F	Game Port
210-277	Uncommitted
278-27F	Parallel Printer Port 2 (LPT2:)
2E8-2EF	Serial Port 4 (COM4:)
2F0-2F7	Uncommitted
2F8-2FF	Serial Port 2 (COM2:)
300-31F	Prototype Card
320-35F	Uncommitted
360-36F	Reserved by IBM
370-377	Uncommitted
378-37F	Parallel Printer Port 1 (LPT1:)
380-38F	SDLC, Bisynchronous Port 2
390-39F	Uncommitted
3A0-3AF	Bisynchronous Port 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	EGA or VGA
3D0-3DF	Color Graphics Display Adapter (CGA)
3E0-3E7	Rsvd by IBM
3E8-3EF	Serial Port 3 (COM3:)
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1 (COM1:)

Table C.1
PC/AT/386 I/O Map

Shaded address ranges are **NOT** suggested base addresses for add-in boards.

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PC/XT	
I/O ADDRESS (HEX)	**DESCRIPTION**
000-0FF	Do not use
100-1FF	Uncommitted
200-207	Game Port
208-20F	Uncommitted
210-217	PC and XT expansion chassis
218-21F	Uncommitted
220-24F	reserved by IBM
250-277	uncommitted
278-27F	Parallel Printer Port 2 (LPT2:)
280-2EF	uncommitted
2F0-2F7	reserved by IBM
2F8-2FF	Serial Port 2 (COM2:)
300-31F	Prototype Card
320-32F	Fixed Disk Controller (XT)
330-377	uncommitted
378-37F	Parallel Printer Port 1 (LPT1:)
380-38F	SDLC Communications
390-39F	uncommitted
3A0-3AF	reserved by IBM
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Enhanced Graphics Display Adapter (EGA)
3D0-3DF	Color Graphics Display Adapter (CGA)
3E0-3EF	reserved by IBM
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1 (COM1:)

Table C.2
PC/XT I/O Map

Shaded address ranges are **NOT** suggested base addresses for add-in boards.

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C.2 STANDARD PC INTERRUPT USAGE

PC/AT/386+	
INTERRUPT REQUEST LEVEL	**DESCRIPTION**
highest priority	
NMI	I/O Channel Check / Parity Error
IRQ0	System Timer
IRQ1	Keyboard
IRQ2	Slave Interrupt Controller
IRQ8	Real-Time Clock
IRQ9	uncommitted (redirected to IRQ2)
IRQ10	uncommitted
IRQ11	uncommitted
IRQ12	uncommitted
IRQ13	Math Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	uncommitted
IRQ3	Serial Port 2 (COM2:)
IRQ4	Serial Port 1 (COM1:)
IRQ5	Parallel Port 2 (LPT2:)
IRQ6	Diskette Controller
IRQ7	Parallel Port 1 (LPT1:)
lowest priority	

Table C.3
PC/AT Interrupt Usage

Shaded Interrupts are unavailable or **NOT** recommended. Unshaded interrupts should be selected with care.

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PC/XT	
INTERRUPT REQUEST LEVEL	**DESCRIPTION**
highest priority	
NMI	I/O Channel Check / Parity Error
IRQ0	System Timer
IRQ1	Keyboard
IRQ2	uncommitted
IRQ3	Serial Port 2 (COM2:)
IRQ4	Serial Port 1 (COM1:)
IRQ5	Fixed Disk Controller
IRQ6	Diskette Controller
IRQ7	Parallel Port 1 (LPT1:)
lowest priority	

Table C.4
PC/XT Interrupt Usage

Shaded Interrupts are unavailable or **NOT** recommended. Unshaded interrupts should be selected with care.

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C.3 STANDARD PC DMA USAGE

PC/AT/386+	
DMA REQUEST LEVEL	**DESCRIPTION**
highest priority	
DRQ0	unused
DRQ1	uncommitted
DRQ2	Diskette Controller
DRQ3	SDLC
DRQ4	Slave DMA Controller
DRQ5	uncommitted
DRQ6	uncommitted
DRQ7	uncommitted
lowest priority	

Table C.5
PC/AT DMA Request Levels

PC/XT	
DMA REQUEST LEVEL	**DESCRIPTION**
highest priority	
DRQ0	Memory Refresh
DRQ1	uncommitted
DRQ2	Diskette Controller
DRQ3	Fixed Disk Controller
lowest priority	

Table C.6
PC/XT DMA Request Levels

***NOTE**: Many PCs use an SCSI hard disk controller which may use any of the above channels. Most ETHERNET cards have the option of using DMA Channels 1 or 3. Shaded request levels are unavailable or **NOT** recommended. Unshaded request levels should be selected with care.*

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D. 5800 CALIBRATION PROCEDURE

D.1 GENERAL

The 5800 is calibrated at the factory on the ±10 V and 0-10 V ranges and should require little or no recalibration for any of the available ranges. Calibration should only be attempted when a voltage standard of suitable accuracy is available. Occasionally, small calibration adjustments may be desirable to match the range of another instrument or to optimize the calibration over a particular portion of the full scale range.

Calibration should only be attempted after the board has warmed up (power applied) for a minimum of 5 minutes.

D.2 ADC CALIBRATION 5801MF & 5802MF

The following procedure applies to boards with 12-bit ADCs only. Adjustment interaction is avoided by calibrating offset first followed by range. The TB5800-16 is available as a convenient method of making the required connections for calibration.

BIPOLAR OFFSET ADJUSTMENT

The first adjustment does not require an input voltage. Instead, the input circuit is broken at the ADC and tied to ground. This is accomplished by temporarily moving a jumper.

1. Program 5800 board for the following parameters (CONTROL3, G/C RAM):

Input Offset	Bipolar
Gain	×1
Channel	Any available
Input Configuration	Single Ended

2. Move the jumper located next to P11 from TP2 (left) to TP1 (right).

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3. Perform a series of A/D conversions and adjust P8 until the output readings are steady at 0000_H.

ZERO ADJUSTMENT

At this point it is necessary to connect a voltage source to one of the input channels. The voltage source should be accurate to at least 1/4 LSB and should be have a fully floating output. Connect the plus (+) lead to one of the channel inputs, and connect the minus (–) lead to SGND (Signal Ground).

4. Program 5800 board for the following parameters:

Input Offset	Bipolar
Gain	×8 (5801MF)
Gain	×100 (5802MF)
Channel	Any available
Input Configuration	Single Ended

5. Move the jumper located next to P11 from TP1 (right) back to TP2 (left).

6. Set the voltage standard to 0.0000 V.

7. Perform a series of A/D conversions and adjust P11 until the output readings are again steady at 0000_H.

BIPOLAR RANGE ADJUSTMENT

Voltage is next set to 1/2 LSB below positive full scale.

8. Program 5800 board for the following parameters:

Input Offset	Bipolar
Gain	×1
Channel	Any available
Input Configuration	Single Ended

9. Set the voltage standard to 9.9927 V.

10. Perform a series of A/D conversions and adjust P10 until the output readings flicker evenly between are $07FF_H$ and $07FE_H$.

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UNIPOLAR OFFSET ADJUSTMENT

Next switch to Unipolar input range and set input voltage to 1/2 LSB above minus full scale.

11. Program 5800 board for the following parameters:

Input Offset	Unipolar
Gain	×1
Channel	Any available
Input Configuration	Single Ended

12. Set the voltage standard to 0.0012 V.

13. Perform a series of A/D conversions and adjust P7 until the output readings flicker evenly between are 0000_H and 0001_H.

UNIPOLAR RANGE ADJUSTMENT

Finally, set the input voltage to 1/2 LSB below full scale range.

14. Program 5800 board for the following parameters:

Input Offset	Unipolar
Gain	×1
Channel	Any available
Input Configuration	Single Ended

15. Set the voltage standard to 9.9963 V.

16. Perform a series of A/D conversions and adjust P9 until the output readings flicker evenly between are 0000_H and 0001_H.

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D.3 ADC CALIBRATION 5803HR & 5804HR

The following procedure applies to boards with 16-bit ADCs only. Adjustment interaction is avoided by calibrating offset first followed by range. The TB5800-16 is available as a convenient method of making the required connections for calibration.

OFFSET ADJUSTMENT

First it is necessary to connect a voltage source to one of the input channels. The voltage source should be accurate to at least 1/4 LSB and should be have a fully floating output. Connect the plus (+) lead to one of the channel inputs, and connect the minus (–) lead to SGND (Signal Ground).

1. Program 5800 board for the following parameters (CONTROL3,G/C RAM):

Gain	×4 (5803HR)
Gain	×10 (5804HR)
Channel	Any available
Input Configuration	Single Ended

2. Set the voltage standard to 0.0000 V.

3. Perform a series of A/D conversions and adjust P11 until the output readings are steady at 0000_H.

RANGE ADJUSTMENT

Voltage is next set to 3/4 full scale.

4. Program 5800 board for the following parameters:

Gain	×1
Channel	Any available
Input Configuration	Single Ended

5. Set the voltage standard to 7.5000V.

6. Perform a series of A/D conversions and adjust P12 until the output readings are steady at 6000_H.

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×2 / ×10 GAIN ADJUSTMENT

Next switch to the next higher gain and make a similar adjustment.

7. Program 5800 board for the following parameters:

Gain	×2 (5803HR)
Gain	×10 (5804HR)
Channel	Any available
Input Configuration	Single Ended

8. Set the voltage standard to 3.7500 V (5803HR) or 0.7500 V(5804HR).

9. Perform a series of A/D conversions and adjust P13 until the average output reading is 6000_H.

×4 / ×100 GAIN ADJUSTMENT

Next switch to the next higher gain and make a similar adjustment.

10. Program 5800 board for the following parameters:

Gain	×4 (5803HR)
Gain	×100 (5804HR)
Channel	Any available
Input Configuration	Single Ended

11. Set the voltage standard to 1.8750 V (5803HR) or 0.0750 V(5804HR).

12. Perform a series of A/D conversions and adjust P14 until the average output reading is 6000_H.

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×8 / ×500 GAIN ADJUSTMENT

Next switch to the next higher gain and make a similar adjustment.

13. Program 5800 board for the following parameters:

Gain	×8 (5803HR)
Gain	×500 (5804HR)
Channel	Any available
Input Configuration	Single Ended

14. Set the voltage standard to 0.9375 V (5803HR) or 0.0150 V(5804HR).

15. Perform a series of A/D conversions and adjust P15 until the average output reading is 6000_H.

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D.4 DAC CALIBRATION

The following procedure applies to boards with the optional 16 bit DACs installed. Adjustment interaction is avoided by calibrating offset first followed by range. The TB5800-16 is available as a convenient method of making the required connections for calibration.

BIPOLAR OFFSET ADJUSTMENT

First it is necessary to connect the DAC to a voltage meter. The meter should be accurate to at least 1/4 LSB. Connect the plus (+) input to the DAC output (DACnOUT), and connect the minus (–) input to the DAC return (DACnRET).

1. Program 5800 board for the following parameters (CONTROL6):
   Output Range Bipolar
   Data Coding 2's complement

2. Write 8000_H to the DAC0 and DAC1 data registers.

3. Adjust P2 until the voltage at DAC0 is –10.0000 V.

4. Adjust P5 until the voltage at DAC1 is also –10.0000 V.

RANGE ADJUSTMENT

Voltage is next set to Plus full scale.

5. Program 5800 board for the following parameters:
   Output Range Bipolar
   Data Coding 2's complement

6. Write $7FFF_H$ to the DAC0 and DAC1 data registers.

7. Adjust P3 until the voltage at DAC0 is +9.9997 V.

8. Adjust P6 until the voltage at DAC1 is also +9.9997 V.

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UNIPOLAR OFFSET ADJUSTMENT

Next set the unipolar offset.

9. Program 5800 board for the following parameters:
   Output Range Unipolar

10. Write 0000_H to the DAC0 and DAC1 data registers.

11. Adjust P1 until the voltage at DAC0 is +0.0000 V.

12. Adjust P4 until the voltage at DAC1 is also +0.0000 V.

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D.5 TB5800-TC CALIBRATION

This procedure should only be performed after the main ADC board has been accurately calibrated. A precision voltage source and temperature calibration meter is required.

Offset Adjust (P4)

Configure the ADC board for the ±10V two's complement input range (JP1-Bip, JP2-Bip).

Attach a voltage source to the channel input terminals as follows: connect positive (+) lead to TC0(+); connect the negative (-) lead to TC0(-).

Set the voltage source to 00.000 mV.

Perform a series of A/D conversions on the TC0 with the A/D gain set to **x8**. Do not enable cold junctions compensation on the main A/D board.

Adjust the offset pot (**P4**) until an ADC reading of 0000H is obtained.

NOTE: P1 *may be used to tune the offset if necessary.*

Gain Adjust (P2)

Set the voltage source (connected as described above) to 37.500 mV.

Perform a series of A/D conversion on TC0 with the A/D gain set to **x1**. Again, do not enable cold junction compensation.

Adjust the range pot (**P2**) until an ADC reading of 0600H is obtained (6000H for 16 bit board).

Cold Junction Compensation Adjust (P3)

Position a temperature calibration meter probe close to Q1 on panel.

Set the temperature calibration meter to read temperature in °C.

Set the voltage source (connected as described above) to 00.000 mV.

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Perform a series of A/D conversions on TC0 with the A/D gain set to **x8** and cold junction compensation **enabled**.

Adjust the range pot (**P3**) until the temperature reading matches the calibration meters source.

***NOTE**: It is helpful to shield the temperature sensor (Q1) from any drafts.*

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E. MIXED RATE SAMPLING USING THE CHANNEL/GAIN RAM

The 5400/5800 series of boards incorporate a 256 word RAM device which is used to pre-program the sequence of channels and gains to be sampled. The size of the list is programmable, and "random" (non sequential) sampling is possible. If for example you wish to sample channels 1, 3 and 6, simply set the list size to 3 elements and write these channels to the list. The board will automatically and repeatedly sample the specified channels, in the specified order. By applying the techniques of this application note, it is possible to take advantage of the RAM list and achieve different data rates on different channels in a single acquisition run.

E.1 AGGREGATE VS INDIVIDUAL CHANNEL SAMPLE RATE

Consider the following sample sequence for 4 inputs. If the ADC clock were set to 100 kHz, the ADC would perform an A/D conversion 100,000 times per second. Thus, the aggregate sample rate would be 100 **kilo-Samples per second** (**kS/s**). However, each individual channel is sampled once every fourth clock, so the individual channel sample rate would be 25 kS/s.

Sample #1	CH0
Sample #2	CH1
Sample #3	CH2
Sample #4	CH3

REPEAT...

Aggregate Sample Rate: 100 kS/s Individual Channel Sample Rate: 25 kS/s

Normally, in order to achieve a higher sample rate for an individual channel, it is necessary either to increase the overall sample speed of the ADC, or to decrease the number of channels sampled. For example with a 100 kS/s aggregate sample rate, it is possible to sample 1 channel at 100 kS/s, 2 channels at 50 kS/s, 4 channels at 25 kS/s, etc.

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E.2 MULTIPLE SAMPLE RATE REQUIREMENTS

Now, consider that only one channel actually needs to be sampled at a high rate, and the remaining channels only need some lesser rate. For example out of six channels, one needs to be sampled at 50 kS/s and the other five need only to be sampled at 10 kS/s. One way to handle this situation is to set the ADC clock to 300 kHz and set the gain list to sample each channel at 50 kS/s.

RAM List:

Sample #1	CH0
Sample #2	CH1
Sample #3	CH2
Sample #4	CH3
Sample #5	CH4
Sample #6	CH5

REPEAT ...

For the channels with the lower data rate requirement, only one sample in 5 is used, and the other 4 are thrown out. In the following table, the gray areas represent unneeded data. This will work, but it is inefficient, and uses up more system bandwidth than is necessary.

Sample #1	CH0
Sample #2	CH1
Sample #3	CH2
Sample #4	CH3
Sample #5	CH4
Sample #6	CH5
Sample #7	CH0
Sample #8	CH1
Sample #9	CH2
Sample #10	CH3
Sample #11	CH4
Sample #12	CH5
Sample #13	CH0
Sample #14	CH1
Sample #15	CH2
Sample #16	CH3
Sample #17	CH4
Sample #18	CH5
Sample #19	CH0
Sample #20	CH1

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Sample #21	CH2
Sample #22	CH3
Sample #23	CH4
Sample #24	CH5
Sample #25	CH0
Sample #26	CH1
Sample #27	CH2
Sample #28	CH3
Sample #29	CH4
Sample #30	CH5

REPEAT...

Shaded data is not used

Aggregate Rate: 300 kS/s

Sampling Requirements:

CH0	50 kS/s
CH1	10 kS/s
CH2	10 kS/s
CH3	10 kS/s
CH4	10 kS/s
CH5	10 kS/s

The following channel list is an alternative approach to achieving the same results as above. This approach runs the ADC at 1/3 the speed (and hence 1/3 the data bandwidth) of the previous example.

Sample #1	CH0
Sample #2	CH1
Sample #3	CH0
Sample #4	CH2
Sample #5	CH0
Sample #6	CH3
Sample #7	CH0
Sample #8	CH4
Sample #9	CH0
Sample #10	CH5

REPEAT...

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Aggregate Sample Rate: 100 kS/s	
Sample Rates:	
CH0:	50 kS/s
CH1:	10 kS/s
CH2:	10 kS/s
CH3:	10 kS/s
CH4:	10 kS/s
CH5:	10 kS/s

This technique can be used with the 256 element RAM list to achieve sampling rates with as diverse a rate ratio as 128:1.

E.3 MAXIMUM ACQUISITION RATE

The maximum Acquisition rate of the 5400/5800 Series boards varies depending on which board type and gain selection is in use. When sampling multiple channels at multiple gains, the **AGGREGATE SAMPLE RATE MUST NOT EXCEED THE MAXIMUM ACQUISITION RATE OF THE HIGHEST GAIN IN USE**.

For example, the maximum acquisition rate on a 5802MF when using the ×100 gain setting is 33 kS/s. If the channel / gain list from the above example were set up so that any of the channels were set for a gain of ×100, the aggregate sample rate should not exceed 33 kHz. This is true even if all channels use a gain of ×1 except CH1. CH1 has an individual rate of 10 kS/s in the above example, but the aggregate still violates the maximum sampling rate.

The reason for this limitation is because the max sampling rate is defined by the time it takes the front end circuitry to settle on a new channel. Each time a conversion starts, the ADC goes into hold mode and the channel/gain RAM is automatically incremented to select the next channel. The board then has the time from the start of the current conversion to the start of the next conversion to settle on a new channel. A max sample rate of 33 kS/s means the board needs 30 µseconds to settle on a new channel at that gain.

Refer to the user manual Specifications Section for more information on the maximum acquisition rate of your board.

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E.4 OVER SAMPLING TO INCREASE AGGREGATE LIMIT

This sounds like a contradiction, but it works. Consider the following setup. You have a 5802MF and need to sample 6 channels as fast as possible. Channels 0 and 1 are to be set to a gain of ×100 and the rest are to be set to ×1. The high gain channels have a maximum sampling rate of 33 kS/s. If this were used as the aggregate clock rate, the individual channel sample rate would work out as 5.5 kS/s.

However, as mentioned above, the real limitation is that when sampling the high gain channels, it is necessary to allow the front end circuitry to settle sufficiently once the channel/gain has been changed. In the case of a 33 kS/s limit, the board needs 30 µseconds (1/33,000). The following channel/gain list samples the same channel three times in a row to extend the settling time to 30 µseconds. This example uses a 100 kHz aggregate clock (which translates to 10 µsecond between samples. The first two data points on the high gain channels are ignored. The net result is a 10 kS/s individual channel rate.

Sample #1	CH0	×100
Sample #2	CH0	×100
Sample #3	CH0	×100
Sample #4	CH1	×100
Sample #5	CH1	×100
Sample #6	CH1	×100
Sample #7	CH2	×1
Sample #8	CH3	×1
Sample #9	CH4	×1
Sample #10	CH5	×1

REPEAT...

Grey Samples are ignored

Using a 5802MF
Aggregate Sample Rate: 100 kS/s

Sample Rates:

CH0:	10 kS/s
CH1:	10 kS/s
CH2:	10 kS/s
CH3:	10 kS/s
CH4:	10 kS/s

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E.5 TRICKS WITH THE TB5800-TC

The TB5800-TC is a special active circuitry terminal panel which introduces a 16 channel multiplexer and a second stage instrumentation amplifier which applies a gain of ×200 to the signal. The output of the multiplexer is fed into on-board channel 0. The remaining 7/14 (SE/DI) on-board channels are available as high level channels. The maximum sampling rate of the low level (Thermocouple) channels is 10 kS/s. If used with a 5801MF, the maximum sampling rate of the high level channels is 333 kS/s.

As in the above example, the 10 kS/s limit is due to the time required for the instrumentation amp to settle on a new channel. This means the panel requires 100 µseconds between when the channel is set and a conversion is initiated. The on-board channels are selected using the low byte (4 bits) of the channel RAM. The panel multiplexer is controlled by the next byte. Because of the way these two multiplexers are configured, the state of the panel multiplexer is a "don't care" when one of the high level channels is selected. Hence, it is possible to set the panel multiplexer and allow it to settle while sampling the on-board high level channels. This means the high level channel may be sampled at a higher rate.

The following sample RAM list illustrates this technique. Note that the TC channels (low level) multiplexer remains static for the required 100 µseconds before the low level channel is sampled by the ADC.

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	On Board Multiplexer Select Byte	PANEL Multiplexer Select Byte	Channel Selected	
Sample #1	1	0	CH1	
Sample #2	2	0	CH2	
Sample #3	1	0	CH1	
Sample #4	3	0	CH3	
Sample #5	1	0	CH1	
Sample #6	4	0	CH4	
Sample #7	1	0	CH1	
Sample #8	5	0	CH5	
Sample #9	1	0	CH1	
Sample #10	0	0	TC0	(Low Level)
Sample #11	1	1	CH1	
Sample #12	2	1	CH2	
Sample #13	1	1	CH1	
Sample #14	3	1	CH2	
Sample #15	1	1	CH1	
Sample #16	4	1	CH1	
Sample #17	1	1	CH1	
Sample #18	5	1	CH1	
Sample #19	1	1	CH1	
Sample #20	0	1	TC1	(Low Level)

REPEAT...

Aggregate Sample Rate: 100 kS/s

Sample Rates:

CH1:	50 kS/s
CH2:	10 kS/s
CH3:	10 kS/s
CH4:	10 kS/s
CH5:	10 kS/s
TC0:	5 kS/s
TC1:	5 kS/s

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