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Specifications: 5803/4HR

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General

Function:

High resolution, 16 channel multiplexed analog to digital converter with programmable gain, two optional digital to analog converters, and 40 digital I/O lines for IBM PC compatibles.

Bus Interface:

The 5800 Series plugs into the 16 bit (AT) PC ISA bus.

A/D Inputs

Number of Inputs (Software Selectable):

16 Single-ended
16 pseudo-differential
8 differential.

A/D Expansion: Up to 64 channels external

Resolution: 16 bit

Acquisition Rate:

Single Channel
Any Gain: 100kHz max
Changing Channels
Gain=x1, x2: 100kHz max
Gain=x4, x8, x10: 50kHz max
Gain=x100: 10kHz max
Gain=x500: 1kHz max

A/D Full Scale Ranges: $\pm 10V$

Programmable Gain (Software Selectable):

High level (5803HR)

x1, x2, x4, x8

Low level (5804HR)

x1, x10, x100, x500

Full Scale Input Ranges:

A/D Full Scale Range Plus Input Gain

5803HR

$\pm 10V, \pm 5V, \pm 2.5V, \pm 1.25V$

5804HR

$\pm 10V, \pm 1V, \pm 0.1V, \pm 20mV$

Differential Linearity: no missing codes

Linearity: ± 1.5 LSB

Gain Error: Adjustable to Zero

Gain Drift: ± 5 ppm/ $^{\circ}C$, 0.0015% of FSR

Zero Error: Adjustable to Zero

Zero Drift: 0.0015% of FSR

Signal to Noise and Distortion:

(S/N+D) 87 dB min.

@ gain = 1, 83 ksps

Total Harmonic Distortion:

97 dB (typical) @ gain = 1, measured to 5th harmonic

Full Power Bandwidth: 200 kHz

Input Impedance:

Shunt Res. to Ground

10 M ohm

Shunt Capacitance

5 pf

Series Resistance

300

Overvoltage Protection:

± 35 V (powered)

± 20 V (unpowered)

Acceptable Operating Limit:

Signal Plus Common Mode

± 12

Output Coding (Software Selectable):

Unipolar

Straight binary

Bipolar

Offset binary
2's complement

Gain/Channel Selection:
256 element RAM

Data Format:
16-bit right justified

Data Storage:
1024 word FIFO

Data Transfer Methods:
- 16-bit ISA bus access
- 16-bit DMA
- 16-bit Dual DMA

A/D Trigger

Clock Sources (Software Selectable):
- software
- programmable pacer, 82C54
- user defined external TTL

Trigger Sources (Software Selectable):
- software
- pacer 82C54 (Burst mode)
- external (TTL)

Triggering Modes (Software Selectable):
- software gate
- external gate
- periodic burst
- pre-trigger (sample until trigger)
- post-trigger (sample after trigger)
- around trigger (sample before and after trigger)

D/A Outputs

Number of Outputs: 2 (optional)

Resolution: 16 bit (0.15mV/bit on 0 to 10V range)

D/A Full Scale Range (Software Selectable):
 $\pm 10V$
0 to 10V

Settling Time to 0.0008%:
13 μ sec for 20V step
2.5 μ sec for 1 bit step

Differential Linearity: ± 1 LSB, monotonic

Linearity: ± 1 LSB

Gain Error: Manually adjustable to zero

Gain Drift: $\pm 15\text{ppm}$ of FSR/ $^{\circ}\text{C}$

Zero Error: Manually adjustable to zero

Zero Drift:

Bipolar

$\pm 5\text{ppm}$ of FSR/ $^{\circ}\text{C}$

Unipolar

$\pm 3\text{ppm}$ of FSR/ $^{\circ}\text{C}$

Data Coding:

(Software Selectable):

- straight binary

- offset binary

- 2's complement

Data Format: 16-bit right justified on ISA bus

Data Storage: Single word latch

Data Transfer Methods: 16-bit ISA bus access

DAC Clock Update Source: Update on write

Output Current: $\pm 5\text{mA}$

Capacitive Load (DC): 1000pf max.

Signal to Noise Ratio: 83 dB

Total Harmonic Distortion: Not specified \forall DACs for DC level only

Absolute Accuracy (DC):

$\pm 0.3\text{mV}$ @ 25°C

Digital Inputs

Number of Input lines:

4 accessible from main I/O connector

16 accessible from auxiliary I/O connector

High Level Input Voltage:

2 V min.

Low Level Input Voltage:

0.8V max.

High Level Input Current:

20 μA max ($V_{\text{IN}} = 2.4\text{V}$)

Low Level Input Current:

200 μA max ($V_{\text{IN}} = 0.4\text{V}$)

Data Coding: Positive logic

Data Storage: Single word latch

Data Transfer Methods:
8-bit ISA bus access
16-bit ISA bus access

Clock Sources: (Software Selectable):
- software read by ISA host
- Timer A2 (A/D clock)
- external (edge selectable)

Digital Outputs

Number of Output lines:
4 accessible from main I/O connector
16 accessible from auxiliary I/O connector

High Level Output Voltage: 2.4 V (15mA sourcing)

Low Level Output Voltage: 0.5 V (48mA sinking)

Data Coding: Positive logic

Data Storage: Single word latch

Data Transfer Methods:
8-bit AT bus access
16-bit AT bus access

Clock Source: Software write

Output Strobe: TTL pulse

Physical & Environmental

Size: 4.8"x 13.35"

Main I/O Connector: 50-Pin "High Density D" (SCSI Type 2 or 3)

Aux. Digital I/O Connectors: Two 40 pin IDC headers

Temp. Range of Operation: 0° C - 55° C

Power Requirements: +5v @ 2.2 Amps

CE Conformity

EN 55022 Class B
EN50082-1
IEC801-2
IEC801-3
IEC801-4

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