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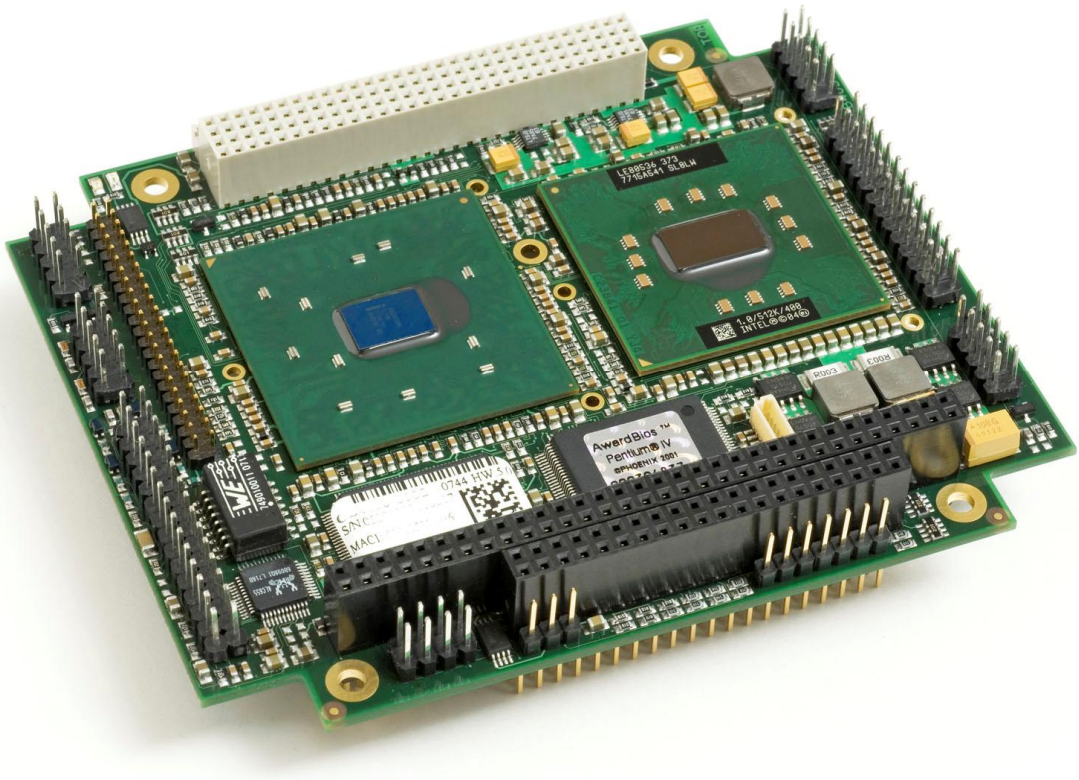
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ADL855PC

Manual

Revision 3.4



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0 Document History

Revision	Changes
0.9	first AuthorIT-managed version, many changes, e.g.: - new photographs (D5) - "merging" effort between several English versions - new connector symbols - several minor bugs corrected todo: update dimensional drawing
1.0	updated PCI table, minor changes
1.1	updated dimensional drawings
3.0	- new version number (older, pre-AIT versions had already reached 2.x) - added connector map - updated block diagram - updated temperature ranges - several small changes
3.1	updated contact details, minor changes
3.2	minor changes
3.3	added caution note regarding PS_ON, minor changes
3.4	improved output quality of dimensional drawings, minor changes



NOTE

All company names, brand names, and product names referred to in this manual are registered or unregistered trademarks of their respective holders and are, as such, protected by national and international law.

1 Introduction

1.1 Important Notes

Please read this manual carefully before you begin installation of this hardware device. To avoid Electrostatic Discharge (ESD) or transient voltage damage to the board, adhere to the following rules at all times:

- You must discharge your body from electricity before touching this board.
- Tools you use must be discharged from electricity as well.
- Please ensure that neither the board you want to install, nor the unit on which you want to install this board, is energized before installation is completed.
- Please do not touch any devices or components on the board.



CAUTION

As soon as the board is connected to a working power supply, touching the board may result in electrical shock, even if the board has not been switched on yet. Please also note that the mounting holes for heat sinks are connected to ground, so when using an externally AC powered device, a substantial ground plane differential can occur if the external device's AC power supply or cable does not include an earth ground. This could also result in electrical shock when touching the device and the heat sink simultaneously.

1.2 Technical Support

Technical support for this product can be obtained in the following ways:

- By contacting our support staff at +1 858-490-0597 or +49 (0) 271 250 810 0
- By contacting our staff via e-mail at support@adl-usa.com or support@adl-europe.com
- Via our website at www.adl-usa.com/support or www.adl-europe.com/support

1.3 Warranty

This product is warranted to be free of defects in workmanship and material. ADL Embedded Solutions' sole obligation under this warranty is to provide replacement parts or repair services at no charge, except shipping cost. Such defects which appear within 12 months of original shipment of ADL Embedded Solutions will be covered, provided a written claim for service under warranty is received by ADL Embedded Solutions no less then 30 days prior to the end of the warranty period of within 30 days of discovery of the defect – whichever comes first. Warranty coverage is contingent upon proper handling and operation of the product. Improper use such as unauthorized modifications or repair, operation outside of specified ratings, or physical damage may void any service claims under warranty.

1.4 Return Authorization

All equipment returned to ADL Embedded Solutions for evaluation, repair, credit return, modification, or any other reason must be accompanied by a Return Material Authorization (RMA) number. ADL Embedded Solutions requires a completed RMA request form to be submitted in order to issue an RMA number. The form can be found under the Support section at our website: www.adl-usa.com or www.adl-europe.com. Submit the completed form to support@adl-usa.com or fax to +1 858-490-0599 for the USA office, or to rma@adl-europe.com or fax to +49 (0) 271 250 810 20 to request an RMA from the European office in Germany. Following a review of the information provided, ADL Embedded Solutions will issue an RMA number.

1.5 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.



ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!



RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!



HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.



NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

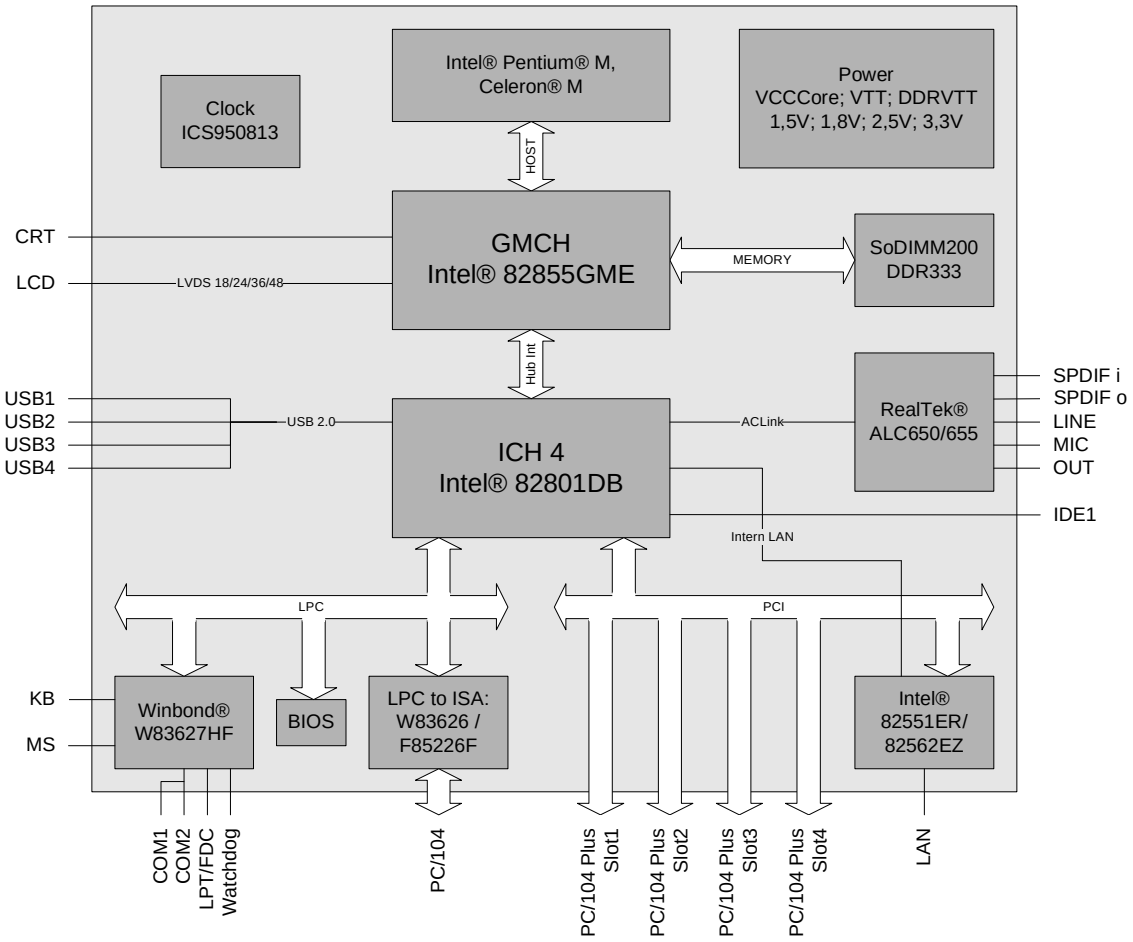
1.6 RoHS

The PCB and all components are RoHS compliant (RoHS = Restriction of Hazardous Substances Directive). The soldering process is lead free.

2 Overview

2.1 Features

The ADL855PC is a highly complex PC/104-Plus board with the functionalities of a motherboard. Standard features include an Intel® Pentium® M or Intel® Celeron® M CPU, up to 1 GByte RAM (DDR-333) via SoDIMM200, PCI (PC/104-Plus™) and ISA (PC/104™) bus connectors. The ADL855PC also has many additional onboard peripherals: two serial interfaces, one printer interface, floppy connection (via LPT port), LAN connection, Audio in and out, four USB interfaces, CRT and IDE connection.



- o Processor Intel® Celeron® M, Pentium® M
- o Chipset Intel® 855GME and Intel® ICH4
- o SoDIMM200 socket for up to 1 GByte RAM (DDR-333), capable of ECC
- o Two serial interfaces COM1 and COM2
- o One parallel interface LPT (also for floppy)
- o Ethernet 10/100 (Base-T)
- o IDE interface
- o PS2 keyboard / mouse interface
- o Four USB 2.0 interfaces
- o AWARD® BIOS 6.10
- o CRT connection
- o TFT connection, LVDS 18/24Bit (single and dual pixel displays)

- AC97 compatible sound controller with SPDIF in and out
- RTC with external CMOS battery
- 5V single supply voltage
- ISA bus via PC/104 connector
- PCI bus via PC/104-Plus connector
- Size 96 mm x 90 (115,5) mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation, the following documents, specifications and web-pages were used and are recommended.

- § ISA specification
  IEEE996P
  www.ieee.org
- § PC/104™ specification
  revision 2.5
  www.pc104.org
- § PC/104-Plus™ specification
  revision 2.0
  www.pc104.org
- § PCI specification
  revision 2.3 resp. 3.0
  www.pcisig.com
- § ACPI specification
  revision 3.0
  www.acpi.info
- § ATA/ATAPI specification
  version 7 rev. 1
  www.t13.org
- § USB specifications
  www.usb.org
- § SM-Bus specification
  revision 2.0
  www.smbus.org
- § Intel® chipset description
  855GM/GME Datasheet, Design Guide
  www.intel.com
- § Intel® chipset description
  ICH4 Datasheet
  www.intel.com
- § Intel® chip description
  Celeron® M, Pentium® M
  www.intel.com
- § Winbond® chip description
  W83627HF, W83626 Datasheet
  www.winbond-usa.com oder www.winbond.com.tw
- § Fintek® chip description
  F85226F Datasheet
  www.fintek.com.tw
- § Intel® chip description
  82562EZ Datasheet
  www.intel.com
- § Intel® chip description
  82551ER Datasheet
  www.intel.com
- § ICS® chip description
  ICS950813 Datasheet
  www.icst.com

3 Detailed Description

3.1 Power Supply

The power supply of the hardware module is effected via the power connector. The board only requires an operating voltage of 5 volt ± 5%.

3.2 CPU

The board can be ordered with one of the following processors employed: Intel® Celeron® M, Intel® Celeron® M ULV, Intel® Pentium® M. The package type allows a maximum DIE temperature of 100 degrees Celsius and accords highest possible security even in rough environment.
The processors include a second level cache of up to 2 MByte, depending on which model is used. Furthermore the processors offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.

3.3 Memory

There is one conventional SoDIMM200 socket available to equip the board with memory. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules.
With currently available SoDIMM200 modules a memory extension up to 1 GByte is possible (DDR-333).

4 Connectors

This section describes all the connectors found on the ADL855PC.

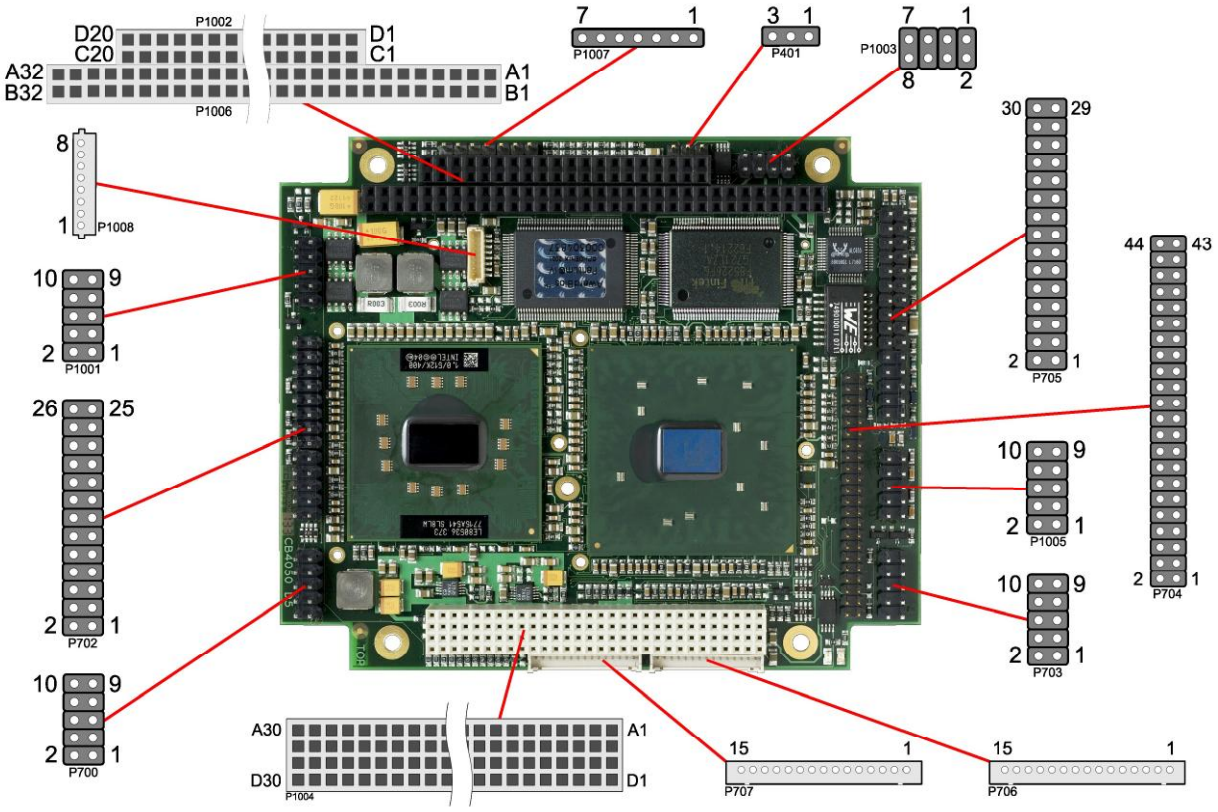


CAUTION

For most interfaces, the cables must meet certain requirements. For instance, USB 2.0 requires twisted and shielded cables to reliably maintain full speed data rates. Restrictions on maximum cable length are also in place for many high speed interfaces and for power supply. Please refer to the respective specifications and use suitable cables at all times.

4.1 Connector Map

Please use the connector map below for quick reference. Only connectors on the component side are shown. For more information on each connector refer to the table below.



Ref-No.	Function	Page
P401	"Fan"	p. 34
U403*	"Memory"	p. 16
P700	"Serial Interface COM1"	p. 30
P702	"Parallel Interface LPT"	p. 29
P703	"Serial Interface COM2"	p. 31
P704	"IDE Interface"	p. 28
P705	"USB 1 to 4, LAN, Sound"	p. 26
P706/7	"LCD"	p. 24
P1001	"System"	p. 15
P1002/6	"PC/104-Bus"	p. 19
P1003	"Power Supply"	p. 14
P1004	"PC/104-Plus Bus"	p. 21
P1005	"VGA"	p. 23
P1007	"SMBus"	p. 32
P1008	"Monitoring Functions"	p. 33

* not in the picture above (cf. bottom side of board)

4.2 Power Supply

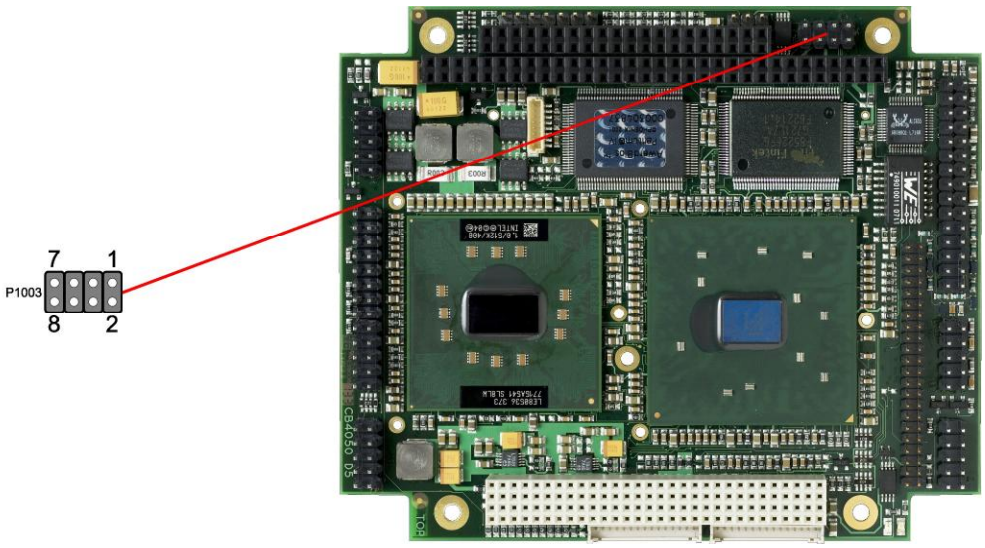
The connector for the power supply is a standard IDC socket connector with a spacing of 2.54 mm.
The board only requires an operating voltage of 5 volt ± 5%. 3.3V output to the PC/104-Plus bus is the only off-board supply available.
Should additional voltages be needed for PC/104 expansion cards, these must be provided externally by connecting the respective pins (see below).
For maximum current availability, it is recommended to use both this power connector and the PC/104 connector for power supply.

NOTE

For "Real Time Clock" an external battery (3.3V) must be connected. You can use pins 1 & 3 here or the "System" connector (see next page).

CAUTION

The ADL855PC includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is no longer pulled low, an intelligent power supply would take this as a signal to shut down power. For this to work, PS_ON# must be connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the ADL855PC can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.



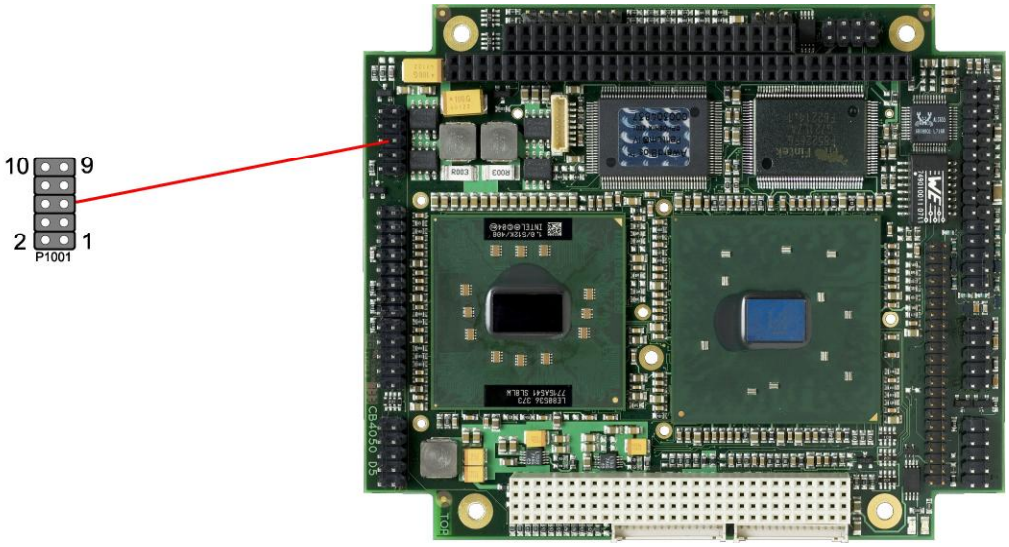
Description	Name	Pin		Name	Description
ground	GND	1	2	VCC	5 volt supply
CMOS battery >= 3 volt	VBAT	3	4	12V	12 volt supply
-5 volt supply	-5V	5	6	-12V	-12 volt supply
ground	GND	7	8	VCC	5 volt supply

4.3 System

The system connector, which has the main functions that are necessary to start the board, is provided via a standard IDC socket connector with a spacing of 2.54 mm.
This connector supports the following interfaces: PS/2 keyboard, PS/2 mouse, speaker, external RTC-battery and reset of the board.

NOTE

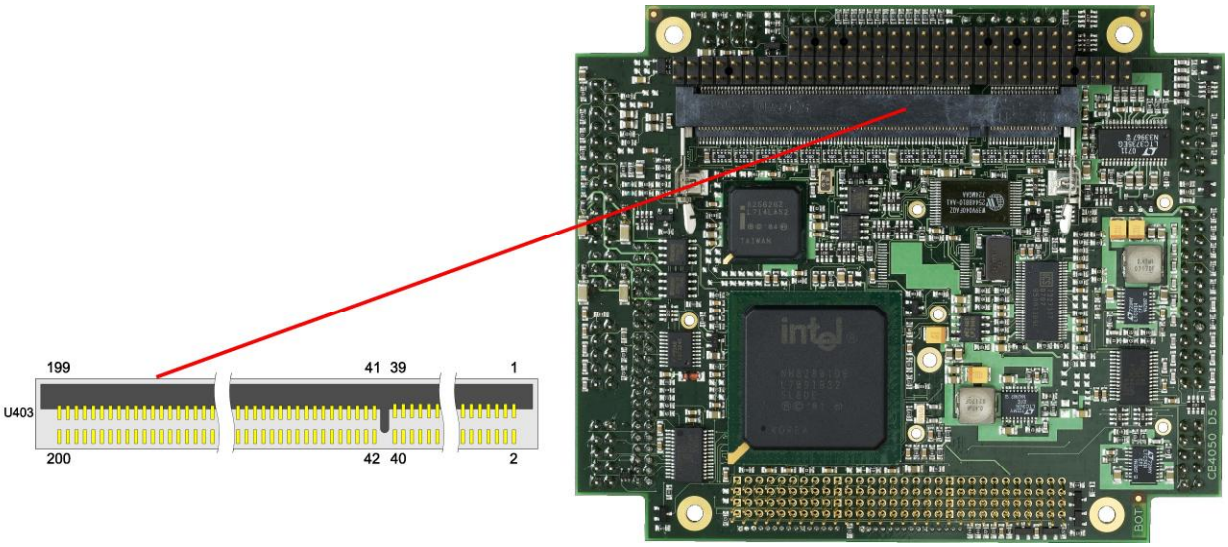
For "Real Time Clock" an external battery (3.3V) must be connected. Connect "+" to VBAT and "-" to GND.



Description	Name	Pin		Name	Description
speaker to 5 volt	SPEAKER	1	2	GND	ground
reset to ground	RESET#	3	4	KLOCK#	keyboard lock
keyboard Data	KDAT	5	6	KCLK	keyboard clock
mouse data	MDAT	7	8	MCLK	mouse clock
CMOS battery ≥ 3 volt	VBAT	9	10	VCC	5 volt supply

4.4 Memory

There is one conventional SoDIMM200 socket available to equip the board with memory (DDR-333). It is located on the bottom side of the board. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules.
With currently available SO-DIMM modules a memory extension up to 1 GByte is possible. The timing parameters for different memory modules are automatically set by BIOS.



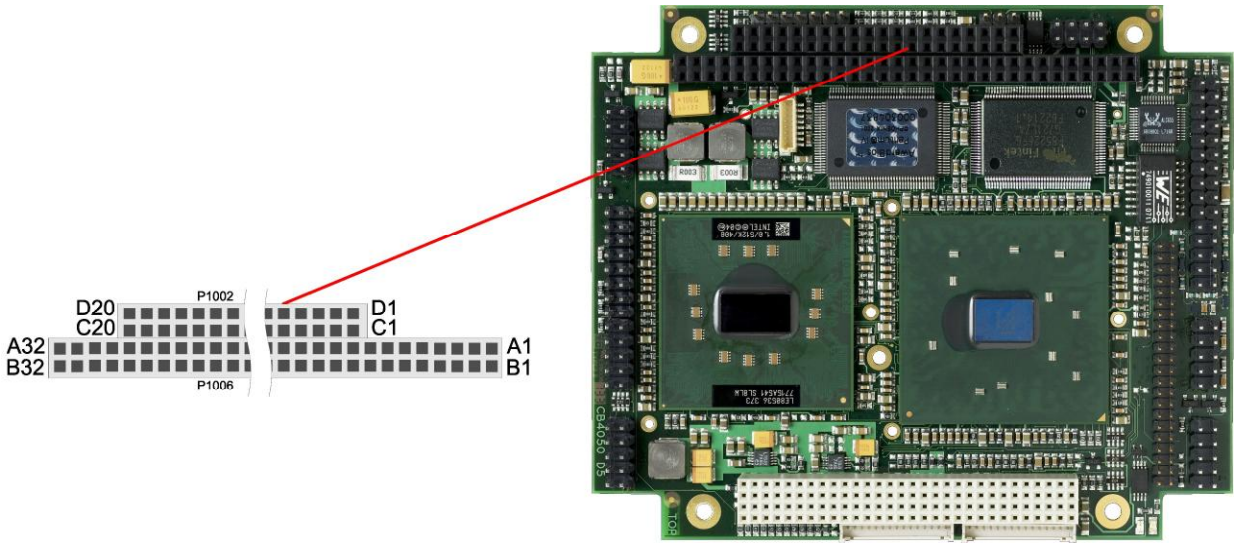
Description	Name	Pin		Name	Description
memory reference current	REF	1	2	REF	memory reference current
ground	GND	3	4	GND	ground
data 0	DQ0	5	6	DQ4	data 4
data 1	DQ1	7	8	DQ5	data 5
2.5 volt supply	2.5V	9	10	2.5V	2.5 volt supply
data strobe 0	DQS0	11	12	DQM0	data mask 0
data 2	DQ2	13	14	DQ6	data 6
ground	GND	15	16	GND	ground
data 3	DQ3	17	18	DQ7	data 7
data 8	DQ8	19	20	DQ12	data 12
2.5 volt supply	2.5V	21	22	2.5V	2.5 volt supply
data 9	DQ9	23	24	DQ13	data 13
data strobe 1	DQS1	25	26	DQM1	data mask 1
ground	GND	27	28	GND	ground
data 10	DQ10	29	30	DQ14	data 14
data 11	DQ11	31	32	DQ15	data 15
2.5 volt supply	2.5V	33	34	2.5V	2.5 volt supply
clock	CK0	35	36	2.5V	2.5 volt supply
clock	CK0#	37	38	2.5V	2.5 volt supply
ground	GND	39	40	GND	ground
data 16	DQ16	41	42	DQ20	data 20
data 17	DQ17	43	44	DQ21	data 21
2.5 volt supply	2.5V	45	46	2.5V	2.5 volt supply
data strobe 2	DQS2	47	48	DQM2	data mask 2
data 18	DQ18	49	50	DQ22	data 22

Description	Name	Pin		Name	Description
ground	GND	51	52	GND	ground
data 19	DQ19	53	54	DQ23	data 23
data 24	DQ24	55	56	DQ28	data 28
2.5 volt supply	2.5V	57	58	2.5V	2.5 volt supply
data 25	DQ25	59	60	DQ29	data 29
data strobe 3	DQS3	61	62	DQM3	data mask 3
ground	GND	63	64	GND	ground
data 26	DQ26	65	66	DQ30	data 30
data 27	DQ27	67	68	DQ31	data 31
2.5 volt supply	2.5V	69	70	2.5V	2.5 volt supply
data check bit 0	CB0	71	72	CB4	data check bit 4
data check bit 1	CB1	73	74	CB5	data check bit 5
ground	GND	75	76	GND	ground
data strobe 8	DQS8	77	78	DQM8	data mask 8
data check bit 2	CB2	79	80	CB6	data check bit 6
2.5 volt supply	2.5V	81	82	2.5V	2.5 volt supply
data check bit 3	CB3	83	84	CB7	data check bit 7
reserved	N/C	85	86	N/C	reserved
ground	GND	87	88	GND	ground
clock	CK2	89	90	GND	ground
clock	CK2#	91	92	2.5V	2.5 volt supply
2.5 volt supply	2.5V	93	94	2.5V	2.5 volt supply
clock enables 1	CKE1	95	96	CKE0	clock enables 0
reserved	N/C	97	98	N/C	reserved
address 12	A12	99	100	A11	address 11
address 9	A9	101	102	A8	address 8
ground	GND	103	104	GND	ground
address 7	A7	105	106	A6	address 6
address 5	A5	107	108	A4	address 4
address 3	A3	109	110	A2	address 2
address 1	A1	111	112	A0	address 0
2.5 volt supply	2.5V	113	114	2.5V	2.5 volt supply
address 10	A10	115	116	BA1	SDRAM bank 1
SDRAM bank 0	BA0	117	118	RAS#	row address strobe
write enable	WE#	119	120	CAS#	column address strobe
chip select	S0#	121	122	S1#	chip select
reserved	N/C	123	124	N/C	reserved
ground	GND	125	126	GND	ground
data 32	DQ32	127	128	DQ36	data 36
data 33	DQ33	129	130	DQ37	data 37
2.5 volt supply	2.5V	131	132	2.5V	2.5 volt supply
data strobe 4	DQS4	133	134	DQM4	data mask 4
data 34	DQ34	135	136	DQ38	data 38
ground	GND	137	138	GND	ground
data 35	DQ35	139	140	DQ39	data 39
data 40	DQ40	141	142	DQ44	data 44
2.5 volt supply	2.5V	143	144	2.5V	2.5 volt supply
data 41	DQ41	145	146	DQ45	data 45
data strobe 5	DQS5	147	148	DQM5	data mask 5
ground	GND	149	150	GND	ground
data 42	DQ42	151	152	DQ46	data 46
data 43	DQ43	153	154	DQ47	data 47
2.5 volt supply	2.5V	155	156	2.5V	2.5 volt supply
2.5 volt supply	2.5V	157	158	CK1#	clock
ground	GND	159	160	CK1	clock

Description	Name	Pin		Name	Description
ground	GND	161	162	GND	ground
data 48	DQ48	163	164	DQ52	data 52
data 49	DQ49	165	166	DQ53	data 53
2.5 volt supply	2.5V	167	168	2.5V	2.5 volt supply
data strobe 6	DQS6	169	170	DQM6	data mask 6
data 50	DQ50	171	172	DQ54	data 54
ground	GND	173	174	GND	ground
data 51	DQ51	175	176	DQ55	data 55
data 56	DQ56	177	178	DQ60	data 60
2.5 volt supply	2.5V	179	180	2.5V	2.5 volt supply
data 57	DQ57	181	182	DQ61	data 61
data strobe 7	DQS7	183	184	DQM7	data mask 7
ground	GND	185	186	GND	ground
data 58	DQ58	187	188	DQ62	data 62
data 59	DQ59	189	190	DQ63	data 63
2.5 volt supply	2.5V	191	192	2.5V	2.5 volt supply
SPD data	SDA	193	194	SA0	SPD address
SPD clock	SCL	195	196	SA1	SPD address
3.3 volt supply	3.3V	197	198	SA2	SPD address
reserved	N/C	199	200	N/C	reserved

4.5 PC/104-Bus

An onboard LPC-to-ISA bridge (Fintek® F85226F) makes it possible to expand the functionality of the board with additional PC/104 cards. This interface offers full 16bit ISA compliance. For further information on this interface please refer to the PC/104 specifications (see "Specifications and Documents", p. 10).



Pinning of the standard 8 bit PC/104 connector.

Description	Name	Pin		Name	Description
ISA - IO channel check	IOCHK#	A1	B1	GND	ground
ISA – data 7	SD7	A2	B2	RSTDRV	reset drive
ISA – data 6	SD6	A3	B3	VCC	5 volt supply
ISA – data 5	SD5	A4	B4	IRQ9	ISA – interrupt 9 (2)
ISA – data 4	SD4	A5	B5	-5V	-5 volt supply
ISA – data 3	SD3	A6	B6	DRQ2	ISA – DMA request 2
ISA – data 2	SD2	A7	B7	-12V	-12 volt supply
ISA – data 1	SD1	A8	B8	IOCHRDY	ISA – IO channel ready
ISA – data 0	SD0	A9	B9	12V	12 volt supply
ISA – IO channel ready	IOCHRDY	A10	B10	N/C	reserved
ISA – address enable	AEN	A11	B11	SMEMW#	ISA – system memory write
ISA – address 19	SA19	A12	B12	SMEMR#	ISA – system memory read
ISA – address 18	SA18	A13	B13	IOW#	ISA – IO write
ISA – address 17	SA17	A14	B14	IOR#	ISA – IO read
ISA – address 16	SA16	A15	B15	DACK3#	ISA – DMA acknowledge 3
ISA – address 15	SA15	A16	B16	DRQ3	ISA – DMA request 3
ISA – address 14	SA14	A17	B17	DACK1#	ISA – DMA acknowledge 1
ISA – address 13	SA13	A18	B18	DRQ1	ISA – DMA request 1
ISA – address 12	SA12	A19	B19	REFRESH#	ISA – refresh
ISA – address 11	SA11	A20	B20	SYSCLK	ISA – system clock
ISA – address 10	SA10	A21	B21	IRQ7	ISA – interrupt 7
ISA – address 9	SA9	A22	B22	IRQ6	ISA – interrupt 6
ISA – address 8	SA8	A23	B23	IRQ5	ISA – interrupt 5
ISA – address 7	SA7	A24	B24	IRQ4	ISA – interrupt 4
ISA – address 6	SA6	A25	B25	IRQ3	ISA – interrupt 3
ISA – address 5	SA5	A26	B26	DACK2#	ISA – DMA acknowledge 2
ISA – address 4	SA4	A27	B27	T/C	ISA – terminal count
ISA – address 3	SA3	A28	B28	BALE	ISA – address latch en.

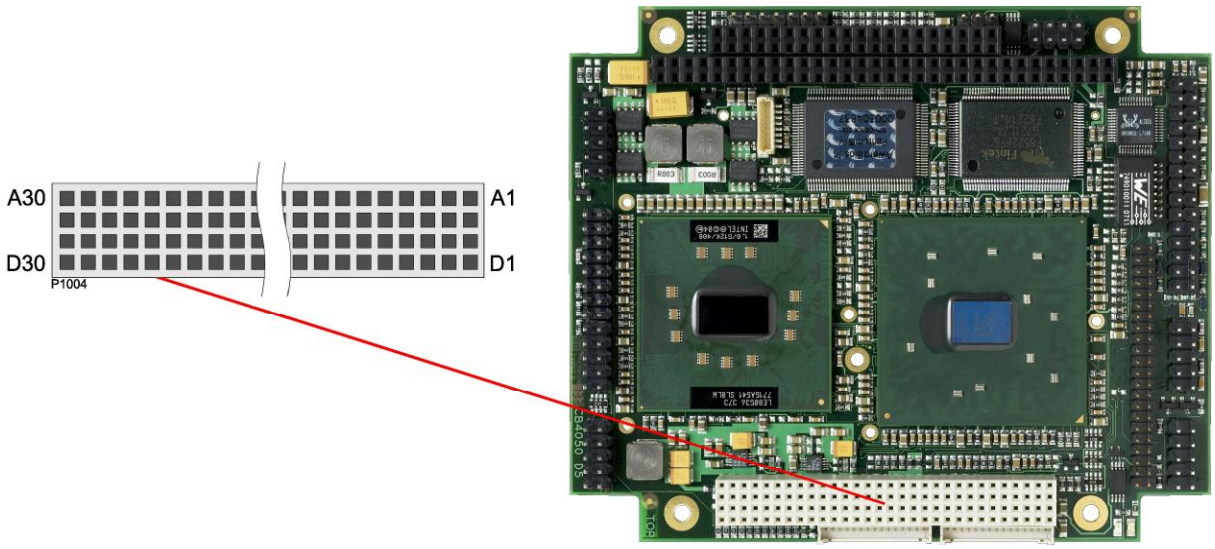
Description	Name	Pin		Name	Description
ISA – address 2	SA2	A29	B29	VCC	5 volt supply
ISA – address 1	SA1	A30	B30	OSC	ISA – 14,318MHz
ISA – address 0	SA0	A31	B31	GND	ground
ground	GND	A32	B32	GND	ground

Pinning of the 16 bit expansion PC/104 connector.

Description	Name	Pin		Name	Description
ground	GND	C0	D0	GND	ground
ISA – byte high enable	SBHE#	C1	D1	MEMCS16#	ISA – memory chip select
ISA – latched address 23	LA23	C2	D2	IOCS16#	ISA – IO chip select
ISA – latched address 22	LA22	C3	D3	IRQ10	ISA – interrupt 10
ISA – latched address 21	LA21	C4	D4	IRQ11	ISA – interrupt 11
ISA – latched address 20	LA20	C5	D5	IRQ12	ISA – interrupt 12
ISA – latched address 19	LA19	C6	D6	IRQ15	ISA – interrupt 15
ISA – latched address 18	LA18	C7	D7	IRQ14	ISA – interrupt 14
ISA – latched address 17	LA17	C8	D8	DACK0#	ISA – DMA acknowledge 0
ISA – memory read	MEMR#	C9	D9	DRQ0	ISA – DMA request 0
ISA – memory write	MEMW#	C10	D10	DACK5#	ISA – DMA acknowledge 5
ISA – data 8	SD8	C11	D11	DRQ5	ISA – DMA request 5
ISA – data 9	SD9	C12	D12	DACK6#	ISA – DMA acknowledge 6
ISA – data 10	SD10	C13	D13	DRQ6	ISA – DMA request 6
ISA – data 11	SD11	C14	D14	DACK7#	ISA – DMA acknowledge 7
ISA – data 12	SD12	C15	D15	DRQ7	ISA – DMA request 7
ISA – data 13	SD13	C16	D16	VCC	5 volt supply
ISA – data 14	SD14	C17	D17	MASTER#	ISA – bus master
ISA – data 15	SD15	C18	D18	GND	ground
reserved	N/C	C19	D19	GND	ground

4.6 PC/104-Plus Bus

Expansion cards can be connected to the board using the PCI connector first introduced with the PC/104-Plus standard. A maximum of four PC/104-Plus cards are supported.
The interrupt routing and the IDSEL signals for the expansion cards are specified in the PC/104-Plus specification (see "Specifications and Documents", p. 10).

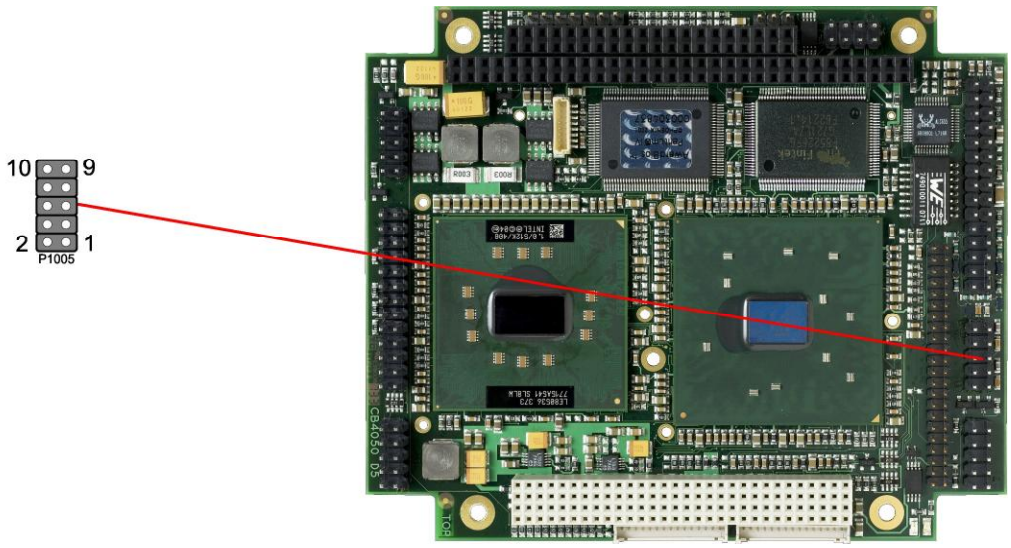


Description	Name	Pin		Name	Description
ground	GND	A1	B1	N/C	reserved
3.3 volt - IO buffer power	VIO	A2	B2	AD2	PCI – address/data 2
PCI – address/data 5	AD5	A3	B3	GND	ground
PCI – com/byte enable 0	CBE0#	A4	B4	AD7	PCI – address/data 7
ground	GND	A5	B5	AD9	PCI – address/data 9
PCI – address/data 11	AD11	A6	B6	VIO	3.3 volt - IO buffer power
PCI – address/data 14	AD14	A7	B7	AD13	PCI – address/data 13
3.3 volt supply	3.3V	A8	B8	CBE1#	PCI – com/byte enable 1
PCI – system error	SERR#	A9	B9	GND	ground
ground	GND	A10	B10	PERR#	PCI – parity error
PCI – stop	stop#	A11	B11	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A12	B12	TRDY#	PCI – target ready
PCI – frame	FRAME#	A13	B13	GND	ground
ground	GND	A14	B14	AD16	PCI – address/data 16
PCI – address/data 18	AD18	A15	B15	3.3V	3.3 volt supply
PCI – address/data 21	AD21	A16	B16	AD20	PCI – address/data 20
3.3 volt supply	3.3V	A17	B17	AD23	PCI – address/data 23
PCI – ID select slot 1	IDSEL0	A18	B18	GND	ground
PCI – address/data 24	AD24	A19	B19	CBE3#	PCI – com/byte enable 3
ground	GND	A20	B20	AD26	PCI – address/data 26
PCI – address/data 29	AD29	A21	B21	VCC	5 volt supply
5 volt supply	VCC	A22	B22	AD30	PCI – address/data 30
PCI – bus request slot 1	REQ0#	A23	B23	GND	ground
ground	GND	A24	B24	REQ2#	PCI – bus request slot 3
PCI – bus grant slot 4	GNT1#	A25	B25	VIO	5 volt - IO buffer power
5 volt supply	VCC	A26	B26	CLK0	PCI – clock slot 1
PCI – clock slot 3	CLK2	A27	B27	VCC	5 volt supply

Description	Name	Pin		Name	Description
ground	GND	A28	B28	INTD#	PCI – interrupt D
12V supply	12V	A29	B29	INTA#	PCI – interrupt A
-12V supply	-12V	A30	B30	REQ3#	PCI – bus request slot 4
5 volt supply	VCC	C1	D1	AD0	PCI – address/data 0
PCI – address/data 1	AD1	C2	D2	VCC	5 volt supply
PCI – address/data 4	AD4	C3	D3	AD3	PCI – address/data 3
ground	GND	C4	D4	AD6	PCI – address/data 6
PCI – address/data 8	AD8	C5	D5	GND	ground
PCI – address/data 10	AD10	C6	D6	M66EN	PCI – 66MHz enable
ground	GND	C7	D7	AD12	PCI – address/data 12
PCI – address/data 15	AD15	C8	D8	3.3V	3.3 volt supply
reserved	N/C	C9	D9	PAR	PCI – parity bit
3.3 volt supply	3.3V	C10	D10	N/C	reserved
PCI – lock	LOCK#	C11	D11	GND	ground
ground	GND	C12	D12	DEVSEL#	PCI – device select
PCI – initiator ready	IRDY#	C13	D13	3.3V	3.3 volt supply
3.3 volt supply	3.3V	C14	D14	CBE2#	PCI – com/byte enable 2
PCI – address/data 17	AD17	C15	D15	GND	ground
ground	GND	C16	D16	AD19	PCI – address/data 19
PCI – address/data 22	AD22	C17	D17	3.3V	3.3 volt supply
PCI – ID select slot 2	IDSEL1	C18	D18	IDSEL2	PCI – ID select slot 3
3,3 volt - IO buffer power	VIO	C19	D19	IDSEL3	PCI – ID select slot 4
PCI – address/data 25	AD25	C20	D20	GND	ground
PCI – address/data 28	AD28	C21	D21	AD27	PCI – address/data 27
ground	GND	C22	D22	AD31	PCI – address/data 31
PCI – bus request slot 2	REQ1#	C23	D23	VIO	3,3 volt - IO buffer power
5 volt supply	VCC	C24	D24	GNT0#	PCI – bus grant slot 1
PCI – bus grant slot 3	GNT2#	C25	D25	GND	ground
ground	GND	C26	D26	CLK1	PCI – clock slot 2
PCI – clock slot 4	CLK3	C27	D27	GND	ground
5 volt supply	VCC	C28	D28	RST#	PCI – reset
PCI – interrupt B	INTB#	C29	D29	INTC#	PCI – interrupt C
PCI – bus grant slot 4	GNT3#	C30	D30	GND	ground

4.7 VGA

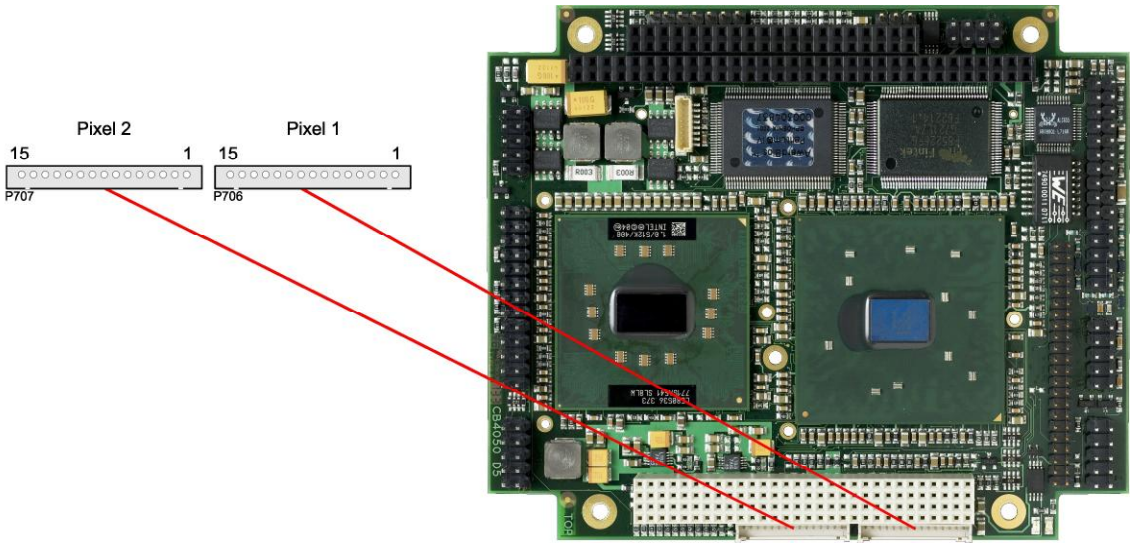
The CRT-VGA signals are provided by a standard IDC socket connector with a spacing of 2.54 mm. This interface allows the connection of a standard VGA-monitor. I2C communication is supported.



Description	Name	Pin		Name	Description
analog red	RED	1	2	GND	ground
analog green	GREEN	3	4	DDDA	DD data
analog blue	BLUE	5	6	DDCK	DD clock
vertikal sync	VSYNC	7	8	GND	ground
horizontal sync	HSYNC	9	10	GND	ground

4.8 LCD

The LCD is connected via two 15 pin connectors (Hirose DF13-15P-1.25DSA, mating connector: DF13-15S-xxx). The power supply for the display is also provided through these connectors. The ADL855PC board only supports displays with LVDS interface. For displays with digital interface an extra receiver board is available. There is no support for DSTN displays.
With the LVDS interface it is possible to trigger LVDS displays with a maximum of 24 Bit colour depth and one or two pixels per clock. For single pixel displays only one connector is necessary. However, if you want to read the display's EDID data the second connector must be connected.
The display type can be chosen over the BIOS setup. Please contact your sales representative regarding an appropriate cable to connect your display.



The following table shows the pin description for the first bit ("even" pixel).

Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO00#	LVDS even data 0 -
4	TXO00	LVDS even data 0 +
5	TXO01#	LVDS even data 1 -
6	TXO01	LVDS even data 1 +
7	TXO02#	LVDS even data 2 -
8	TXO02	LVDS even data 2 +
9	TXO0C#	LVDS even clock -
10	TXO0C	LVDS even clock +
11	TXO03#	LVDS even data 3 -
12	TXO03	LVDS even data 3 +
13	BL_VCC	switched 5 volt for backlight
14	FP_3.3V	switched 3.3 volt for display
15	FP_3.3V	switched 3.3 volt for display

The following table shows the pin description for the second bit ("odd" pixel). This connector will only be used if a display with two pixels per clockcycle is to be connected.

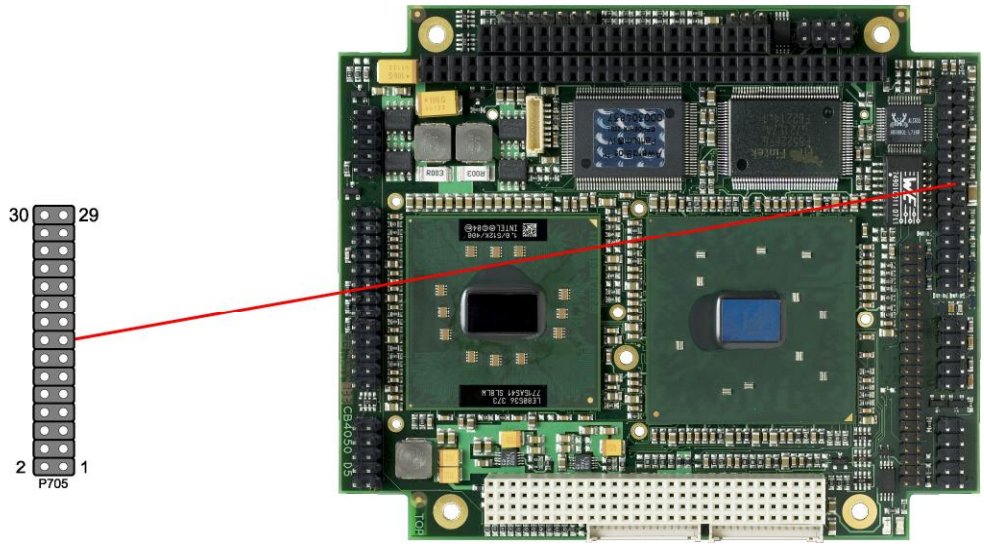
Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO10#	LVDS odd data 0 -
4	TXO10	LVDS odd data 0 +
5	TXO11#	LVDS odd data 1 -
6	TXO11	LVDS odd data 1 +
7	TXO12#	LVDS odd data 2 -
8	TXO12	LVDS odd data 2 +
9	TXO1C#	LVDS odd clock -
10	TXO1C	LVDS odd clock +
11	TXO13#	LVDS odd data 3 -
12	TXO13	LVDS odd data 3 +
13	DDC_CLK	EDID clock for LCD
14	DDC_DAT	EDID data for LCD
15	VCC	5 volt supply

4.9 USB 1 to 4, LAN, Sound

USB 1-4, LAN and sound are provided via a standard IDC socket connector with a spacing of 2.54 mm. Necessary settings can be accomplished in BIOS setup.
All USB-channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running a USB supporting OS (such as Microsoft® Windows®) with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.
The LAN-interface on this connector supports 10BaseT and 100BaseT compatible network components with automatic bandwidth selection. Additional outputs are provided for status LEDs. Auto-negotiate and auto-cross functionality is available, PXE and RPL are available on request.
AC'97 - 2.3 compatible audio I/O is available on this connector. There are two ways to use these signals. Default functionality is the familiar audio in, audio out, and microphone (2-channel mode). OS dependent device drivers can switch these signals to support an 5.1 output; thus in this mode no audio input signals are available. In 2-channel mode LOUT is the only active audio output. Moth MIC inputs are available. In 6-channel mode the speaker outputs are: LOUT to Front, AUXA to Surround, MIC1 to Center and MIC2 to LFE (Sub).
The signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.

CAUTION

The same IDC socket connector supports all three devices and is not "keyed"! Misconnected support cables may short two devices together and damage the board. Please check diagrams before installing any connecting cables to ensure proper connection.



Description	Name	Pin		Name	Description
5 volt for USB1	USB1 VCC	1	2	USB2 VCC	5 volt for USB2
USB- channel 1	USB1#	3	4	USB2#	USB- channel 2
USB+ channel 1	USB1	5	6	USB2	USB+ channel 2
ground	GND	7	8	GND	ground
USB+ channel 3	USB3	9	10	USB4	USB+ channel 4
USB- channel 3	USB3#	11	12	USB4#	USB- channel 4
5 volt for USB3	USB3 VCC	13	14	USB4 VCC	5 volt for USB4

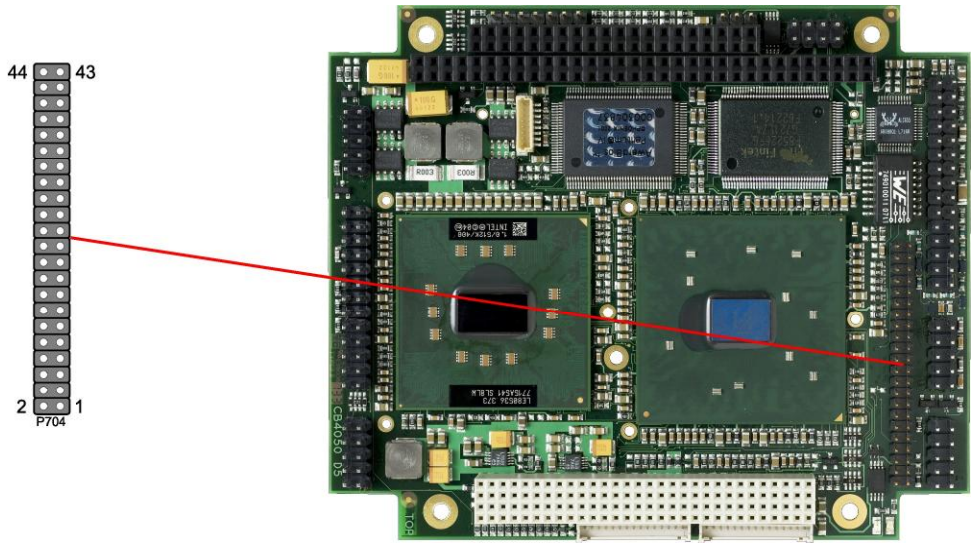
Description	Name	Pin		Name	Description
LAN activity	ACTLED	15	16	SPEEDLED	LAN 10/100 speed
LAN RX+	LANRX	17	18	LANTX	LAN TX+
LAN RX-	LANRX#	19	20	LANTX#	LAN TX-
digital output SPDIF	SPDIFO	21	22	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	23	24	S_AGND	analog ground sound
sound output right / frond output right	LOUT_R / FRONT_R	25	26	LOUT_L / FRONT_L	sound output left / frond output left
AUX input right / rear output right	AUXA_R / REAR_R	27	28	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	29	30	MIC2 / LFE	microphone input 2 / LFE output

4.10 IDE Interface

The primary IDE interface is a standard IDC socket connector with a spacing of 2 mm. All commercial IDE devices are supported but an adapter to connect may be necessary.
The required settings are made in the BIOS setup.

CAUTION

Pins are not keyed! Please be sure to connect the cable properly, otherwise you risk damaging the IDE interface, the CPU and the drive, voiding respective warranties.

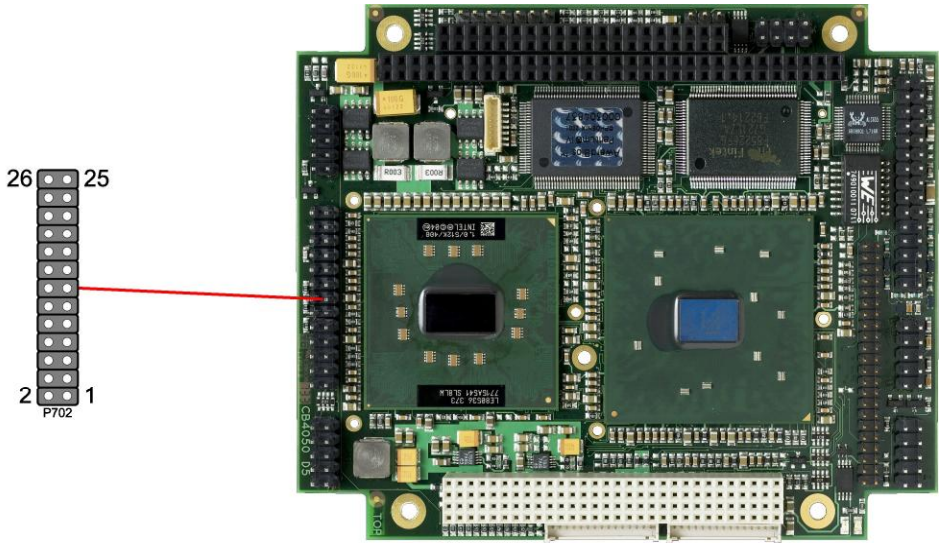


Pinout for primary IDE

Description	Name	Pin		Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	reserved
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 0	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
reserved	N/C	39	40	GND	ground
supply HDD 5V	VCC	41	42	VCC	supply HDD 5V
ground	GND	43	44	N/C	reserved

4.11 Parallel Interface LPT

The parallel interface is a standard IDC socket connector with a spacing of 2.54 mm. The port address and the interrupt are set via the BIOS setup.
The parallel port may be selected in BIOS-setup to interface to a standard PC floppy drive, but a special cable is required for such operation. Please contact your sales representative for such a cable.



Pinout LPT interface (FDC signals in brackets):

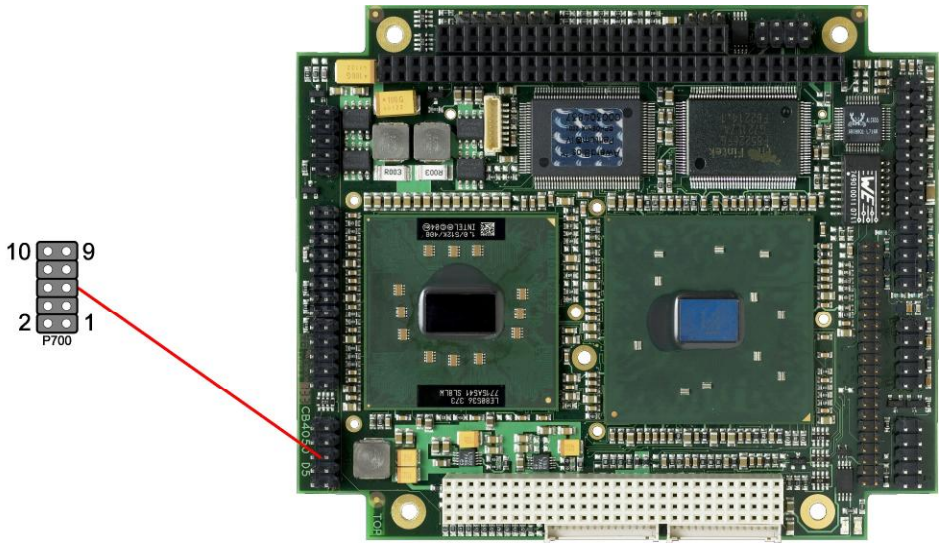
Description	Name	Pin		Name	Description
strobe	STB#	1	2	AFD# (DRVDEN0)	automatic line feed (drive density 0)
LPT data 0 (Index)	PD0 (IDX#)	3	4	ERR# (HDSL#)	error (head select)
LPT data 1 (track 0)	PD1 (TR0#)	5	6	INIT# (DIR#)	init (direction)
LPT data 2 (write protect)	PD2 (WPRT#)	7	8	SLIN# (STP#)	select input (step)
LPT data 3 (read data)	PD3 (RDATA#)	9	10	GND	ground
LPT data 4 (disk change)	PD4 (DC#)	11	12	GND	ground
LPT data 5	PD5	13	14	GND	ground
LPT data 6 (motor 0)	PD6 (MT0#)	15	16	GND	ground
LPT data 7 (drive select 0)	PD7 (DR0#)	17	18	GND	ground
acknowledge (drive select 1)	ACK# (DR1#)	19	20	GND	ground
busy (motor 1)	BUSY (MT1#)	21	22	GND	ground
paper end (write data)	PE (WD#)	23	24	GND	ground
select printer (write enable)	SLCT (WG#)	25	26	VCC	5 volt supply

4.12 Serial Interface COM1

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. Signals default to RS232 but can be ordered as TTL level too.
The port address and the interrupt are set via the BIOS setup.

CAUTION

COM 1 & 2 cables are not the same pin orientation and you may damage the COM interface and CPU attached if you use the incorrect COM cable.



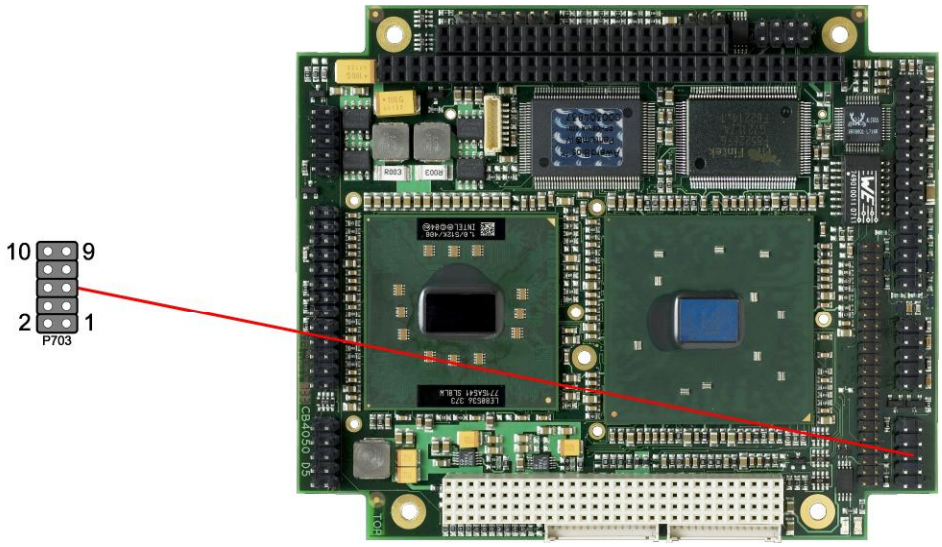
Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

4.13 Serial Interface COM2

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. Signals default to RS232 but can be ordered as TTL level too.
The port address and the interrupt are set via the BIOS setup.

CAUTION

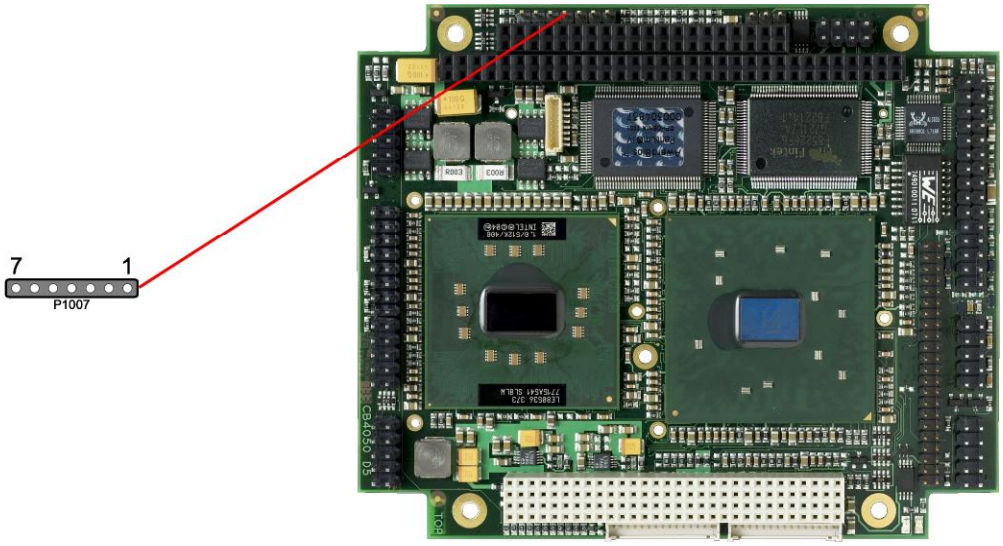
COM 1 & 2 cables are not the same pin orientation and you may damage the COM interface and CPU attached if you use the incorrect COM cable.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

4.14 SMBus

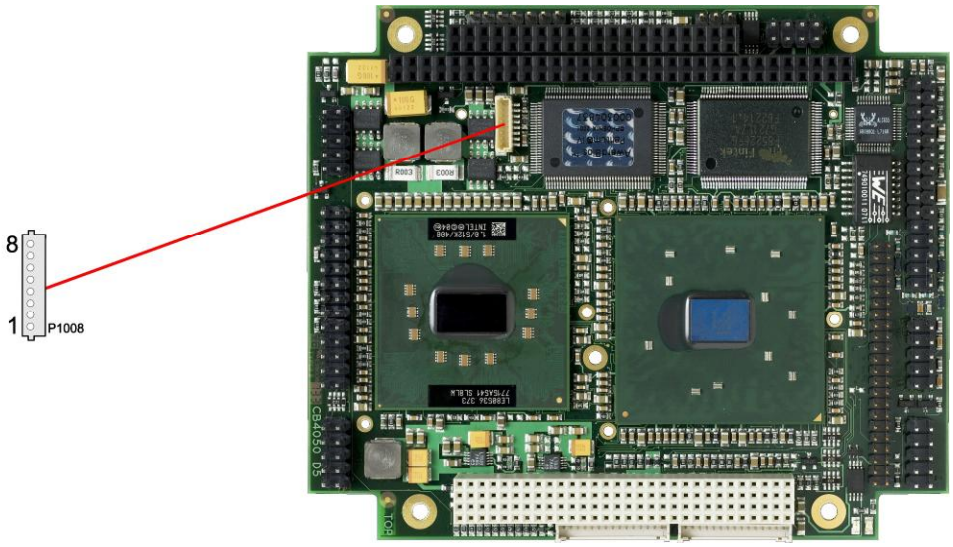
The ADL855PC can communicate with external devices via the SMBus protocol. The signals for this protocol are available through a standard IDC socket connector with a spacing of 2.54 mm. A 3.3 volt power supply is also available for these SMBus devices. Additionally, you can use this connector to access the PWRBTN# and PS_ON# signals used for power control. If PWRBTN# is held low for four seconds an unconditional hardware power-down event will occur.



Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	SMB-ALERT#	SMBus alert
5	PWRBTN#	power button
6	PS_ON#	power supply on
7	GND	ground

4.15 Monitoring Functions

Additional monitoring functions, such as the status of the fan or of other devices connected over SM-Bus (e. g. temperature sensor), are accessible via an 8 pin connector (JST BM08B-SRSS-TB, mating connector: SHR-08V-S(-B)).



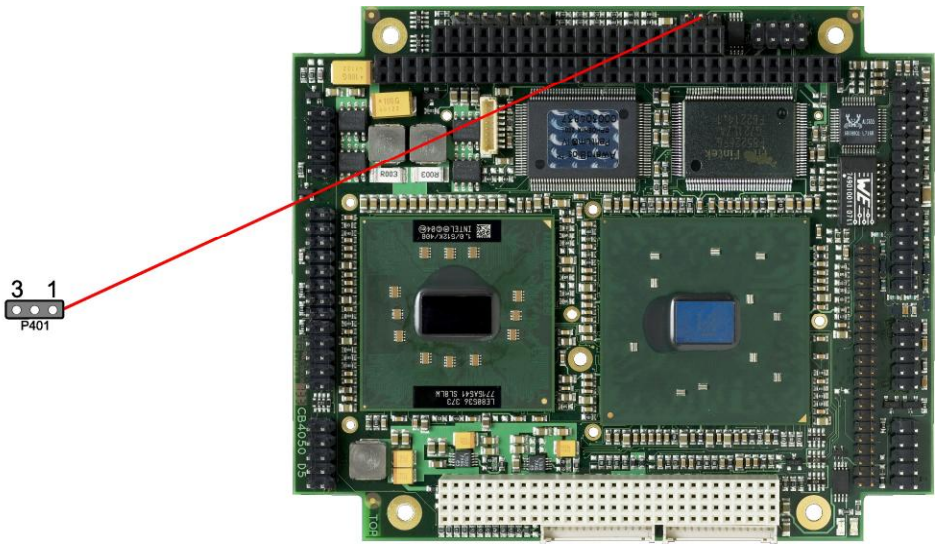
Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	GND	ground
5	FANON1	5 volt supply (switched)
6	FANCTRL1	fan 1 monitoring signal
7	VCC	5 volt supply
8	FANCTRL3	fan 3 monitoring signal

NOTE

This connector is present on boards of the revision D2 and onwards.

4.16 Fan

A 3 pin connector is available for controlling and monitoring an external fan (5 volt). For the monitoring the fan must provide a corresponding speed signal.



Pin	Name	Description
1	GND	ground
2	FANON2	5 volt supply (switched)
3	FANCTRL2	fan monitoring signal

5 BIOS Settings

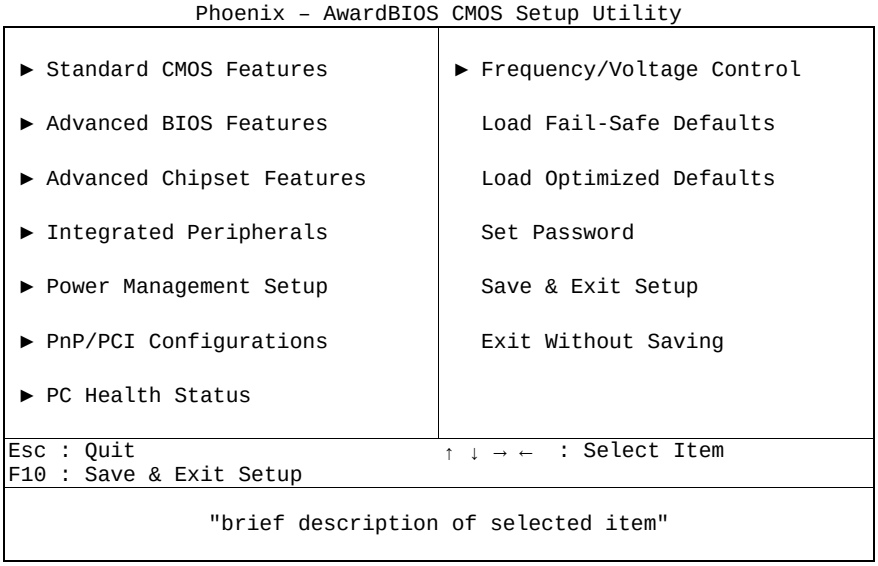
5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

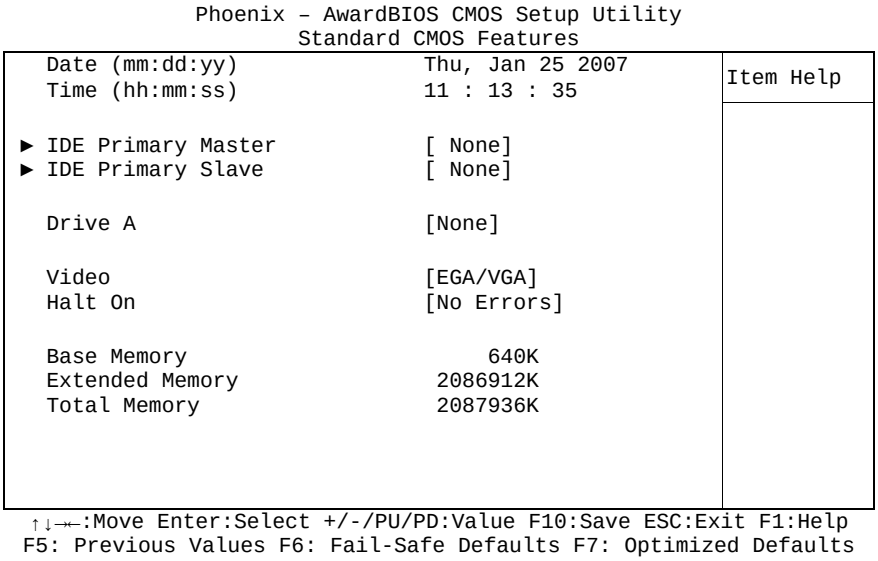
BIOS features and setup options are subject to change without notice. The settings displayed in the screenshots on the following pages are meant to be examples only. They do not represent the recommended settings or the default settings. Determination of the appropriate settings is dependent upon the particular application scenario in which the board is used.

5.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).
Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

5.3 Standard CMOS Features



- **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- **IDE Primary Master**
  Sub menu: see "IDE Primary Master/Slave" (p. 37)

- **IDE Primary Slave**
  Sub menu: see "IDE Primary Master/Slave" (p. 37)

- **Drive A**
  Options: None / 360K, 5.25 in. / 1.2M, 5.25 in. / 720K, 3.5 in. / 1.44M, 3.5 in. / 2.88M, 3.5 in.

- **Video**
  Options: EGA/VGA / CGA 40 / CGA 80 / Mono

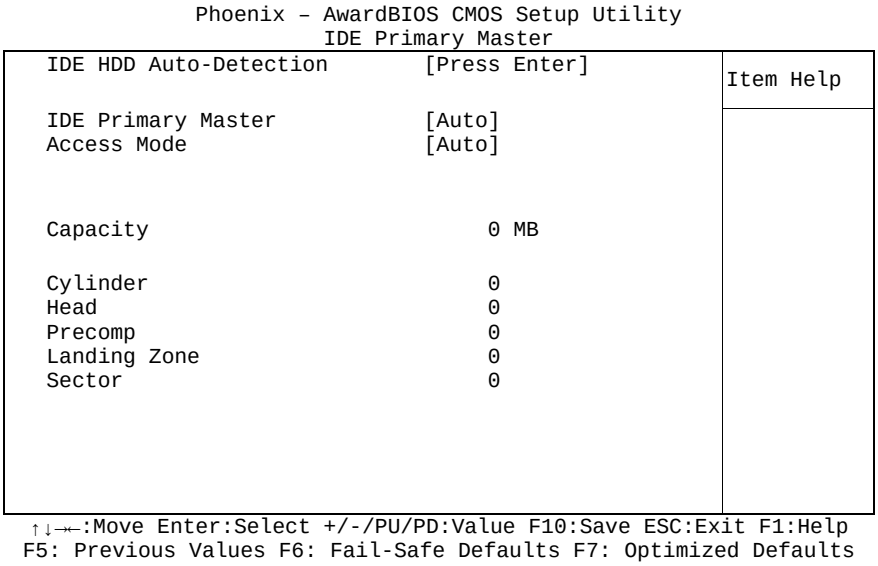
- **Halt On**
  Options: All Errors / No Errors / All, But Keyboard / All, But Diskette / All, But Disk/Key

- **Base Memory**
  Options: none

- **Extended Memory**
  Options: none

- **Total Memory**
  Options: none

5.3.1 IDE Primary Master/Slave



- **IDE HDD Auto-Detection**
  Options: none

- **IDE Primary Master**
  Options: None / Auto / Manual

- **Access Mode**
  Options: CHS / LBA / Large / Auto

- **Capacity**
  Options: none

- **Cylinder**
  Options: none

- **Head**
  Options: none

- **Precomp**
  Options: none

- **Landing Zone**
  Options: none

- **Sector**
  Options: none

5.4 Advanced BIOS Features

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      Advanced BIOS Features
┌──────────────────────────────────────────────────────┬──────────────┐
│ ► CPU Feature                  [Press Enter]         │ Item Help    │
│   Virus Warning                [Disabled]            │              │
│   CPU L1 & L2 Cache            [Enabled]             │              │
│   Quick Power On Self Test     [Enabled]             │              │
│   First Boot Device            [HDD-0]               │              │
│   Second Boot Device           [Disabled]            │              │
│   Third Boot Device            [Disabled]            │              │
│   Boot Other Device            [Enabled]             │              │
│   Boot Up Floppy Seek          [Disabled]            │              │
│   Boot Up NumLock Status       [On]                  │              │
│   Gate A20 Option              [Fast]                │              │
│   Typematic Rate Setting       [Disabled]            │              │
│ x Typematic Rate (Chars/Sec)    6                    │              │
│ x Typematic Delay (Msec)        250                  │              │
│   Security Option              [Setup]               │              │
│   APIC Mode                    [Disabled]            │              │
│   MPS Version Control For OS   1.4                   │              │
│   OS Select For DRAM > 64MB    [Non OS2]             │              │
│   Report No FDD For WIN 95     [No]                  │              │
│   Full Screen LOGO Show        [Disabled]            │              │
└──────────────────────────────────────────────────────┴──────────────┘
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **CPU Feature**
  Sub menu: see "CPU Feature" (p. 40)

- **Virus Warning**
  Options: Enabled / Disabled

- **CPU L1 & L2 Cache**
  Options: Enabled / Disabled

- **Quick Power On Self Test**
  Options: Enabled / Disabled

- **First Boot Device**
  Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

- **Second Boot Device**
  Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

- **Third Boot Device**
  Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

- **Boot Other Device**
  Options: Enabled / Disabled

- **Boot Up Floppy Seek**
  Options: Enabled / Disabled

- **Boot Up NumLock Status**
  Options: Off / On

- **Gate A20 Option**
  Options: Normal / Fast

- **Typematic Rate Setting**
  Options: Enabled / Disabled

- **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- **Security Option**
  Options: Setup / System

- **APIC Mode**
  Options: Enabled / Disabled

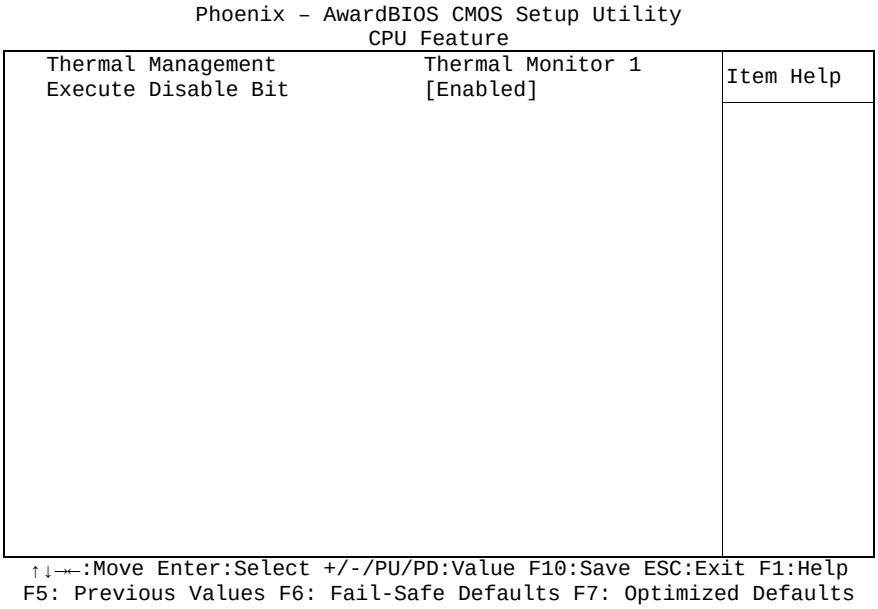
- **MPS Version Control For OS**
  Options: 1.1 / 1.4

- **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- **Report No FDD For WIN 95**
  Options: No / Yes

- **Full Screen LOGO Show**
  Options: Enabled / Disabled

5.4.1 CPU Feature



ü **Thermal Management**
Options: none

ü **Execute Disable Bit**
Options: Enabled / Disabled

5.5 Advanced Chipset Features

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                        Advanced Chipset Features
  DRAM Timing Selectable        [By SPD]          | Item Help
x CAS Latency Time               2.5              |
x Active to Precharge Delay     7                 |
x DRAM RAS# to CAS# Delay       3                 |
x DRAM RAS# Precharge           3                 |
x DRAM Data Integrity Mode      Non-ECC           |
  MGM Core Frequency            [Auto Max 266MHz] |
  System BIOS Cacheable         [Enabled]         |
  Video BIOS Cacheable          [Enabled]         |
  Memory Hole At 15M-16M        [Disabled]        |
  Delayed Transaction           [Enabled]         |
  Delay Prior to Thermal        [16 Min]          |
  AGP Aperture Size (MB)        [64]              |
  ** On-Chip VGA Setting **                       |
  On-Chip VGA                   [Enabled]         |
  On-Chip Frame Buffer Size     [32MB]            |
  Boot Display                  [LFP]             |
  Panel Scaling                 [Off]             |
  Panel Number                  [ 800*600 *18b-sp]|
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **DRAM Timing Selectable**
  Options: By SPD / Manual

- **CAS Latency Time**
  Options: 2.5 / 2

- **Active to Precharge Delay**
  Options: 5 / 6 / 7

- **DRAM RAS# to CAS# Delay**
  Options: 2 / 3

- **DRAM RAS# Precharge**
  Options: 2 / 3

- **DRAM Data Integrity Mode**
  Options: none

- **MGM Core Frequency**
  Options: Auto Max 266MHz /
  400/266/133/200 MHz /
  400/200/100/200 MHz /
  400/200/100/133 MHz /
  400/266/133/267 MHz /
  400/333/166/250 MHz /
  Auto Max 400/333 MHz

- **System BIOS Cacheable**
  Options: Enabled / Disabled

- **Video BIOS Cacheable**
  Options: Enabled / Disabled

- **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- **Delayed Transaction**
  Options: Enabled / Disabled

- **Delay Prior to Thermal**
  Options: 4 Min / 8 Min / 16 Min / 32 Min

- **AGP Aperture Size**
  Options: 4 / 8 / 16 / 32 / 64 / 128 / 256

- **On Chip VGA**
  Options: Enabled / Disabled

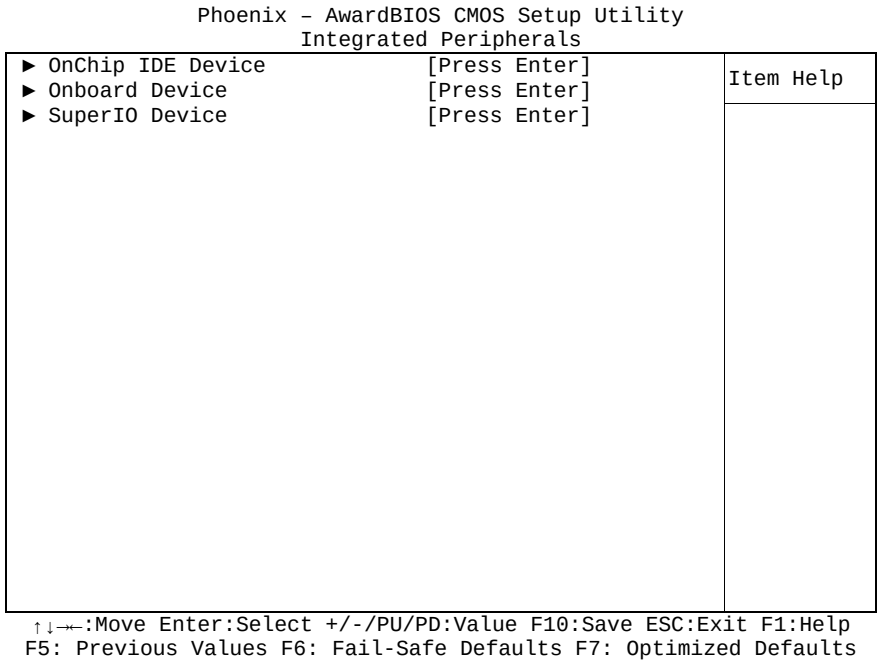
- **On Chip Frame Buffer Size**
  Options: 1MB / 4MB / 8MB / 16MB / 32MB

- **Boot Display**
  Options: VBIOS Default / CRT / LFP / CRT+LFP

- **Panel Scaling**
  Options: Auto / On / Off

- **Panel Number**
  Options: 640*480 *18b-sp / 800*600 *18b-sp / 1024*768 *18b-sp / 1024*768 *18b-dp / 1280*1024*18b-dp / 1400*1050*18b-dp / 1400*1050*18b-rb / 1600*1200*18b-dp / 640*480 *24b-sp / 800*600 *24b-sp / 1024*768 *24b-sp / 1024*768 *24b-dp / 1280*1024*24b-dp / 1400*1050*24b-dp / 1400*1050*24b-rb / 1600*1200*24b-dp

5.6 Integrated Peripherals

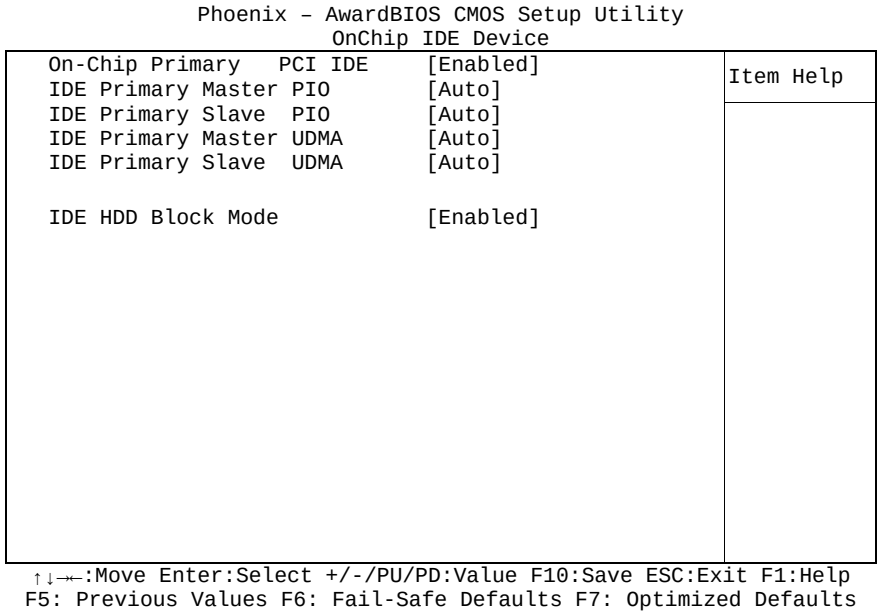


- **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (p. 44)

- **Onboard Device**
  Sub menu: see "Onboard Devices" (p. 45)

- **SuperIO Device**
  Sub menu: see "SuperIO Devices" (p. 46)

5.6.1 OnChip IDE Devices



- **On-Chip Primary PCI IDE**
  Options: Enabled / Disabled

- **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

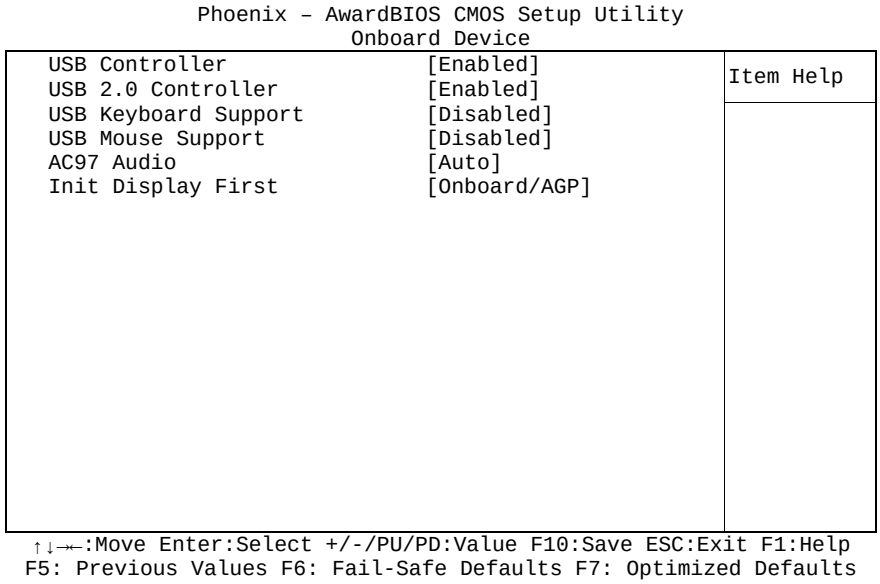
- **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- **IDE Primary Master UDMA**
  Options: Disabled / Auto

- **IDE Primary Slave UDMA**
  Options: Disabled / Auto

- **IDE HDD Block Mode**
  Options: Enabled / Disabled

5.6.2 Onboard Devices



- **USB Controller**
  Options: Enabled / Disabled

- **USB 2.0 Controller**
  Options: Enabled / Disabled

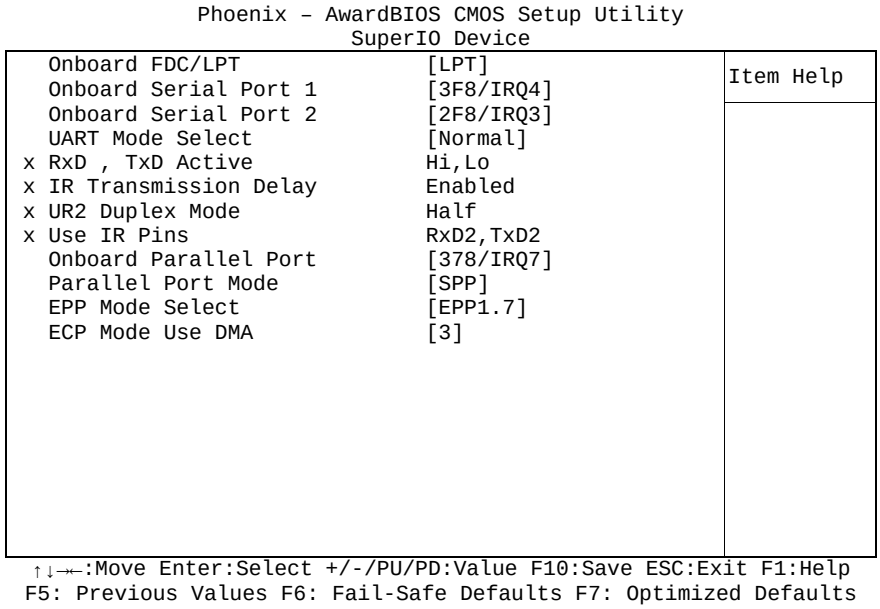
- **USB Keyboard Support**
  Options: Enabled / Disabled

- **USB Mouse Support**
  Options: Enabled / Disabled

- **AC97 Audio**
  Options: Disabled / Auto

- **Init Display First**
  Options: Onboard/AGP / PCI Slot

5.6.3 SuperIO Devices



- **Onboard FDC/LPT**
  Options: FDC / LPT / Disabled

- **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / 3E8/IRQ11 / 2E8/IRQ10

- **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / 3E8/IRQ11 / 2E8/IRQ10

- **UART Mode Select**
  Options: IrDA / ASKIR / Normal

- **RxD , TxD Active**
  Options: Hi,Hi / Hi,Lo / Lo,Hi / Lo,Lo

- **IR Transmission Delay**
  Options: Enabled / Disabled

- **UR2 Duplex Mode**
  Options: Full / Half

- **Use IR Pins**
  Options: RxD2,TxD2 / IR-Rx2Tx2

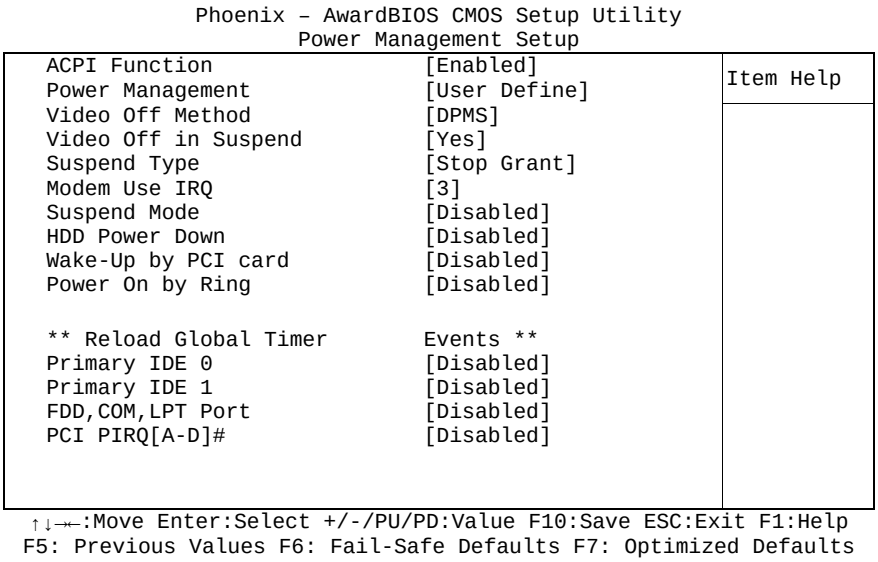
- **Onboard Parallel Port**
  Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

- **Parallel Port Mode**
  Options: SPP / EPP / ECP / ECP+EPP / Normal

- **EPP Mode Select**
  Options: EPP1.9 / EPP1.7

- **ECP Mode Use DMA**
  Options: 1 / 3

5.7 Power Management Setup



- **ACPI function**
  Options: Enabled / Disabled

- **Power Management**
  Options: User Define / Min Saving / Max Saving

- **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- **Video Off In Suspend**
  Options: No / Yes

- **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min / 30 Min / 40 Min / 1 Hour

- **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- **Wake Up by PCI Card**
  Options: Enabled / Disabled

- **Power-On by Ring**
  Options: Enabled / Disabled

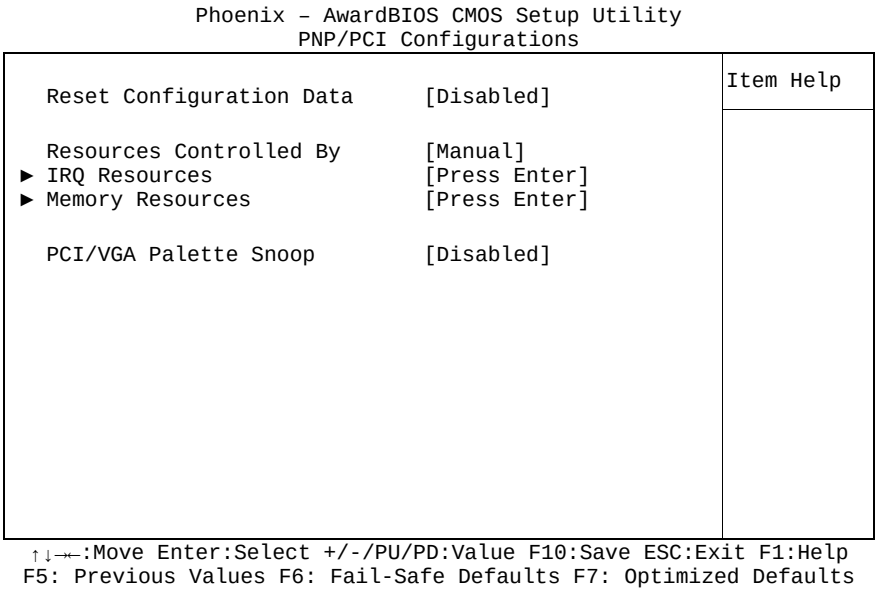
- **Primary IDE 0**
  Options: Enabled / Disabled

- **Primary IDE 1**
  Options: Enabled / Disabled

- **FDD,COM,LPT Port**
  Options: Enabled / Disabled

- **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

5.8 PnP/PCI Configuration



- **Reset Configuration Data**
  Options: Enabled / Disabled

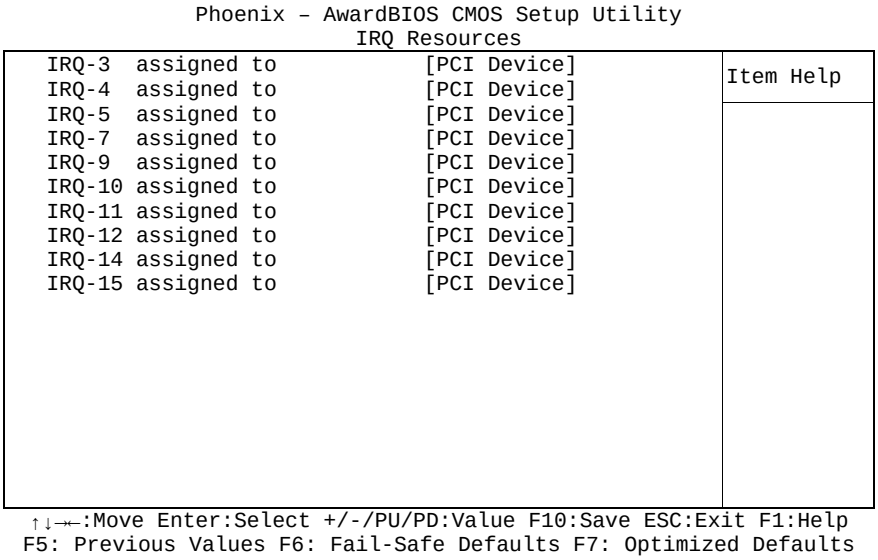
- **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- **IRQ Resources**
  Sub menu: see "IRQ Resources" (p. 50)

- **Memory Resources**
  Sub menu: see "Memory Resources" (p. 51)

- **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

5.8.1 IRQ Resources



- **IRQ-3 assigned to**
  Options: PCI Device / Reserved

- **IRQ-4 assigned to**
  Options: PCI Device / Reserved

- **IRQ-5 assigned to**
  Options: PCI Device / Reserved

- **IRQ-7 assigned to**
  Options: PCI Device / Reserved

- **IRQ-9 assigned to**
  Options: PCI Device / Reserved

- **IRQ-10 assigned to**
  Options: PCI Device / Reserved

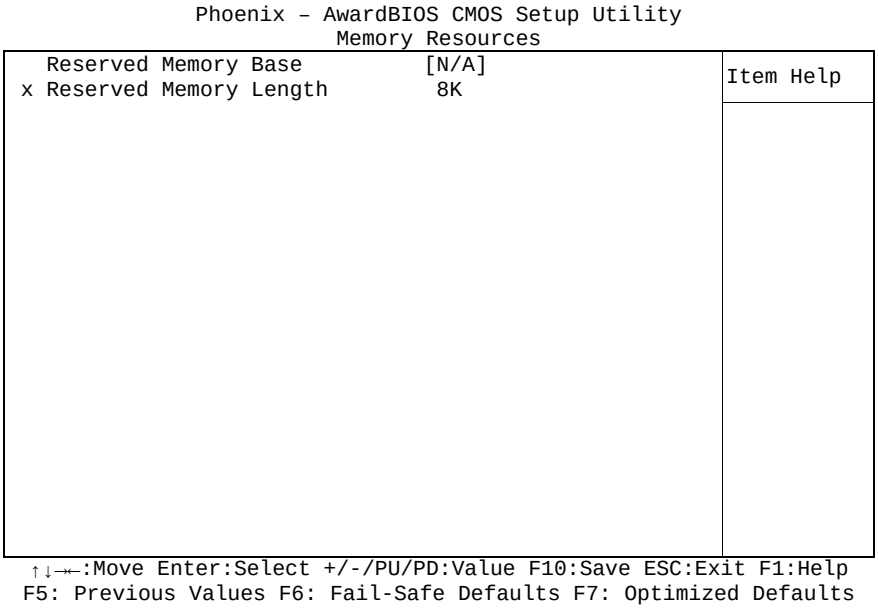
- **IRQ-11 assigned to**
  Options: PCI Device / Reserved

- **IRQ-12 assigned to**
  Options: PCI Device / Reserved

- **IRQ-14 assigned to**
  Options: PCI Device / Reserved

- **IRQ-15 assigned to**
  Options: PCI Device / Reserved

5.8.2 Memory Resources



- **Reserved Memory Base**
  Options: N/A / D000 / D400 / D800 / DC00

- **Reserved Memory Length**
  Options: 8K / 16K / 32K / 64K

5.9 PC Health Status

```
                Phoenix – AwardBIOS CMOS Setup Utility
                          PC Health Status
┌──────────────────────────────────────────────────────┬──────────────┐
│ Shutdown Temperature          [Disabled]             │ Item Help    │
│ Temp. Board                    51°C                  │              │
│ Temp. CPU                      54°C                  │              │
│ CPU Core                        0.89V                │              │
│ GMCH Core                       1.18V                │              │
│ CPU VTT                         1.07V                │              │
│ Memory 2.5V                     2.51V                │              │
│ +3.3 V                          3.29V                │              │
│ +5.0 V                          4.99V                │              │
│ Fan1 Speed                     12500 RPM             │              │
│ Fan2 Speed                         0 RPM             │              │
│ Fan3 Speed                         0 RPM             │              │
│ VBatt                           3.10V                │              │
│                                                      │              │
│ Board Revision                 5                     │              │
│                                                      │              │
│                                                      │              │
└──────────────────────────────────────────────────────┴──────────────┘
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Shutdown Temperature**
  Options: 60°C/140°F / 65°C/149°F / 70°C/158°C / Disabled

- **Temp. Board**
  Options: none

- **Temp. CPU**
  Options: none

- **CPU Core**
  Options: none

- **GMCH Core**
  Options: none

- **CPU VTT**
  Options: none

- **Memory 2.5V**
  Options: none

- **+3.3 V**
  Options: none

- **+5.0 V**
  Options: none

- **Fan1 Speed**
  Options: none

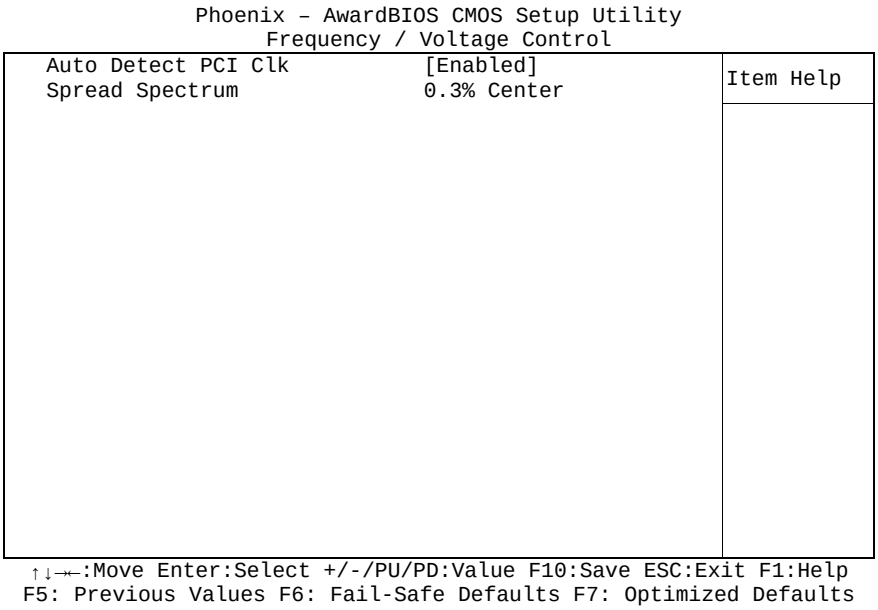
- **Fan2 Speed**
  Options: none

- **Fan3 Speed**
  Options: none

- **VBatt**
  Options: none

- **Board Revision**
  Options: none

5.10 Frequency/Voltage Control



- **Auto Detect PCI Clk**
  Options: Enabled / Disabled

- **Spread Spectrum**
  Options: none

5.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.12 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

5.14 Save & Exit Setup

Settings are saved and the board is restarted.

5.15 Exit Without Saving

This option leaves the setup without saving any changes.

6 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” from Phoenix Technologies is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cp	Clear the PnP information

The erasure of CMOS and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. DMI should only be erased (option /cd) if the BIOS supplier advises to do so.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

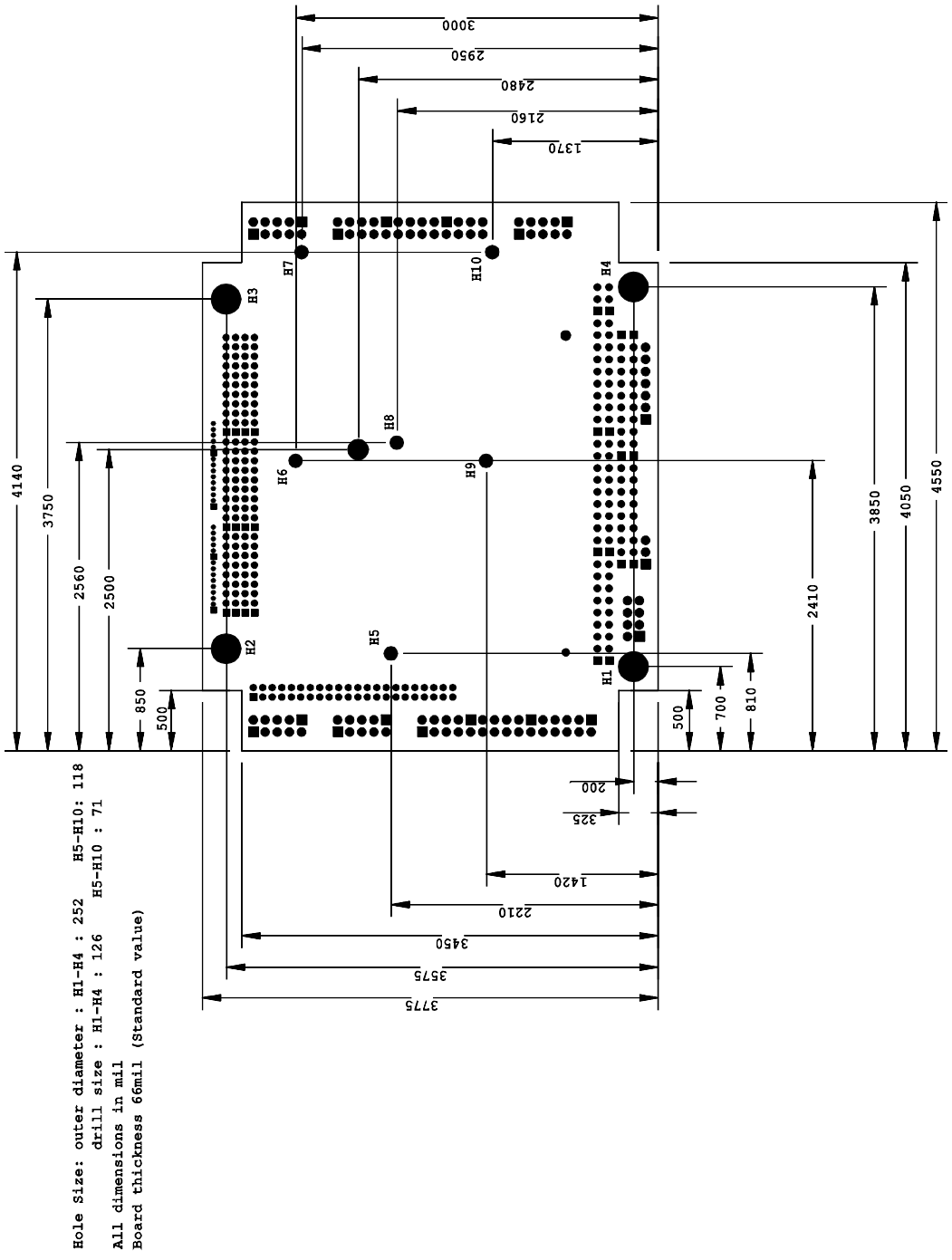
7 Mechanical Drawing

7.1 PCB: Dimensions

For additional dimensional drawings please refer to the PC/104 specification.

NOTE

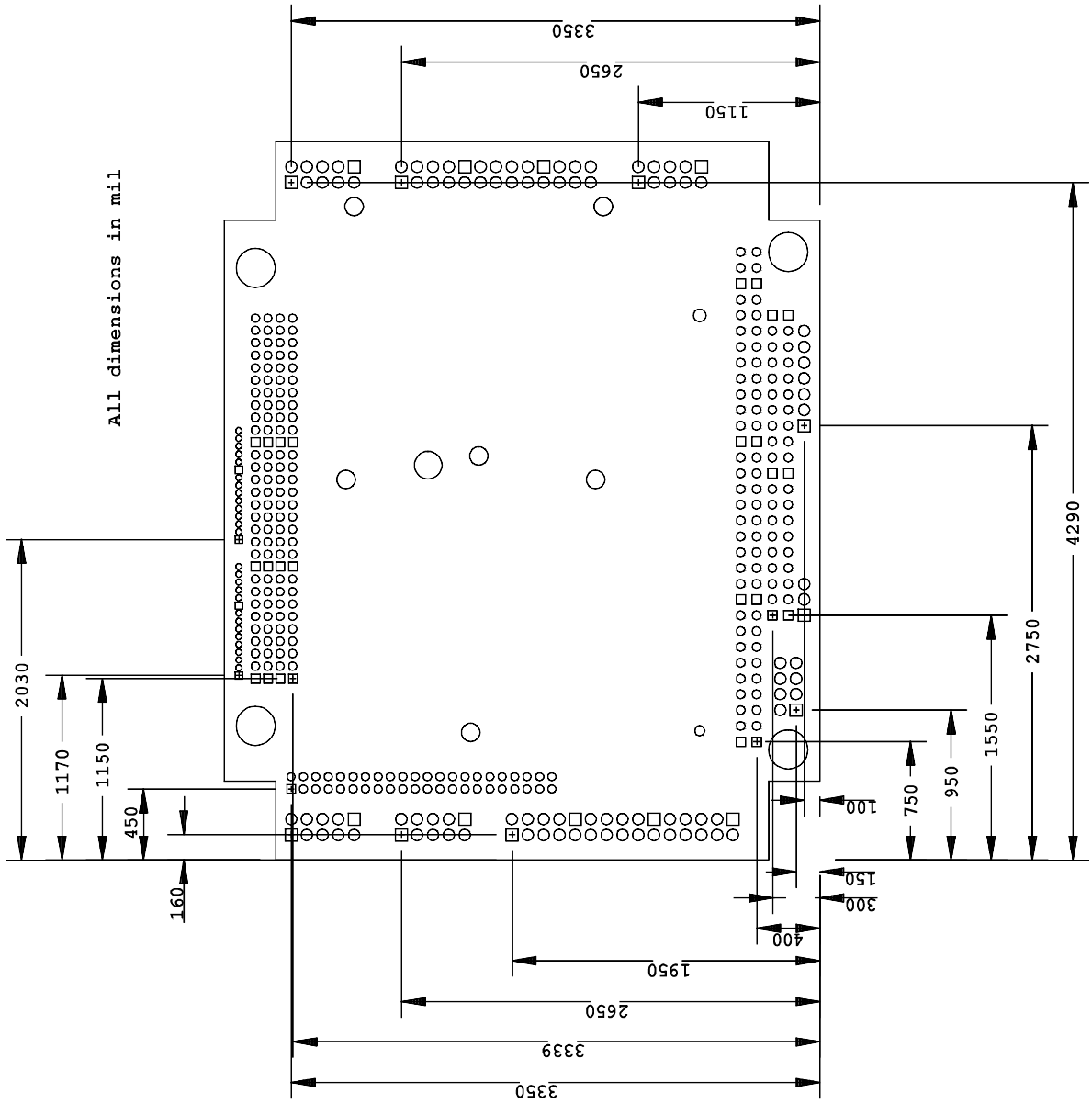
All dimensions are in mil (1 mil = 0,0254 mm)



7.2 PCB: Pin1 Dimensions

NOTE

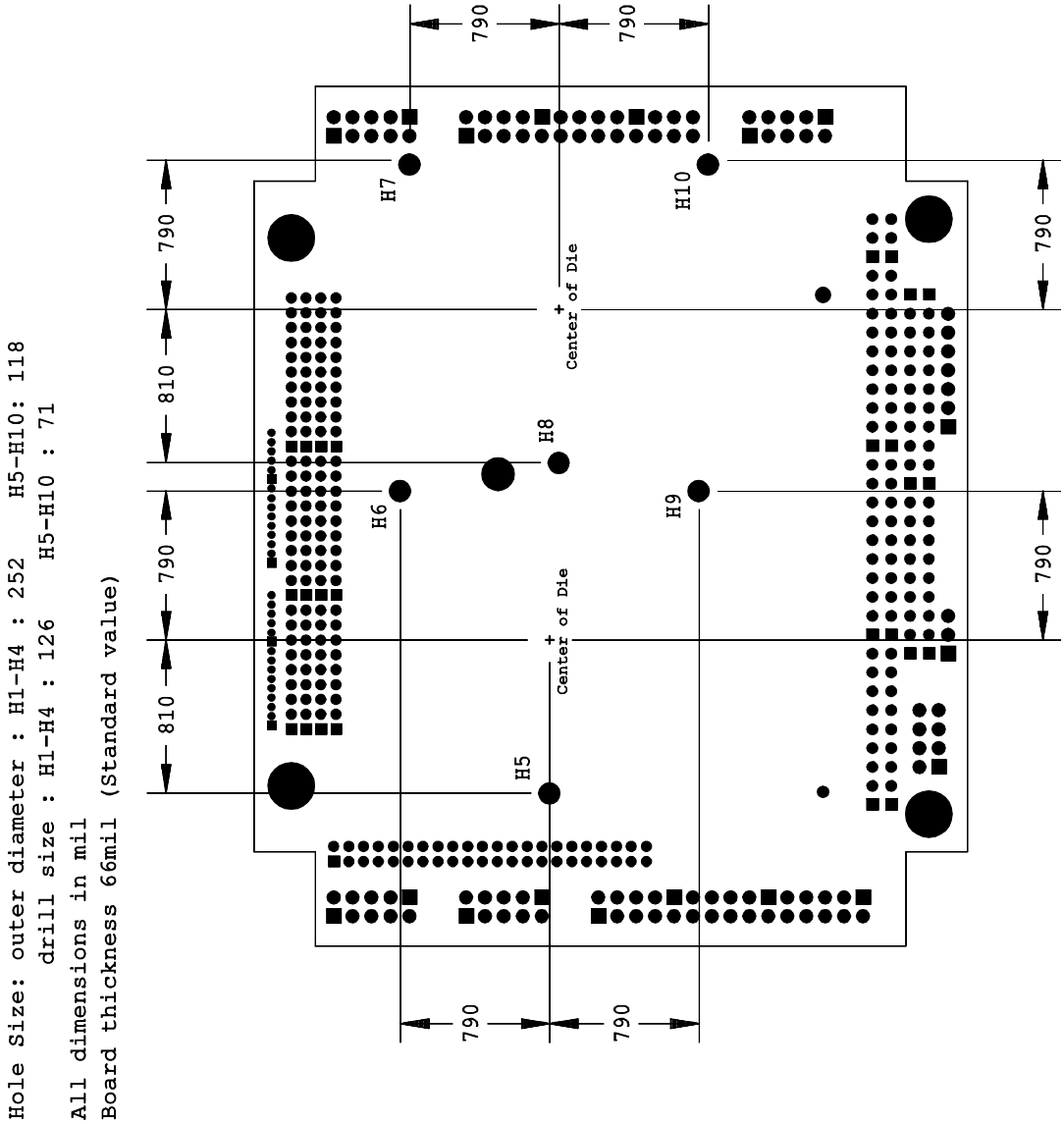
All dimensions are in mil (1 mil = 0,0254 mm)



7.3 PCB: Heatsink Dimensions

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)

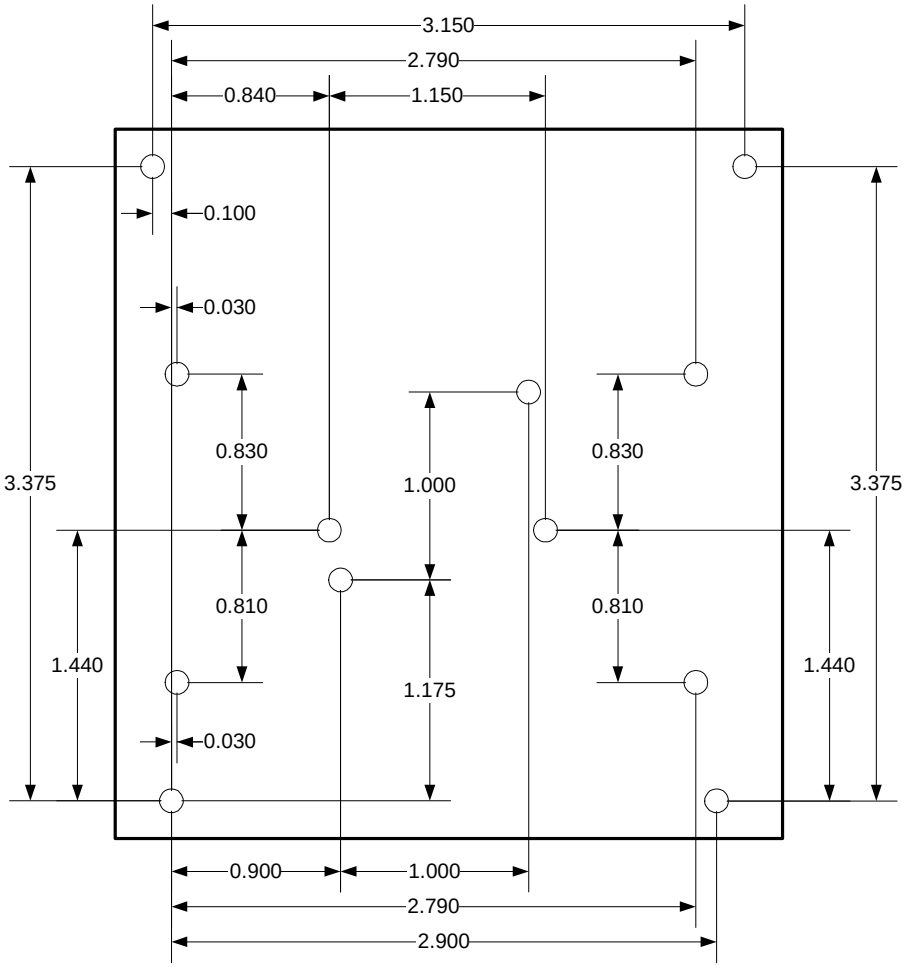


7.4 Heat Spreader: Chassis Mount

The figure below includes all hole spacing for each heat spreader available and can be used to aid in mating the heat spreader to a bulkhead or chassis.

NOTE

Dimensions are in inch (1 in = 2.54cm; 1 mil = 0.0254 mm)



8 Technical Data

8.1 Electrical Data

Power Supply:

Board:	5 Volt +/- 5%
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	1.98A idle, 3.10A full (Pentium M 1.4GHz, 25°C)
RTC:	<= 10µA

8.2 Environmental Conditions

Temperature Range:

Operating:	-25°C to +70°C (using approved thermal solution)
	-40°C up to +85°C (when pre-screened for use with an approved thermal solution)
Storage:	-40°C up to +85°C
Shipping:	-40°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

8.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from -25°C to +70°C when using an approved thermal solution, and an extended temperature range of -40°C to +85°C when pre-screened for use with an approved thermal solution.
Maximum die temperature is 100°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!
In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

CAUTION

The ADL855PC includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is no longer pulled low, an intelligent power supply would take this as a signal to shut down power. For this to work, PS_ON# must be connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the ADL855PC can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

A IO Range

The used resources depend on setup settings.
The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	IDE2
1F0-1F7	IDE1
278-27F	LPT2
2E8-2EF	COM4
2F8-2FF	COM2
370-377	FDC2
378-37F	LPT1
3BC-3BF	LPT3
3E8-3EF	COM3
3F0-3F7	FDC1
3F8-3FF	COM1

B Memory Range

The used resources depend on setup settings.
If the entire range is clogged through option ROMs, these functions do not work anymore.

Address	Function
A0000-BFFFF	VGA RAM
C0000-CFFFF	VGA BIOS
D0000-DFFFF	AHCI BIOS / RAID / PXE (if available)
E0000-EFFFF	System BIOS while booting
F0000-FFFFF	System BIOS

C Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup. The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	(COM3)
IRQ3	COM1
IRQ4	COM2
IRQ5	(COM4)
IRQ6	FDC
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	

Address	Function
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	(IDE Secondary)

D PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	PCI	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge ID3580
	-	-	0	0	1	ID3584
	-	-	0	0	3	ID3585
	A	-	0	2	0	VGA Graphics ID3582
	-	-	0	2	1	Graphics Controller ID3582
	A	-	0	29	0	USB UHCI Controller #1 ID24C2
	D	-	0	29	1	USB UHCI Controller #2 ID24C4
	C	-	0	29	2	USB UHCI Controller #3 ID24C7
	H	-	0	29	7	USB 2.0 EHCI Controller ID24CD
	-	-	0	30	0	Hub Interface to PCI Bridge ID244E
	-	-	0	31	0	PCI to LPC Bridge ID24C0
	C	-	0	31	1	IDE Controller ID24CB
	B	-	0	31	3	SMBus Controller ID24C3
	B	-	0	31	5	AC ’97 Audio Controller ID24C5
	B	-	0	31	6	AC ’97 Modem Controller ID24C6
17	E	4	1 or 2	1	0	LAN Intel 82551ER ID1209
20	A	0	1 or 2	4		External Slot 1
21	B	1	1 or 2	5		External Slot 2
22	C	2	1 or 2	6		External Slot 3
23	D	3	1 or 2	7		External Slot 4
24	E	-	1 or 2	8	0	LAN intern ICH4 ID103A

E SMB Devices

The following table contains all reserved SM-Bus device addresses in 8-bit notation. Note that external devices must not use any of these addresses even if the component mentioned in the table is not present on the motherboard.

Address	Function
10-11	Standard slave address
40-41	GPIO
60-61	BIOS internal
70-73	POST code output
88-89	BIOS-defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	BIOS internal
B0-BF	BIOS internal
D2-D3	Clock

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