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NuDAQ â

ACL-7120

Digital I/O & Counter Card

User's Guide



Recycled Paper

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How to Use This Guide

This manual is designed to help you use the ACL-7120. The manual describes how to modify various settings on the ACL-7120 card to meet your requirements. It is divided into five chapters:

- **Chapter 1,** "Introduction," gives an overview of the product features, applications, and specifications.
- **Chapter 2,** "Installation," describes how to install the ACL-7120. The layout of ACL-7120 is shown, the DIP switch setting for base address, and jumpers setting for clock frequency are specified.
- **Chapter 3,** "Signal Connection," describes the connectors pin assignment, timer/counter signal pad, and clock source on the ACL-7120.
- **Chapter 4,** "Programming," describes how to program the ACL-7120 for digital I/O and timer/counter.

1

Introduction

The ACL-7120 Digital I/O and Counter card consists of 32 digital input channels, 32 digital output channels and 6 counter/timer channels. All digital input/output channels are TTL/DTL compatible. The most outstanding feature of ACL-7120 is its full hardware and software compatible with Advantech's PCL-720.

ACLD-9182 , and ACLD-9185 are external daughter boards for use with ACL-7120. The ACLD-9182 is a 16 channel opto-isolated digital board to input digital data to the ACL-7120 when the ground isolation is required. The ACLD-9185 is a 16-channel relay output board which can be driven by the digital output of the ACL-7120.

A three channel programmable interval timer (8254) are provided for the functionality of timer and counter in the ACL-7120. For convenient of use the counter on this card, Three frequency sources 10KHz, 100KHz, and 1MHz are on-board for the input of each counter. In addition, the sources can also be double (X2), half (1/2) or quartered (1/4) by the jumper settings. It gives more flexibility for different frequency timer and counter applications.

An optional timer/counter chip is used to support for timer pacer which can generate interrupt periodically. Also, an event counter is used to external event counting.

1.1 Features

The ACL-7120 Relay Actuator and D/I Card provides the following advanced features:

- 32 TTL digital input channels
- 32 TTL digital output channels
- High output driving and low input loading
- 3 independent programmable 16 bit down counter
- one 32-bit timer(two 16-bit counter cascaded together) with a 4MHz time base
- One 16-bit counter with a 4MHz time base
- Crystal based frequency source
- Breadboard area for customized circuit
- Fully compatible with Advantech's PCL-720

1.2 Applications

- Industrial and laboratory ON/OFF control
- Energy management
- Annunciation
- Security controller
- Product test
- Period and pulse width measurement
- Event and frequency counting
- Waveform and pulse generation
- BCD interface driver

1.3 Specifications

- **General Specification:**
  - **Dimensions:** 19.3 cm x 10.3 cm
  - **Bus:** PC-AT bus
  - **Slot:** One 36 pin slot and one 62-pin slot
  - **I/O port address:** Hex 200 ~ Hex 3F8(8 bytes)
  - **Interrupt IRQ Level:** IRQ3 ~ IRQ15

- **Digital Input:**
  - Input logic low voltage: Min. -0.5V; Max. 0.8V
  - Input logic high voltage: Min. 2.0V; Max. 5.0V
  - Input loading current: Max. 0.2 mA at 0.4V
  - Input hysteresis: Typical 0.4V; Min. 0.2V

- **Digital Output:**
  - Output logic low voltage (Sink): Max. 0.5V at 24mA;
  - Output logic high voltage(Source): Max. 0.4V at 12mA
  - Driving Capacity: All inputs and outputs are TTL/DTL compatible and outputs will drive 1 standard TTL load (74 series) or 4 LSTTL (74LS) loads
  - Input hysteresis: Typical 0.4V; Min. 0.2V

- **Programmable Counter:**
  - **Chips:** 8254 or 8253
  - **Frequency:** 4MHz
  - **Counter:** six 16-bit counters (counter0 ~ counter 5)
  - **Mode:** 6 programmable modes
  - **Usable pins:** CLK and GATE for counter 0 ~ counter 3

- **counter usage :** counter 0 -counter 2 are flexible for users counter 3 is used for event counting interrupt source ,counter 4 - counter 5 are cascaded together for timer pacer generation
- **Bread Area:** plate-through 'donuts" hole. each with a .036: hole on 0.10" centers
- **Operating temperature:** 0 ~ 60°C
- **Humidity:** 0 to 90% non-condensing

1.4 Software Supporting

The ACL-7122 is programmed using simple 8-bit I/O port commands. Users can use high level language, such as BASIC, C, or PASCAL, or low- level language, such as assembly to program the board. For the programming under Windows or LabView, please contact your dealer to purchase ACLS-DLL1 or ACLD-LVIEW.

1.4.1 ACLS-DLL1

For easily program the board under Windows environment, we also provide **ACLS-DLL1**, which include the DLL for Windows 95/98/NT. With ACLS-DLL1, you can use compilers such as VB, VC/C++, or Delphi.

1.4.2 ACLS-LVIEW

For easily link the ACL-7122 with LabView of National Instrument, the ACLS-LVIEW includes the Vis of the ACL-7122 under for Windows 3.1/95/98 and NT.

2

Installation

This chapter describes how to install the ACL-7120. At first, the contain in the package and unpacking information that you should be careful are described. The jumper and switche settings for the ACL-7120's base address, clock sources, interrupt IRQ level, and IRQ trigger sources are also specified.

2.1 What You Have

In addition to this *User's Manual*, the package includes the following items:

- ♦ ACL-7120 Digital I/O & Counter Card
- ♦ ADLINK CD

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

Your ACL-7120 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be done on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handing damages on the module before processing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your ACL-7120.

2.3 ACL-7120's Layout

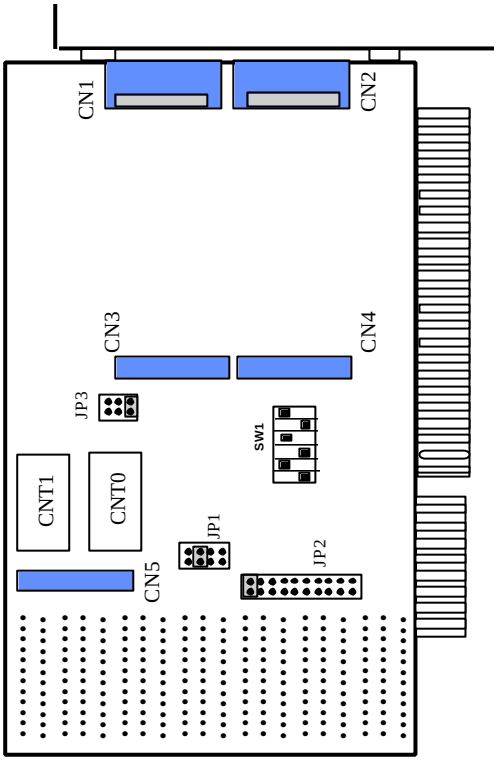


Figure 2.1

2.4 Jumper and DIP Switch Description

You can change the ACL-7120's channels and base address by setting jumpers and DIP switches on the card. The card's jumpers and switches are preset at the factory. Under normal circumstances, you should not need to change the jumper settings.

A jumper switch is closed (sometimes referred to as "shorted") with the plastic cap inserted over two pins of the jumper. A jumper is open with the plastic cap inserted over one or no pin(s) of the jumper.

2.5 Base Address Setting

The ACL-7120 requires eight consecutive address locations in I/O address space. The base address of the ACL-7120 is restricted by the following conditions.

1. The base address must be within the range 200hex to 3FFhex.

2. The base address should not conflict with any PC I/O address.

The ACL-7120's default I/O port base address **0x2A0** is set by an 6 positions DIP switch SW1 (refer to Figure 2.2). The possible address settings for I/O port from Hex 200 to Hex 3FE are listed in Table 2.2 next page.

Default Base Address = 0x2A0

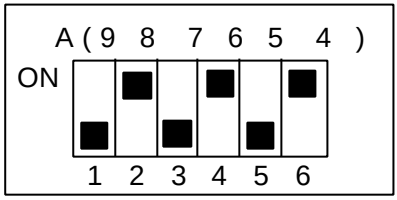


Figure 2.2 Default Base Address Setting

I/O port address(hex)	1 A9	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	OFF	ON	ON	ON	ON	ON
:						
(*)2A0-2AF	OFF	ON	OFF	ON	OFF	ON
2B0-2BF	OFF	ON	OFF	ON	OFF	OFF
:						
3D0-3DF	OFF	OFF	OFF	OFF	ON	OFF
3E0-3E0	OFF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

(*): default setting

X: don't care

A9, ...,A4 are corresponding to PC address lines

Table 2.2

How to define the base address for the ACL-7120?

The DIP1 to DIP6 in the switch SW1 are one to one corresponding to the PC bus address line A8 to A4. A9 is always 1 and A0~A3 are always 0. If you want to change the base address, you can only change the values of A8 to A4 (the shadow area of below table). The following table is an example, which shows you how to define the base address as ***Hex 2A0***

Base Address: ***Hex 2A0***

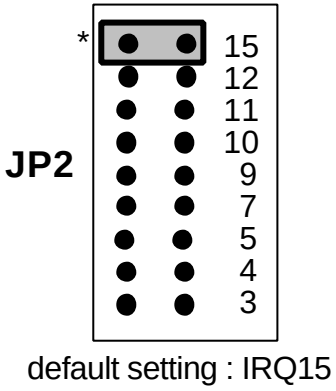
2		A				0			
1	0	1	0	1	0	0	0	0	0
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.6 Interrupt Setting

This interrupt function can be supported when the second counter chip (CNT 1) is installed. If you order ACL-7120/6 the CNT1 counter chips is on-board, otherwise you have to install counter chip before you wish to use timer pacer or event counting to trigger interrupt.

The ACL-7120 offer AT Bus interrupt levels (IRQ3 ~ IRQ15), and three interrupt trigger sources which are timer pacer, event, and external. The IRQ level is set by JP2 and it is used to define the interrupt IRQ level. The default setting is IRQ15 and its illustration is shown below.

Note : Be aware that there is no other add-on card shares the same interrupt level at the same system.



default setting : IRQ15

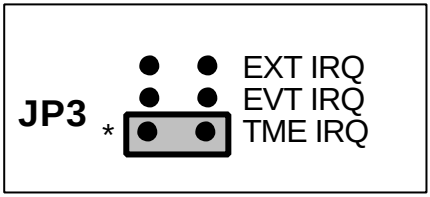
Figure 2.3

The interrupt trigger source is set by JP3. The default setting is “TME IRQ” and is shown below.

EXT IRQ: External source to trigger interrupt

EVT IRQ: Event counting to trigger interrupt

TME IRQ: Timer Pacer to trigger interrupt

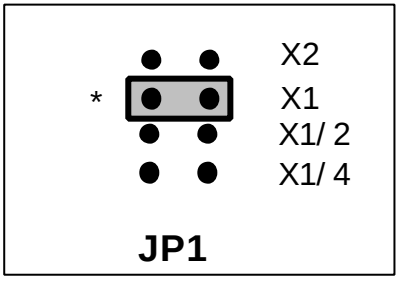


default setting :TME IRQ

Figure 2.4

2.7 Clock Frequency Setting

The ACL-7120 board offers 3 frequency sources which are 10KHz, 100KHz and 1 MHz. These frequencies can be double, half or quartered by placing a jumper on position " X2", "X1/2" or "X1/4" of the JP1.



* : default setting

Figure 2.5

2.8 ACL-7120 Software Library Installation

This section describes the DOS software library, which is free supplied. The function prototypes and some useful constants are defined in the header files in LIB directory. The DOS library software includes a utility program, C language library, and some demonstration programs, which can help you reduce the programming work. Please refer to the ACLS-DLL1 function reference manual, which included in ADLINK CD. The DOS functions are compatible with ACLS-DLL1 functions except without "W" prefix in function names.

To program in Windows environment, please use ACLS-DLL1 which needs license.

To install the DOS library software and utilities, please follow the following installation procedures:

1. Put *ADLINK CD* into the appropriate CD-ROM drive.

2. Type the following commands to change to the card's directory (*X* indicates the CD-ROM drive): *X*:\>**CD \NuDAQISA\7120.**

3. Execute the setup batch program to install the software: *X*:\NuDAQISA\7120>**SETUP.**

After installation, all the files *of ACL-7120 Library & Utility for DOS* are stored in C:\ADLINK\7120\DOS sub-directory.

3

Signal Connection

3.1 Connector Pin Assignment

The ACL-7120 comes equipped with five 20-pin insulation displacement connectors - CN1 ~ CN5. The CN1 and CN2 are located at the rear plate; the CN3, CN4, and CN5 are located on board. All these connectors can be connected to flat cables of the same type.

CN1 and CN3 are used for digital outputs, CN2 and CN4 are used for digital inputs, CN5 is used for timer/counter. The following diagrams below show the connectors' pin assignments.

Legend:

DO : Digital Output

DI : Digital Input

GND : Ground

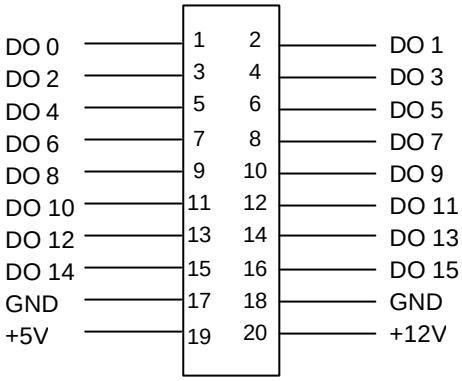
CLK : Clock input for 8254(8253)

GATE : Gate input for 8254(8253)

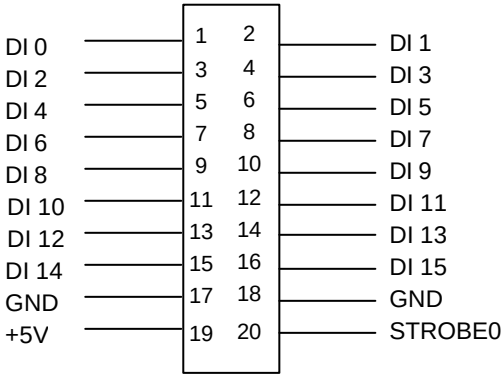
OUT : Signal output for 8254(8253)

STROBE : External signal to latch the DI data

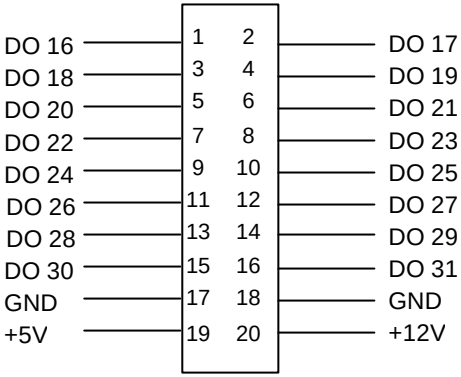
CN1: DIG OUT (0-15)



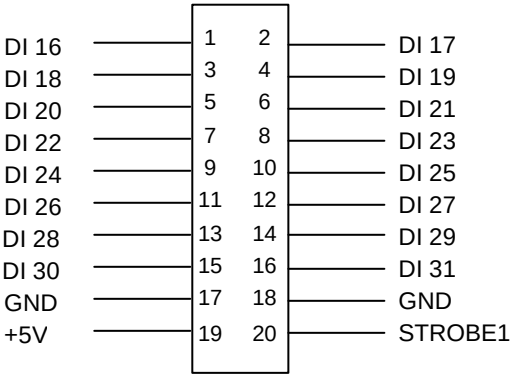
CN 2: DIG IN (0-15)



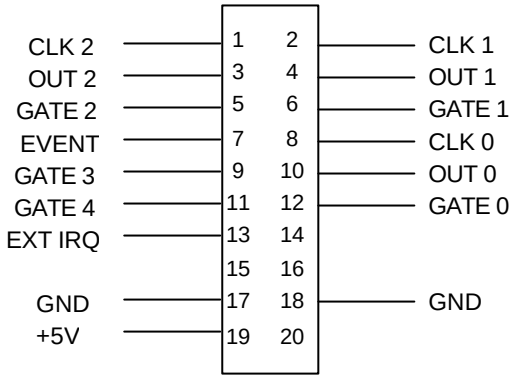
CN 3: DIG OUT (16 - 31)



CN 4: DIG IN (16 - 31)



CN 5: COUNTER


CLK 2
OUT 2
GATE 2
EVENT
GATE 3
GATE 4
EXT IRQ
GND
+5V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
CLK 1
OUT 1
GATE 1
CLK 0
OUT 0
GATE 0
GND

3.2 Timer/counter signal pads

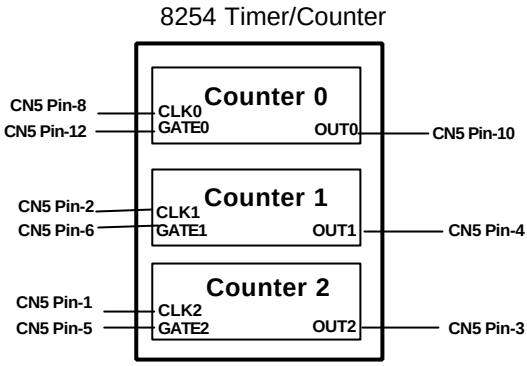


Figure 3.1

The first internal timer/counter 8254 (Counter 0 ~ Counter 2) in the ACL-7120 is configure as above diagram (figure 3.1). User can use the capability of 8254 through the CN5.

In addition to access the counters through CN5, it also offers another kind of wiring for using the capability of the 8254. A signal solder pads are on the board, and your applications can wire the signal through these soldering pads. The signals of these pads are the same as the signals of CN5. The layout of signal pads is shown in next page.

This feature is very useful for the applications which need to wire some circuits on the bread area of the ACL-7120.

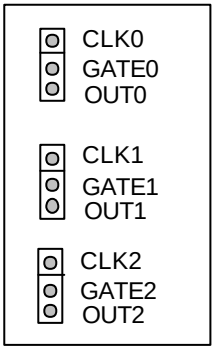


Figure 3.2

3.3 Interrupt Trigger Source

The second interval timer/counter 8254 chip on the ACL-7120 is used to generate sources for interrupt. The block diagram of this chip is illustrated as below (figure 3.3).

The Counter 3 of 8254 is used for event counting, it will accept event signals from CN5 pin-7, and its output will trigger interrupt when the count value of Counter 3 is become to 0.

The Counter 4 and Counter 5 are cascaded together for timer pacer trigger of interrupt; its clock source is 4Mhz.

Note : The second internal timer/counter 8254 is installed when you order ACL-7120/6 only. If this chip is not installed on-board, all above functions can be not workable.

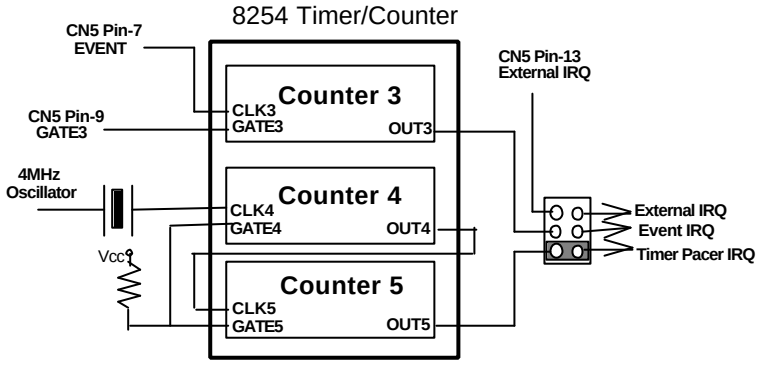


Figure 3.3 Block Diagram of 8254 Timer/Counter

The pacer rate of above configuration is determined by the formula:

pacer rate = 4 Mhz / (C4 * C5)

The maximum pacer signal rate is 4MHz/1=4Mhz. The minimum signal rate is 4MHz/65535/65535, which is a very slow frequency that user may never use it.

For example, if you wish to get a pacer rate 2.5 Khz, you can set C1 = 40 and C2 = 40. That is

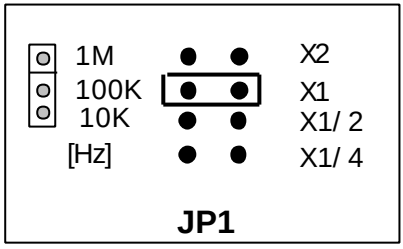
2.5KHz = 4Mhz / (40 x 40)

3.4 Clock Source Pads

In addition to the clock signal pads, the frequency sources can also be wired through the soldering pads. You can link one of the clock source to the clock input of the 8254 timer/counter by soldering a wire between the corresponding pads.

For example:

If you want that the counter 1 has 10 KHz clock input ,you can solder a wire between pads " 10K" and "CLK1" and insert a jumper in the position "X1" of the JP1. As shown below.



3.5 Latch Digital Inputs

The ACL-7120 offers a very useful capability to latch the input status for some special applications. The latch input means when the **STROBE** signal (20 pin of CN2 or CN4) is keep in high status, the data read form the input port will always reflect the current status. As the STROBE signal goes from High to Low, it will latch the input signal and stored in input buffer. If the STROBE is still keep on Low, the data read from input port is keep the same as the latched data. You can not get the current input signal until the STROBE signal becomes High or open status.

In general case, the STROBE signal is always kept as HIGH. The following table is used to describe the relationship between STROBE signal and input status.

STROBE SIGNAL	Digital Input Data
High	Transparent
High -> Low	Latched

Two STROBE signals are offered in ACL-7120, one is in connector CN2, and the other is in CN4.

4

Programming

4.1 I/O Registers Format

The ACL-7120 occupies 16 consecutive addresses in the PC I/O address space. Table 4.1 shows the I/O Map

Address	Write	Read
Base + 0	DO 0-7	DI 0-7
Base + 1	DO 8-15	DI 8-15
Base + 2	DO 16-23	DI 16-23
Base + 3	DO 24-31	DI 24-31
Base + 4	LSB OR MSB OF COUNTER 0	
Base + 5	LSB OR MSB OF COUNTER 1	
Base + 6	LSB OR MSB OF COUNTER 2	
Base + 7	CONTROL BYTE CW0	
Base + 8	LSB OR MSB OF COUNTER 3	
Base + 9	LSB OR MSB OF COUNTER 4	
Base + 10	LSB OR MSB OF COUNTER 5	
Base + 11	CONTROL BYTE CW1	

DO -- Digital Output

DI -- Digital Input

LSB -- Least Significant Byte

MSB -- Most Significant Byte

Table 4.1

4.2 Digital I/O Programming

The ACL 7120 provides 32 digital input channels and 32 digital output channels. Four I/O port address (Base+0,..., Base+3) are reserved for these digital I/O channels. The relationship between I/O address and I/O channels are specified as following:

**** Digital Input Register Format:**

Address: BASE + 0, BASE + 1, BASE + 2, BASE + 3

Attribute: Read for digital input

Data Format:

Bit	7	6	5	4	3	2	1	0
Base + 0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Base + 1	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
Base + 2	DI23	DI22	DI21	DI20	DI19	DI18	DI17	DI16
Base + 3	DI31	DI30	DI29	DI28	DI27	DI26	DI25	DI24

**** Digital Output Register Format:**

Address : BASE + 0, BASE + 1, BASE + 2, BASE + 3

Attribute: write for digital output

Data Format:

Bit	7	6	5	4	3	2	1	0
Base + 0	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Base + 1	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
Base + 2	DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
Base + 3	DO31	DO30	DO29	DO28	DO27	DO26	DO25	DO24

- **Digital Input Operation (Read):**

  The digital input states are read as a single byte from the port at address BASE+N (N= 0,1,2,3). Each of the 8 bits within the byte corresponding to particular digital input, a high bit (1) signifies the input is energized, a low bit (0) signifies the input is de-energized.

  For example:

  In BASIC ,

  ```
  05  BASE=&H2A0
  10  VALUE1 = INP(BASE + 0)  'Read DO0 ~ DI 7
  20  VALUE2 = INP(BASE + 2)  'Read DO16 ~ DI 23
  ```

- **Write operation:**

  The digital output states are written as 1 single byte to the port at address BASE+N (N=0,1,2,3). Data is written to all 8 bits as a single byte.

  For example:

  In BASIC:

  05 BASE=&H2A0

  06 VALUE1% = &H3F

  07 VALUE2% = &HF3

  10 OUT(BASE + 0), VALUE1% ‘ the digital outputs (DO0-DO7) will ’ be (00111111)

  20 OUT(BASE + 2), VALUE2% ‘ the digital outputs (DO16 - DO23) ’will be (11110011)

4.3 Programmable Interval Timer

Note : The material of this section is adopted from
"Intel Microprocessor and Peripheral Handbook Vol. II --Peripheral"

4.3.1 The Intel (NEC) 8254

The Intel(NEC) 8254 contains three independent, programmable, multi-mode 16 bit counter/timers. The three independent 16 bit counters can be clocked at rates from DC to 5 MHz. Each counter can be individually programmed with 6 different operating modes by appropriately formatted control words. The most commonly uses for the 8254 in microprocessor based system are:

- programmable baud rate generator
- Event counter
- binary rate multiplier
- real-time clock
- digital one-shot
- motor control

For more information about the 8254 , please refer to the NEC Microprocessors and peripherals or Intel Microprocessor and Peripheral Handbook.

4.3.2 The Control Byte

The 8254 occupies 8 I/O address locations in the ACL-7120 I/O map. As shown below.

Base + 4	LSB OR MSB OF COUNTER 0
Base + 5	LSB OR MSB OF COUNTER 1
Base + 6	LSB OR MSB OF COUNTER 2
Base + 7	CONTROL BYTE for Chip 0
Base + 8	LSB OR MSB OF COUNTER 3
Base + 9	LSB OR MSB OF COUNTER 4
Base + 10	LSB OR MSB OF COUNTER 5
Base + 11	CONTROL BYTE for Chip 1

Before loading or reading any of these individual counters, the **control byte** (Base + 7, Bae + 11**)** must be loaded first. The format of control byte is:

Control Byte: (Base + 7, Base + 11)

Bit	7	6	5	4	3	2	1	0
	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

- SC1 & SC1 - Select Counter (Bit7 & Bit 6)

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	ILLEGAL

- RL1 & RL0 - Select Read/Load operation (Bit 5 & Bit 4)

RL1	RL0	OPERATION
0	0	COUNTER LATCH
0	1	READ/LOAD LSB
1	0	READ/LOAD MSB
1	1	READ/LOAD LSB FIRST, THEN MSB

- M2, M1 & M0 - Select Operating Mode (Bit 3, Bit 2, & Bit 1)

M2	M1	M0	MODE
0	0	0	0
0	0	1	1
x	1	0	2
x	1	1	3
1	0	0	4
1	0	1	5

- BCD - Select Binary/BCD Counting (Bit 0)

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4 DECADES)

Note :

1. The count of the binary counter is from 0 up to 65,535.
2. The count of the BCD counter is from 0 up to 99,999.

4.3.3 Mode definition

In 8254, there are six different operating modes can be selected. The they are:

Mode 0 : Interrupt on terminal count

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.

(2) Write 2nd byte starts the new count.

Mode 1 : Programmable One-Shot.

The output will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at anytime without affecting the one-shot pulse.

The one-shot is re-triggerable, hence the output will remain low for the full count after any rising edge of the gate input.

Mode 2 : Rate Generator.

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input when low, will force the output high. When the gate input goes high, the counter will start form the initial count. Thus, the gate input can be used to synchronized by software.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

Mode 3 : Square Wave Rate Generator.

Similar to MODE 2 except that the output will remain high until one half the count has been completed (or even numbers) and go low for the other half of the count. This is accomplished by decrement the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

if the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2 After time-out, the output goes low and the full count is reloaded. the first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until time-out. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

In Modes 2 and 3, if a CLK source other then the system clock is used, GATE should be pulsed immediately following Way Rate of a new count value.

Mode 4 : Software Triggered Strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

Mode 5 : Hardware Triggered Strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is re-triggerable. the output will not go low until the full count after the rising edge of any trigger.

The detailed description of the mode of 8254, please refer the Intel Microsystem Components Handbook.

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