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cPCI-6840 Series

6U CompactPCI Pentium M
Single Board Computer

User's Manual

Manual Rev. 2.20

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Revision History

Revision	Release Date	Description of Change(s)
2.00	2005/01/19	Initial Release
2.10	2005/06/15	Correct specification errors, typos
2.20	2008/08/05	Update CPU support, GbE Controller version, Baseboard Management Controller, add cPCI-R6841P, IPMI instructions

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Preface

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Using this Manual

Audience and Scope

The cPCI-6840 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade CompactPCI modules.

Manual Organization

This manual is organized as follows:

Chapter 1, Introduction: Introduces the cPCI-6840, its specifications, features, and package contents.

Chapter 2, Jumpers and Connectors: Presents the board layout, connector pin assignments, and jumper setup.

Chapter 3, Getting Started: Explains how to install necessary components on the cPCI-6840.

Chapter 4, Windows Driver Installation: Describes the driver installation procedures.

Chapter 5, Utilities: Describes the operation of the cPCI-6840's watchdog timer and PXE Environment.

Chapter 6, IPMI User Guide: Describes the Intelligent Platform Management Interface.

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The cPCI-6840 is a 6U CompactPCI single board computer based on Intel® Pentium® M processor, 855GME and 6300ESB chipset. The Pentium® M processor comes with 1MB L2 cache in FC-mPGA package. The operating frequency ranges from 1.3GHz up to 1.6GHz. The cPCI-6840 is designed to be forward compatible with future 1.7GHz or higher speed Pentium® M compatible processor. The combination of the longevity of the Intel® 855GME and 6300ESB chipset and low power consumption of the Pentium® M CPU make the cPCI-6840 the best solution for embedded applications.

The 855GME supports 400MHz FSB and DDR333 memory up to 2GB. Two 200 pins SO-DIMM sockets support up to a maximum 2GB DIMM with 144-bit wide PC2700 registered DDR memory. A 32-bit 3D graphic controller is integrated to provide analog VGA or LVDS output.

The low power consumption 6300ESB south bridge provides dual PCI buses (PCI 64 bit/66-MHz and 32-bit/33MHz) to maximize I/O bandwidth. The I/O features are highly integrated, including four USB 2.0 port, two UART, two E-IDE channels, two Serial ATA ports, and a watchdog timer.

The 6300ESB's PCI 64 bit/66 MHz bus connects to two PMC sites, a dual port GbE controller 82546GB, and the universal PCI-to-PCI bridge PLX PCI-6540. The two 64-bit/66MHz PMC sites provide extreme expansion capability and flexibility for varieties of applications. The upper PMC site provides the rear I/O (Jn4 of PMC) capability for either SCSI PMC or telecom PMC modules.

The CompactPCI bus is based on the universal PCI-to-PCI bridge chip PCI-6540 (made by PLX Technology), providing either a transparent or non-transparent PCI interface. cPCI-6840 can be used as either a system slot or peripheral slot. cPCI-6840 can also be a server blade for stand alone operation on any non-system slot (without PCI bus). The cPCI-6840 is hot-swappable on peripheral slot or non-PCI bus slot which provide the best MTTR performance for telecom applications.

The cPCI-6840 is equipped with three Gigabit Ethernet (GbE) ports. Two GbE ports use the 82546GB dual ports GbE controllers

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on the 66MHz PCI bus to achieve the full communication bandwidth between the LAN and CPU. These two ports are connected to J3 (or rear I/O) which conform to the PICMG 2.16 specification. The third LAN port uses a 82541PI GbE controller on the 32-bit/33MHz PCI bus.

A Management Controller (BMC) (which follows the Intelligent Platform Management Interface (IPMI) v1.0 specification), is built into the system to meet the demands of high reliability and serviceability.

Please refer to the following block diagram for the cPCI-6840 architecture.

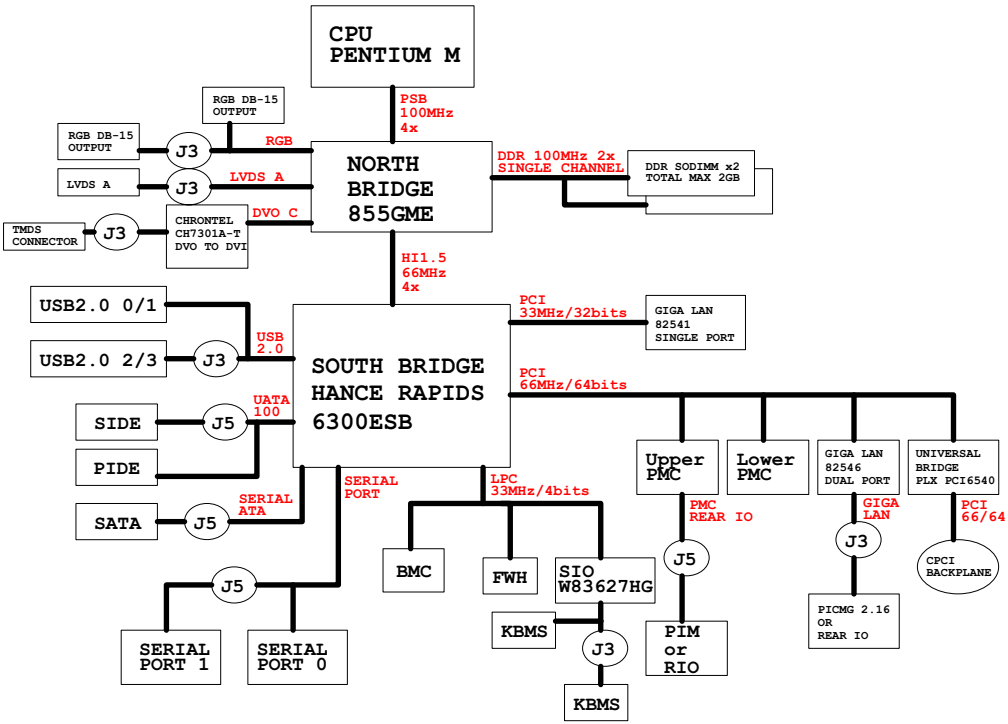


Figure 1-1: cPCI-6840 Block Diagram

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1.1 Main Functions

The following sections explain the main functions on cPCI-6840

CPU Support

The cPCI-6840 SBC is designed for the Intel® Pentium® M and Celeron® M Processors. The standard cPCI-6840 SBC comes with CPU socket which can be installed with µFC-PGA2 package CPU, with the following options:

- Pentium® M 1.3GHz, 1.4GHz, 1.5GHz, 1.6GHz, 1.7GHz, 1.8GHz, and 2.0GHz
- Celeron® M 1.3GHz

The Low Voltage (LV) or Ultra Low Voltage (ULV) version of the Pentium® M or Celeron® M Processors, which are in µFCBGA2 packages, can also be mounted on the cPCI-6840 SBC. However, µFCBGA2 CPU support is reserved for OEM programs only. The possible CPU options include:

- LV Pentium® M 1.1, 1.2, 1.3GHz
- ULV Celeron® M 600MHz

CompactPCI Bus Interface

The PLX Technology PCI-6540 is a tri-mode universal PCI-to-PCI Bridge and is used to implement the system/peripheral slot on the cPCI-6840. The tri-mode bridge is capable of operating in Transparent, Non-Transparent or Universal mode. The PCI-6540 Non-Transparent mode permits independent memory mapping of both primary and secondary buses with powerful configuration options to support intelligent subsystems. The Universal mode permits jumper-less configuration between application to CompactPCI interface at Peripheral Slot and System Slot. With the Universal option, the PCI-6540 Bridge can be configured as a transparent bridge in a System Slot supporting a host, or as a Non-Transparent bridge in a Peripheral Slot as an intelligent subsystem. These options allow the cPCI-6840 board to be inserted into both the Peripheral Slot and the System Slot.

The cPCI-6840 CompactPCI bus supports up to 64 bit/66 MHz PCI, as well as allowing the host bus and subsystem bus to

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operate at different speeds. Together with 64-bit to 32-bit access conversion, system architects can utilize the bridge and connect slower or higher speed controllers on primary or secondary bus, hence supporting independent speed and data bus frequency on either side of the PCI bus. The 64-bit/66 MHz PCI bus is backward compatible with 64-bit/33 MHz PCI, 32-bit/66 MHz PCI and 32-bit/33 MHz PCI busses. The SBC design is compliant with the PICMG 2.1 hot-swap specification so it can be hot-swappable in the peripheral slots. The cPCI-6840 can also be a hot-swappable server blade for stand alone operation on any non-PCI backplane without a system slot.

PCI Mezzanine Card (PMC) Interface

The cPCI-6840 supports up to two PMC slots at 64-bit/66 MHz PCI, providing expansion capability and flexibility for varieties of applications. The Jn4 rear I/O of the upper PMC site (PMC2) are implemented by connecting to the CompactPCI J5 connector, which complies with the PICMG 2.3 specification.

When the ADLINK SCSI PMC module (PMC-8631) is installed in PMC2 along with the cPCI-R6840 RTM, it can provide SCSI-320 interfaces on the rear panel of the Rear I/O Transition Module (RTM) for external storage devices. Some telecom PMC modules may also utilize the J24 rear I/O connection and the PMC Interface Module (PIM) site on the RTM to provide telecom I/O connection on the rear panel. The cPCI-R6841P RTM provides a PIM site.

IDE Interfaces

The cPCI-6840 supports dual Ultra ATA100 IDE channels. Primary IDE is implemented on the cPCI-6840 and Secondary IDE is routed to the RTM via J5 connector. Two 44-pin connectors for 2.5 inches IDE drives are reserved on both Primary and Secondary IDE interfaces.

The space of lower PMC site (PMC1) shall be used for installing the 2.5 inches IDE HDD, flash disk, or a CompactFlash carrier baord, DB-6840CF. When an application installs a storage device on the SBC, the PMC1 is occupied. Also note that the PMC1 connectors are not available on the cPCI-6840V because its front panel is occupied by VGA and PS2 keyboard/mouse connectors.

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On the RTM, the Secondary IDE is implemented on a Compact-Flash socket and a 44-pin connectors for 2.5 inches IDE drive.

Gigabit Ethernet Ports

The cPCI-6840 has three 10/100/1000Mbps Ethernet (GbE) ports. Every port is assigned a unique static MAC Address.

The onboard Intel® 82546GB dual-port Gigabit Ethernet controller provides two Ethernet ports. The 82546GB is connected to the 64-bit/66 MHz PCI bus to achieve the full communications bandwidth. The 82546GB supports IEEE 802.3x compliant flow control and IEEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation. The two GbE ports are connected to J3 based on PICMG 2.16 specifications.

The third LAN port uses a 82541PI controller on the 32-bit/33 MHz PCI bus. The RJ-45 connector of the third LAN port is on the front panel for system management or serviceability requirement. Users can disable or enable the third LAN port from the BIOS menu.

Universal Serial Bus (USB)

The cPCI-6840 provides four USB version 2.0 ports. Two ports are on the front panel and another two ports are on the RTM. The Universal Serial Bus (USB) provides a common interface to versatile peripherals such as keyboard, mouse, printer, USB flash disk, etc.

Serial I/O

Two serial ports are supported on cPCI-6840. COM1 is available as a RJ45 connector on the front panel. COM2 is also a standard RJ-45 connector on the rear panel of RTM. Both ports are be configured as Data Terminal Equipment (DTE). Firmware initializes the two serial ports as COM1 and COM2 with ISA I/O base addresses of 3F8h and 2F8h respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3. Optional COM3 and COM4 ports are available for ODM/OEM projects via the Winbond 83627HG. COM3 may be accessed via a cable, however COM4 may require a custom RTM.

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Keyboard/Mouse Controller

The cPCI-6840 uses a Winbond W83627HG to implement the keyboard/mouse controller. The controller is fully 8042 compatible. The cPCI-6840V provides a combo PS2 connector on the front panel. Both cPCI-6840 and 6840V route the keyboard and mouse signals to the J3.

Power Ramp Circuitry

The cPCI-6840 features a power controller with power ramp circuitry to allow the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by hot-swapping boards. This controlled ramping is a requirement of the CompactPCI hot-swap specification, PICMG 2.1 Version 1.0. The cPCI-6840's power controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. These limits are defined as 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

Watchdog Timer

Application can utilize watchdog timer to monitor system operation and to recover the operation when an abnormal and unexpected occurrence arises. The timeout period of the watchdog timer can be programmed from one micro second to ten minutes. Failure to strobe the watchdog timer within the programmed time period may result in an interrupt or reset request. A register bit can be enabled to indicate if the watchdog timer caused the interrupt or reset event. This watchdog timer register can be cleared by the system or auto-cleared after power-up, enabling system software to take appropriate action if the watchdog generated the reboot. Please refer Chapter 5, "Watchdog Timer," for more information.

Hardware Monitoring

The cPCI-6840 series use Winbond W83627HG to detect system voltages and temperatures. When it detects the voltages or temperatures over the safety range, it will inform the south bridge 6300ESB to send the signals out halting the system in order to protect the CPU board.

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Operating System Support

The cPCI-6840 is compatible with Microsoft® Windows 2000, Windows 2003 Server, Windows XP, Red Hat Linux 9 and VxWorks 5.5. The device drivers for Windows are included in the ADLINK CD. For Linux support and VxWork BSP, please contact ADLINK.

Baseboard Management

A baseboard management controller is implemented such that the system manager can control or get status form cPCI-6840 through the Intelligent Platform Management Bus (IPMB). The firmware is based on the Intelligent Platform Management Interface (IPMI) specification version 1.5. Please refer to Chapter 6 for the IPMI User Guide.

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1.2 Features

- Low power consumption, support Intel® Pentium® M and Celeron® M CPU from 1.3G up to 1.6G, and forward compatible to future higher speed CPU.
- Low power consumption Intel® 855GME and 6300ESB embedded chipset, provides longevity for OEM.
- Compliant with PICMG 2.0, 2.1, 2.9, and 2.16 specifications.
- 64-bit/66MHz CompactPCI interface based on PCI specifications, universal operations as system slot SBC or peripheral SBC.
- Two 64-bit/66MHz PMC sites, PMC rear I/O is reserved, optional PIM on RTM.
- Two 200-Pin SODIMM sockets support up to 2GB PC2700 DDR ECC SDRAM.
- Provides both IDE and Serial ATA interface for storage devices.
- Full feature I/O ports, including VGA, KB, MS, four USB 2.0, two COM ports, optional DVI, SCSI.

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1.3 Product List

The cPCI-6840 series products include the following SBCs and Rear I/O Transition Modules (RTM):

SBC

- cPCI-6840: Pentium® M SBC with two PMC sites
- cPCI-6840V: Pentium® M SBC with VGA/Keyboard/Mouse on the front panel, and one PMC site

RTM

- cPCI-R6840: RTM with SCSI rear I/O connector and DVI interface
- cPCI-R6841: RTM with IDE drive bay
- cPCI-R6841P: RTM with PMC Interface Module (PIM) site

The following table shows the possible combinations and configurations of cPCI-6840 SBC and RTM.

		SBC Features			RTM Features		
SBC	**RTM options**	**Front panel VGA KB/MS**	**PMC Sites**	**IDE(5) HDD option**	**IDE(5) HDD option**	**PIM Site**	**SCSI(5) and DVI connectors on rear faceplate**
6840	none	No	PMC1(1,2) PMC2(3)	Yes(1)	N/A		
	R6840		PMC1(1) PMC2		No	No	Yes(3)
	R6841		PMC1(1) PMC2		Yes	No	No
	R6841P		PMC1(1) PMC2		No	Yes	No
6840V	none	Yes	PMC2	Yes(1)	N/A		
	R6840		PMC2(3)		No	No	Yes(3)
	R6841		PMC2		Yes	No	No
	R6841P		PMC2		No	Yes	No

Table 1-1: cPCI-6840 Configurations

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Note 1: When an IDE HDD is installed on the front board, it occupies the PMC1 (lower PMC) site.

Note 2: When cPCI-6840 is functioning as a standalone without RTM, the PMC1 site shall be occupied by IDE storage device.

Note 3: The PMC-8631 is a SCSI-320 PMC module with rear I/O capability. When installing the PMC-8631 on the PMC2 (upper PMC) site, the cPCI-R6840/6840V can provide SCSI interfaces on the RTM and rear faceplate.

Note 4: The PIM will only work with a PMC module with rear I/O connectivity on PMC2 site.

Note 5: Should the user choose the SBC and RTM configuration, first consider where the storage device will be installed. Users can choose external SCSI device, IDE device on the RTM, or IDE device on the SBC.

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1.4 Specifications

cPCI-6840V SBC Specifications

CompactPCI Compliancy

- PICMG 2.0 CompactPCI Rev. 3.0
- PICMG 2.1 CompactPCI hot-swap specification R2.0
- PICMG 2.3 PMC I/O R1.0
- PICMG 2.9 System Management Bus
- PICMG 2.16 CompactPCI Packet Switch Backplane R1.0
- PCI Rev.2.1 compliant

Form Factor

- Standard 6U CompactPCI (board size: 233.35mm x 160mm)
- One slot (4TE or 4HP, 20.32mm) width

CPU/Cache

- Single Intel® Pentium® M 1.6/1.8 GHz or Celeron® M 1.3GHz Processors with µFC-PGA package
- 1MB/2MB on die L2 cache, 400MHz FSB

Chipset

- Intel® 855GME Graphic Memory Controller Hub (GMCH)
- Intel® 6300ESB I/O Hub

Host Memory

- Two SO-DIMM sockets, 2GB maximum
- Suppprt DDR333 SDRAM

BIOS

- Phoenix/Award Plug and Play BIOS with 4Mb Flash ROM
- BIOS write protection, provide anti-virus capability
- Bootable from USB storage devices including USB-Floppy, USB-ZIP, USB-CD-ROM, and USB-HDD.
- DMI BIOS Support: Desktop Management Interface (DMI)
- Onboard Ethernet ports can be disabled by BIOS setting (Intel® 82541PI Only)
- Option OEM BIOS features
  - Customized OEM splash image / power on screen

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NOTE:

Due to BIOS limitations, enabling the remote console function may occupy the same memory space as other ROM mapping add-on or boot-up devices such as Pre-boot Agent of Ethernet Boot ROM, SCSI Boot ROM, or add-on EIDE Boot ROM. It is recommended that only one ROM-mapping add-on or boot-up device be enabled when enabling the remote console function.

CompactPCI Bus Controller

- PLXtech PCI-6540 Univeral PCI-to-PCI bridge, supports transparent and non-transparent mode
- PCI Rev 2.1 compliant
- Supports 64-bit/66 MHz, 64-bit/33 MHz, 32-bit/33 MHz, and 32-bit/33 MHz

Graphic

- Integrated in 855GME Graphic Memory Controller Hub
- Shared memory, up to 32MB
- Dual channel display
- Front panel analog VGA DB-15 connector is available on cPCI-6840V only.
- LVDS and analog VGA signals are available on the J3 for RTM

Gigabit Ethernet

- Three 10/100/1000bps Gigabit Ethernet ports
- Dual GbE ports with Intel® 82546GB Ethernet controller, based on local 64-bit/66 PCI bus connected to J3 for Packet Switched Backplane (PSB) or RTM rear access
- Single GbE port with Intel® 82541PI Ethernet controller, based on 32-bit/33 PCI bus, RJ-45 connector on the front panel.

Onboard Peripherals

- Integrated in Intel® 6300ESB south bridge.

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- Bus master IDE controller supports two ultra ATA-100 interfaces.
  - Primary IDE is on SBC with 44-pin IDE connector. A 2.5 inches IDE HDD can be mounted on the lower PMC site.
  - Secondary IDE ports is on J5 for RTM extension.
- Four USB ports with USB Spec Rev. 2.0 compliant.
  - USB 0, 1 are on the front panel.
  - USB 2, 3 are on the RTM.
  - USB ports support 0.5A@5V for peripherals with individual over-current protection.
- Two SATA ports on RTM with data transfer rates up to 150 MB/s.
- Two RS-232 serial ports. COM1 on the front with RJ-45 type connector. COM2 is on the J3 and can be accessed on the RTM.
- PS2 keyboard / mouse connector on the front panel and RTM.

Front Panel LED Indicators and Reset

- Four LEDs on the front panel including storage access LED (RED), Power LED (GREEN), hot-swap status (Blue), and Watchdog timer LED (Yellow).
- Flush tact switch for system reset.

IPMI Interface

- Supports PICMG 2.9 secondary system managing bus. Implements IPMI functions as defined in the IPMI specification v 1.5
- Atmel ATMEGA128L Baseboard Management Controller (BMC)

Real -Time Clock and Nonvolatile Memory

- Build into Intel® 6300ESB southbridge RTC.
- Battery-backed memory is used for BIOS configuration
- Separate 3V coin cell CR2032 battery used for RTC and nonvolatile memory

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Environment

- Operating temperature: 0 to 55°C[(1)]
- Storage temperature: -20 to 80°C
- Humidity: 5% to 95% non-condensed
- Shock: 15G peak-to-peak, 11ms duration, non-operation
- Vibration:[(2)]
  - Non-operation: 1.88Grms, 5-500Hz, each axis
  - Operation: 0.5Grms, 5-500Hz, each axis, with 2.5” HDD

Safety Certificate and Test

- CE, FCC Class A
- All plastic material, PCB and Battery used are all UL-94V0 certified
- Designed for NEBS 3.0 requirement

Power Requirement[(3)]

Configuration	+5V	+3.3V	+12V	-12V	Total
Single Pentium 1.6G 512MB RAM, 20GB HDD	10.0A	4.1A	0.2A	0	> 61.2W

Table 1-2: Power Ratings

Note 1: Certified with ADLINK thermal design. The thermal performance is dependent on the chassis cooling design. Forced air-cooling with 50 CFM is required. Temperature limit of optional mass storage devices can impact the thermal specification.

Note 2: Operational vibration is limited by the 2.5 inches HDD. When application requires higher definition for anti-vibration, we recommend using Flash disk or CompactFlash.

Note 3: The power requirement is measured by Windows 2000 and a few computing power stressed application software. The following devices are installed when testing the power consumption: DDR333 RAM, a 20GB HDD, a 16MB CF, keyboard, mouse, and GbE. The power requirements for 5V and 3.3V rails are varied for different applications. This table lists the peak power requirement of 5V and 3.3V for different applications. The total power requirement is listed.

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cPCI-R6840 RTM Specifications

Form Factor

- Standard 6U CompactPCI rear I/O (board size: 233.35x80mm2)
- 1-slot (4TE/HP, 20.32mm) wide
- CompactPCI connectors: with rJ3 and rJ5, without rJ1, rJ2 and rJ4 connectors. AB type connector is used on rJ3 and rJ5.

Faceplate I/O Connectors

- Two GbE ports on RJ-45 connectors
- Serial COM2 ports on RJ-45 connectors
- Two USB ports: USB2, USB3 (type A connector)
- DVI connector
- SCSI connector (need use with ADLINK PMC-8631 SCSI module)
- DB-15 VGA connector

On Board Connectors

- IDE: Secondary IDE supported on one 44-pin connector, and one CompactFlash type-II socket.
- Serial ATA: Two S-ATA connectors
- LVDS

cPCI-R6841, cPCI-R6841P Specifications

Form Factor

- Standard 6U CompactPCI rear I/O (board size: 233.35x80mm2)
- 1-slot (4TE/HP, 20.32mm) wide
- CompactPCI connectors: with rJ3 and rJ5, without rJ1, rJ2 and rJ4 connectors. AB type connector is used on rJ3 and rJ5

Faceplate I/O Connectors

- Two GbE ports on RJ-45 connectors
- Serial COM2 ports on RJ-45 connectors

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- Two USB ports: USB2, USB3 (type A connector)
- VGA DB-15 connector
- PS2 Keyboard and Mouse connector

On Board Connectors

- IDE: Secondary IDE supported on one 44-pin connector, and one CompactFlash type-II socket. 2.5 inches HDD space is reserved (cPCI-R6841 only)
- Serial ATA: Two SATA connectors
- LVDS
- PIM socket (cPCI-R6841P only)

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I/O Connectivity

I/O	cPCI-6840		cPCI-6840V		CPCI	cPCI-R6840		cPCI-R6841(P)	
	Face-plate	On board	Face-plate	On board	J3/ J5	On board	Face-plate	On board	Face-plate
Serial Port (COM1)	RJ-45	--	RJ-45	--	--	--	--	--	--
Serial Port (COM2)	--	--	--	--	J3	--	RJ-45	--	RJ-45
USB (port 0, port 1)	Y	--	Y	--	--	--	--	--	--
USB (port 2, port 3)	--	--	--	--	J5	--	Y	--	Y
Gigabit Ether-net Port 1	--	2.16	--	2.16	J3	--	RJ-45	--	RJ-45
Gigabit Ether-net Port 2	--	2.16	--	2.16	J3	--	RJ-45	--	RJ-45
Gigabit Ether-net Port 3	RJ-45	--	RJ-45	--	--	--	--	--	--
Primary IDE	--	44-pin	--	44-pin	--	--	--	--	--
Secondary IDE	--	--	--	--	J5	40-pin 44-pin CF	--	40-pin 44-pin CF	--
Reset button	Y	--	Y	--	--	--	--	--	--
PMC1 (lower)	--	Y	--	--	--	--	--	--	--
PMC2 (upper)	--	Y	--	Y	J5	--	--	PIM (cPCI-R6841P only)	PIM (cPCI-R6841P only)
SCSI via PMC2 J24	--	--	Y	--	J5	SCSI	SCSI	--	--
PS2 KB/MS	--	--	Y	--	J3	--	--	--	Y
VGA	--	--	DB-15	--	J3	--	DB-15	--	DB-15
SATA	--	--	--	--	J5	Y	--	Y	--
LVDS	--	--	--	--	J3	Y	--	Y	--

Table 1-3: I/O Connectivity Table

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1.5 Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing materials for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check the following items are included in the package, if there are any items missing, please contact your dealer:

SBC:

- The cPCI-6840 or cPCI-6840V SBC (May be equipped with different specifications of CPU, RAM, and HDD).
- This User's Manual
- ADLINK CD
- RJ45-DB9 Cable

RTM:

- cPCI-R6840, cPCI-R6841, or cPCI-R6841P RTM
- HDD bracket and 44-pin IDE cable (cPCI-R6840/1 only)
- SATA HDD cable and power cable
- PS2 Y-cable (for cPCI-R6841(P) only)



The packaging of OEM versions with non-standard configuration, functionality, or package may vary according to different configuration requests.



The boards must be protected from static discharge and physical shock. Never remove any of the sock-eted parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a grounded wrist strap when servicing

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2 Jumpers and Connectors

This chapter illustrates the board layout, connector pin assignments, and jumper setup. Users should be familiar with the products before use. The following sections are included:

- cPCI-6840 and cPCI-6840V board outline
- cPCI-6840/6840V connectors pin assignments
- cPCI-6840/6840V jumpers setting
- cPCI-R684x series RTM board outline
- cPCI-R684x series RTM connectors pin assignments
- cPCI-R684x series RTM jumpers settings

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2.1 cPCI-6840 and cPCI-6840V Board Outline

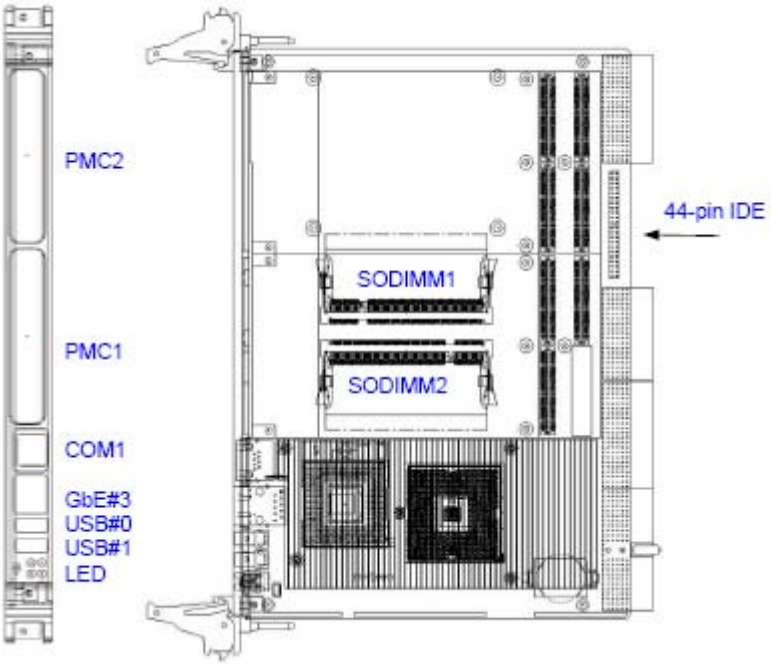


Figure 2-1: cPCI-6840 Front and Top View

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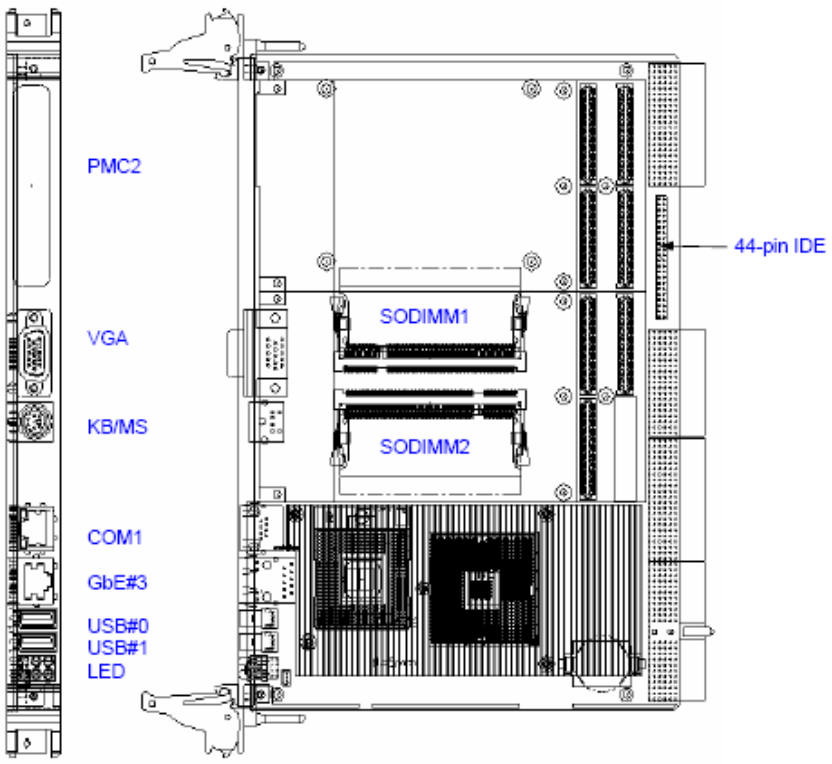
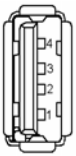


Figure 2-2: cPCI-6840V Front and Top View

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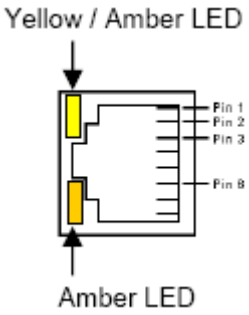
2.2 cPCI-6840/V Connector Pin Assignments

USB Connectors



PIN	SIGNAL
1	VCC
2	USB-
3	USB+
4	Ground

Ethernet (RJ-45) Connector



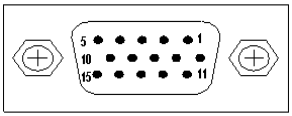
Pin #	Signal Name	Function
1	LAN_TDP1	Transmit Data1 +
2	LAN_TDN1	Transmit Data1 -
3	LAN_RDP2	Receive Data2 +
4	LAN_RDP3	Receive Data3 +
5	LAN_RDN3	Receive Data3 -
6	LAN_RDN2	Receive Data2 +
7	LAN_TDP4	Transmit Data4 +
8	LAN_TDN4	Transmit Data4 -

Status		Left LED (Amber)	Right LED (Yellow or Amber)
Network link is not established		OFF	OFF
10 Mbps (10 BaseT)	Link	Amber	OFF
	Active	Blinking Amber	OFF
100 Mbps (100 BaseTX)	Link	Amber	Yellow
	Active	Blinking Amber	Yellow
1000 Mbps (1000 BaseT)	Link	Amber	Amber
	Active	Blinking Amber	Amber

Table 2-1: Ethernet LED Status

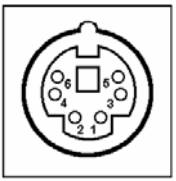
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VGA Connector (on cPCI-6840V only)



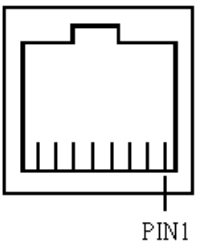
Signal Name	Pin	Pin	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V	9	10	GND
N.C.	11	12	DDCDAT
HSYNC	13	14	VSYNC
DDCCLK	15		

PS2 Connector (on cPCI-6840V only)



Pin	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

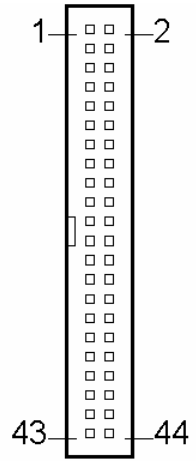
RS-232 Serial Port Connector



Pin	Signal Name
1	DCD, Data carrier detect
2	RTS, Request to send
3	DSR, Data set ready
4	TXD, Transmit data
5	RXD, Receive data
6	GND, ground
7	CTS, Clear to send
8	DTR, Data terminal ready

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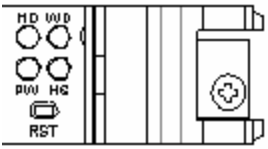
IDE Connector



Signal Name	Pin	Pin	Signal Name
BRSTDRVJ	1	2	GND
DDP7	3	4	DDP8
DDP6	5	6	DDP9
DDP5	7	8	DDP10
DDP4	9	10	DDP11
DDP3	11	12	DDP12
DDP2	13	14	DDP13
DDP1	15	16	DDP14
DDP0	17	18	DDP15
GND	19	20	NC
PDDREQ	21	22	GND
PDIOWJ	23	24	GND
PDIORJ	25	26	GND
PIORDY	27	28	PCSEL
PDDACKJ	29	30	GND
IRQ14	31	32	NC
DAP1	33	34	DIAG
DAP0	35	36	DAP2
CS1P	37	38	CS3PJ
IDEACTPJ	39	40	GND
+5V	41	42	+5V
GND	43	44	NC

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General Purpose LED definitions



LED	Color	Status	Description
IDE Media Access	Red	OFF	IDE idle
		ON	IDE access
Power OK	Green	OFF	System is not power-on or power failed
		ON	Power ON
Hot-swap status	Blue	OFF	Board inserted and power on OK.
		ON	Board inserted but not power on yet.
WDT LED	Yellow	OFF	WDT is not enabled
		Blinking	WDT is enabled

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PMC Connector Pin Assignments (J11, J21)

Signal Name	J11/J21 Pin	J11/J21 Pin	Signal Name	Signal Name	J11/J21 Pin	J11/J21 Pin	Signal Name
TCK(3)	1	2	-12V	+12V	1	2	TRST#(3)
GND	3	4	INTA#	TMS(2)	3	4	TDO(1)
INTB#	5	6	INTC#	TDI(2)	5	6	GND
BM1(1)	7	8	+5V	GND	7	8	N/C
INTD#	9	10	N/C	N/C	9	10	N/C
GND	11	12	+3.3V	BM2(2)	11	12	+3.3V
CLKP1	13	14	GND	RST#	13	14	BM3(3)
GND	15	16	GNT0#	+3.3V	15	16	BM4(3)
REQ0#	17	18	+5V	PME#	17	18	GND
VIO(4)	19	20	AD31	AD30	19	20	AD29
AD28	21	22	AD27	GND	21	22	AD26
AD25	23	24	GND	AD24	23	24	+3.3V
GND	25	26	CBE3#	IDSEL	25	26	AD23
AD22	27	28	AD21	+3.3V	27	28	AD20
AD19	29	30	+5V	AD18	29	30	GND
VIO(4)	31	32	AD17	AD16	31	32	CBE2#
P1FRAME#	33	34	GND	GND	33	34	IDSL_B(1)
GND	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSL	37	38	+5V	GND	37	38	STOP#
GND	39	40	LOCK#	PERR#	39	40	GND
N/C	41	42	N/C	+3.3V	41	42	SERR#
PAR	43	44	GND	CBE1#	43	44	GND
VIO(4)	45	46	AD15	AD14	45	46	AD13
AD12	47	48	AD11	M66EN	47	48	AD10
AD9	49	50	+5V	AD8	49	50	+3.3V
GND	51	52	CBE0#	AD7	51	52	REQ_B#(1)
AD6	53	54	AD5	+3.3V	53	54	GNT_B#(1)
AD4	55	56	GND	N/C	55	56	GND
VIO(4)	57	58	AD3	N/C	57	58	EREADY(1)
AD2	59	60	AD1	GND	59	60	RSTOUT#(1)
AD0	61	62	+5V	ACK64#	61	62	+3.3V
GND	63	64	REQ64#	GND	63	64	Monarch#(1)

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PMC Connector Pin Assignments (J13, J23, J24)

Signal Name	J13, J23 Pin	J13, J23 Pin	Signal Name	Signal Name	J24(5) Pin	J24(5) Pin	Signal Name
N/C	1	2	GND	PMCIO1	1	2	PMCIO2
GND	3	4	CBE[7]	PMCIO3	3	4	PMCIO4
CBE[6]	5	6	CBE[6]	PMCIO5	5	6	PMCIO6
CBE[5]	7	8	GND	PMCIO7	7	8	PMCIO8
VIO(4)	9	10	PAR64	PMCIO9	9	10	PMCIO10
AD63	11	12	AD62	PMCIO11	11	12	PMCIO12
AD61	13	14	GND	PMCIO13	13	14	PMCIO14
GND	15	16	AD60	PMCIO15	15	16	PMCIO16
AD59	17	18	AD58	PMCIO17	17	18	PMCIO18
AD57	19	20	GND	PMCIO19	19	20	PMCIO20
VIO(4)	21	22	AD56	PMCIO21	21	22	PMCIO22
AD55	23	24	AD54	PMCIO23	23	24	PMCIO24
AD53	25	26	GND	PMCIO25	25	26	PMCIO26
GND	27	28	AD52	PMCIO27	27	28	PMCIO28
AD51	29	30	AD50	PMCIO29	29	30	PMCIO30
AD49	31	32	GND	PMCIO31	31	32	PMCIO32
GND	33	34	AD48	PMCIO33	33	34	PMCIO34
AD47	35	36	AD46	PMCIO35	35	36	PMCIO36
AD45	37	38	GND	PMCIO37	37	38	PMCIO38
VIO(4)	39	40	AD44	PMCIO39	39	40	PMCIO40
AD43	41	42	AD42	PMCIO41	41	42	PMCIO42
AD41	43	44	GND	PMCIO43	43	44	PMCIO44
GND	45	46	AD40	PMCIO45	45	46	PMCIO46
AD39	47	48	AD38	PMCIO47	47	48	PMCIO48
AD37	49	50	GND	PMCIO49	49	50	PMCIO50
GND	51	52	AD36	PMCIO51	51	52	PMCIO52
AD35	53	54	AD34	PMCIO53	53	54	PMCIO54
AD33	55	56	GND	PMCIO55	55	56	PMCIO56

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Signal Name	J13, J23 Pin	J13, J23 Pin	Signal Name	Signal Name	J24(5) Pin	J24(5) Pin	Signal Name
VIO(4)	57	58	AD32	PMCIO57	57	58	PMCIO58
N/C	59	60	N/C	PMCIO59	59	60	PMCIO60
N/C	61	62	GND	PMCIO61	61	62	PMCIO62
GND	63	64	N/C	PMCIO63	63	64	PMCIO64

Note 1: These signals are not connected on the board.

Note 2: These signals are pulled high on the board.

Note 3: These signals are pulled low on the board.

Note 4: The VIO signals by default set to +3.3V via zero ohm resistors. Therefore, DO NOT apply any 5V only PMC module to the PMC sockets.

Note 5: J24 signals are connected to the CompactPCI J5 connector. To use these signals, the RTM needs to be either custom designed for special purposes or have a PIM connector available on RTM.

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CompactPCI J1 Pin Assignment

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#(4)	+3.3V	+5V	GND
24	GND	AD [1]	+5V	V (I/O)	AD [0]	ACK64#	GND
23	GND	+3.3V	AD [4]	AD [3]	+5V	AD [2]	GND
22	GND	AD [7]	GND	+3.3V	AD [6]	AD [5]	GND
21	GND	+3.3V	AD [9]	AD [8]	M66EN	C/BE [0]#	GND
20	GND	AD [12]	GND	V (I/O)	AD [11]	AD [10]	GND
19	GND	+3.3V	AD [15]	AD [14]	GND	AD [13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE [1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V (I/O)	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	BDSEL	TRDY#	GND
12-14	Key						
11	GND	AD [18]	AD [17]	AD [16]	GND	C/BE [2]#	GND
10	GND	AD [21]	GND	+3.3V	AD [20]	AD [19]	GND
9	GND	C/BE[3]#	IDSE	AD [23]	GND	AD [22]	GND
8	GND	AD [26]	GND	V (I/O)	AD[25]	AD [24]	GND
7	GND	AD [30]	AD [29]	AD [28]	GND	AD [27]	GND
6	GND	REQ#	GND	+3.3V	CLK	AD [31]	GND
5	GND	Reserved(1)	Reserved(1)	PCIRST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V (I/O)	INTP(1)	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK(3)	+5V	TMS(2)	TDO(1)	TDI(2)	GND
1	GND	+5V	-12V	TRST#(3)	+12V	+5V	GND

Note 1: These signals are not connected.

Note 2: These signals are pulled high on the board.

Note 3: These signals are pulled low on the board.

Note 4: To support PICMG 2.1 hot-swap for peripheral boards, the backplane should bus all peripheral slots ENUM# together to the system slot. The ENUM# signal can be polled by software or generates interrupt.

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CompactPCI J2 Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	GA4(2)	GA3(2)	GA2(2)	GA1(2)	GA0(2)	GND
21	GND	CLK6	GND	BRSV(1)	BRSV(1)	BRSV(1)	GND
20	GND	CLK5	GND	BRSV(1)	GND	BRSV(1)	GND
19	GND	GND	GND	ICMBSDA(1)	ICMBSCL(1)	ICMBALR(1)	GND
18	GND	BRSV(1)	BRSV(1)	BRSV(1)	GND	BRSV(1)	GND
17	GND	BRSV(1)	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSV(1)	BRSV(1)	DEG#	GND	BRSV(1)	GND
15	GND	BRSV(1)	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD [35]	AD [34]	AD [33]	GND	AD [32]	GND
13	GND	AD [38]	GND	V (I/O)	AD [37]	AD [36]	GND
12	GND	AD [42]	AD [41]	AD [40]	GND	AD [39]	GND
11	GND	AD [45]	GND	V (I/O)	AD [44]	AD [43]	GND
10	GND	AD [49]	AD [48]	AD [47]	GND	AD [46]	GND
9	GND	AD [52]	GND	V (I/O)	AD [51]	AD [50]	GND
8	GND	AD [56]	AD [55]	AD [54]	GND	AD [53]	GND
7	GND	AD [59]	GND	V (I/O)	AD [58]	AD [57]	GND
6	GND	AD [63]	AD [62]	AD [61]	GND	AD [60]	GND
5	GND	C/BE [5]#	GND	V (I/O)	C/BE [4]#	PAR 64	GND
4	GND	V (I/O)	BRSV(1)	C/BE [7]#	GND	C/BE [6]#	GND
3	GND	CLK4	GND	GNT3#	REQ#4	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note 1: These signals are not connected.

Note 2: These signals are pulled high on the board.

Note 3: These signals are pulled low on the board.

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CompactPCI J3 Pin Assignment

Pin	Z	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND	GND
18	GND	LPA_DA+	LPA_DA-	GND	LPA_DC+	LPA_DC-	GND
17	GND	LPA_DB+	LPA_DB-	GND	LPA_DD+	LPA_DD-	GND
16	GND	LPB_DA+	LPB_DA-	GND	LPB_DC+	LPB_DC-	GND
15	GND	LPB_DB+	LPB_DB-	GND	LPB_DD+	LPB_DD-	GND
14	GND	GND	GND	2.5V	GND	GND	GND
13	GND	LANA_1G#	LANA_100#	ACTA#	LINKA#	LANB_1G#	GND
12	GND	LINKB#	LANB_100#	ACTB#	5V(1)	5V(1)	GND
11	GND	IYAM0	IYAM1	IYAM2	IYAM3	ICLKAM	GND
10	GND	IYAP0	IYAP1	IYAP2	IYAP3	ICLKAP	GND
9	GND	IYBM0	IYBM1	IYBM2	IYBM3	ICLKBM	GND
8	GND	IYBP0	IYBP1	IYBP2	IYBP3	ICLKBP	GND
7	GND	CTS#	DSR#	RTS#	DTR#	NC	GND
6	GND	HSYNC	VSYNC	SIN	SOUT	DCD#	GND
5	GND	RED	GREEN	BLUE	DDCDATA	DDCCLK	GND
4	GND	TMDS1_TX1N	TMDS1_TX2N	TMDS1_TX3N	TMDS1_TXCN	TMDS_I2CC	GND
3	GND	TMDS1_TX1P	TMDS1_TX2P	TMDS1_TX3P	TMDS1_TXCP	TMDS_I2CD	GND
2	GND	LVDS_VDDEN	LVDS_TEN	LVDS_TCTL	NC	HTPLG	GND
1	GND	KBCLK	KBDATA	MSCLK	MSDATA	3.3V(1)	GND

Note: The +3.3V and +5V power lines are supplied from the main board to the RTM.

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CompactPCI J3 Signal Descriptions

Signals	Description	Signals	Description
KBCLK, KBDATA, MSCLK, MSDATA	Keyboard and Mouse signals	IYAM0/AP0, IYAM1/AP1, IYAM2/AP2, IYAM3/AP3, ICLKAM/AP, IYBM0, IYBM1, IYBM2, IYBM3, ICLKBM, IYBP0, IYBP1, IYBP2, IYBP3, ICLKBP, LVDS_VDDEN, LVDS_TEN, LVDS_TCTL.	LVDS Signals
TMDS1_TX1P/N, TX2P/N, TX3P/N, TXCP/N, TMDS_I2CC/I2CD, HTPLG	TMDS signals for DVI interfaced panel	LANA_1G#, LANA_100#, ACTA#, LINKA#, LANB_1G#, LANB_100#, ACTB#, LINKB#	LED Signals for Rear GbE LAN Connectors
HSYNC, VSYNC, RED, GREEN, BLUE, DDCDATA, DDCCLK	CRT signals	LPA_DA+/DA-, LPA_DB+/DB-, LPA_DC+/DC-, LPA_DD+/DD-, LPB_DA+/DA-, LPB_DB+/DB-, LPB_DC+/DC-, LPB_DD+/DD-,	GbE Signals for PICMG 2.16 or Rear Connectors
CTS#, DSR#, RTS#, DTR#, SIN, SOUT, DCD#	Serial port signals		

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CompactPCI J5 Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	PMC I/O 5	PMC I/O 4	PMC I/O 3	PMC I/O 2	PMC I/O 1	GND
21	GND	PMC I/O 10	PMC I/O 9	PMC I/O 8	PMC I/O 7	PMC I/O 6	GND
20	GND	PMC I/O 15	PMC I/O 14	PMC I/O 13	PMC I/O 12	PMC I/O 11	GND
19	GND	PMC I/O 20	PMC I/O 19	PMC I/O 18	PMC I/O 17	PMC I/O 16	GND
18	GND	PMC I/O 25	PMC I/O 24	PMC I/O 23	PMC I/O 22	PMC I/O 21	GND
17	GND	PMC I/O 30	PMC I/O 29	PMC I/O 28	PMC I/O 27	PMC I/O 26	GND
16	GND	PMC I/O 35	PMC I/O 34	PMC I/O 33	PMC I/O 32	PMC I/O 31	GND
15	GND	PMC I/O 40	PMC I/O 39	PMC I/O 38	PMC I/O 37	PMC I/O 36	GND
14	GND	PMC I/O 45	PMC I/O 44	PMC I/O 43	PMC I/O 42	PMC I/O 41	GND
13	GND	PMC I/O 50	PMC I/O 49	PMC I/O 48	PMC I/O 47	PMC I/O 46	GND
12	GND	PMC I/O 55	PMC I/O 54	PMC I/O 53	PMC I/O 52	PMC I/O 51	GND
11	GND	PMC I/O 60	PMC I/O 59	PMC I/O 58	PMC I/O 57	PMC I/O 56	GND
10	GND	PMC VIO(1)	PMC I/O 64	PMC I/O 63	PMC I/O 62	PMC I/O 61	GND
9	GND	D15	D14	D13	D12	D11	GND
8	GND	D10	D9	D8	D7	D6	GND
7	GND	D5	D4	D3	D2	D1	GND
6	GND	D0	REQ	IOW#	IORDY	IOR#	GND
5	GND	DIAG	IRQ15	ACK#	ACT#	RST#	GND
4	GND	CS#1	CS#3	A0	A1	A2	GND
3	GND	SATA1_TXN	SATA1_TXP	RSVD	SATA1_RXN	SATA1_RXP	GND
2	GND	SATA2_TXN	SATA2_TXP	5VS (2)	SATA2_RXN	SATA2_RXP	GND
1	GND	USB2_DN	USB2_DP	USB_OC#	USB3_DN	USB3_DP	GND

Note 1: The VIO is connected to the VIO plane (default is +3.3V) of the PMC slot #2.

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2.3 cPCI-6840/V Switch and Jumper Settings

The following table lists the switch and jumpers on the cPCI-6840 and cPCI-6840V.

Switch	Function
SW1	Reset
JP1	Enforce SYSEN#
JP3	Clear CMOS Content
Miniature switch on ejector	Hot-swappable front panel ejector

Table 2-2: Switch and Jumper Functions

SW1: Reset Button

SW1 is a push-button on the front panel. Pressing SW1 generates a hard reset.

JP1: Enforce System Enable

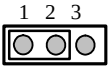
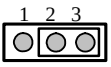
Status	JP1
SYSEN# Open (Default)	
SYSEN# GND	

Table 2-3: JP1 Settings

The system enable signal (SYSEN#) is located on the CompactPCI J2 connector's C2 position. The SYSEN# is used to determine the operation mode of the SBC. When the SYSEN# on the backplane is tightened to GND, then the SBC will boot as a CompactPCI system slot otherwise the SBC will boot as a CompactPCI peripheral slot.

However, for some "none PCI bus" backplanes, the SYSEN# pin on the backplane is floating. Install JP1 will short the SYSEN# signal to GND and enforce the cPCI-6840/V as a system slot SBC.

Please note do not install JP1 when the cPCI-6840 is installed in a peripheral slot of CompacPCI system.

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JP3: Clear CMOS

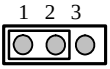
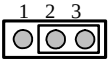
Status	JP3
Normal operation (Default)	
Clear CMOS	

Table 2-4: JP3 Settings

The CMOS RAM stores the real time clock (RTC) information, BIOS configuration, and default BIOS setting. The CMOS is powered by the button cell battery when the system is power off.

Please follow the following steps to erase the CMOS RAM data:

1. Unplug the SBC from system
2. Short pins 2 and 3 of JP3, then reinstall the jumper to normal location
3. Insert the SBC back to the chassis.

Miniature Switch on the Front Panel Lower Ejector:

The miniature switch is designed for power control and hot-swap control. When the cPCI-6840 is plugged into system slot, the whole system will not be powered up until the lower ejector is closed. It will issue a power button signal when users open the lower ejector. When the cPCI-6840 is plugged into a peripheral slot, the entire system will not be powered up until the lower ejector is closed and it will send out an ENUM# signal to the system to indicate that a board has been plugged into the CompactPCI backplane. When the lower ejector is opened, the cPCI-6840 will send out an ENUM# to the system and wait for the command from system.

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2.4 RTM Board Outline

The differences between cPCI-R6840 and cPCI-R6841 are described as following. The cPCI-R6840 implements a DVI connector and two SCSI connectors. The cPCI-R6841 implements a PS2 connector and four screw holes for 2.5' HDD and PIM connectors (mouted either in the 2.5" HDD bay or with the PIM card on the cPCI-R6841).

cPCI-R6840 Top View and Faceplate

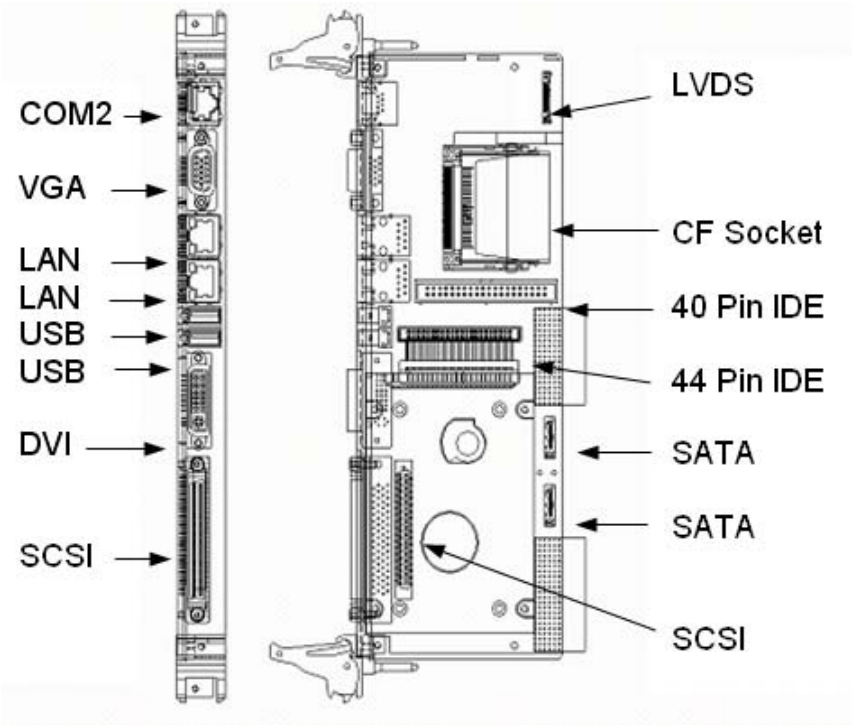


Figure 2-3: cPCI-R6840 Board Layout

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cPCI-R6841P Top View and Faceplate

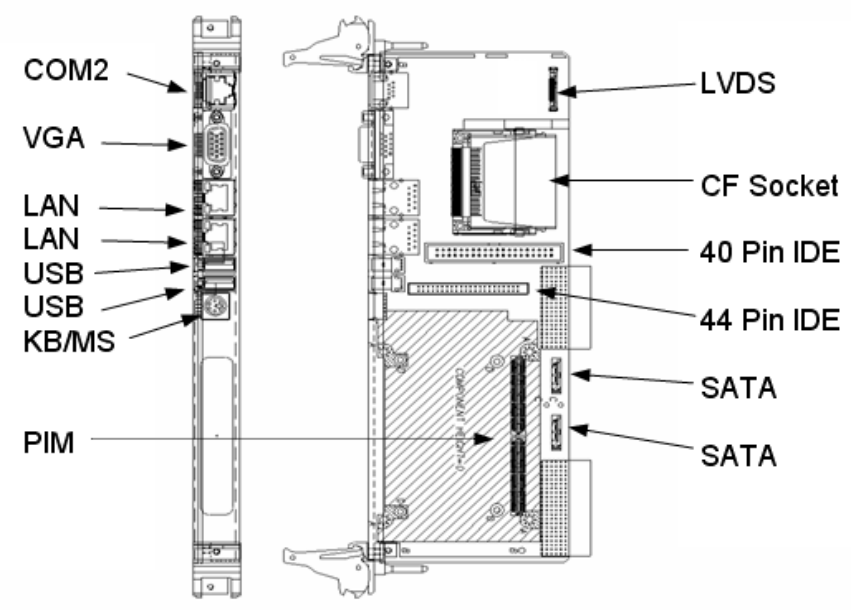


Figure 2-4: cPCI-R6841P Diagram

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2.5 RTM Connectors Pin Assignments

The USB, GbE LAN, IDE, RS-232 COM2, VGA, and PS2 Keyboard/Mouse combo connector pin assignments on the cPCI-R684X series RTM are identical to those on the SBC. Please refer to section 2.3 for pin assignments.

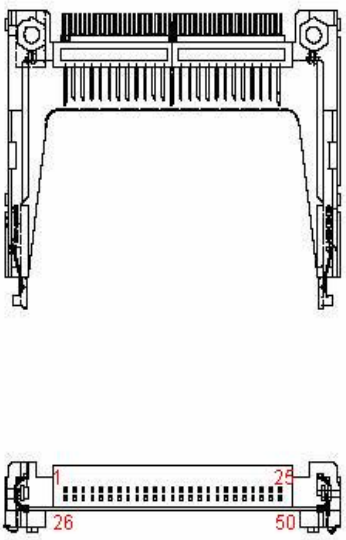
The CompactFlash, DVI, LVDS, SATA, IDE, PIM, and SCSI connector pin assignments are illustrated in the following sections.

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CompactFlash Connector

NOTE:

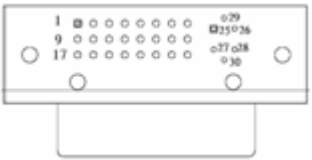
The CompactFlash is shared with Secondary IDE. Only two devices can be installed simultaneously



Signal Name	Pin	Pin	Signal Name
GND	1	26	GND
SDD3	2	27	SDD11
SDD4	3	28	SDD12
SDD5	4	29	SDD13
SDD6	5	30	SDD14
SDD7	6	31	SDD15
SDCS#1	7	32	SDCS#3
GND	8	33	GND
GND	9	34	SDIOR#
GND	10	35	SDIOW#
GND	11	36	+5V
GND	12	37	IDEIRQ15
+5V	13	38	+5V
GND	14	39	PCSEL
GND	15	40	NC
GND	16	41	SIDERST#
GND	17	42	SIORDY
SDA2	18	43	NC
SDA1	19	44	SDDACK#
SDA0	20	45	IDEACT#
SDD0	21	46	S66DECT
SDD1	22	47	SDD8
SDD2	23	48	SDD9
IOIS16#	24	49	SDD10
GND	25	50	GND

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DVI Connector (cPCI-R6840 only)



Pin	Signal	Pin	Signal
1	TX2-	16	HTPLG
2	TX2+	17	TX0-
3	GND	18	TX0+
4	NC	19	GND
5	NC	20	NC
6	I2CCLK	21	NC
7	I2CDATA	22	GND
8	VSYNC	23	TXC+
9	TX1-	24	TXC-
10	TX1+	25	RED
11	GND	26	GREEN
12	NC	27	BLUE
13	NC	28	HSYNC
14	+5V	29	GND
15	GND	30	GND

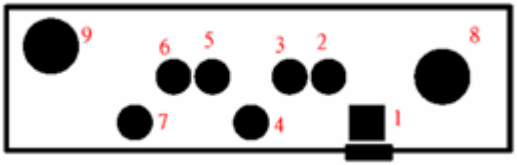
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LVDS A and LVDS B connectors



Pin	Signal	Pin	Signal
1	3.3V	12	IYP2
2	3.3V	13	GND
3	GND	14	ICLKM
4	GND	15	ICLKP
5	IYM0	16	GND
6	IYP0	17	IYM3
7	GND	18	IYP3
8	IYM1	19	GND
9	IYP1	20	GND
10	GND	21	GND
11	IYM2	22	GND

SATA1 and SATA2 connectors



Pin	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND
8	NC
9	NC

SCSI Connector (cPCI-R6840 only)

There are two SCSI-68 connectors on cPCI-R6840: the CN10 is onboard 180 degrees connector for inner chassis SCSI drives; the CN14 is on the rear faceplate for external SCSI drives connection.

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PIM Connector (cPCI-R6841P only)

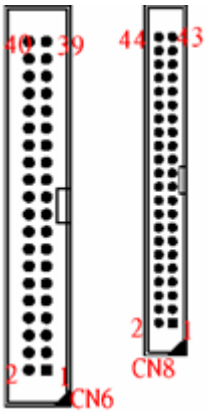
JN1				JN2			
Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
PMCIO01	1	2	PMCIO02	NC	1	2	NC
PMCIO03	3	4	PMCIO04	NC	3	4	NC
PMCIO05	5	6	PMCIO06	5V	5	6	NC
PMCIO07	7	8	PMCIO08	NC	7	8	NC
PMCIO09	9	10	PMCIO10	NC	9	10	3.3V
PMCIO11	11	12	PMCIO12	NC	11	12	NC
PMCIO13	13	14	PMCIO14	GND	13	14	NC
PMCIO15	15	16	PMCIO16	NC	15	16	NC
PMCIO17	17	18	PMCIO18	NC	17	18	GND
PMCIO19	19	20	PMCIO20	NC	19	20	NC
PMCIO21	21	22	PMCIO22	5V	21	22	NC
PMCIO23	23	24	PMCIO24	NC	23	24	NC
PMCIO25	25	26	PMCIO26	NC	25	26	3.3V
PMCIO27	27	28	PMCIO28	NC	27	28	NC
PMCIO29	29	30	PMCIO30	GND	29	30	NC
PMCIO31	31	32	PMCIO32	NC	31	32	NC
PMCIO33	33	34	PMCIO34	NC	33	34	GND
PMCIO35	35	36	PMCIO36	NC	35	36	NC
PMCIO37	37	38	PMCIO38	5V	37	38	NC
PMCIO39	39	40	PMCIO40	NC	39	40	NC
PMCIO41	41	42	PMCIO42	NC	41	42	3.3V
PMCIO43	43	44	PMCIO44	NC	43	44	NC
PMCIO45	45	46	PMCIO46	GND	45	46	NC
PMCIO47	47	48	PMCIO48	NC	47	48	NC
PMCIO49	49	50	PMCIO50	NC	49	50	GND
PMCIO51	51	52	PMCIO52	NC	51	52	NC
PMCIO53	53	54	PMCIO54	5V	53	54	NC
PMCIO55	55	56	PMCIO56	NC	55	56	NC
PMCIO57	57	58	PMCIO58	NC	57	58	3.3V
PMCIO59	59	60	PMCIO60	NC	59	60	NC
PMCIO61	61	62	PMCIO62	NC	61	62	NC
PMCIO63	63	64	PMCIO64	NC	63	64	NC

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Secondary IDE .

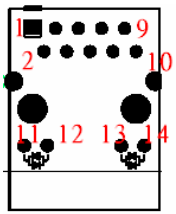
NOTE:

There are three Secondary IDE connectors (40-pin, 44-pin, CompactFlash), but only two devices can be installed simultaneously



Pin	Signal	Pin	Signal	Pin	Signal
1	Reset	16	D14	31	IRQ
2	GND	17	D0	32	IOIS16#
3	D7	18	D15	33	A1
4	D8	19	GND	34	DIAG
5	D6	20	NC	35	A0
6	D9	21	REQ	36	A2
7	D5	22	GND	37	CS#1
8	D10	23	IOW#	38	CS#3
9	D4	24	GND	39	ACT#
10	D11	25	IOR#	40	GND
11	D3	26	GND	41	5V
12	D12	27	IORDY	42	5V
13	D2	28	NC	43	GND
14	D13	29	ACK#	44	NC
15	D1	30	GND		

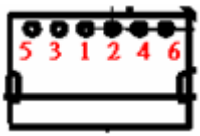
GigaLAN Connectors



Pin	Signal	Pin	Signal	Pin	Signal
1	MX0+	6	VCC	11	LAN_1G#
2	MX0-	7	MX2+	12	LAN_100#
3	MX1+	8	MX2-	13	LINKA#
4	MX1-	9	MX3+	14	ACT#
5	VCC	10	MX3-		

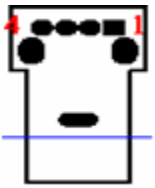
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PS2 connector



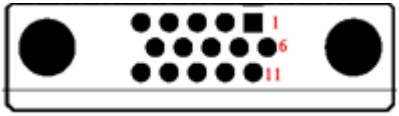
Pin	Signal	Pin	Signal	Pin	Signal
1	KBDATA	3	GND	5	KBCLK
2	MSDATA	4	VCC	6	MSCLK

USB connectors



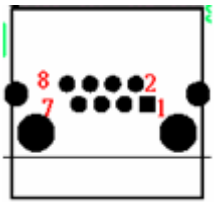
Pin	Signal
1	VCC
2	DN
3	DP
4	GND

CRT connector



Pin	Signal	Pin	Signal	Pin	Signal
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	DDC_DATA
3	BLUE	8	GND	13	HSYNC
4	NC	9	GND	14	VSYNC
5	GND	10	GND	15	DDC_CLK

COM port connector



Pin	Signal	Pin	Signal
1	DCD#	5	SIN#
2	RTS#	6	GND
3	DSR#	7	CTS#
4	SOUT#	8	DTR#

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2.6 RTM Switch and Jumper Setting

cPCI-R6840

Switch	Functions
SW1 and SW2	Enable either 2.16 plane or RTM LAN2 access
SW3 and SW4	Enable either 2.16 plane or RTM LAN1 access
SW5	Enable rear VGA signals
CN9	Determine the CF as master or slave

Table 2-5: RTM Switch and Jumper Settings

LAN1 and LAN2 Dip Switches on RTM

The cPCI-6840 supports LAN1 and LAN2 on both the 2.16 backplane and rear I/O. PICMG 2.16 backplane and rear I/O cannot be accessed simultaneously. SW1 and SW2 must be set to either the 2.16 backplane or the RTM. The table below shows how to set the DIP switches to enable either the 2.16 backplane or RTM for LAN1 and LAN2.

Connect to:	LAN2 (SW1 and SW2)	LAN1 (SW3 and SW4)
PICMG 2.16 Backplane	All OFF	All OFF
Rear faceplate RJ-45 connectors	All ON (default)	All ON (default)

Table 2-6: LAN Dip Switch Settings



All switches in the SW1, SW2, SW3, and SW4 bank must all be either ON or OFF. 2.16 backplane and rear LAN1 and LAN2 cannot be accessed simultaneously.

SW5: VGA Signal Enable

The cPCI-6840 supports VGA outputs to both front and rear panels. If SW5 on the RTM is set all off, the RGB signal won't be connected to the rear connector. Users should set SW5 on to enable the rear VGA signal output (default: All ON).

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Master/Slave Selection of Compact Flash (CN9)

The cPCI-R6840 RTM uses a jumper (CN9) to determine master or slave IDE state of the CompactFlash disk.

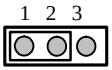
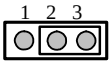
CF Status	CN9
Slave (default)	
Master	

Table 2-7: CF Master/Slave Jumper Settings

cPCI-R6841(P) Jumpers and Other Settings

SW1, SW4	All ON (default)	LAN2 rear panel
	All OFF	LAN2 2.16 backplane
SW2, SW3	All ON (default)	LAN1 rear panel
	All OFF	LAN1 2.16 backplane
SW5	All ON (default)	Rear VGA on
	All OFF	Rear VGA off

Table 2-8: cPCI-R6841(P) Switch Settings

Master/Slave Selection of Compact Flash (CN8)

The cPCI-R6841(P) RTM uses a jumper (CN8) to determine master or slave IDE state of the CompactFlash disk

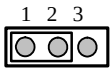
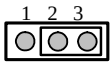
CF Status	CN8
Slave (default	
Master	

Table 2-9: JP3 Settings

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3 Getting Started

This chapter explains how to install necessary components on the cPCI-6840/cPCI-6840V and cPCI-R6840 and cPCI-R6841(P) RTMs, including:

- CPU and heat sink
- Memory module installation
- HDD installation on main board – for cPCI-6840
- HDD installation on main board – for cPCI-6840V
- HDD installation on RTM
- CF installation on RTM
- PMC installation
- RTM installation
- Main board installation

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3.1 CPU and Heatsink

The cPCI-6840 and cPCI-6840V support the Intel® Pentium® M processor. The heat sink is necessary to help the CPU heat dissipation. Please follow the illustration below to install your heat sink.

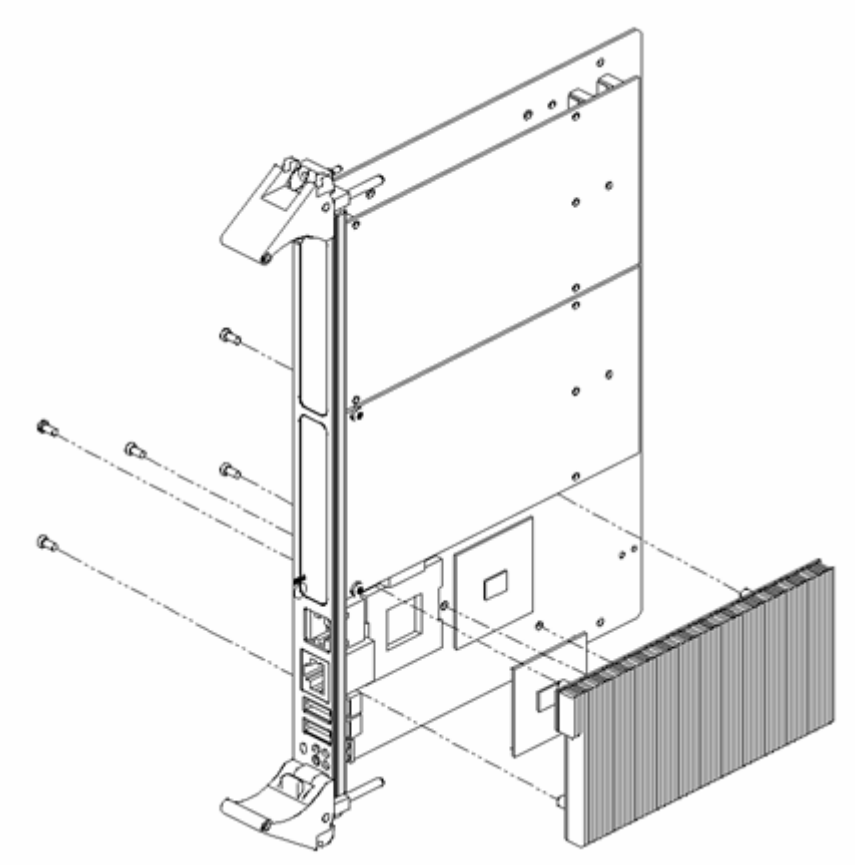


Figure 3-1: Heatsink installation

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3.2 Memory Module Installation

The cPCI-6840 series SBC supports up to two sockets of 200-pin PC2700 ECC DDR-SDRAM. The maximum memory capacity is 2GB. If memory modules are pre-installed when the package is received, this section may be skipped.

The GMCH system memory controller directly supports the following:

- One channel of PC1600/2100/2700 SO-DIMM DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mb, 256-Mb, and 512-Mb technology
- Up to 2GB (512-Mb technology) using high density devices with two SO-DIMMs

Technology	Width	System Memory Capacity	System Memory Capacity with Stacked Memory
128Mb	16	256MB	-
256Mb	16	512MB	-
512Mb	16	1GB	-
128Mb	8	256MB	512MB
256Mb	8	512MB	1GB
512Mb	8	1GB	2GB

Table 3-1: DDR SDRAM Memory Capacity

While installing the memory, ensure that the SODIMM modules are firmly seated in its sockets and do not interfere with any components.

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3.3 HDD Installation on Main Board – for cPCI-6840

A slim-type 2.5-inch HDD can be mounted to the cPCI-6840 main board. If a HDD is pre-installed the cPCI-6840 this section may be skipped.

1. Remove the PMC from the PMC slot if any.
2. Screw the bolts on to the HDD and attach a 44-pin IDE cable.
3. Install the assembly onto the board; tighten the four screws from the bottom side of the main board to secure the HDD in to place.
4. Attach the other end of the 44-pin IDE cable to CN6 onboard.

Please follow the picture shown below to install your 2.5” Hard Disk.

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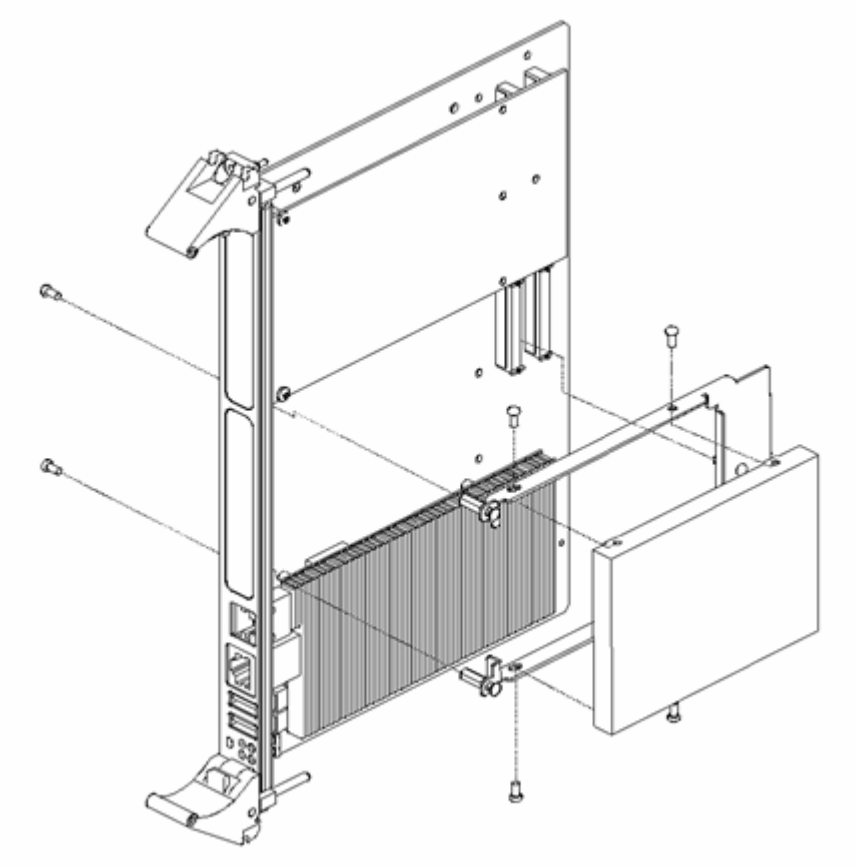


Figure 3-2: cPCI-6840 2.5” Hard Disk Installation

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3.4 HDD Installation on Main Board – for cPCI-6840V

A slim-type 2.5-inch HDD can be mounted to the cPCI-6840V main board. If a HDD is pre-installed when the cPCI-6840V is received, this section may be skipped.

1. Screw the HDD on the HDD bracket and attach 44-pin IDE cable.
2. Install the assembly on to the board; tighten the three screws from the bottom side of the main board to secure the HDD in place.
3. Attach the other end of the 44-pin IDE cable to CN6 on board.

Please follow the illustration shown below to install your 2.5” Hard Disk.

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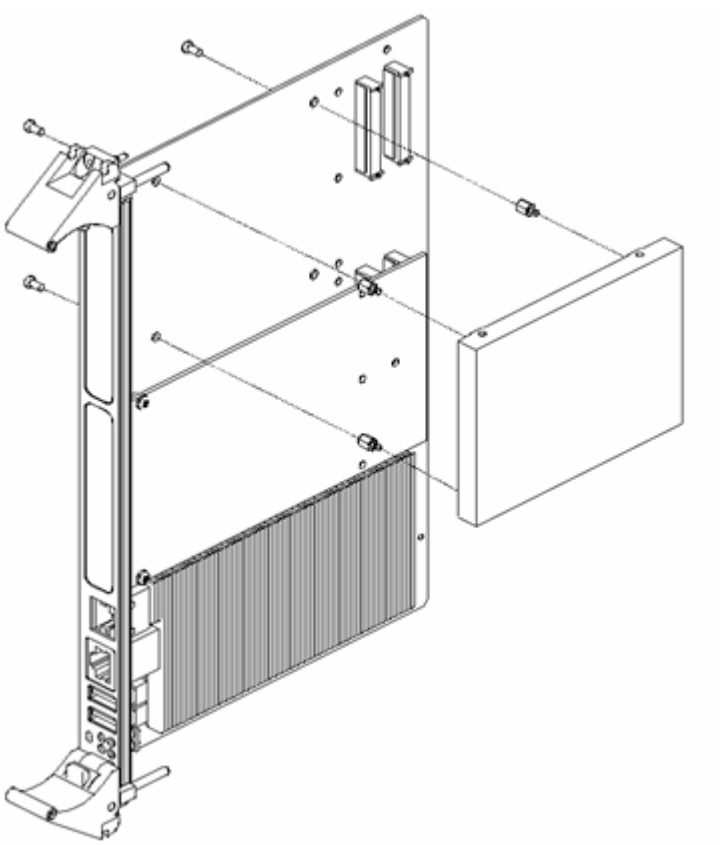


Figure 3-3: cPCI-6840V 2.5” Hard Disk Installation

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3.5 HDD Installation on RTM

A 2.5-inch HDD or Flash Disk can be installed on the cPCI-R6841 directly. If a HDD is pre-installed when the cPCI-R6841 is received, please skip this section.

1. Attach the IDE cable to the HDD or Flash Disk
2. Put the HDD on component side of the RTM, align the HDD mounting holes with the holes on the PCB.
3. Tighten the four screws from the bottom side of the RTM to secure the HDD in place
4. Connect the IDE cable to the 44-pin connector.

3.6 CF Installation on RTM

The CompactFlash card is widely applied in digital consumer devices such as PDAs, digital cameras and MP3 players. Due to its CF anti-shock, anti-vibration, better environment tolerance, low power consumption, small form factor, and high reliability characteristics, it has been widely accepted in mission critical embedded applications.

The CompactFlash socket is available on the (cPCI-R6840 and cPCI-R6841(P) rear transition modules.

3.7 PCI Mezzanine Card (PMC) Installation

The PMC slots are designed as 3.3V and/or as a universal PCI interfaces. The PMC sites are keyed to prevent users from installing a 5V only PMC module.

Refer to section 2.2 for detailed PMC I/O signal routing. If a HDD is mounted to the main board, the HDD will occupy one of the PMC slots.

To install the PMC modules:

1. Prepare an ESD protected area including an anti-ESD table and ESD strap. Attach the ESD strap to your wrist and connect the end of the ESD strap to ground of the anti-ESD table.
2. Remove the PMC panel from the front panel.

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3. Install the PMC module on to the PMC sockets.
4. Screw the PMC mounting bolts to the main board from the bottom side up to fix the PMC module in place.

3.8 RTM Installation

This section describes important information regarding the use of the rear I/O connections. Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-6840 series and related RTM, make sure the RTM is the correct model that matches each other.

Note: Use the correct RTM to enable functions (I/O interfaces) on rear side. The RTM or system board can be damaged if the incorrect RTM is used.

Some I/O ports are supported on both the front board and the RTM, including Keyboard, Mouse, VGA and USB. These I/O ports can be connected either via the front or rear modules but DO NOT access these ports on both front and rear simultaneously.

3.9 Main Board Installation

Use the following procedure to install the cPCI-6840/cPCI-6840V main board to its CompactPCI chassis.

1. Refer to the relevant chassis user manual for pre-preparation of the chassis before installing the main board. Users need to assign a slot to the board. Be sure to select the correct slot (system or peripheral) depending on the operational purpose of the board. The system power may now be powered on.
2. Remove the blank face panel from the slot.
3. Align the top and bottom edges of the board with the card guides on the chassis then slide the board into the chassis until resistance is felt. If the system power is on, the blue LED (hot-swap status) should light up.
4. Move the upper and lower ejectors in an inward direction simultaneously. Note that slight resistance will be felt while inserting the board. If this resistance is more than under normal conditions, check to ensure that there are

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no pins bent on the backplane and that the board's connector pins are aligned properly with the connectors on the backplane.

5. Verify that the board is seated properly. With the board in place and the blue LED on, wait for the blue LED to go out before proceeding to the next step.
6. Secure the two screws hidden behind the upper and lower ejector; connect the proper cables to the board.

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4 Windows Driver Installation

The following sections show the driver installation procedures for Windows 2000, Windows XP or Windows Server 2003. When installing the Windows drivers, we recommend the following steps:

1. Fully install the Windows properly before installing any driver. Most of the standard I/O devices' driver will be installed during the standard Windows installation.
2. Install the chipset driver.
3. Install the graphic driver and utilities.
4. Install the LAN drivers.

It is recommended that the chipset, graphic, and LAN drivers provided on the ADLINK CD be used to ensure compatibility. Please contact ADLINK for support for Linux drivers and VxWorks BSP.

4.1 Chipset Drivers Installation

1. Ensure Windows 2000/XP/Windows Server 2003 be fully installed and running prior to executing the "Intel Chipset Software Installation Utility".
2. Close any running applications.
3. The files are stored in an integrated application setup program. This program is designed for a Windows 2000, XP and Windows Server 2003.
4. Locate the directory X:\cPCI\cPCI-6840\Chipset in the CD-ROM, and then run "infinst_enu.exe".
5. Click 'Next' on the Welcome screen to read and agree to the license agreement. Click Yes if you agree to continue. NOTE: If you click No, the program will terminate.
6. Click 'Next' on Readme Information screen to install INF files.
7. Click 'Finish' to restart the system when prompted to do so.
8. Follow the screen instructions and use the default settings to complete the setup when Windows 2000/XP/

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Windows Server 2003 re-starts. Upon re-start, Windows will display that it has found new hardware and is installing drivers for them. If New Hardware Found dialog box is displayed requesting the location of the drivers, use the mouse to click on the scrollbar and click on the <Windows directory>.

9. Select Yes, when prompted to re-start Windows 2000/XP/Windows Server 2003.

4.2 VGA Driver Installation

1. Boot Windows 2000/XP/Windows Server 2003.
2. The driver is included in the driver CD. Run the win2k_xp142.exe under the following directory: X:\cPCI\cPCI-6840\VGA.
3. Click ‘Next’ on the Welcome screen. Select ‘Typical’ on the setup type screen and click Next’.
4. Use default program folders on Select Program Folder screen. Click ‘Next’ to install driver.
5. Finally, click 'Finish' to restart.

4.3 LAN Driver Installation

This section describes the LAN driver installation for the Intel® 82541PI and Intel® 82546GB onboard Ethernet controllers. The relevant drivers are located in the following driver CD directory:

1. Boot Windows 2000/XP/Windows Server 2003.
2. The driver is included in the driver CD. Run the PRO2KXP.exe under the following directory: X:\cPCI\cPCI-6840\LAN.
3. Read the license agreement. Click 'I accept the terms in the license agreement’ if you agree to continue.
4. Location to Save Files, click Next to save files in folder.
5. Intel® PRO Network Connections. Click Install Software to install drivers and Intel PROSet.

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5 Utilities

5.1 Watchdog Timer

This section explains the operation of the cPCI-6840's watchdog timer. It provides an overview of watchdog operation and features, as well as a sample code to help you learn how the watchdog timer works.

WDT Overview

The primary function of the watchdog timer is to monitor the cPCI-6840's operation and to generate IRQ or reset the system if the software fails to function as programmed. The major features of the watchdog timer are:

- Enabled and disabled through software control
- Armed and strobed through software control

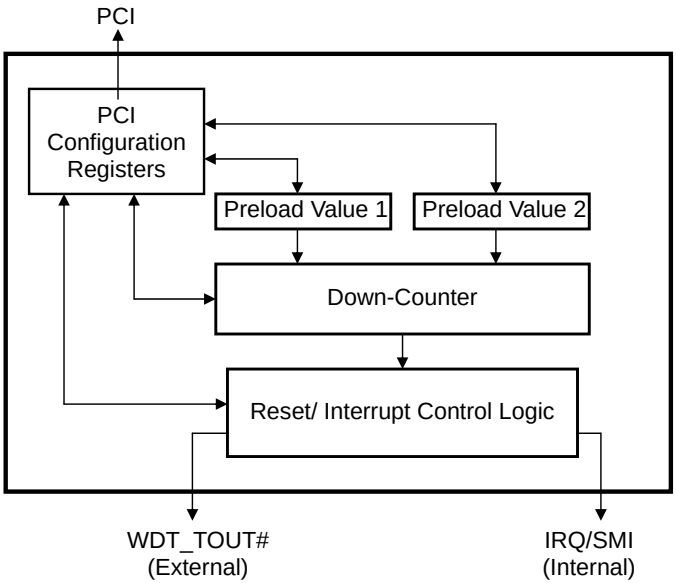


Figure 5-1: WDT Block Diagram

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The cPCI-6840's custom watchdog timer circuit is integrated in the 6300ESB south bridge.

The Intel® 6300ESB ICH includes a two-stage Watchdog Timer (WDT) that provides a resolution ranging from one micro second to ten minutes. The timer uses a 35-bit Down-Counter. The counter is loaded with the value from the first Preload register. The timer is then enabled and it starts counting down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low. The WDT_TOUT# pin is held low until the system is reset.

The WDT of 6300ESB also supports multiple modes, WDT and free-running. Free-running mode is a one stage timer and it will toggle WDT_TOUT# after programmable time. WDT mode is a two stage timer and its operation is described as above.

Configuration Registers

The Intel® 6300ESB ICH WDT, appears to BIOS as PCI Bus 0, Device 29, Function 4, and has the standard set of PCI Configuration register. The configuration registers is described below.

Offset 10H: Base Address Register (BAR)

This register determines the memory base for WDT down-counter setting. It will be used to set Preload value 1 register, Preload value 2 register, General Interrupt Status register and Reload register.

Preload Value 1 & 2 registers

These two registers are used to hold the preload value for the WDT timer. Its value will be automatically transferred into the down-counter every time the WDT enters the first stage and second stage. Preload Value 1 register locates at Base + 00H and Preload Value 2 register locates at Base + 04H. Only bit [19:0] are settable. The register unlocking sequence is neces-

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sary when writing to the Preload registers. The following is the procedure of how to write a value into preload value 1 and 2 register.

1. Write 80H to offset BAR + 0CH.
2. Write 86H to offset BAR + 0CH.
3. Write desired value to preload register. (BAR + 00H or BAR + 04H)

General Interrupt Status Register

This register is at Base + 08H. Bit 0 is set when the first stage of down-counter reaches zero.

- Bit 0 = 0 – No Interrupt
- Bit 1 = 1 – Interrupt Active

Note: This bit is not set in free running mode.

Reload Register

This register is at Base + 0CH. Write 1 to bit 8 will reload the down-counter's value. Following is the procedure of how to prevent a timeout.

1. Write 80H to offset BAR + 0CH
2. Write 86H to offset BAR + 0CH
3. Write a '1' to RELOAD[8] of the reload register

Offset 60 – 61H: WDT Configuration Register

- Bit 5 indicates whether or not the WDT will toggle the WDT_TOUT# pin when WDT times out. (0 = Enabled, 1 = Disabled)
- Bit 2 provides two options for prescaling the main down-counter. (0 = 1ms – 10min, 1 = 1us – 1sec)
- Bit [1:0] allows the user to choose the type of interrupt desired when the WDT reached the end of the first stage without being reset. (00 = IRQ, 01 = reserved, 10 = SMI, 11 = Disabled)

Note: The WDT doesn't support SMI. IRQ uses APIC 1, INT 10 and it is active low, level triggered.

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Offset 68H: WDT Lock Register

- Bit 2 is used to choose the functionality of the timer. (0 = Watchdog Timer mode, 1 = Free running mode) The free running mode ignores the first stage and only uses Preload Value 2. In free running mode it is not necessary to reload the timer as it is done automatically every time the down counter reaches zero.
- Bit 1 enables or disables the WDT. (0 = Disabled, 1 = Enabled)
- Bit 0 will lock the values of this register until a hard reset occurs or power is cycled. (0 = unlocked, 1 = locked) The default is Unlocked.

GPIO Control Registers

There are three GPIOs on cPCI-6840 relate to watchdog timer. They are listed as following. The GPIO control base port is 480H.

WDT_TOUT# pin selection

WDT_TOUT# signal is multiplexed with GPIO32. When using WDT, this signal must be switched to WDT_TOUT# function. It uses bit 0 of GPIOBASE + 30H to set WDT_TOUT function. (0 = WDT_TOUT#, 1 = GPIO32)

RESET hardware circuit selection

GPO24 of 6300ESB is designed to control reset circuit. When GPO24 is low, system will reset according to the level of WDT_TOUT# signal. When GPO24 is high, system will not be reset by WDT_TOUT#. Set bit 24 of GPIOBASE + 04H to 0 for output use. Bit 24 of GPIOBASE + 0CH determines the level of GPO24. (0 = Low, 1 = High) There already exists a setting in BIOS setup menu. (Integrated Peripherals page) User can set this item before programming WDT.

WDT LED Control

GPO25 of 6300ESB is designed to control WDT LED. Two features of WDT LED are supported on cPCI-6840. WDT LED lights or blinks.

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WDT LED light

Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 0CH determines the state of WDT LED. (0=light, 1=dark)

WDT LED blink

Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 18H enables WDT LED blinking function. (0=function normally, 1=enable blinking) The high and low times have approximately 0.5 seconds each.

WDT Programming Procedure

1. Set BIOS Setting in Integrated Peripherals\Onboard Device Page Watch Dog Timer Item to “Enabled”.
2. Make sure WDT_TOUT# signal is functional. (Not GPIO32 function).
3. Set WDT output enable, presecaler and interrupt type into WDT configuration register.
4. Obtain control base from Base Address register.
5. Program Preload register’s value according to unlocking sequence.
6. Set WDT timer mode into WDT Lock Register.
7. Enable WDT from WDT Lock register and program the functionality of WDT LED.

To prevent the timer from causing an interrupt or driving WDT_TOUT#, the timer must be reloaded periodically. The frequency of reloads required is dependent on the value of the preload values. To reload the down-counter, the register unlocking sequence must be performed.

If the user wishes to disable WDT, set bit 1 of WDT Lock Register to 0.

Utilities

ADLINK provides a demo DOS utility, `HRWDT.EXE`. It is included in the driver CD. Run “`hrwdt /?`” under the following directory: X:\CHIPDRV\WDT\HRWDT for a more detailed description.

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The user can also download the Intel® WDT demo windows application from Intel® driver download center.

5.2 Intel Preboot Execution Environment (PXE)

The cPCI-6840 series supports Intel® Preboot Execution Environment (PXE), which provides the capability of boot up or executing an OS installation through the Ethernet ports. There should be a DHCP server in the network with one or more servers running PXE and MTFTP services. It could be a Windows NT or Windows 2000 server running DHCP, PXE and MTFTP service or a dedicated DHCP server with one or more additional server running PXE and MTFTP service. This section describes the major items required for building a network environment with PXE support.

1. Setup a DHCP server with PXE tag configuration.
2. Install the PXE and MTFTP services
3. Make boot image file on PXE server (that is the boot server).
4. Enable the PXE boot function on the client computer.

For further details, please refer to pdkrel30.pdf under the directory X:\Utility\PXE_PDK.

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6 IPMI User Guide

6.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 1.5. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

6.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the BMR-AVR-cPCI. The rightmost column indicates if a particular command is required by PICMG 3.0/ PICMG 2.9, or is optional.

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 3.0/ 2.9)
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory/Mandatory
Cold Reset	17.2	App	02h	Optional/Optional
Warm Reset	17.3	App	03h	Optional/Optional
Get Self Test Results	17.4	App	04h	Mandatory/Mandatory
Get Device GUID	17.8	App	08h	Optional/Optional
Broadcast "Get Device ID"	17.9	App	01h	Mandatory/Mandatory
IPMI Messaging Support Commands				
Send Message	18.7	App	34h	Optional
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory/Optional
Set Watchdog Timer	21.6	App	24h	Mandatory/Optional
Get Watchdog Timer	21.7	App	25h	Mandatory/Optional
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory/Optional
Get Event Receiver	23.2	S/E	01h	Mandatory/Optional
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory/Optional
Sensor Device Commands				

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Get Device SDR Info	29.2	S/E	20h	Mandatory/Optional
Get Device SDR	29.3	S/E	21h	Mandatory/Optional
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory/Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional/Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional/Optional
Set Sensor Threshold	29.8	S/E	26h	Optional/Optional
Get Sensor Threshold	29.9	S/E	27h	Optional/Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional/Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional/Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional/Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory/Optional
Get Sensor Type	29.16	S/E	2Fh	Optional/Optional
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory/Optional
Read FRU Data	28.2	Storage	11h	Mandatory/Optional
Write FRU Data	28.3	Storage	12h	Mandatory/Optional

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6.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (C0h)	12h
OemRescanGaInput	OEM (C0h)	22h
OemTestFunction	OEM (C0h)	30h
OemReportGeoAddress	OEM (C0h)	F0h
OemEnableSmbus	OEM (C0h)	F2h
OemDisableSmbus	OEM (C0h)	F3h
OemDispDebugVariable	OEM (C0h)	F4h
OemResetHost	OEM (C0h)	F5h
OemPowerOff	OEM (C0h)	F6h
OemPowerOn	OEM (C0h)	F7h

OemShowRevision

This command is used to show the current information of the firmware including the firmware revision, the product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	*Firmware Rev	‘V’ in ASCII code for verification
	3	*Firmware Rev	Revision info high byte
	4	*Firmware Rev	Revision info low byte
	5	*Product ID	‘P’ in ASCII code for verification
	6	*Product ID	Product info high byte
	7	*Product ID	Product info low byte
	8	*Special info	‘S’ in ASCII code for verification
	9	*Special info	Addition info byte
	10	5Ah	Internal check byte. Always 5Ah

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OemRescanGaInput

This command is used to rescan the geo-address input pins and reset the IPMB address according to the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

This command is used to turn on the I2C bus when it is off during boot up process. Usually BIOS will perform this command after booting in boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command
Response	0	Complete Code	00h means OK

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OemDisableSmbus

This command is used to shut down I2C bus access.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

OemDispDebugVariable

This command can report up to 5 interval values for debug purposes. For developers only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	

OemResetHost

This command is implemented to control the system's status if rebooting is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

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OemPowerOff

This command is implemented to control the system's status if power-off is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOn

This command is implemented to control the system's status if power-on is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

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6.4 CompactPCI Address Map

Since we may insert more than one system in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping

Geo. Addr.	IPMB Addr.	Geo. Addr.	IPMB Addr.
0	Disabled	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	BAh	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	C0h	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	31	Disabled

6.5 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Remark
01h	BMC Watchdog		
02h	3.3	3.3 V	
03h	5V	5 V	
04h	12V	12 V	
05h	SYSTEM Temp	25 °C	

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6.6 Known Issues

Timestamp resets after power up:

There is no real time clock built-in with the BMC in our IPMI solution. As a result, the internal timer resets itself after power up.

SDR records readonly:

Due to the hardware design, all sensor data records (SDR) are stored in Flash ROM. Flash ROM cannot be accessed randomly.

6.7 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v1.5	Document Revision 1.1 February 20, 2002	Intel Corp. http:// www.intel.com/design/ servers/ipmi/license_ipmi.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/ servers/ipmi/license_ipmi.htm

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Important Safety Instructions

Please read and follow all instructions marked on the product and in the documentation before operating the system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User's Manual for future reference.
- The equipment should be operated within the recommended operating temperature.
- The equipment should be operated only from the type of power source indicated on the rating label. Make sure the voltage of the power source is correct when connecting the equipment to the power outlet.
- If the user's equipment has a voltage selector switch, make sure that the switch is set to the proper position for the area. The voltage selector switch is set at the factory to the correct voltage.
- For pluggable equipment, ensure they are installed near a socket-outlet that is easily accessible.
- Secure the power cord to prevent unnecessary accidents. Do not place anything over the power cord.
- If the equipment will not be in use for long periods of time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
- All cautions and warnings on the equipment should be noted.
- Please keep this equipment away from humidity.
- Do not use this equipment near water or a heat source.
- Place this equipment on a reliable surface when installing. A drop or fall could cause injury.
- Never pour any liquid into the opening, this could cause fire or electrical shock.

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- Openings in the case are provided for ventilation. Do not block or cover these openings. Make sure there is adequate space around the system for ventilation when setting up the work area. Never insert objects of any kind into the ventilation openings.
- To avoid electrical shock, always unplug all power and modem cables from the wall outlets before removing covers.
- Lithium Battery provided (real time clock battery)

  “CAUTION - Risk of explosion if battery is replaced by an incorrect type. Dispose used batteries as instructed in the instructions”
- The equipment should be checked by service personnel if one of the following situation arises:
  - The power cord or plug is damaged.
  - Liquid has penetrated the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is not functioning or does not function according to the user’s manual.
  - The equipment has been dropped and damaged.
  - If the equipment has obvious sign of breakage.
- Never open the equipment. For safety reasons, the equipment should only be opened by qualified service personnel.

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Getting Service

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