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cPCI-6510 Series

Low Power 6U CompactPCI Processor Blade with Intel® Core™ i7 and two PMC sites

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	2010/09/24	Initial Release
2.01	2010/11/24	Updated RTM list, Mode Switch (SW2) definition, IPMI User Guide; added NT Mode EEPROM programming instructions
2.02	2014/11/13	Add PMC slot -12V support note

Preface

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Using this Manual

Audience and Scope

The cPCI-6510 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade CompactPCI modules.

Manual Organization

This manual is organized as follows:

Chapter 1, Overview: Introduces the cPCI-6510, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information, and power consumption.

Chapter 3, Functional Description: Describes the cPCI-6510's main functions.

Chapter 4, Board Interfaces: Describes the cPCI-6510 board interfaces, pin definitions, and jumper settings.

Chapter 5, Getting Started: Describes the installation instructions of the cPCI-6510.

Chapter 6, Driver Installation: Describes the driver installation procedures.

Chapter 7, Utilities: Describes the Watchdog Timer and Preboot Execution Environment functions.

Chapter 8, BIOS Setup Utility: Describes the AMIBIOS®8 BIOS setup utility.

Chapter 9, IPMI User Guide: Provides relevant information for the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI).

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Overview

1.1 Introduction

The cPCI-6510 Series is a 6U CompactPCI single board computer in single slot width (4HP) form factor supporting 32nm Intel® Core™ i7 SV, LV, ULV processors with integrated graphics and ECC memory controller onboard. The cPCI-6510 provides up to 8GB of dual channel DDR3-800/1066 ECC memory soldered onboard and implements the Mobile Intel® QM57 Express Chipset to provide a full feature set and optimal performance per watt.

The cPCI-6510 Series provides a 64bit/66MHz CompactPCI bus, up to two PMC sites with 64-bit/133MHz PCI-X bus supporting rear I/O (PIM), and one PCI Express x8 XMC site (shared with inner PMC site). Featured I/O includes four PCI Express Gigabit Ethernet ports (two on front panel, two for PICMG 2.16), two USB ports and a CompactFlash socket. DVI-I, COM and additional USB ports are available on the cPCI-6510V version which also provides a SATA connector for an onboard 2.5” SATA HDD. Optional Rear Transition Modules provide versatile additional I/O including two additional GbE, USB, COM, High Definition Audio, and storage interfaces such as SATA, SCSI, and SAS with RAID support. The cPCI-6510V supports dual independent display via two DVI or one DVI and one VGA when accompanied by the appropriate Rear Transition Module.

For flexibility of use, the cPCI-6510 Series can be installed in a standard CompactPCI system slot as system master, or peripheral slot as a PCI device. Through hardware switch setting, the cPCI-6510 optionally supports operation in system or peripheral slots as a standalone blade. The cPCI-6510 Series is ideally suited for military, aviation, communication and other industrial applications.

1.2 Features

- 6U CompactPCI SBC in 4HP width form factor
- µFC-BGA package Intel® Core™ i7 processor, up to 2.53GHz
- Mobile Intel® BD82QM57 PCH (Platform Controller Hub)
- Dual Channel DDR3 ECC SDRAM at 800 or 1066MHz soldered onboard, up to 8GB
- 64-bit/66MHz CompactPCI Interface based on PCI specifications, 3.3V and 5V signaling
- Supports operation in system slot as system master or in peripheral slot with connectivity to CompactPCI bus* (optional isolation from CompactPCI bus)
- Dual PMC sites with 64-bit/133MHz PCI bus
- Single XMC site with PCIe x8 lane (shared with inner PMC site)
- Up to two DVI ports for dual independent displays
- Four PCIe Gigabit Ethernet ports, two at front, two for PICMG 2.16 or RTM
- Onboard CompactFlash socket
- 2.5” SATA HDD direct connector onboard, occupies outer PMC site
- Up to -40°C to 80°C optional extended temperature support
- RTM models available with multiple I/O options: SATA, HD audio, COM, USB, Gigabit Ethernet, PS/2 KB/MS, PIM, SAS, SCSI, CF, SD socket
- Hardware RAID on SCSI, SAS interfaces supported (dependent on RTM module)


NOTE:

*See “Programming NT Mode EEPROM Map” on page 59 for instructions on how to set the PCIe-to-PCI bridge on the cPCI-6510 to NT-mode to allow operation in a peripheral slot.

1.3 Block Diagram

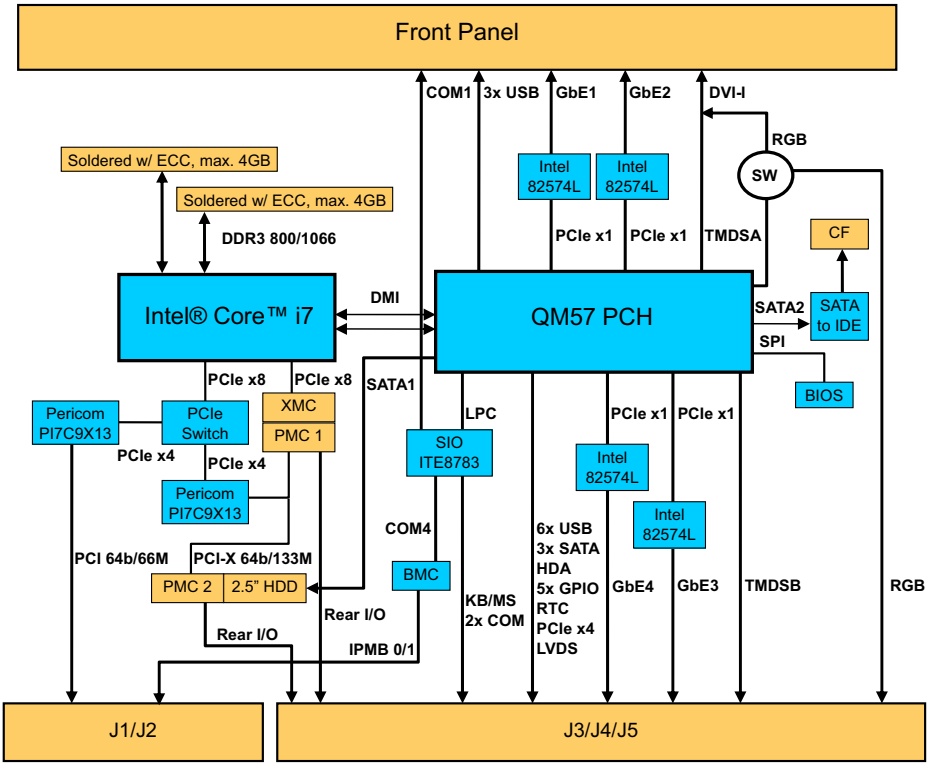


Figure 1-1: cPCI-6510 Series Block Diagram

1.4 Product List

Products included in the cPCI-6510 Series include:

Processor Blade

- **cPCI-6510:** 4HP width (single-slot) 6U CompactPCI blade featuring single Intel® Core™i7 processor, dual channel DDR3-800/1066 soldered onboard SDRAM with ECC, 2x PMC or 1x PMC and 1x XMC, 2x USB, 2x GbE and CF socket
- **cPCI-6510V:** 4HP width (single-slot) 6U CompactPCI blade featuring single Intel® Core™i7 processor, dual channel DDR3-800/1066 soldered onboard SDRAM with ECC, 1x PMC/XMC, 3x USB, 2x GbE, RJ-45 COM, DVI-I, SATA for 2.5” HDD and CF socket

Rear Transition Modules

- **cPCI-R6000:** 4HP width RTM with DVI-I, 2x COM, 3x USB, 2x GbE, SCSI, 2xSATA
- **cPCI-R6100:** 4HP width RTM with 4x GbE, 4x USB, 2xSATA, DVI, VGA, PS/2 KB/MS, CF & SD sockets
- **cPCI-R6110:** 4HP width RTM with 2x GbE, 4x USB, 3x SATA, VGA, PS/2 KB/MS, CF, & SD sockets
- **cPCI-R6200:** 8HP width RTM with 2x GbE, 2x COM, 4x USB, DVI-I, 3x SATA, Mic-in, Line-out, PS/2 KB/MS, 8x SAS
- **cPCI-R6210:** 4HP width RTM with 2xUSB, DVI-I, COM, 2x SATA, 2x PIM

Adapter Kit

- **DB-CF-SA:** CompactFlash socket kit for cPCI-R6000D & cPCI-R6200 RTMs, including DB-6920CF adapter board, card guide and screws to replace SATA adapter with CompactFlash socket

1.5 Package Contents

The cPCI-6510 is packaged with the components listed below (RTMs and adapter kits are optional). If any of the items in the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of non-standard configurations may vary depending on customer requests.

Processor Blade

- The cPCI-6510 Series Processor Blade
  - CPU, RAM will differ depending on options selected
  - Thermal module is assembled on the board
- RJ-45 to DB-9 cable for RJ-45 COM port (cPCI-6510V only)
- 2.5” SATA HDD mounting kit, including HDD bracket, screws for HDD, and DB-6920SAT SATA adapter card (cPCI-6510V only)
- ADLINK All-in-One CD
- User’s manual


NOTE:

The contents of non-standard cPCI-6510 configurations may vary depending on customer requests.


CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 cPCI-6510 Specifications

CompactPCI Standard	PICMG® 2.0 CompactPCI® Rev. 3.0 PICMG® 2.1 Hot Swap Specification Rev.2.0 PICMG® 2.9 System Management Bus Rev. 1.0 PICMG® 2.16 Packet Switching Backplane Rev.1.0
Mechanical	Standard 6U CompactPCI®
	Board size: 233.23 mm x 160mm
	Single slot (4HP, 20.32mm) width
	CompactPCI® connectors J1, J2, J3, J4 and J5
Processor	µFC-BGA Intel® Core™i7-610E, 4MB L2 cache, 2.53GHz µFC-BGA Intel® Core™i7-620LE, 4MB L2 cache, 2.0GHz µFC-BGA Intel® Core™i7-620UE, 4MB L2 cache, 1.06GHz
Chipset	Intel® QM57 Platform Controller Hub (PCH)
Memory	Dual channel DDR3-800/1066 soldered onboard SDRAM with un-buffered ECC DDR3-800 for Core™i7-620UE processor DDR3-1067 for Core™i7-610E/620LE processors Maximum 8GB capacity
CompactPCI Bus	PCI 64-bit/ 66MHz; V(I/O) 3.3V and 5V signaling Supports operation in system slot or in peripheral slot with connectivity to CompactPCI bus (Universal Mode)[1] Optional Satellite mode by switch setting
PMC/XMC	Two PCI 64-bit/133MHz PMC sites, V(I/O) 3.3V (contact ADLINK for 5V support) One PCIe x8 XMC site (shared with inner PMC site)
Graphics	Integrated in Intel® Core™i7 processor One DVI-I port on front panel of cPCI-6510V provides digital and analog signals. Analog RGB signal to front or rear by switch selection Second DVI port routed to rear Supports dual independent display Analog RGB up to QXGA
Ethernet	Four PCIe x1 Intel® 82574L GbE controllers Two 10/100/1000BASE-T egress ports Two 10/100/1000BASE-T ports on rear panel, optional PICMG 2.16 support by switch selection

Serial Ports	One 16C550 compatible RJ-45 RS-232 port on front panel (cPCI-6510V only) Two serial ports routed to rear I/O
Storage Interfaces	2.5” SATA HDD direct connector onboard (cPCI-6510V only)
	CompactFlash Type II socket onboard[1]
BIOS	AMI® EFI BIOS 64Mbit SPI flash memory
IPMI Interface	Supports PICMG® 2.9 secondary system management bus IPMI functions implemented as defined by IPMI Spec. v1.5; ATmega128L-8AU Baseboard Management Controller (BMC) with 128KB programmable in-system flash, 4KB EEPROM, and 4KB internal SDRAM
Faceplate I/O	**cPCI-6510:** 2x USB 2.0 ports 2x 10/100/1000BASE-T Ethernet ports 2x PMC and one XMC slots
	cPCI-6510V: 3x USB 2.0 ports 2x 10/100/1000BASE-T Ethernet ports PMC/XMC slot RJ-45 Serial port DVI-I port (digital and analog)
Supported OS	Microsoft® Windows® 7 Ultimate Microsoft® Windows® Vista Enterprise Microsoft® Windows® XP Professional SP3 Fedora™ 12 Other OS support upon request
Operating Temperature[2]	0°C to 60°C standard -20°C to +70°C (cPCI-ET6510) -40°C to +80°C (cPCI-EX6510)
Storage temperature	-40°C to 85°C
Humidity	20% to 95% non-condensing
Shock	20G peak-to-peak, 11ms duration, non-operating
Vibration[3]	Operating: 1.88Grms. 5 to 500Hz, each axis (without HDD)
Compliance	CE EN55022, FCC Class A

Table 2-1: cPCI-6510 Specifications

Notes:

1. 7.4 "Programming NT Mode EEPROM Map" on page 59 for instructions on how to set the PCIe-to-PCI bridge on the cPCI-6510 to Non-Transparent mode to allow operation in a peripheral slot.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required (see 2.4 "Thermal Requirements" on page 13). Temperature limit of optional mass storage devices may affect the thermal specification.
3. The hard drive limits the operational vibration tolerance. When application requires higher specification for anti-vibration, it is recommended to use a solid state drive (SSD) or Compact-Flash card.


NOTE:

Specifications are subject to change without prior notice.

2.2 I/O Connectivity

cPCI-6510 Processor Blade

Function	cPCI-6510		cPCI-6510V	
	Faceplate	Board	Faceplate	Board
GbE	2	—	2	—
USB 2.0	2	—	2	—
COM	—	—	1 (RJ-45)	—
DVI-I	—	—	1	
PMC	—	2	—	1
XMC	—	1	—	1
Serial ATA	—	—	—	1 (2.5” HDD)
CompactFlash	—	1	—	1

Table 2-2: cPCI-6510 I/O Connectivity

2.3 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/ -3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

Table 2-3: CompactPCI Input Voltage Characteristics

Power Consumption

This section provides information on the power consumption of the cPCI-6510 Series with different CPUs, 2GB DDR3-800/1066 soldered memory, and 100GB SATA HDD. The system was tested in Idle Mode and Full Load Mode under Windows XP running Burn-in Test 6.0. The cPCI-6510 is powered by 5V and 3.3V.

Idle Mode under Windows XP

CPU	Core™ i7 610E		Core™ i7 620LE		Core™ i7 620UE	
Voltage (V)	Current (A)	Power (W)	Current (A)	Power (W)	Current (A)	Power (W)
+3.3	4.19	13.82	4.12	18.41	3.85	12.71
+5	1.14	5.69	1.07	5.35	1.05	5.25
Total		19.51		23.76		17.96

Table 2-4: Idle Mode Power Consumption

100% CPU Usage under Windows XP

CPU	Core™ i7 610E		Core™ i7 620LE		Core™ i7 620UE	
Voltage (V)	Current (A)	Power (W)	Current (A)	Power (W)	Current (A)	Power (W)
+3.3	6.09	20.10	5.83	19.25	5.31	17.52
+5	4.44	22.21	3.57	17.83	2.07	10.35
Total		42.31		37.08		27.87

Table 2-5: 100% CPU Usage Power Consumption

2.4 Thermal Requirements

This section provides information on the thermal requirements of the cPCI-6510 Series. Cooling of the board and its components is provided by the thermal module (passive heatsink) and is dependent on sufficient airflow from the chassis.

The amount of thermal energy that can by dissipated from the board is dependent on the ambient air temperature and the airflow rate of the chassis. To provide the user with guidelines for the upper limits of operating conditions for the cPCI-6510, the following sections give information on the maximum ambient air temperature as a function of airflow rate for a given level of power consumption.

Power Dissipation Graphs

The graphs shown below illustrate the level of CPU power dissipation that can be maintained dependent on ambient air temperature and airflow rate. One graph is provided for each CPU supported by the cPCI-6510. The curves on each graph indicate the upper limits of operating conditions under which the CPU will not be affected by its thermal management and protection systems at a given percentage of the CPU's thermal design power (TDP).

The CPU's thermal management and protection systems begin to take effect when the CPU temperature exceeds the maximum junction temperature ($T_{j,Max}$=105°C). When the ambient air temperature and airflow rate are in the ranges below the TDP curves on the graphs, the CPU temperature will remain below $T_{j,Max}$ and the CPU will be able to operate at full performance (i.e. not limited by thermal management).

The power dissipation graphs show two curves:

- 100% TDP
- 75% TDP

The detailed specifications for each processor can be found in Section 3.1 "Processor" on page 17.

Intel® Core™ i7-610E

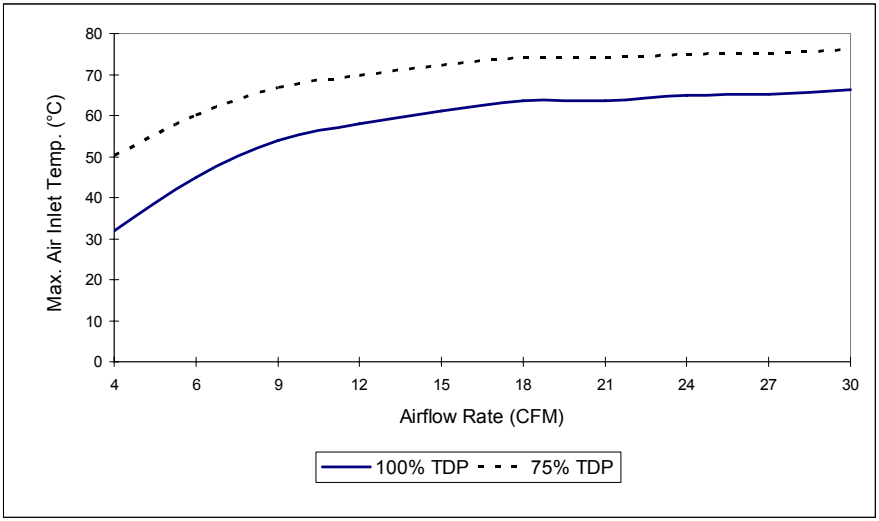


Figure 2-1: Core i7-610E Power Dissipation Graph (TDP 35W)

Intel® Core™ i7-620LE

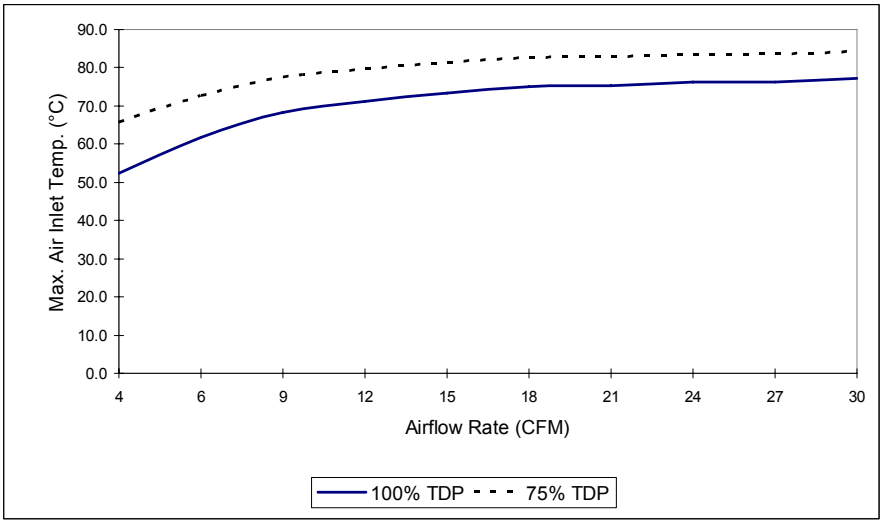


Figure 2-2: Core i7-620LE Power Dissipation Graph (TDP 25W)

Intel® Core™ i7-620UE

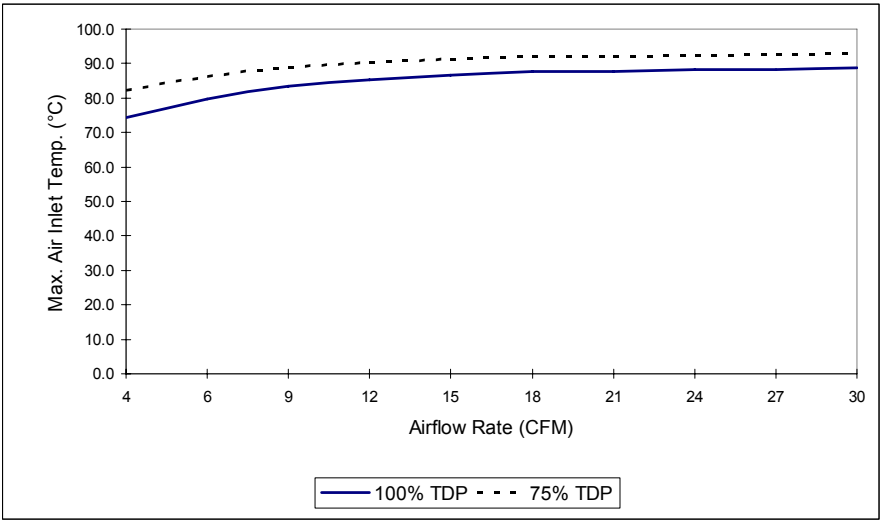


Figure 2-3: Core i7-620UE Power Dissipation Graph (TDP 18W)

Thermal Management Features

When the CPU temperature exceeds its maximum junction temperature ($T_{j,Max}$), the CPU's thermal management features will reduce power consumption (and thus performance) in an attempt to reduce the core junction temperature. Use of the CPU's thermal management features is intended for short periods of time when running power intensive applications. If the system is operated under conditions below the TDP curves above, activation of the thermal management features will be minimal and reduction in CPU performance will be minor.

However, if the operating conditions are outside the limits set out above, the CPU temperature may exceed $T_{j,Max}$ for prolonged periods, resulting in noticeable performance loss and reduced reliability of the processor.

In extreme situations, the thermal management features may be incapable of cooling the processor. If the CPU temperature exceeds approximately 130°C, a catastrophic cooling failure will be detected and the processor will automatically shut down to prevent physical damage to the processor.



Prolonged operation above the CPU's maximum junction temperature (Tj,Max=105°C) may damage the CPU and/or reduce its long term reliability. Be sure to follow the thermal guidelines set out in this document.

3 Functional Description

The following sections describe the cPCI-6510 Series features and functions.

3.1 Processor

Intel® Core™ i7 Processor

The Intel® Core™ i7-620LE/UE and i7-610E are 64-bit, multi-core mobile processors built on a 32 nanometer process technology. The processors are designed for a two-chip platform consisting of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The Intel® Core™ i7-620LE/UE and i7-610E processors are offered in a BGA1288 package and include an integrated graphics and memory controller die on the same package as the processor core die.

The following table lists the processors supported by the cPCI-6510 Series and their specifications.

Features	SV Core i7-610E	LV Core i7-620LE	ULV Core i7-620UE
Clock	2.53GHz	2.0GHz	1.06GHz
Max. Turbo Freq.	3.2GHz	2.8GHz	2.13GHz
L2 cache	4MB	4MB	4MB
Max. Power (TDP[1])	35W	25W	18W
$T_{j,Max}$[2]	105°C	105°C	105°C
Process	32nm	32nm	32nm
# of cores/threads	2/4	2/4	2/4

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. Maximum junction temperature ($T_{j,Max}$). The maximum supported operating temperature.

System Memory Support

- Two channels of DDR3 memory soldered onboard
- Memory DDR3 data transfer rates of 800 and 1066 MT/s
- 64-bit wide channels (72-bit wide including ECC)
- Supports ECC unbuffered DDR3 memory
- Theoretical maximum memory bandwidth of:
  - 12.8 GB/s in dual-channel mode assuming DDR3 800 MT/s
  - 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
- 1-Gb and 2-Gb DDR3 DRAM technologies for x8 devices
- Using 2Gb device technologies, the largest memory capacity is 8GB

3.2 Chipset

Mobile Intel® QM57 Express Chipset

The cPCI-6510 Series incorporates the Mobile Intel® QM57 Express Chipset, also referred to as PCH (Platform Controller Hub), to provide extensive I/O support. Functions and capabilities include:

- PCI Express Base 2.0 Specification support for up to eight ports
- 4 PCI Express x1 connected to LAN controllers
- 4 PCI Express x1 are configured to PCI Express x4 and routed to J5 for I/O expansion
- ACPI Power Management Logic Support
- Two integrated SATA host controllers with up to six ports, supporting independent DMA operation and data transfer rates of up to 3.0GB/s (the cPCI-6510 supports up to four SATA ports)
- Supports Advanced Host Controller Interface (AHCI)
- Intel Rapid Storage Technology provides high performance RAID 0, 1, 5, and 10 functionality
- High speed USB 2.0 allows data transfers up to 480 Mb/s
- Provides Intel Virtualization Technology with Directed I/O (Intel VT-d) support.

3.3 Super I/O

The ITE IT8783F Super I/O is on a Low Pin Count interface supporting PS/2 keyboard/mouse, 16C550-compatible serial ports, floppy drive interface, hardware monitor function to monitor CPU voltage, CPU temperature, power supply voltages and system temperature, and Watchdog Timer with time resolution from minimum 1 second or minute to maximum 65,535 seconds or minutes.

3.4 Battery

The cPCI-6510 is provided with a 3.0V coin cell lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 is equipped on board by default.

3.5 PMC/XMC Sites

The cPCI-6510 series supports two PMC sites for front panel I/O expansion. The PMC sites provides a maximum 64bit/133MHz PCI-X bus link using a Pericom PI7C9X130 PCIe-to-PCI bridge and PCIe x4 link. The PMC/XMC sites support +3.3V signaling and 5V VPWR by default. For optional 5V signaling and 12V VPWR support, contact your ADLINK sales representative.

The JN1/5 and JN2/6 connectors provide the signals for the 32-bit PCI bus. The JN3/7 connector provides the 64 bit extension for the PMC interface. The JN3/7 connectors support user defined I/O signals and are routed to the CompactPCI J4/5 connectors to rear I/O.

The cPCI-6510 provides a PCIe x8 XMC interface sharing the same space as the inner PMC site for high speed I/O expansion, such as 10GbE or high-end graphics.

3.6 BIOS Recovery

The cPCI-6510 Series features AMI® EFI BIOS with BIOS recovery. If the BIOS becomes corrupted and you are unable to boot your system, follow the instructions in Section 7.3 “BIOS Recovery” on page 57.

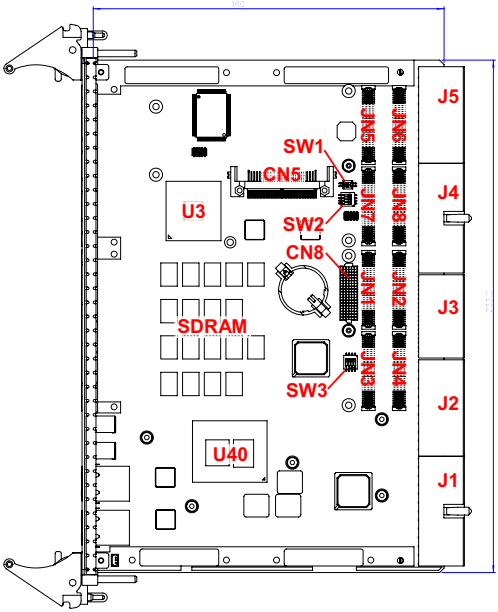
4 Board Interfaces

This chapter describes the board layout, connector pin assignments, and jumper settings of the cPCI-6510 Series.

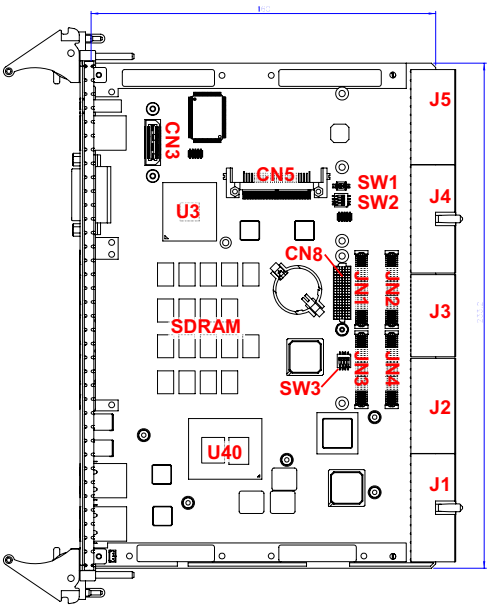
4.1 cPCI-6510 Series Board Layout - Top Side

The cPCI-6510 and cPCI-6510V have the same PCB layout but different BOM options to offer different features.

cPCI-6510



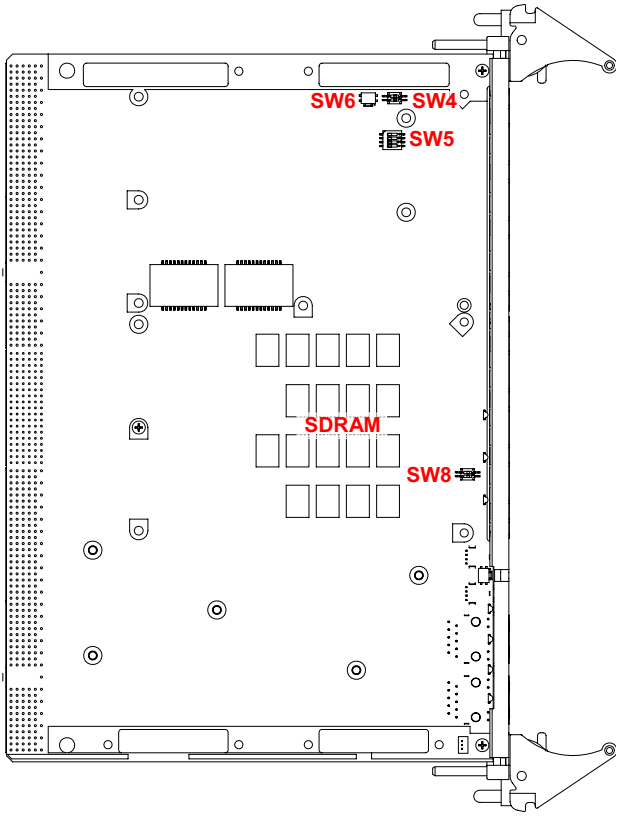
cPCI-6510V



U40	CPU	**CN3**	DB-6920SAT connector
U3	QM57 PCH	**CN5**	CompactFlash socket
SDRAM	Soldered SDRAM	**CN8**	XMC connector
J1-5	CompactPCI connectors	**JN1-8**	PMC connectors
SW1-3	Switches		

Figure 4-1: cPCI-6510 Series Board Layout - Top Side

4.2 cPCI-6510 Series Board Layout - Bottom Side



SW4/5/6/8	Switches	**SDRAM**	Soldered SDRAM

Figure 4-2: cPCI-6510 Series Board Layout - Bottom Side

4.3 cPCI-6510 SBC Front Panel

cPCI-6510V

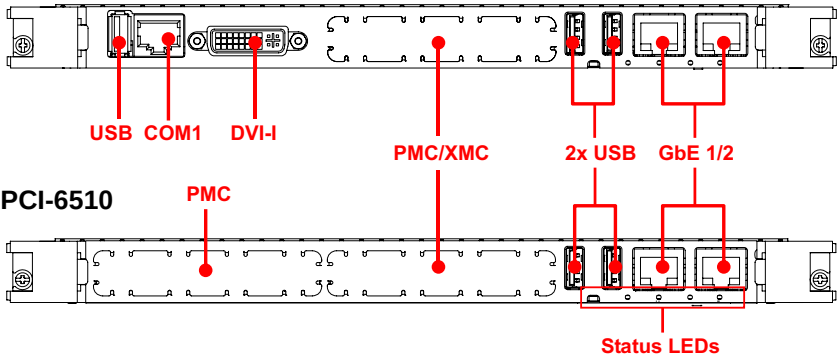


Figure 4-3: cPCI-6510 Series Front Panel Layout

Status LEDs



LED	Color	Condition	Indication
Power (P)	Green	OFF	System is off
		ON	System is on
Hot Swap (H)	Blue	OFF	Handles closed, System is on
		Fast Blink	Preparing to shut down system (LED: 0.1s on, 0.9s off)
		ON	Handles open and SBC ready to be removed
		Slow Blink	Voltages out of tolerance: 3.3V, 5V, 12V, 1.5V over ±5% (LED: 2s on, 1s off)
HDD (D)	Red	OFF	No HDD activity
		Blink	Data read/write in process
WDT (W)	Amber	OFF	No Watchdog event
		ON	Watchdog event alert

Table 4-1: cPCI-6510 Front Panel Status LED Descriptions

4.4 Connector Pin Assignments

Refer to "cPCI-6510 Series Board Layout - Top Side" on page 21 and "cPCI-6510 Series Front Panel Layout" on page 23 for connector locations

USB Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

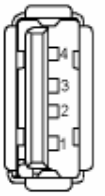


Table 4-2: USB Connector Pin Definition

RJ-45 COM1 Port

Pin #	COM Signal
1	DCD#
2	RTS#
3	DSR#
4	TXD
5	RXD
6	GND
7	CTS#
8	DTR#

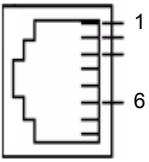


Table 4-3: RJ-45 Serial Port Pin Definition

RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/100BASE-TX	1000BASE-T
1	TX+	BI_DA+
2	TX-	BI_DA-
3	RX+	BI_DB+
4	--	BI_DC+
5	--	BI_DC-
6	RX-	BI_DB-
7	--	BI_DD+
8	--	BI_DD-

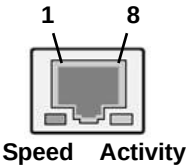
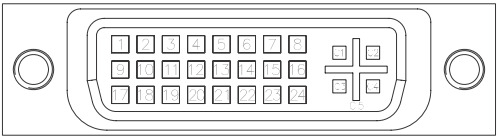


Table 4-4: GbE Connector Pin Definitions

Status (CN4, CN5)		Speed LED (Green/Amber)	Activity LED (Amber)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Amber	ON
	Active	Amber	Blinking

DVI-I Connector



Pin #	Signal	Pin #	Signal
1	TMDS Data2-	16	Hot Plug Detect
2	TMDS Data2+	17	TMDS Data0-
3	GND	18	TMDSData0+
4	NC	19	GND
5	NC	20	NC
6	DDC Clock [SCL]	21	NC
7	DDC Data [SDA]	22	GND
8	Analog vertical sync	23	TMDS Clock +
9	TMDS Data1-	24	TMDS Clock -
10	TMDS Data1+	C1	Analog Red
11	GND	C2	Analog Green
12	NC	C3	Analog Blue
13	NC	C4	Analog Horizontal Sync
14	+5 V Power	C5	Analog GND Return
15	GND		

Table 4-5: DVI-I Connector Pin Definition

Serial ATA Connector on DB-6920SAT

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	Reserved
P12	GND
P13~P15	12V

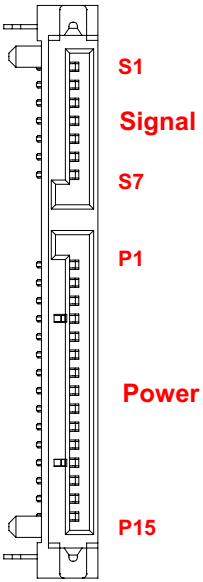


Table 4-6: DB-6920SAT SATA Connector Pin Definition

PMC Connector (JN1/5, JN2/6, JN3/7, JN4/8)

Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4/8 Signal
1	PMC_TCK	P12V	NC	PIO1
2	N12V*	PMC_TRST-L	GND	PIO2
3	GND	PMC_TMS	GND	PIO3
4	PCIX_INTA-L	NC (PMC_TDO)	PCIX_CBE-L7	PIO4
5	PCIX_INTB-L	PMC_TDI	PCIX_CBE-L6	PIO5
6	PCIX_INTC-L	GND	PCIX_CBE-L5	PIO6
7	PMC_MOD-L1	GND	PCIX_CBE-L4	PIO7
8	P5V	NC	GND	PIO8
9	PCIX_INTD-L	NC	PMC_VIO	PIO9
10	NC	NC	PCIX_PAR64	PIO10
11	GND	PMC_MOD-L2	PCIX_AD63	PIO11
12	P3V3_PMCAUX	P3V3	PCIX_AD62	PIO12
13	CLK66_PCIX_PMC	PMC_RST-L	PCIX_AD61	PIO13
14	GND	PMC_MOD-L3	GND	PIO14
15	GND	P3V3	GND	PIO15
16	PCIX_GNT-L0	PMC_MOD-L4	PCIX_AD60	PIO16
17	PCIX_REQ-L0	PMC_PME-L	PCIX_AD59	PIO17
18	P5V	GND	PCIX_AD58	PIO18
19	PMC_VIO	PCIX_AD30	PCIX_AD57	PIO19
20	PCIX_AD31	PCIX_AD29	GND	PIO20
21	PCIX_AD28	GND	GND	PIO21
22	PCIX_AD27	PCIX_AD26	PCIX_AD56	PIO22
23	PCIX_AD25	PCIX_AD24	PCIX_AD55	PIO23
24	GND	PCIX_AD23	PCIX_AD54	PIO24
25	GND	PMC_IDSEL	PCIX_AD53	PIO25
26	PCIX_CBE-L3	PCIX_AD23	GND	PIO26
27	PCIX_AD22	P3V3	GND	PIO27
28	PCIX_AD21	PCIX_AD20	PCIX_AD52	PIO28
29	PCIX_AD19	PCIX_AD18	PCIX_AD51	PIO29
30	P5V	GND	PCIX_AD50	PIO30
31	PCIX_FRAME-L	PCIX_AD16	PCIX_AD49	PIO31
32	PCIX_AD17	PCIX_CBE-L2	GND	PIO32

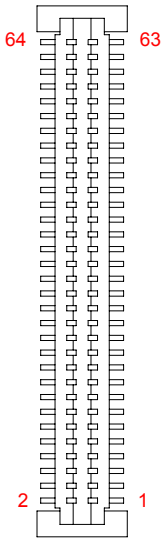


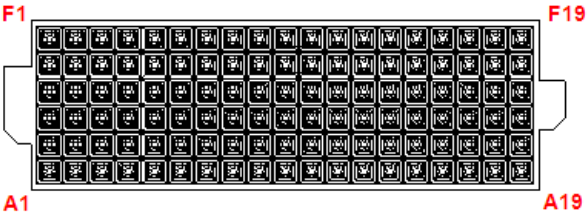
Table 4-7: PMC Connector Pin Definitions

***Note:** -12V signal not supported on JN1/5 pin 2. Contact ADLINK for more information.

Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4/8 Signal
33	PCIX_FRAME-L	GND	GND	PIO33
34	GND	NC	PCIX_AD48	PIO34
35	GND	PCIX_TRDY-L	PCIX_AD47	PIO35
36	PCIX_IRDY-L	P3V3	PCIX_AD46	PIO36
37	PCIX_DEVSEL-L	GND	PCIX_AD45	PIO37
38	P5V	PCIX_STOP-L	GND	PIO38
39	PCIX_PCIXCAP	PCIX_PERR-L	GND	PIO39
40	PCIX_LOCK-L	GND	PCIX_AD44	PIO40
41	NC	P3V3	PCIX_AD43	PIO41
42	NC	PCIX_SERR-L	PCIX_AD42	PIO42
43	PCIX_PAR	PCIX_CBE-L1	PCIX_AD41	PIO43
44	GND	GND	GND	PIO44
45	PMC_VIO	PCIX_AD14	GND	PIO45
46	PCIX_AD15	PCIX_AD13	PCIX_AD40	PIO46
47	PCIX_AD12	PCIX_M66EN	PCIX_AD39	PIO47
48	PCIX_AD11	PCIX_AD10	PCIX_AD38	PIO48
49	PCIX_AD9	PCIX_AD8	PCIX_AD37	PIO49
50	P5V	P3V3	GND	PIO50
51	GND	PCIX_AD7	GND	PIO51
52	PCIX_CBE-L0	NC	PCIX_AD36	PIO52
53	PCIX_AD6	P3V3	PCIX_AD35	PIO53
54	PCIX_AD5	NC	PCIX_AD34	PIO54
55	PCIX_AD4	NC	PCIX_AD33	PIO55
56	GND	GND	GND	PIO56
57	PMC_VIO	NC	GND	PIO57
58	PCIX_AD3	NC	PCIX_AD32	PIO58
59	PCIX_AD2	GND	NC	PIO59
60	PCIX_AD1	NC	NC	PIO60
61	PCIX_AD0	PCIX_ACK64-L	NC	PIO61
62	P5V	P3V3	GND	PIO62
63	GND	GND	GND	PIO63
64	PCIX_REQ64-L	NC	NC	PIO64

Table 4-7: PMC Connector Pin Definitions (cont'd)

XMC Connector (CN8)



Pin#	A	B	C	D	E	F
1	PETp0	PETn0	3.3V	PETp1	PETn1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PETp2	PETn2	3.3V	PETp3	PETn3	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	PETp4	PETn4	3.3V	PETp5	PETn5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PETp6	PETn6	3.3V	PETp7	PETn7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PERp0	PERn0	MBIST#	PERp1	PERn1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERp2	PERn2	3.3V AUX	PERp3	PERn3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PERp4	PERn4	NC	PERp5	PERn5	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	PERp6	PERn6	NC	PERp7	PERn7	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	ROOT0#	NC

Table 4-8: XMC Connector Pin Definition

CompactFlash Connector

Signal Name	Pin#	Pin#	Signal Name
GND	1	26	GND
DD3	2	27	DD11
DD4	3	28	DD12
DD5	4	29	DD13
DD6	5	30	DD14
DD7	6	31	DD15
CS1#	7	32	CS3#
GND	8	33	GND
GND	9	34	SDIOR#
GND	10	35	SDIOW#
GND	11	36	5V
GND	12	37	IRQ15
5V	13	38	5V
GND	14	39	PCSEL
GND	15	40	NC
GND	16	41	BRSTDRV#
GND	17	42	SDIORDY
DA2	18	43	DMARQ
DA1	19	44	DMACK#
DA0	20	45	IDEACT#
DD0	21	46	66DECT
DD1	22	47	DD8
DD2	23	48	DD9
IOIS16#	24	49	DD10
GND	25	50	GND



Table 4-9: CompactFlash Connector Pin Definition

DB-6920SAT Connector (CN3)

Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
P3V3	31	32	P5V
P3V3	33	34	P5V
P3V3	35	36	P5V
P3V3	37	38	P5V
P1V8	39	40	NC
P1V8	41	42	NC
P1V8	43	44	NC
GND	45	46	GND
GND	47	48	SATA-TXN0
GND	49	50	SATA-TXP0
SATA-RXN0	51	52	GND
SATA-RXP0	53	54	GND
GND	55	56	RESET#
GND	57	58	GND
GND	59	60	GND

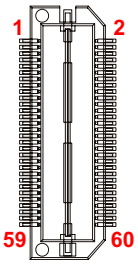


Table 4-10: DB-6920SAT Connector Pin Definition

CompactPCI J1 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	+5V	-12V	TRST#	+12V	+5V	GND
2	GND	TCK#	+5V	TMS#	NC	TDI#	GND
3	GND	IRQA#	IRQB#	IRQC#	+5V	IRQD#	GND
4	GND	+5V_IPMB	HEALTHY#	V(I/O)	NC	NC	GND
5	GND	NC	NC	RESET#	GND	GNT0#	GND
6	GND	REQ0#	GND	+3.3V	CLK0	AD31	GND
7	GND	AD30	AD29	AD28	GND	AD27	GND
8	GND	AD26	GND	V(I/O)	AD25	AD24	GND
9	GND	CBE3#	IDSEL	AD23	GND	AD22	GND
10	GND	AD21	GND	+3.3V	AD20	AD19	GND
11	GND	AD18	AD17	AD16	GND	CBE2#	GND
12-14	Key						
15	GND	+3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
17	GND	+3.3V	IPMB_CLK	IPMB_DAT	GND	PERR#	GND
18	GND	SERR#	GND	+3.3V	PAR	CBE1#	GND
19	GND	+3.3V	AD15	AD14	GND	AD13	GND
20	GND	AD12	GND	VIO	AD11	AD10	GND
21	GND	+3.3V	AD9	AD8	M66EN	CBE0#	GND
22	GND	AD7	GND	+3.3V	AD6	AD5	GND
23	GND	+3.3V	AD4	AD3	+5V	AD2	GND
24	GND	AD1	+5V	V(I/O)	AD0	ACK64#	GND
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND

Table 4-11: CompactPCI J1 Connector Pin Definition

CompactPCI J2 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
4	GND	V(I/O)	NC	CBE7#	GND	CBE6#	GND
5	GND	CBE5#	GND	V(I/O)	CBE4#	PAR64	GND
6	GND	AD63	AD62	AD61	GND	AD60	GND
7	GND	AD59	GND	V(I/O)	AD58	AD57	GND
8	GND	AD56	AD55	AD54	GND	AD53	GND
9	GND	AD52	GND	V(I/O)	AD51	AD50	GND
10	GND	AD49	AD48	AD47	GND	AD46	GND
11	GND	AD45	GND	V(I/O)	AD44	AD43	GND
12	GND	AD42	AD41	AD40	GND	AD39	GND
13	GND	AD38	GND	V(I/O)	AD37	AD36	GND
14	GND	AD35	AD34	AD33	GND	AD32	GND
15	GND	NC	GND	FAL#	REQ5#	GNT5#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
17	GND	NC	GND	RSTBTN#	REQ6#	GNT6#	GND
18	GND	NC	NC	NC	GND	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
20	GND	CLK5	GND	NC	GND	NC	GND
21	GND	CLK6	GND	NC	NC	NC	GND
22	GND	GA4	GA3	GA2	GA1	GA0	GND

Table 4-12: CompactPCI J2 Connector Pin Definition

CompactPCI J3 Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	HDA_RST#	HDA_SYNC	HDA_BIT_CLK	HDA_SDOUT	HDA_SDIN0	GND
2	GND	HDA_SDIN1	HDA_SDIN2	NC	HDA_DOCK_EN#	HAD_DOCK_RST#	GND
3	GND	KBDATA	KBCLK	NC	MSDATA	MSCLK	GND
4	GND	SATA-TX4+	SATA-TX4-	GND	SATA-TX3+	SATA-TX3-	GND
5	GND	GND	GND	NC	GND	GND	GND
6	GND	SATA-RX4+	SATA-RX4-	GND	SATA-RX3+	SATA-RX3-	GND
7	GND	COM4-TX	COM4-RX	COM3-DCD#	IPMB_CLK	IPMB_DAT	GND
8	GND	COM3-RX	COM3-TX	COM3-DTR#	COM3-DSR#	COM3-RTS#	GND
9	GND	COM3-CTS#	COM3-RI#	RGB-BLUE	RGB-RED	RGB-GREEN	GND
10	GND	USB-OC3#	RGB-DDCCLK	RGB-DDCDAT	RGB-HSYNC	RGB-VSYNC	GND
11	GND	USB-P3+	USB-P3-	GND	USB-P4+	USB-P4-	GND
12	GND	USB-P5+	USB-P5-	GND	USB-P6+	USB-P6-	GND
13	GND	USB-P7+	USB-P7-	GND	USB-P8+	USB-P8-	GND
14	GND	USB-OC4#	USB-OC5#	USB-OC6#	USB-OC7#	USB-OC8#	GND
15	GND	LAND_TXD1+	LAND_TXD1-	GND	LAND_TXD3+	LAND_TXD3-	GND
16	GND	LAND_TXD0+	LAND_TXD0-	GND	LAND_TXD2+	LAND_TXD2-	GND
17	GND	LANC_TXD1+	LANC_TXD1-	GND	LANC_TXD3+	LANC_TXD3-	GND
18	GND	LANC_TXD1+	LANC_TXD0-	GND	LANC_TXD2+	LANC_TXD2-	GND
19	GND	P5V	P5V	P12V	P5V	P5V	GND

Table 4-13: CompactPCI J3 Connector Pin Definition



High Definition audio
Keyboard/Mouse
Serial ATA
Serial ports
USB ports
Ethernet ports
RGB

CompactPCI J4 Connector Pin Assignment

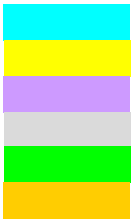
Pin	Z	A	B	C	D	E	F
1	GND	NC	PMC1 IO:64	PMC1 IO:63	PMC1 IO:62	PMC1 IO:61	GND
2	GND	PMC1 IO:60	PMC1 IO:59	PMC1 IO:58	PMC1 IO:57	PMC1 IO:56	GND
3	GND	PMC1 IO:55	PMC1 IO:54	PMC1 IO:53	PMC1 IO:52	PMC1 IO:51	GND
4	GND	PMC1 IO:50	PMC1 IO:49	PMC1 IO:48	PMC1 IO:47	PMC1 IO:46	GND
5	GND	PMC1 IO:45	PMC1 IO:44	PMC1 IO:43	PMC1 IO:42	PMC1 IO:41	GND
6	GND	PMC1 IO:40	PMC1 IO:39	PMC1 IO:38	PMC1 IO:37	PMC1 IO:36	GND
7	GND	PMC1 IO:35	PMC1 IO:34	PMC1 IO:33	PMC1 IO:32	PMC1 IO:31	GND
8	GND	PMC1 IO:30	PMC1 IO:29	PMC1 IO:28	PMC1 IO:27	PMC1 IO:26	GND
9	GND	PMC1 IO:25	PMC1 IO:24	PMC1 IO:23	PMC1 IO:22	PMC1 IO:21	GND
10	GND	PMC1 IO:20	PMC1 IO:19	PMC1 IO:18	PMC1 IO:17	PMC1 IO:16	GND
11	GND	PMC1 IO:15	PMC1 IO:14	PMC1 IO:13	PMC1 IO:12	PMC1 IO:11	GND
12-14	Key						
15	GND	PMC1 IO:10	PMC1 IO:9	PMC1 IO:8	PMC1 IO:7	PMC1 IO:6	GND
16	GND	PMC1 IO:5	PMC1 IO:4	PMC1 IO:3	PMC1 IO:2	PMC1 IO:1	GND
17	GND	NC	PMC2 IO:64	PMC2 IO:63	PMC2 IO:62	PMC2 IO:61	GND
18	GND	PMC2 IO:60	PMC2 IO:59	PMC2 IO:58	PMC2 IO:57	PMC2 IO:56	GND
19	GND	PMC2 IO:55	PMC2 IO:54	PMC2 IO:53	PMC2 IO:52	PMC2 IO:51	GND
20	GND	PMC2 IO:50	PMC2 IO:49	PMC2 IO:48	PMC2 IO:47	PMC2 IO:46	GND
21	GND	PMC2 IO:45	PMC2 IO:44	PMC2 IO:43	PMC2 IO:42	PMC2 IO:41	GND
22	GND	PMC2 IO:40	PMC2 IO:39	PMC2 IO:38	PMC2 IO:37	PMC2 IO:36	GND
23	GND	PMC2 IO:35	PMC2 IO:34	PMC2 IO:33	PMC2 IO:32	PMC2 IO:31	GND
24	GND	PMC2 IO:30	PMC2 IO:29	PMC2 IO:28	PMC2 IO:27	PMC2 IO:26	GND
25	GND	PMC2 IO:25	PMC2 IO:24	PMC2 IO:23	PMC2 IO:22	PMC2 IO:21	GND

Table 4-14: CompactPCI J4 Connector Pin Definition

CompactPCI J5 Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	PCIE-TX0+	PCIE-TX0-	GND	PCIE-RX0+	PCIE-RX0-	GND
2	GND	PCIE-TX1+	PCIE-TX1-	GND	PCIE-RX1+	PCIE-RX1-	GND
3	GND	PCIE-TX2+	PCIE-TX2-	GND	PCIE-RX2+	PCIE-RX2-	GND
4	GND	PCIE-TX3+	PCIE-TX3-	GND	PCIE-RX3+	PCIE-RX3-	GND
5	GND	GND	GND	GND	GND	GND	GND
6	GND	PCIE-CLK+	PCIE-CLK-	GND	RESET#	NC	GND
7	GND	GND	GND	RTC	GND	GND	GND
8	GND	LVDS_DATA3-	LVDS_DATA3+	NC	LVDS_CLK	LVDS_DATA	GND
9	GND	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GND
10	GND	TDC0+	TDC0-	GND	TDC1+	TDC1-	GND
11	GND	TDC2+	TDC2-	GND	TLC+	TLC-	GND
12	GND	DVI_DATA	DVI_CLK	DVI_HTPLG	NC	NC	GND
13	GND	LAND_100#	LANC_100#	NC	LANC_1G#	LAND_1G#	GND
14	GND	PMC2 IO:20	PMC2 IO:19	GND	SATA-TX5+	SATA-TX5-	GND
15	GND	PMC2 IO:18	PMC2 IO:17	GPIO6	SATA-RX5+	SATA-RX5-	GND
16	GND	PMC2 IO:16	PMC2 IO:15	GPIO7	PMC2 IO:14	PMC2 IO:13	GND
17	GND	PMC2 IO:12	PMC2 IO:11	GPIO8	PMC2 IO:10	PMC2 IO:9	GND
18	GND	PMC2 IO:8	PMC2 IO:7	DETECT#	PMC2 IO:6	PMC2 IO:5	GND
19	GND	PMC2 IO:4	PMC2 IO:3	NC	PMC2 IO:2	PMC2 IO:1	GND
20	GND	LVDS_DATA0-	LVDS_DATA0+	GND	LVDS_DATA1-	LVDS_DATA1+	GND
21	GND	LVDS_DATA2-	LVDS_DATA2+	GND	LVDS_CLK-	LVDS_CLD+	GND
22	GND	NC	LAND_LINK_ACT#	+3.3V	LANC_LINK_ACT#	+3.3V	GND

Table 4-15: CompactPCI J5 Connector Pin Definition



PCI-Express x4
GPIO
DVI
Ethernet port
LVDS
Serial ATA

4.5 Switch and Jumper Settings

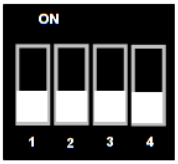
Refer to “cPCI-6510 Series Board Layout - Top Side” on page 21 and “cPCI-6510 Series Board Layout - Bottom Side” on page 22 for switch locations.

SW1 & SW4 (Debug use only)

The switches SW1 & 4 are for debugging purposes and should be left in the default settings. The default setting of SW1 is all OFF; the default setting of SW4 is Pin 1 OFF and Pin 2 ON.

Mode Switch (SW2)

Switch SW2 is a multi purpose switch that allows users to define the board operating mode. Four pins independently control the mode setting. All are set to OFF by default.



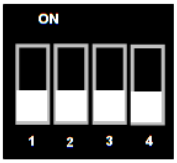
Pin#	Status	Description
1	OFF	**Universal Mode:** The cPCI-6510 in a peripheral slot has CompactPCI bus communication with the host board in the system slot. The cPCI-6510 can boot-up in a peripheral slot and be recognized by the host board in the system slot as a PCI device.
	ON	**Satellite Mode:** The cPCI-6510 in a peripheral slot has no CompactPCI bus communication with the host board in the system slot. The cPCI-6510 behaves a as standalone blade in the peripheral slot.
2	OFF	When the system does not include a CMM (Chassis Management Module), set this pin to OFF to allow IPMI to run in "without CMM mode".
	ON	When the system includes a CMM, set this pin to ON to allow IPMI to run in "with CMM mode".

Pin#	Status	Description
3	OFF	The cPCI-6510 cannot boot-up when installed in a peripheral slot if there is no host board in the system slot.
	ON	The cPCI-6510 is able to boot-up when installed in a peripheral slot if there is no host board in the system slot. The cPCI-6510 behaves as a system board in all slots. (Set this pin to "ON" if the cPCI-6510 is installed in a blade server backplane).
4	OFF	The cPCI-6510 power on/off is state is controlled by the ejector handle state.
	ON	Force the ejector handle state to "closed".

Table 4-16: Mode Switch Settings

PMC Bandwidth/Clock Switch (SW3)

Switch SW3 allows the user to force the PCI bus to lower bandwidth and clock settings. All are set OFF by default to support PCI-X mode up to 64bit/133MHz maximum with the bandwidth and clock determined by the PCI device attached.

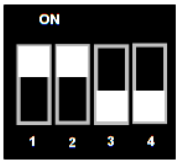


PIN	ON	OFF
1	Force the PCI bandwidth to 32bit	Auto Negotiation
2	Force the PCI clock to 66MHz	
3	Force the PCI bus to PCI mode (no PCI-X mode support)	
4	Force the PCI clock to PCI-X 100MHz	

Table 4-17: PMC Bandwidth/Clock Switch Settings

COM1/Debug Switch (SW5)

Switch SW5 sets the RJ-45 COM1 serial port as a standard RS-232 serial port or as an IPMI debugging port.



Mode	1	2	3	4
RS-232 COM port (default)	ON	ON	OFF	OFF
IPMI debugging port	OFF	OFF	ON	ON

Table 4-18: COM1/Debug Switch Settings

Clear CMOS Switch (SW6)

Press switch SW6 to clear the CMOS and reset the CMOS values to default.



Front/Rear VGA Selection Switch (SW8)

Switch SW8 sets the VGA output to the front panel or to the rear panel of the RTM. The default VGA output is set to front on the cPCI-6510V and to rear on the cPCI-6510.



Mode	1	2
Rear VGA output	ON	Not Used
Front VGA output	OFF	Not Used

Table 4-19: Front/Rear VGA Selection Switch Settings

5 Getting Started

This chapter describes the installation of the following components to the cPCI-6510 and rear transition modules:

- 2.5” SATA hard drive
- CompactFlash card
- PMC/XMC module installation
- cPCI-6510 installation to chassis
- RTM installation to chassis

5.1 Hard Drive Installation

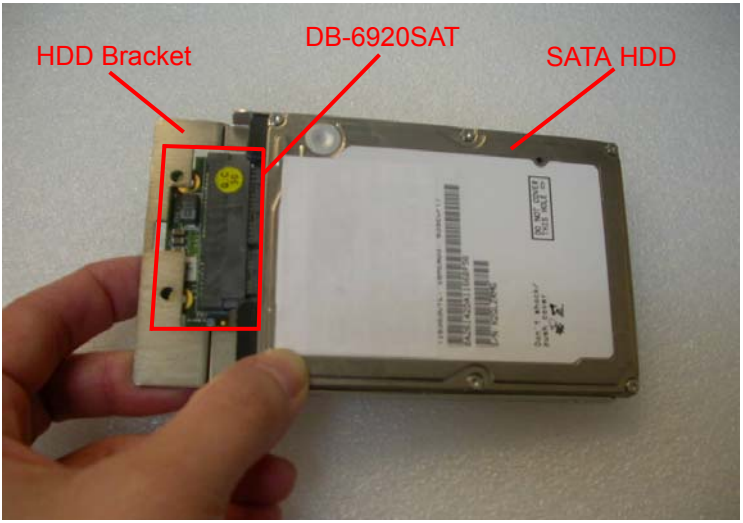
The cPCI-6510V provides space to install a slim type 2.5" Serial-ATA hard drive.

Installing a SATA Hard Drive - cPCI-6510V

NOTE:

Install a CF card to the cPCI-6510 before installing the hard drive (see "Installing a CF card – cPCI-6510" on page 45).

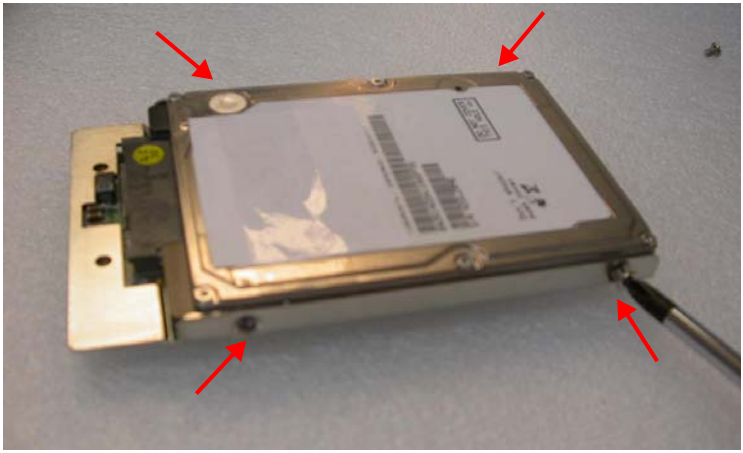
1. Attach the DB-6920SAT adapter board to the SATA hard drive connectors. Position the hard drive on the HDD bracket provided as shown below. Be sure the adapter board is under HDD bracket to avoid damaging the hard drive connectors.



CAUTION:

Make sure the adapter board is under the HDD bracket to avoid damaging the hard drive connectors.

2. Secure the HDD to the bracket with four screws provided.



3. Position the hard drive assembly on the cPCI-6510V so that the standoffs are aligned with the screw holes on the board, and the connector on the DB-6920SAT adapter board is aligned with the board-to-board connector (CN3).



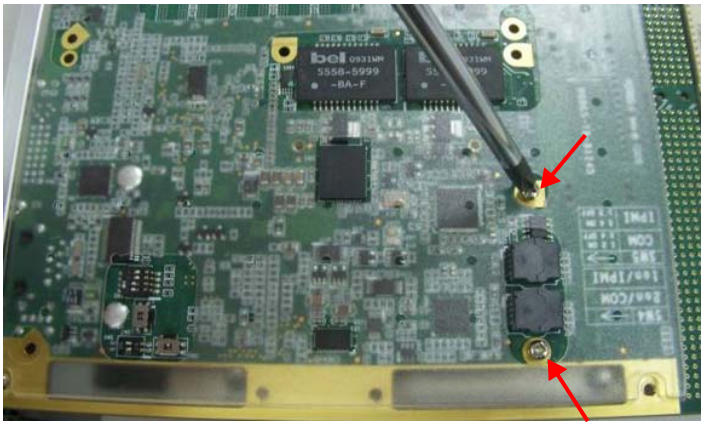
4. Press the DB-6920SAT adapter onto the board-to-board connector until it is properly seated. Secure the adapter to the board with the two screws provided.



CAUTION:

Support the hard drive assembly when turning the board over to proceed with step 5.

5. Secure the hard drive with two screws from the solder side of the board.



Removing the SATA Hard Drive - cPCI-6510V

Reverse steps 1 through 5 above to remove the SATA hard drive.

CAUTION:

When removing the hard drive, be careful to hold the adapter board and lift upwards in a vertical motion to disconnect it from the board-to-board connector. This will avoid damaging the adapter board and connectors.

5.2 CompactFlash Card Installation

Installing a CF card – cPCI-6510

Insert the CF card into the CF slot on the cPCI-6510 (CN5 - see “cPCI-6510 Series Board Layout - Top Side” on page 21). Then install the card retaining bracket with the 2 screws provided to prevent the CF card from sliding out of the slot. If necessary, first remove the hard drive assembly by reversing the steps described in “Installing a SATA Hard Drive - cPCI-6510V” on page 42 above.



5.3 PMC/XMC Module Installation

The cPCI-6510 provides one PMC and one PMC/XMC slot and the cPCI-6510V provides one PMC/XMC slot. The PMC/XMC slots support 3.3V V(I/O) and 5V VPWR only. For optional 5V V(I/O) and 12V VPWR support, please contact ADLINK.

Installing a PMC/XMC Module

1. Remove the PMC filler faceplate from the front panel.
2. Align the male connectors of the PMC/XMC card (component-side down) to the female connectors of the cPCI-6510 and press down.
3. Secure the PMC/XMC card to the cPCI-6510 by attaching four screws (provided with the card) from the bottom side of the board.

5.4 Installing the cPCI-6510 to the Chassis

The cPCI-6510 may be installed in a system or peripheral slot of a 6U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-6510 ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the front panel.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module front panel.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

5.5 Installing the RTM to the Chassis

The installation and removal procedures for a RTM are the same as those for CompactPCI boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-6510 Series and related RTMs, make sure the RTM is the correct matching model.



You must install the correct RTM to enable functions (I/O interfaces) on the rear panel. Installation of non-compatible RTMs may damage the system board and/or other RTMs.

6 Driver Installation

The cPCI-6510 drivers can be found on the ADLINK All-In-One CD at **X:\cPCI\cPCI-6510** or from the ADLINK website (**http://www.adlinktech.com**). ADLINK provides validated drivers for chipset, graphics and LAN on Windows XP Professional, Windows Vista, and Windows 7.

6.1 Driver Installation Procedure

The following describes the driver installation procedures for Windows XP.

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **...\Chipset\ Intel_INF_Update_Utility_WinAllOS_v9.1.1.1023.zip**.
3. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\ Intel_Graphics_Adapter_WinXP32_v6.14.10.5237.zip**.
4. Install the **LAN drivers** by extracting and running the program in **…\LAN\Intel_Network_Adapter_WinXP32_v11.4.7.0.zip**.

We recommend using the drivers provided on the ADLINK All-in-One CD or downloading them from the ADLINK website to ensure compatibility. The Vxworks BSP can be downloaded from the cPCI-6510 product page on the ADLINK website (**http://www.adlinktech.com**).

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7 Utilities

7.1 Watchdog Timer

This section describes the operation of the cPCI-6510's watchdog timer (WDT). The primary function of the WDT is to monitor the cPCI-6510's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- reloading timeout value

The cPCI-6510 custom WDT circuit is implemented using the internal IO of the ITE Super I/O IT8783 which is at address 2Eh of LPC. The basic functions of the WDT include:

- Starting the timer countdown
- Enabling or disabling WDT
- Enabling or disabling WDT countdown LED ON
- Reloading the timeout value to keep the watchdog from timing out
- Setting the range of the timeout period from 1 to 15300 seconds or minutes
- Sending a RESET signal to the system when the watchdog times out

Using the Watchdog in an Application

The following section describes using the WDT functions in an application. The WDT reset function is explained in the previous section. This can be controlled through the registers in the cPCI-6510's Super I/O.

An application using the reset feature enables the watchdog function, sets the count-down period, and reloads the timeout value periodically to keep it from resetting the system. If the timer count-down value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

For a detailed programming sample, refer to the sample code provided on the ADLINK All-In-One CD. You can find it in the following directory: **X:\cPCI\cPCI-6510\WDT**.

Sample Code

The sample program written in C shown below offers an interactive way to test the Watchdog Timer under DOS.

```
#include<stdio.h>
#include<dos.h>

#define IT8783_ID1 0x87
#define IT8783_ID2 0x83

static unsigned int IT8783_ioPort = 0x2e;

//Check index port
void Enter_IT8783_Config(unsigned int flag)
{
     if(flag) IT8783_ioPort = 0x4e;

     switch(IT8783_ioPort)
     {
          case 0x2E:  //Address port = 0x2E, enter keys =
     0x87, 0x01, 0x55, 0x55
               outportb(0x2E, 0x87);
               outportb(0x2E, 0x01);
               outportb(0x2E, 0x55);
               outportb(0x2E, 0x55);
               break;
          case 0x4E:  //Address port = 0x4E, enter keys =
     0x87, 0x01, 0x55, 0xAA
               outportb(0x4E, 0x87);
               outportb(0x4E, 0x01);
               outportb(0x4E, 0x55);
               outportb(0x4E, 0xAA);
               break;
          default:
               break;
        }
}
```

```
//Exit index port
void Exit_IT8783_Config(unsigned int flag)
{
     if(flag) IT8783_ioPort = 0x4e;

     outportb(IT8783_ioPort, 0x02);
     outportb(IT8783_ioPort+1, 0x02);
}

//Check chip
void Get_IT8783_ID(unsigned int &ID1, unsigned int &ID2)
{
     outportb(IT8783_ioPort, 0x20);
     ID1 = inportb(IT8783_ioPort+1);
     outportb(IT8783_ioPort, 0x21);
     ID2 = inportb(IT8783_ioPort+1);
}

//WDT and LED program
void IT8783_3_WDTRun(unsigned int count_value, unsigned
     int PLEDflag)   //for cPCI-6510
{
     unsigned long tempCount;
     unsigned int registerValue;


     outportb(IT8783_ioPort, 0x07);
     outportb(IT8783_ioPort+1, 0x07);// Device 7

     outportb(IT8783_ioPort, 0xf8);
     outportb(IT8783_ioPort+1, 0x00);// PLED mapping to
     nothing, disable PLED function

     if(PLEDflag == 1)
     {
          outportb(IT8783_ioPort, 0x2D);
          registerValue = inportb(IT8783_ioPort + 1);
          registerValue |= 0x01;       // set Pin109 is
     GPIO function GP60
          outportb(IT8783_ioPort+1, registerValue);

          outportb(IT8783_ioPort, 0xC5);
          registerValue = inportb(IT8783_ioPort + 1);
```

```
      registerValue &= 0xfe;      // set GP60 is
alternate function
      outportb(IT8783_ioPort+1, registerValue);

      outportb(IT8783_ioPort, 0xCD);
      registerValue = inportb(IT8783_ioPort + 1);
      registerValue |= 0x01;  // set GP60 is output
      outportb(IT8783_ioPort+1, registerValue);

      outportb(IT8783_ioPort, 0xf8);
      outportb(IT8783_ioPort+1, 0x30);// PLED
mapping to GP60

      outportb(IT8783_ioPort, 0xf9);
      registerValue = inportb(IT8783_ioPort + 1);
      registerValue |= 0x02;
      registerValue &= 0xfb;
      outportb(IT8783_ioPort+1, registerValue);
}
outportb(IT8783_ioPort, 0x71);
registerValue = inportb(IT8783_ioPort + 1);
registerValue |= 0xD0;  // set Mouse & Keyboard
interrupt Enable
outportb(IT8783_ioPort+1, registerValue);

outportb(IT8783_ioPort, 0x73);
outportb(IT8783_ioPort+1, count_value);
// set WDT count LSB
tempCount = tempCount >> 8;
outportb(IT8783_ioPort, 0x74);
outportb(IT8783_ioPort+1, count_value);
// set WDT count MSB

if(count_value >= 60)
{
      outportb(IT8783_ioPort, 0x72);
      registerValue = inportb(IT8783_ioPort+1);
      registerValue &= 0x8f;
      registerValue |= 0x10; //enable WDT output
through PowerOK!
      outportb(IT8783_ioPort+1, registerValue);
      // set WDT count is minute
```

```
            tempCount = count_value / 60;
            if((count_value%60) > 30)
                  tempCount++;
            if(tempCount > 65535)
                  tempCount = 65535;
            printf("WDT timeout in %d minutes.\n",
      tempCount);
      }
      else
      {
            outportb(IT8783_ioPort, 0x72);
            registerValue = inportb(IT8783_ioPort+1);
            registerValue |= 0x80;

            tempCount = count_value;
            if(tempCount != 0)
            {
                  printf("WDT timeout in %d seconds.\n",
      tempCount);
                  registerValue |= 0x40; //Enable WDT
      output through KBRST
            }
            else
            {
                  printf("WDT is Disabled.\n");
                  registerValue &= 0xbf; //Disable WDT
      output through KBRST
            }

            outportb(IT8783_ioPort+1, registerValue);
            // set WDT count is second
      }

}
```

7.2 Preboot Execution Environment (PXE)

The cPCI-6510 series supports the Intel® Preboot Execution Environment (PXE) that is capable of booting up or executing an OS installation through an Ethernet port. To use PXE, there must be a DHCP server on the network with one or more servers running PXE and MTFTP services. It could be a Windows® 2003 server running DHCP, PXE, and MTFTP services or a dedicated DHCP server with one or more additional servers running PXE and MTFTP services.

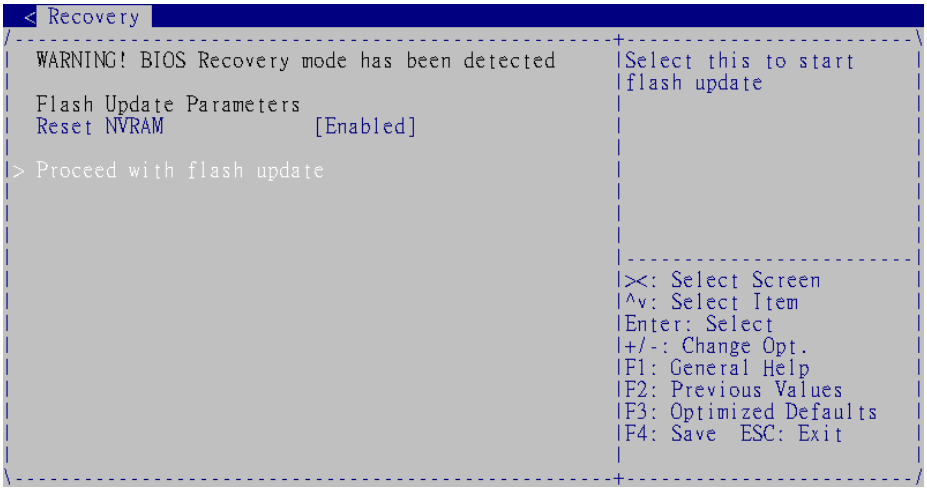
To build a network environment with PXE support:

1. Setup a DHCP server with PXE tag configuration
2. Install the PXE and MTFTP services
3. Make a boot image file on the PXE server (i.e. the boot server)
4. Enable the PXE boot function on the client computer

7.3 BIOS Recovery

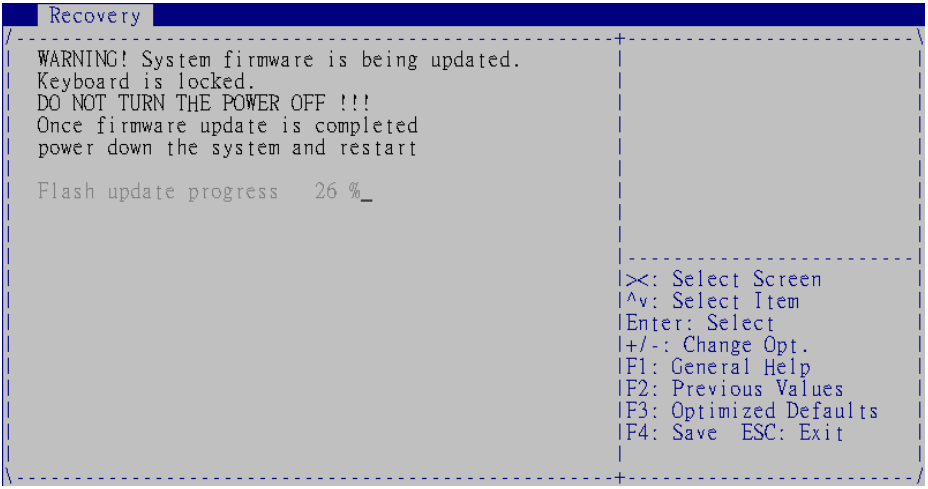
The cPCI-6510 Series features AMI® EFI BIOS with BIOS recovery. If the BIOS becomes corrupted and you are unable to boot your system, the system will sound 4 beeps. Follow the instructions below to re-flash the BIOS and recover the system.

1. Download the BIOS recovery file “C6510000.ROM” from the product website at: www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=943
2. Prepare a bootable USB flash drive and copy the recovery file “C6510000.ROM” to the root directory.
3. Insert the USB flash drive into the cPCI-6510 and power up the system.
4. The system will sound 4 beeps to indicate boot failure, and then it will sound 2 beeps to indicate it is entering Recovery Mode. You will see the screen below:

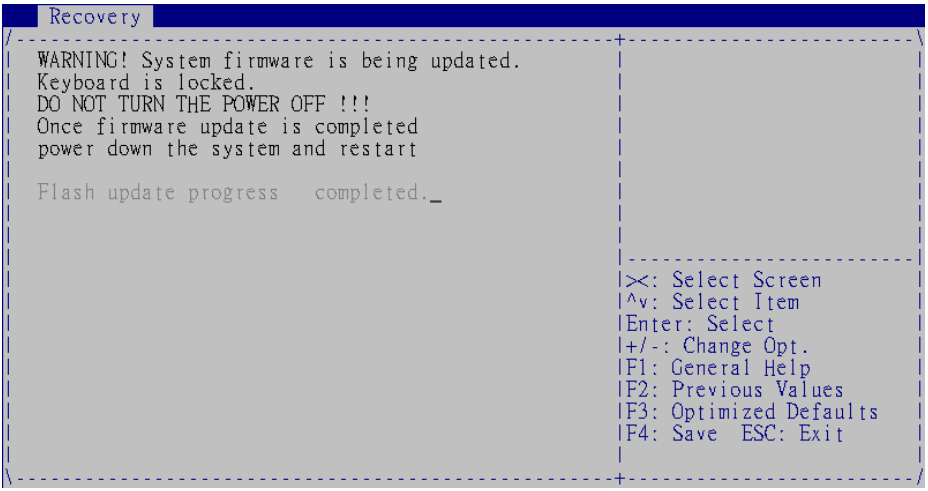


5. Select “Proceed with flash update” and press **Enter**.

6. During the BIOS recovery process, you will see the following:



7. After the flash update is completed, power down the system and restart. The system should now boot up normally.



7.4 Programming NT Mode EEPROM Map

The cPCI-6510 supports operation in peripheral slot as PCI device with PCI bus communication with the system board (Universal Mode). To operate in a peripheral slot in Non-Transparent mode, the PCIe-to-PCI bridge on the cPCI-6510 should be set to Non-Transparent mode by programming the NT mode EEPROM map. The EEPROM map can be downloaded from the cPCI-6510 product page on the ADLINK website:
http://www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=943

To set the PCIe-to-PCI bridge on the cPCI-6510 to NT mode, perform the following steps:

1. Download the EERPOM map cPCI-6510_NT.rar from the cPCI-6510 product website under *Utilities*.
2. Prepare a bootable USB flash drive and extract the contents of the folder cPCI-6510_NT into the root directory.
3. Insert the USB flash drive into the cPCI-6510 in system slot and power up the system.
4. Execute the file NT.bat to program the bridge to Non-Transparent mode. The board will then operate in a peripheral slot as a PCI device.
5. To return the cPCI-6510 to Transparent mode, execute the file TR.bat.

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8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



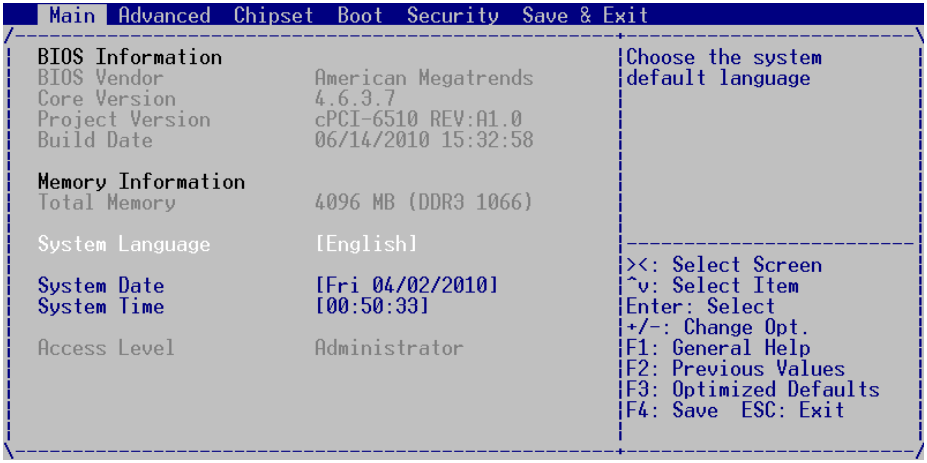
Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

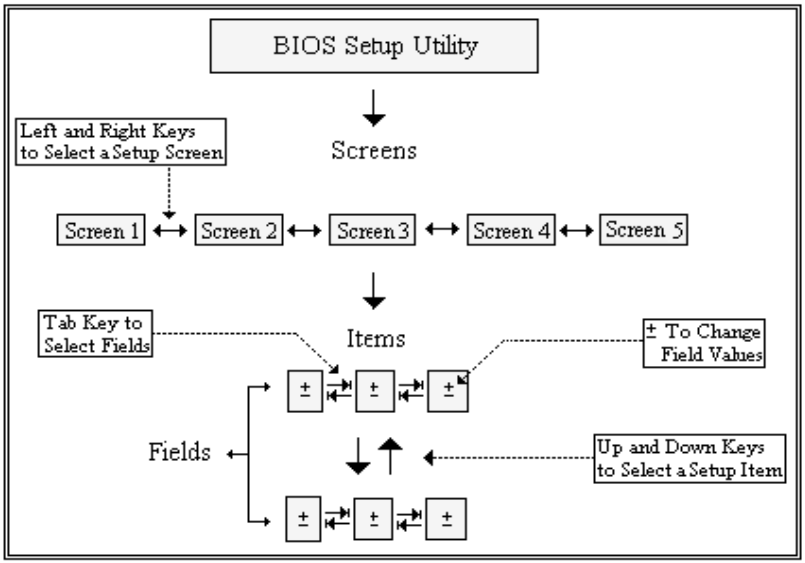
The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



Navigation



Note: There is a hot key legend located in the right frame on most setup screens.

Keyboard Commands

Enter Selects the highlighted option or submenu.

< > The *Left* and *Right* "Arrow" keys allow you to select a setup screen.

^ v The *Up* and *Down* "Arrow" keys allow you to select a setup screen.

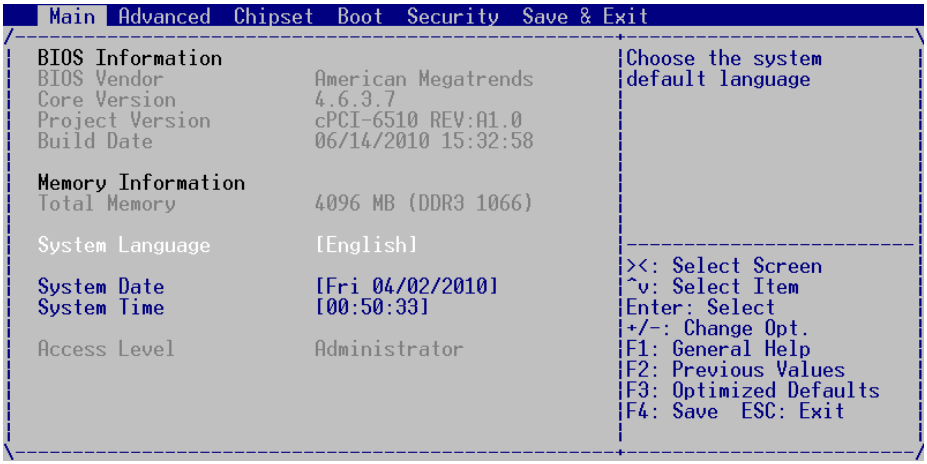
+ - The *Plus* and *Minus* keys allow you to change the field value of a particular setup item.

Tab Moves the cursor to the next configurable item or to the next field.

Esc The *Esc* key allows you to discard any changes you have made and exit the Setup menu. Press the *Esc* key to exit the Setup menu without saving your changes. Press the *Enter* key to discard changes and exit. You can also use the "Arrow" keys to select Cancel and then press the *Enter* key to abort this function and return to the previous screen.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Language

Choose the system default language.

System Time/System Date

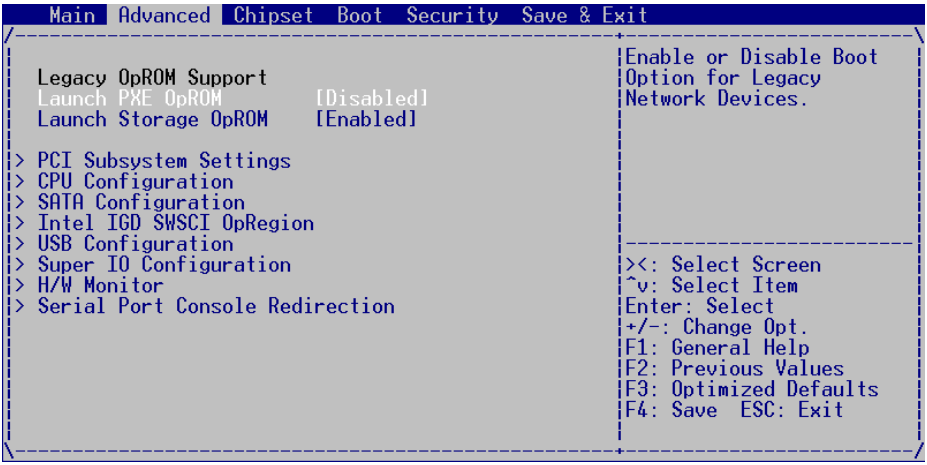
Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



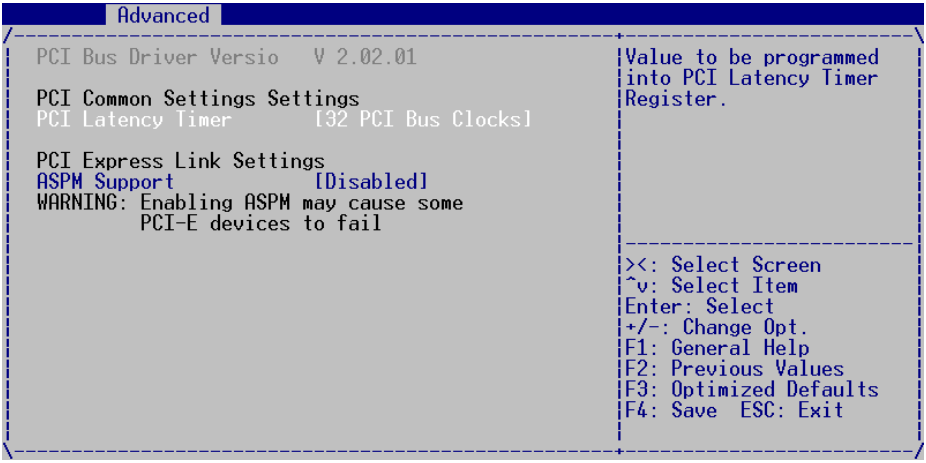
Launch PXE OpROM

Boot option for legacy network devices. Options: LAN1, LAN2, LAN3, LAN4, Disabled.

Launch Storage OpROM

Boot option for legacy mass storage devices with Option ROM. Options: Enabled/Disabled.

PCI Subsystem Settings



PCI Latency Timer

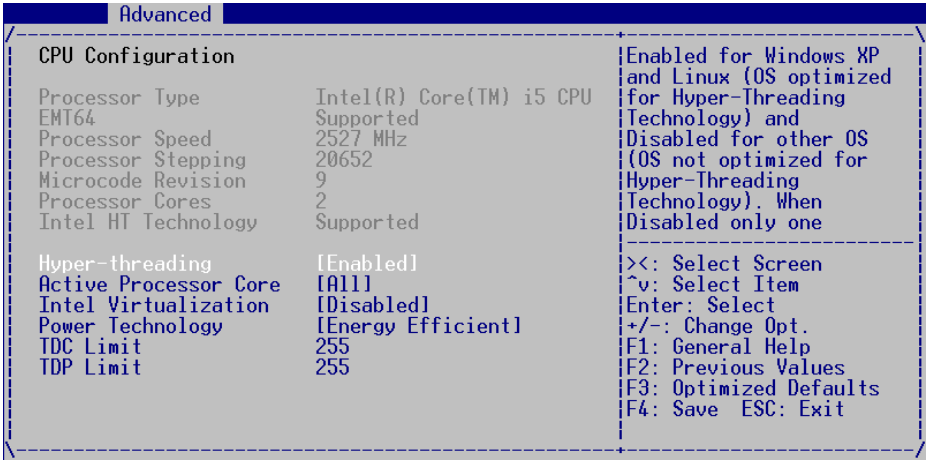
Value to be programmed into PCI Latency Timer Register. Options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks.

ASPM Support

Set the ASPM (Active State Power Management) level. Options:

- **Disabled:** Disable ASPM
- **Auto:** BIOS auto configure
- **Force L0:** Force all links to L0 State

CPU Configuration



Hyper-Threading

Enables/disables Hyper-Threading Technology.

Active Processor Cores

Number of cores to enable in each processor package. Options: All, 1, 2.

Intel Virtualization

Enables/disables Intel Virtualization Technology.

Power Technology

Power management feature. Options: Disabled, Energy Efficient, Custom.

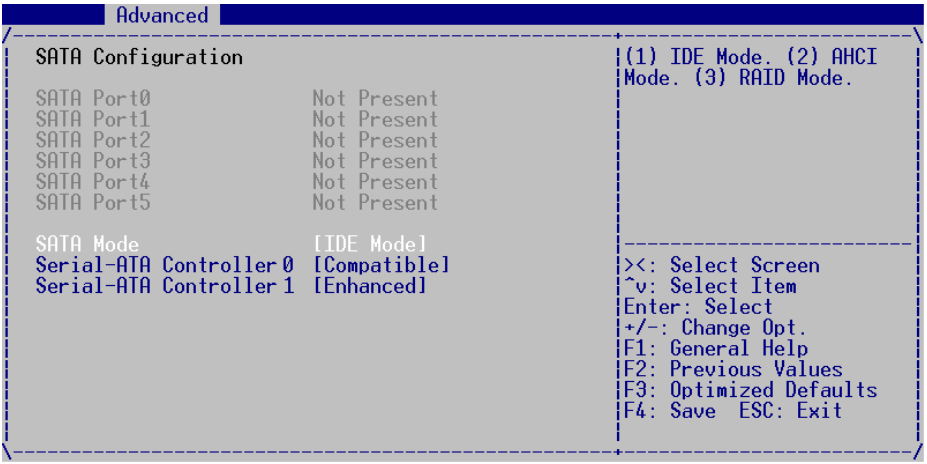
TDC Limit

Turbo-XE Mode Processor TDC Limit in 1/8 A granularity.
0 means use the factory-configured value.

TDP Limit

Turbo-XE Mode Processor TDP Limit in 1/8 W granularity.
0 means use the factory-configured value.

SATA Configuration



SATA Mode

The SATA can be configured as a legacy IDE, RAID and AHCI mode.

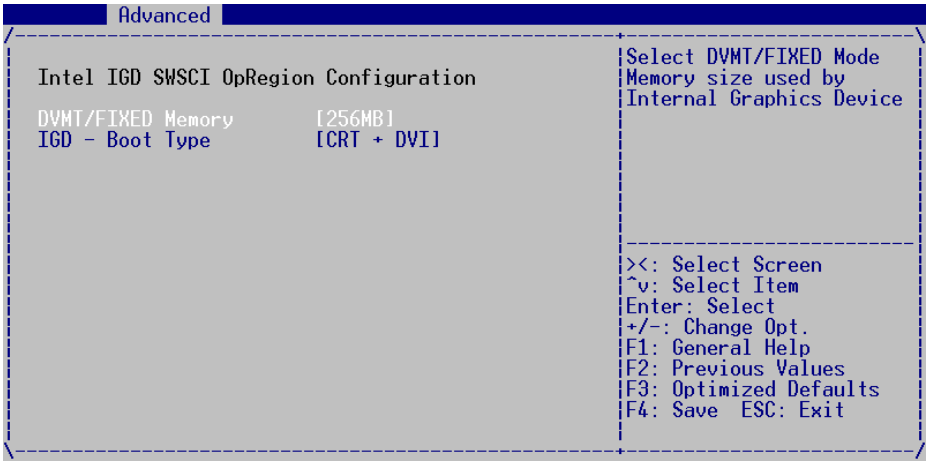
Serial ATA Controller 0

This item specifies whether SATA Controller 0 is initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

Serial ATA Controller 1

This item specifies whether SATA Controller 1 is initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

Intel IGD SWSCI OpRegion Configuration



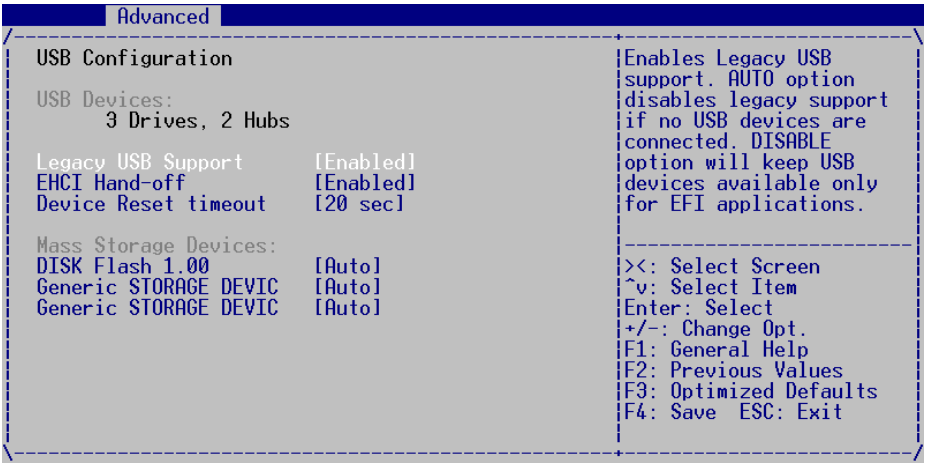
DVMT/FIXED Memory

Select DVMT/FIXED Mode Memory size used by internal Graphics Device. Options: 128MB, 256MB, Maximum.

IGD – Boot Type

Selects the Video Device(s) to be activated during POST. This option has no effect if external graphics present. Options: CRT, DVI, TV, CRT+DVI.

USB Configuration



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even when there is no USB driver loaded on the system. Set this value to enable or disable the Legacy USB Support.

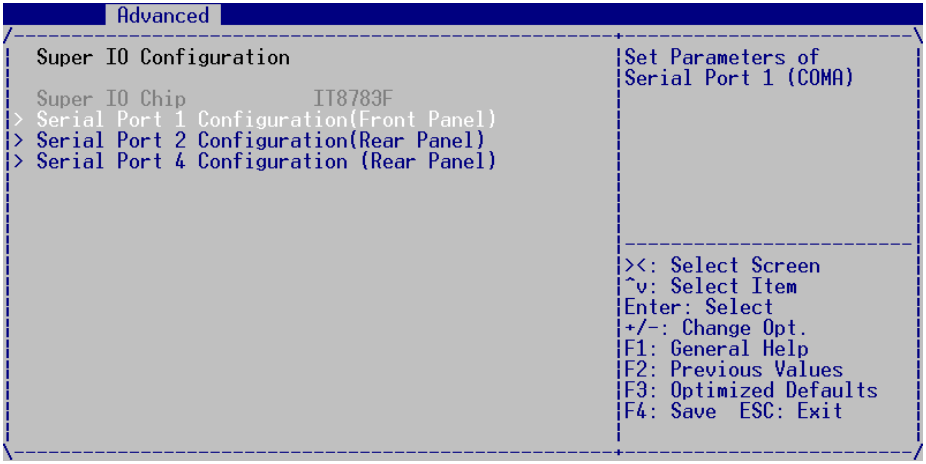
EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI driver. Options: Enable, Disable.

Device Reset Timeout

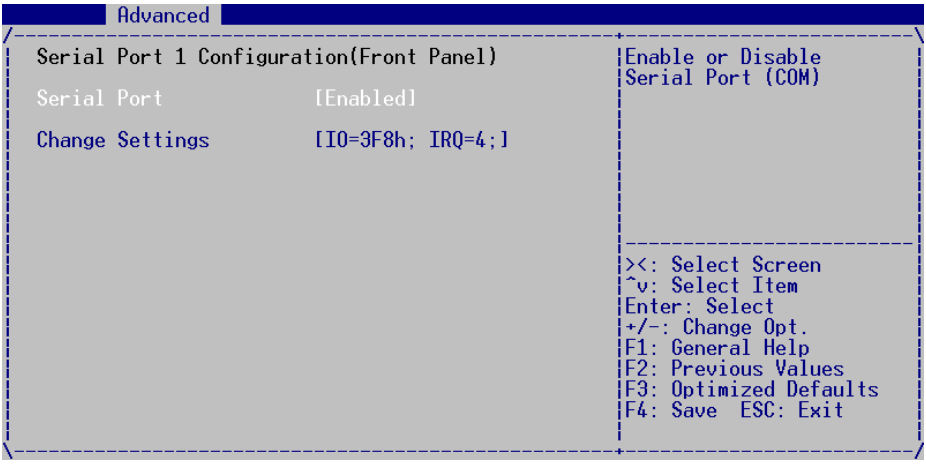
USB mass storage device Start Unit command timeout.

Super IO Configuration

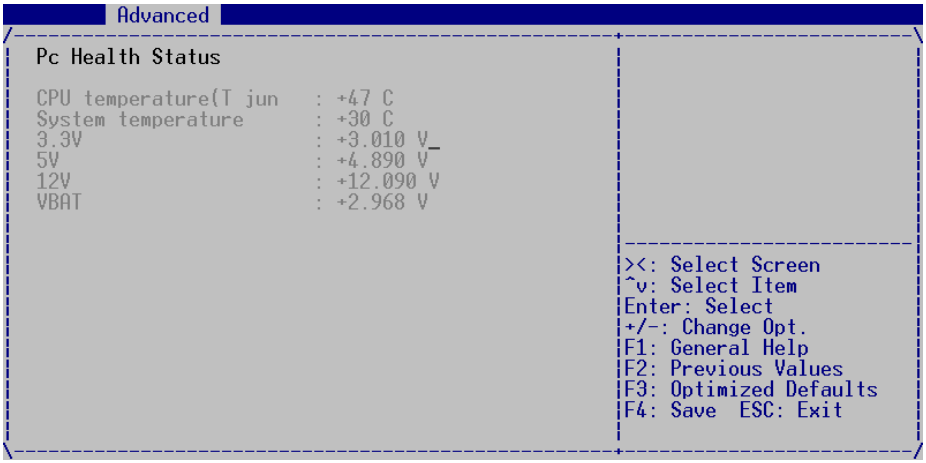


Serial Port 1/2/4 Configuration

Sub-menu allows you to Enable/Disable and set the parameters of Serial Ports 1, 2, 4.

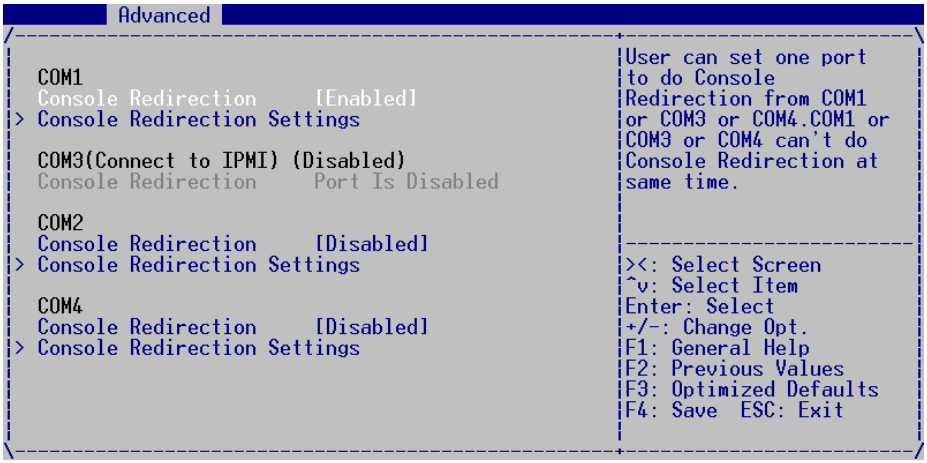


PC Health Configuration

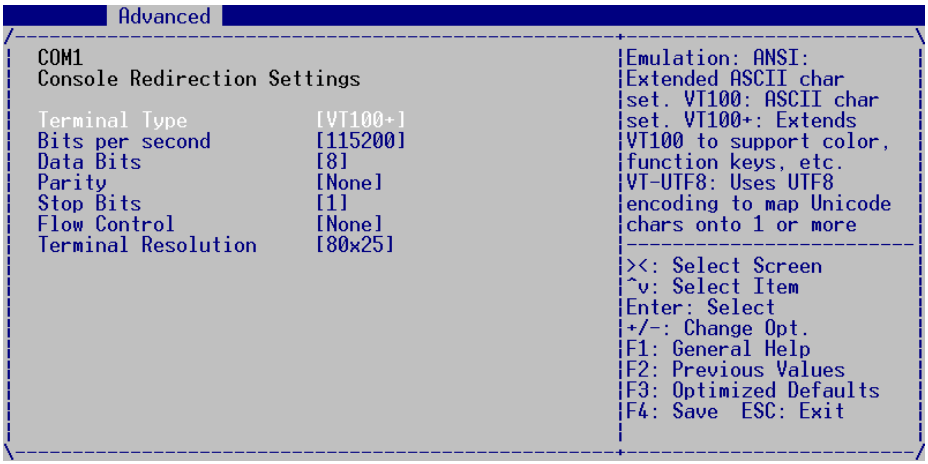


Console Redirection

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings.



The user can enable one serial port for Console Redirection. Only one port can be used for Console Redirection at any time.



Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. Options: VT100, VT100+, VT-UTF8, ASNI.

Bits per Second

Select the bit rate (bits/second) you want the serial port to use for console redirection. Options: 115200, 57600, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7 or 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 or 2.

Flow Control

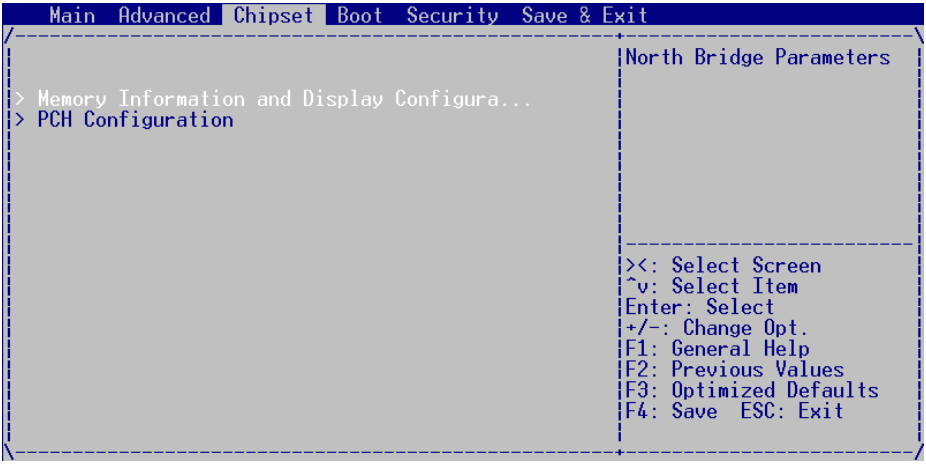
Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware, Software.

Terminal Resolution

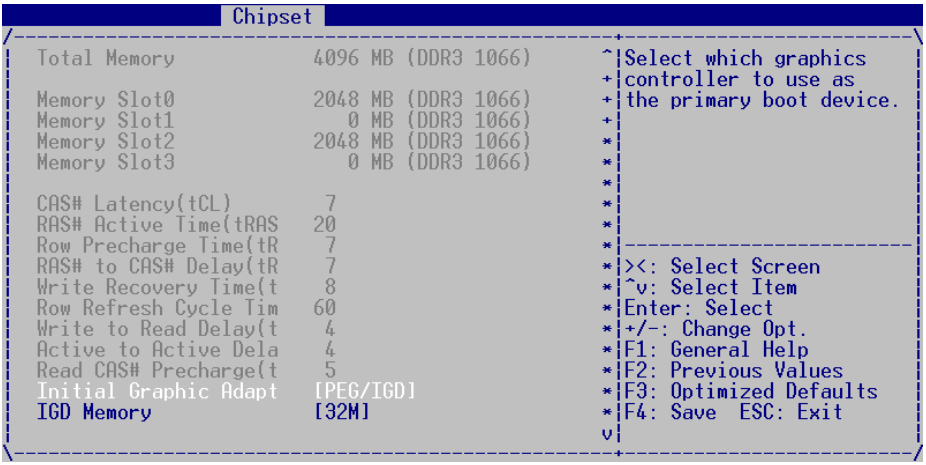
Remote Terminal Resolution. Options: 80x25, 100x31.

8.4 Chipset Configuration

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



Memory Information and Display Configuration



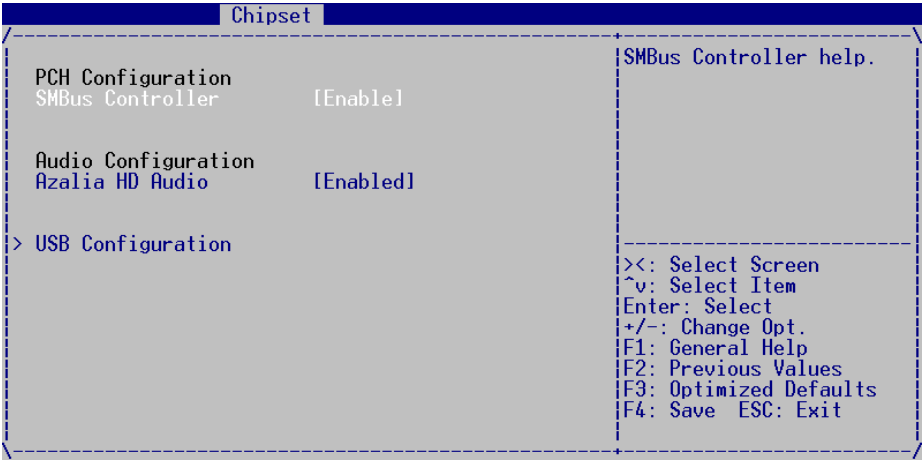
Initial Graphic Adapter

Allows you to select which graphics controller to use as the primary boot device. Configuration options: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

IGD Memory

IGD shared memory size. Options: Disabled, 32M, 64M, 128M.

PCH Configuration



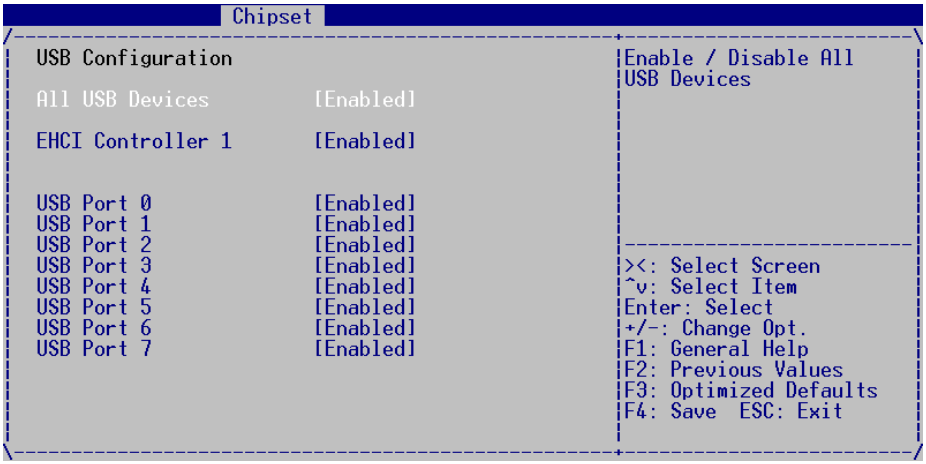
SMBus Controller

The SMBus controller. Set this value to Enable/Disable.

Azalia HD Audio

The onboard HDA Controller. Set this value to Enable/Disable.

USB Configuration



All USB Devices

All USB Devices. Set this value to Enabled/Disabled.

EHCI Controller 1

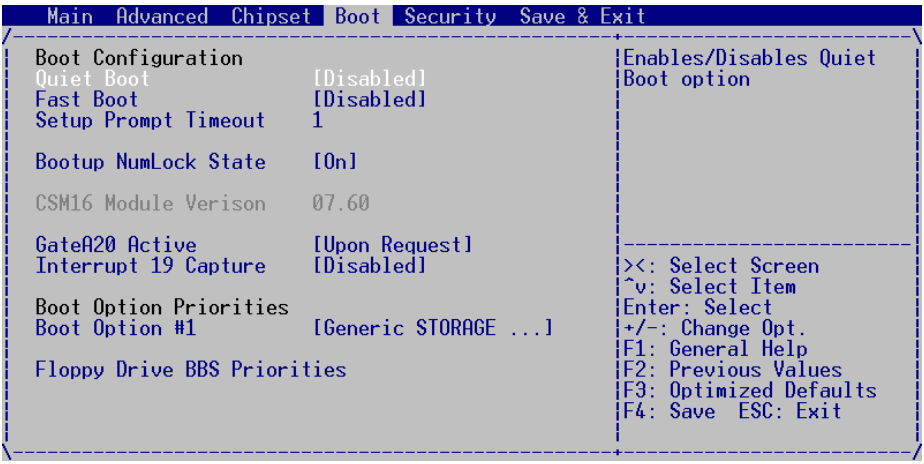
USB 2.0 (EHCI) support. Set this value to Enabled/Disabled.

USB Port

USB Port 0~7.Set this value to Enabled/Disabled.

8.5 Boot Configuration

Select the Boot tab from the setup screen to enter the Boot Configuration screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display a Boot Configuration option by highlighting it using the < Arrow > keys. The Boot Configuration screen is shown below:



Quiet Boot

When this feature is **enabled**, the BIOS will display the OEM logo during the boot-up sequence, hiding normal POST messages. When it is **disabled**, the BIOS will display the normal POST messages, instead of the OEM logo.

Fast Boot

Enabling this setting will cause the BIOS Power-On Self Test routine to skip some of its tests during bootup for faster system boot.

Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.

Bootup Num-Lock

This option sets the Num Lock status when the system is powered on. Setting it to On will turn on the Num Lock key when the system is booted up. Setting it to Off will not enable the Num Lock key on bootup.

GateA20 Active

Upon Request: GA20 can be disabled using BIOS services. **Always:** do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Interrupt 19 Capture

Allows Option ROMs to trap Int 19. Set this value to Enabled or Disabled.

Boot Option #1

Set the boot device options to determine the sequence in which the computer checks which device to boot from.

BBS Priorities

Selects the boot devices available for each device type to be used for Boot Option Priorities settings.

8.6 Security Setup



Administrator Password

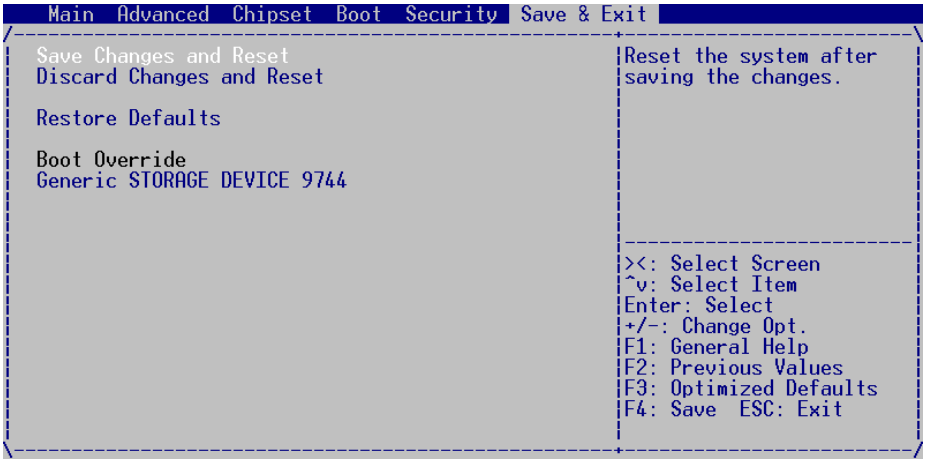
Use this option to set a password for administrators with full control of the BIOS setup utility.

User Password

Use this option to set a password for users with limited access to the BIOS setup utility.

8.7 Save & Exit

Select the Save & Exit tab from the setup screen to enter the Save & Exit setup screen. You can display a Save & Exit BIOS setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS setup screen is shown below.



Save Changes and Reset

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Discard Changes and Reset

Select this option to quit Setup without making any permanent changes to the system configuration.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Boot Override

Use the up/down arrow keys to highlight a boot device to immediately exit the BIOS Setup and boot from the selected device.

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9 IPMI User Guide

9.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

9.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the BMR-AVR-cPCI. For detailed information on supported commands, please refer to the Intelligent Platform Management Interface Specification downloadable from the Intel website (http://www.intel.com/design/servers/ipmi/spec.htm).

Command	IPMI Spec	NetFn	CMD	Description
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself.
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any.
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller.

Command	IPMI Spec	NetFn	CMD	Description
Broadcast “Get Device ID”	20.9	App	01h	This is a broadcast version of the ‘Get Device ID’ command that is provided for the ‘discovery’ of Intelligent Devices on the IPMB
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel.
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command.
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer.
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer.
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages.
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators.
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL).

Command	IPMI Spec	NetFn	CMD	Description
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device.
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned.
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*.
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation.
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor.
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor.
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor.
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit.
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/ disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor.
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection.

Command	IPMI Spec	NetFn	CMD	Description
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request.
Get Sensor Type	35.16	S/E	2Fh	This command is used to assign the Sensor Type and Event/Reading Type to a specified sensor.
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes.
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area.
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area.

9.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (C0h)	12h
OemRescanGaInput	OEM (C0h)	22h
OemTestFunction	OEM (C0h)	30h
OemSetBlueLEDLongBlinking	OEM (C0h)	31h
OemReportGeoAddress	OEM (C0h)	F0h
OemEnableSmbus	OEM (C0h)	F2h
OemDisableSmbus	OEM (C0h)	F3h
OemDispDebugVariable	OEM (C0h)	F4h
OemResetHost	OEM (C0h)	F5h
OemPowerOff	OEM (C0h)	F6h
OemPowerOn	OEM (C0h)	F7h

OemShowRevision

This command is used to show the current information of the firmware including the firmware revision, the product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	*Firmware Rev	'V' in ASCII code for verification
	3	*Firmware Rev	Revision info high byte
	4	*Firmware Rev	Revision info low byte
	5	*Product ID	'P' in ASCII code for verification
	6	*Product ID	Product info high byte
	7	*Product ID	Product info low byte
	8	*Special info	'S' in ASCII code for verification
	9	*Special info	Addition info byte
	10	5Ah	Internal check byte. Always 5Ah

OemRescanGaInput

This command is used to rescan the geo-address input pins and reset the IPMB address according to the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemSetBlueLEDLongBlinking

This command is used to enable or disable the slow blink of the blue HotSwap LED when a voltage is detected to be over ±5% out of range for five seconds (see Table 4-1 on page 22). This function is set to enabled by default.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	31h	OEM defined command
	2	00h or 01h	00h: disable slow blink capability 01h: enable slow blink capability
Response	0	Complete Code	00h means OK

OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

This command is used to turn on the I2C bus when it is off during boot up process. Usually BIOS will perform this command after booting in boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command
Response	0	Complete Code	00h means OK

OemDisableSmbus

This command is used to shut down I2C bus access.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

OemDispDebugVariable

This command can report up to 5 interval values for debug purposes. For developers only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	

OemResetHost

This command is implemented to control the system's status if rebooting is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOff

This command is implemented to control the system's status if power-off is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOn

This command is implemented to control the system's status if power-on is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

9.4 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

9.5 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x3E8 and IRQ: 3. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use “COM3” to communicate with the IPMC.

9.6 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Remark
00h	BMC Watchdog		
01h	3.3V	3.3 V	
02h	5V	5 V	
03h	12V	12 V	
04h	SYSTEM Temp	25°C	
05h	CPU Temp	40°C	
06h	BIOS CHANGE		
07h	BIOS POST ERROR		

9.7 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v2.0	Document Revision 1.1 February 20, 2002	Intel Corp. http://www.intel.com/design/servers/ipmi/spec.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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