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cPCI-3840 Series

3U CompactPCI Pentium(R) M
CPU Module

User's Manual

Manual Rev. 2.01

Revision Date: December 18, 2006

Part No: 50-15034-100

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Product Model	
Environment	OS: M/B: CPU: Chipset: Bios:

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1 Introduction

The cPCI-3840 is designed to be a high performance dual slot 3U CompactPCI CPU Module. It features a single Intel® Pentium® M processor with 1MB L2 cache in a 478-pin Micro-FCPGA package, and is validated with the Intel® 855GME chipset that supports 144-bit wide PC2100/2700 (266/333 MHz) registered ECC DDR DIMM up to a maximum of 2GB. The cPCI-3840 also features the Intel® 82546EB Dual Port Gigabit Ethernet Controller and supports one ATA33/66/100 IDE channel, one Compact Flash type I/II connector, and 2 ports SATA for high volume storage applications.

The Intel® Pentium® M is a high performance, low power mobile processor with several micro-architecture enhancements over existing Intel Mobile processors. Intel® Pentium® M supports Intel® Architecture with Dynamic Execution, on-die primary 32-KB instruction cache and 32-KB write-back data cache, on-die 1-MB second level cache with Advanced Transfer Cache Architecture, Advanced Branch Prediction and Data Prefetch Logic, Streaming SIMD Extensions 2 (SSE2), a 400-MHz Source-Synchronous processor system bus, and Advanced Power Management features including Enhanced Intel® SpeedStep® technology.

The Intel® Pentium® M processor system bus supports AGTL+ bus driver technology with integrated GTL termination resistors, (gated AGTL+ receivers for reduced power), 32-bit AGTL+ bus addressing (no support for 36-bit address extension), 400MT/s BPSB (100MHz), 2X address, 4X data, and 12 deep in-order queues.

The Intel® 855GME chipset north bridge contains a Graphics Memory Controller Hub (GMCH) component for embedded platforms. The GMCH provides the processor interface, system memory interface (DDR SDRAM), hub interface, CRT, and a DVO interface. The GMCH also supports 128-MB, 256-MB, and 512-MB memory technologies, 16 simultaneous open pages, and 64-bit data interface (72-bit with ECC).

Furthermore, the 855GME features a 350 MHz integrated 24bit RAMDAC supporting analog display with pixel resolution up to 1600x1200 at 85Hz and 2048x1536 at 75Hz, dual independent display pipe supporting concurrent or simultaneous display on

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each display device, digital video output with 165 MHz output clock on a 12-bit interface via one port DVO supporting pixel resolution up to 1600x1200 at 85Hz, Tri-view support through a LFP interface, DVO and CRT, and a maximum of 64 MB of dynamic video memory allocation.

The cPCI-3840 is equipped with the highly integrated, multi-functional Intel® 6300ESB I/O Controller Hub that provides the interface to the PCI bus, PCIX bus, and integrates miscellaneous I/O functions for legacy devices. The 855GMEand 6300ESB communicate over a dedicated hub interface (HI-1.5). The 6300ESB's functions and capabilities include an 8-Bit Hub Interface, a PCI-X bus which supports 64-bit/66MHz operations, a PCI Local Bus which supports 32-bit/33MHz operations, an integrated IDE controller which supports Ultra ATA100/66/33, integrated Serial ATA Host Controllers, two USB UHCI host interfaces with support for 4 USB ports, ACPI Power Management Logic Support, an enhanced DMA Controller, Interrupt Controller, Timer Functions, System Management Bus (SMBus) Specification v2.0 with support for I2C devices, Low Pin Count (LPC) interface, and a Watchdog Timer.

Please refer to the following block diagram for the cPCI-3840 architecture.

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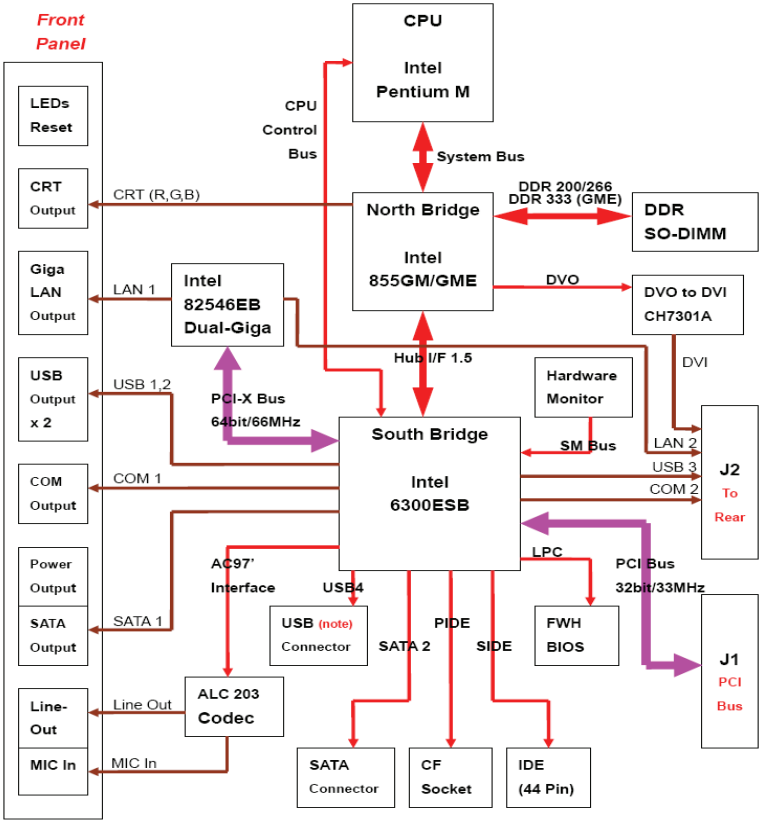


Figure 1-1: cPCI-3840 Architecture

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1.1 Features

The features of the cPCI-3840 are as follows:

- Designed for Micro-FCPGA478/ Micro-FCBGA479 Pentium-M 400MHz PSB processor with 1MB L2 cache
- Supports up to two double-sided 200-pin SODIMMs with up to a total of 2GB of RAM with unbuffered PC2100/PC2700 DDR-SDRAM with or without ECC (64-bit data interface with ECC SODIMM, 72-bit with ECC SODIMM)
- One VGA output supports resolution up to 1600 x 1200 at 85Hz and up to 2048 x 1536 at 75Hz.
- Digital display interface supports one port DVO with 165MHz output clock on each 12-bit interface.
- Hardware Monitoring for system voltages and CPU temperature.
- Supports analog display (RGB) and digital display (DVO).
- Up to 64MB of dynamic video memory allocation
- Supports Intel® Architecture with Dynamic Execution
- CPU temperature monitoring.

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1.2 Main Functions

The cPCI-3840 CPU Module is designed for the Intel® Pentium® M and Celeron® M Processors. The standard cPCI-3840 CPU Module comes with a CPU socket which can be installed with a Micro-FC-PGA package CPU, including the following options:

- Pentium® M 1.3GHz, 1.4GHz, 1.5GHz and 1.6GHz
- Celeron® M 1.3GHz

The Low Voltage (LV) or Ultra Low Voltage (ULV) versions of the Pentium® M or Celeron® M Processors in the Micro-FCBGA2 package can also be mounted on the cPCI-3840 CPU Module. However, Micro-FCBGA package support is reserved for OEM programs only. The possible CPU options include:

- LV Pentium® M 1.1, 1.2, 1.3GHz
- ULV Celeron® M 600MHz

CompactPCI Bus Interface

The Intel® 6300ESB south bridge chipset supports one PCI 33MHz / 32bits interface compliant with the PCI Local Bus Specification, Revision 2.2. The throughput of this PCI bus interface is 132 MB/s, and it supports 44 bit addressing using DAC protocol.

The 6300ESB also supports one PCIX 66MHz / 64-bits interface which is compliant with the PCIX Bus specification, revision 1.0 and is also compliant with the PCI Local Bus Specification, Revision 2.2. The throughput of this PCIX bus is up to 480 MB/s. It supports 64-bit addressing on PCI-X using DAC protocol.

IDE Interfaces

The cPCI-3840 supports dual Ultra ATA33/66/100 IDE channels. The primary IDE is implemented to CompactFlash (CF) interface and the secondary IDE is connected to a 40-pin slim-type IDE connector. The 6300ESB IDE controller supports both legacy mode and native mode IDE interfaces. In native mode, the IDE controller is a fully PCI compliant software interface and does not use any legacy I/O or interrupt resources. Note that for Ultra ATA100/66 mode operations, the proper cables must be installed.

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Gigabit Ethernet Ports

The cPCI-3840 has two 10/100/1000Mbps Ethernet (GbE) ports. Every port is assigned a unique static MAC Address. The BIOS menu can be setup to disable or enable these two LAN ports.

The onboard Intel® 82546EB Dual Port Gigabit Ethernet Controller provides two Ethernet ports. The 82546EB is implemented on the 64-bit/66-MHz PCI-X bus to achieve the full communication. The 82546EB supports IEEE 802.3x compliant flow control and IEEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation. One port is connected to the front panel and the other to rear panel via J2 (see Chapter 2, Jumpers and Connectors).

Universal Serial Bus (USB)

The cPCI-3840 employs one EHCI USB 2.0 Host Controller that compliments the UHCI interfaces on the south bridge for a total of five USB ports. Two USB ports are on the front panel, one is internal, and the remaining two are connected to the rear panel. Overcurrent detection on all USB ports is supported. USB legacy devices, such as keyboard, mouse and floppy drive are supported and can be enabled/disabled in BIOS options. In addition, USB devices boot feature is also implemented on all USB ports.

Serial I/O

The serial port consists of a UART which supports all functions of a standard 16550 UART, including hardware flow control interface. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the processor.

SATA

The 6300ESB I/O Controller Hub SATA controller features two sets of interface signals that may be independently enabled, tri-stated or driven low. Each interface is supported by an independent DMA controller. The controller interacts with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing

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the register interface and follows standard command protocol conventions.

Watchdog Timer

The cPCI-3840 implements a 2-stage Watchdog Timer (WDT) that is embedded on the 6300ESB and can be enabled/disabled in BIOS options. The WatchDog Timer supports selectable prescaler: approximately 1 MHz (1 us to 1 s) and approximately 1 KHz (1 ms to 10 min). The 2-stage WDT mode performs the following steps when the programmed time is up. First, it generates IRQ, SMI, or SCI interrupts. Second, it drives WDT_OUT# low and resets the cPCI-3840.

Hardware Monitoring

The onboard Winbond W83L784R Hardware Monitor tracks critical hardware parameters, including system and CPU voltages and system temperature. All hardware health status can be accessed in the BIOS options menu and using run-time utilities. In addition, once the preset thresholds of the hardware conditions are met, the W83L784R will alert the system or reset the entire system in critical situations. The The onboard Analog Devices ADM1032 is an ACPI compliant two-channel digital thermometer and under/over temperature alarm that allows the cPCI-3840 to be programmable for under/over temperature limits.

Operating System Support

The cPCI-3840 is compatible with Windows XP/2000/NT/Server 2003, and Linux Red Hat 9.0. The device drivers for Windows are included in the ADLINK All-in-One CD. For other Linux support and VxWorks BSP, please contact ADLINK.

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1.3 Specifications

Specifications of the cPCI-3840 CPU Module

CompactPCI Compliancy

- PCI Rev. 2.1 compliant
- PICMG 2.0 CompactPCI Rev. 3.0 Compliant
- PICMG 2.1 CompactPCI Hot Swap Specification R2.0 Compliant

Form Factor

- Standard 3U CompactPCI: 160 mm x 100 mm board size
- Dual Slot, 8TE/HP width

CPU/Cache

- Single Intel® Pentium® M 1.3/1.4/1.5/1.6 GHz or Celeron M 1.3 GHz Processors with Micro-FC-PGA package
- 1MB on die L2 cache, 400MHz FSB

Chipset

- Intel® 855GME Graphic Memory Controller Hub (GMCH)
- Intel® 6300ESB I/O Hub Controller

Host Memory

- Two SODIMM sockets, 2GB maximum
- Supports DDR266/333 SDRAM with ECC capability

BIOS

- Phoenix/Award Plug and Play BIOS with 4MB Flash ROM
- System BIOS flash, SST 49LF004A, in 4MB capacity, is compatible with Intel® 82802 Firmware Hub (FWH) device.
- BIOS write protection, provides anti-virus capability
- Bootable from USB storage devices including USB-Floppy, USB-ZIP, USB-CD-ROM, and USB-HDD.
- On-board Ethernet ports can be disabled using BIOS settings. BIOS write-protect function can be enabled/disabled in the BIOS options menu.

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CompactPCI Bus Controller

- Intel® 6300ESB PCI Bus Interface Controller
- PCI Local Bus Specification Revision 2.2 compaliant
- Support 32-bit/33MHz

Graphic

- Integrated in 855GME Graphics Memory Control Hub.
- Shared memory, up to 32MB
- Dual Channel Display
- Front Panel analog VGA DB-15 connector is available

Gigabit Ethernet

- Dual 10/100/1000bps Gigabit Ethernet ports provided by Intel® 82546EB Ethernet controller on local 66MHz/64-bit PCI-X bus; front panel and RTM rear access

Onboard Peripherals

- Integrated in Intel® 6300ESB south bridge
- Bus master IDE controller supports ultra ATA-100 interface
- Primary IDE on SBC with 44-pin IDE connector. A 2.5” IDE HDD can be mounted
- All USB ports are USB Spec Rev. 2.0 compliant
- USB 1, 2 are on the front panel
- USB 3 is on the RTM Panel
- USB ports support 0.5A@5V for peripherals with individual over-current protection
- Supports DB-9 COM1 Serial Port on the front panel and DB-9 COM2 on the RTM
- Supports one RJ-45 GbE port on the front panel and one RJ-45 GbE port on RTM
- Supports one SATA port and external power connector on the front panel
- Speaker out and MIC IN ports provided on the front panel

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Front Panel LED Indicators and Reset

- 4 LEDs on the front panel including storage access LED (red), Power LED (green), General Purpose Status (Blue), and Watchdog timer LED (Yellow)
- Flush tact switch for system reset

Real -Time Clock and Nonvolatile Memory

- Built-in Intel® 6300ESB south bridge RTC
- Battery-backed memory used for BIOS configurationm
- Separate 3V coin cell CR2032 battery used for RTC and nonvolatile memory

Environment

- Operating ambient temperature: -5 to 55 °C
- Storage temperature: -20 to 80 °C
- Humidity: 5% to 95% non-condensed
- Shock: 15G peak-to-peak, 11ms duration, non-operation
- Vibration:
  - Non-operation: 1.88Grms, 5-500Hz, each axis
  - Operation: 0.5Grms, 5-500Hz, each axis, with 2.5” HDD

Safety Certificate and Test

- CE, FCC Class B
- All plastic material, PCB and batteries used are UL-94V0 certified
- Designed for NEBS 3.0 requirements

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Power Requirements

Full Loading	+5V	+3.3V	Total Power
Pentium® M 1.6GHz CPU, 512MB x 2 DDR, 40G HD	3.16A	2.39A	23.6878 W
Pentium® M 1.1GHz CPU, 512MB x 2 DDR, 40G HD	1.875A	1.746A	15.1368 W
Celeron M 1.3GHz CPU, 512MB x 2 DDR, 40G HD	2.44A	1.683A	17.7539 W
Dothan 1.8GHz CPU, 512MB x 2 DDR, 40G HD	3.334A	1.524A	21.6992 W

Table 1-1: Mean Power Consumption

cPCI-R3840 RTM Specifications

The cPCI-R3840 is a rear transition module designed for the cPCI-3840. It comes with one LAN port, one USB port, one DVI connector, and one DB-9 serial port.

Form Factor

- Standard 3U CompactPCI rear I/O
- 2 Slot (8TE/HP, 40.64 mm) wide

Faceplate I/O Connectors

- One GbE ports on RJ-45 connector
- One DVI connector
- One COM2 port on DB-9 connector
- One USB port

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I/O Connectivity Table

I/O	cPCI-3840		cPCI-R3840	
	Face-plate	On-board	Face-plate\	On-board
Serial Port (COM1)	DB-9	--	--	--
Serial Port (COM2)	--	--	DB-9	--
USB (port 1, port 2)	Y	--	--	--
USB (port 3)	--	--	Y	--
Gigabit Ethernet Port 1	RJ-45	--	RJ-45	--
Gigabit Ethernet Port 2	--	--	--	--
IDE	--	44-pin	--	--
General Purpose LED	Y	--	--	--
Reset button	Y	--	--	--
Speaker Out	Y	--	--	--
MIC In	Y	--	--	--
VGA	Y	--	--	--
SATA	Y	Y	--	--
SATA Power Connector	Y	--	--	--
CF Socket	--	Y	--	--
DVI	--	--	Y	--

Table 1-2: I/O Connectivity

1.4 Unpacking Checklist

Before opening the product box, please check the shipping carton for any damages. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing material for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check the following items are included in the package, if there are any missing items, contact your dealer:

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CPU Module:

- The cPCI-3840 CPU Module (CPU, RAM, and HDD specifications will differ depending on options selected)
- Heat sink kit (incl. thermal pad and heat sink paste)
- HDD bracket
- SATA Cable and SATA power cable
- 44-pin IDE cable
- ADLINK All-in-One CD
- This user's manual

RTM:

- cPCI-R3840 RTM

Note: The packing contents of cPCI-3840 OEM non-standard configurations may vary and is dependent on customer requests.



: This board must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a wrist strap grounded through one of the system's ESD Ground jacks when servicing system components.

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2 Jumpers and Connectors

This chapter illustrates the board layout, connector pin assignments, and jumper setup. Users should familiarize themselves with the products before use. The following sections are included:

- cPCI-3840 board outline
- cPCI-3840 connectors pin assignments
- cPCI-3840 jumpers setting
- cPCI-R3840 RTM board outline
- cPCI-R3840 RTM connectors pin assignments

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2.1 cPCI-3840 Board Outline

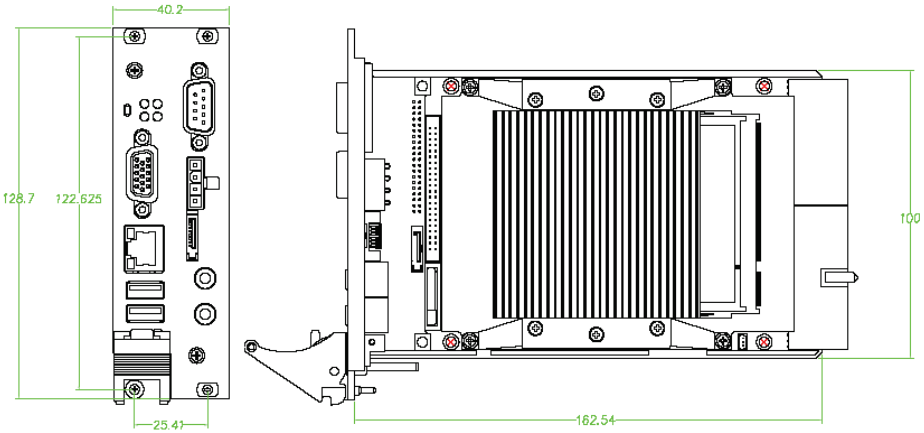


Figure 2-1: cPCI-3840 Front View and Top View

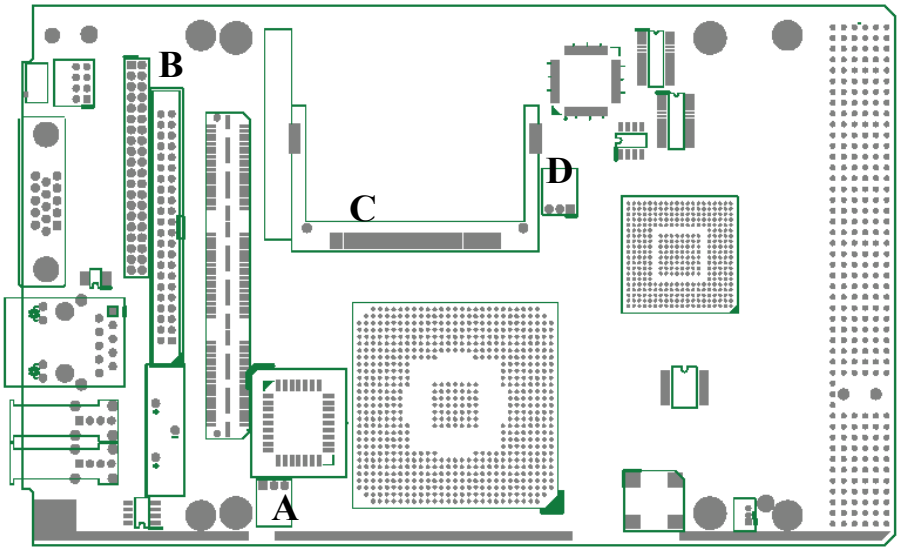


Figure 2-2: cPCI-3840 Carrier Board Top View

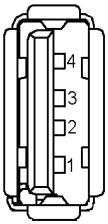
A	Clear CMOS jumper (JP2)	C	CF connector (IDE0)
B	Slim-type IDE (IDE1)	D	CF master/slave (CN5)

Table 2-1: Jumper and Connector Locations

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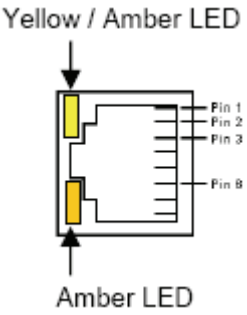
2.2 cPCI-3840 Connector Pin Assignments

USB Connectors



PIN	SIGNAL
1	VCC
2	USB-
3	USB+
4	Ground

Ethernet (RJ-45) Connector



Pin #	Signal Name	Function
1	LAN_TDP1	Transmit Data1 +
2	LAN_TDN1	Transmit Data1 -
3	LAN_RDP2	Receive Data2 +
4	LAN_RDP3	Receive Data3 +
5	LAN_RDN3	Receive Data3 -
6	LAN_RDN2	Receive Data2 +
7	LAN_TDP4	Transmit Data4 +
8	LAN_TDN4	Transmit Data4 -

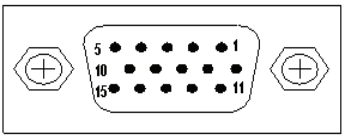
Status		Left LED (Amber)	Right LED (Yellow or Amber)
Network link is not established		OFF	OFF
10 Mbps (10 BaseT)	Link	Amber	OFF
	Active	Blinking Amber	OFF
100 Mbps (100 BaseTX)	Link	Amber	Yellow
	Active	Blinking Amber	Yellow

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1000 Mbps (1000 BaseT)	Link	Amber	Amber
	Active	Blinking Amber	Amber

Table 2-2: Ethernet LED Status

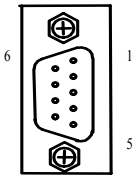
VGA Connector



Signal Name	Pin	Pin	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V	9	10	GND
N.C.	11	12	DDCDAT
HSYNC	13	14	VSYNC
DDCCLK	15		

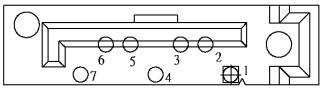
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RS-232 DB-9 Serial Port Connector (COM1)



Pin #	RS-232
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	IsoGND, Isolated ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator

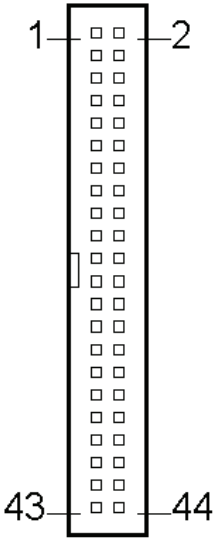
SATA Connector



Pin	Signal	Pin	Signal
1	GND	5	RXN
2	TXP	6	RXP
3	TXN	7	GND
4	GND		

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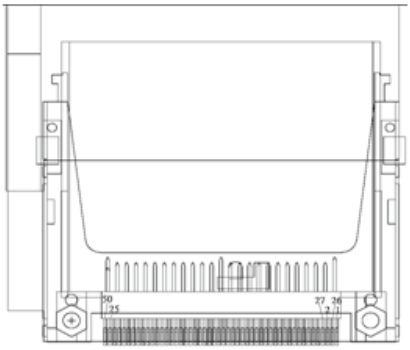
IDE Connector



Signal Name	Pin	Pin	Signal Name
BRSTDRVJ	1	2	GND
DDP7	3	4	DDP8
DDP6	5	6	DDP9
DDP5	7	8	DDP10
DDP4	9	10	DDP11
DDP3	11	12	DDP12
DDP2	13	14	DDP13
DDP1	15	16	DDP14
DDP0	17	18	DDP15
GND	19	20	NC
PDDREQ	21	22	GND
PDIOWJ	23	24	GND
PDIORJ	25	26	GND
PIORDY	27	28	PCSEL
PDDACKJ	29	30	GND
IRQ14	31	32	NC
DAP1	33	34	DIAG
DAP0	35	36	DAP2
CS1P	37	38	CS3PJ
IDEACTPJ	39	40	GND
+5V	41	42	+5V
GND	43	44	NC

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CompactFlash Connector



Pin	Signal	Pin	Signal	Pin	Signal
1	GND	18	DA2	35	SDIOWJ
2	DD3	19	DA1	36	5V
3	DD4	20	DA0	37	IRQ15
4	DD5	21	DD0	38	5V
5	DD6	22	DD1	39	PCSEL
6	DD7	23	DD2	40	NC
7	CS1J	24	IOIS16J	41	BRSTDRVJ
8	GND	25	GND	42	SDIORDY
9	GND	26	GND	43	NC
10	GND	27	DD11	44	SDACKJ
11	GND	28	DD12	45	IDEACTJ
12	GND	29	DD13	46	DIAG
13	5V	30	DD14	47	DD8
14	GND	31	DD15	48	DD9
15	GND	32	CS3J	49	DD10
16	GND	33	GND	50	GND
17	GND	34	SDIORJ		

General Purpose LED Definitions

LED	Color	Status	Description
IDE Media Access	Red	OFF	IDE idle
		ON	IDE access
Power OK	Green	OFF	System is not power-on or power failed
		ON	Power ON
Hot-swap status	Blue	OFF	Board inserted and power on OK.
		ON	Board inserted but not power on yet.
WDT LED	Yellow	OFF	WDT is not enabled
		Blinking	WDT is enabled

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CompactPCI J2 Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	GA4(2)	GA3(2)	GA2(2)	GA1(2)	GA0(2)	GND
21	GND	CLK6	GND	BRSV(1)	BRSV(1)	BRSV(1)	GND
20	GND	CLK5	GND	BRSV(1)	GND	BRSV(1)	GND
19	GND	GND	GND	ICMBSDA(1)	ICMBSCL(1)	ICMBALR(1)	GND
18	GND	BRSV(1)	BRSV(1)	BRSV(1)	GND	BRSV(1)	GND
17	GND	BRSV(1)	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSV(1)	BRSV(1)	DEG#	GND	BRSV(1)	GND
15	GND	BRSV(1)	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD [35]	AD [34]	AD [33]	GND	AD [32]	GND
13	GND	AD [38]	GND	V (I/O)(1)	AD [37]	AD [36]	GND
12	GND	AD [42]	AD [41]	AD [40]	GND	AD [39]	GND
11	GND	AD [45]	GND	V (I/O)(1)	AD [44]	AD [43]	GND
10	GND	AD [49]	AD [48]	AD [47]	GND	AD [46]	GND
9	GND	AD [52]	GND	V (I/O)(1)	AD [51]	AD [50]	GND
8	GND	AD [56]	AD [55]	AD [54]	GND	AD [53]	GND
7	GND	AD [59]	GND	V (I/O)(1)	AD [58]	AD [57]	GND
6	GND	AD [63]	AD [62]	AD [61]	GND	AD [60]	GND
5	GND	C/BE [5]#	GND	V (I/O)(1)	C/BE [4]#	PAR 64	GND
4	GND	V (I/O)(1)	BRSV(1)	C/BE [7]#	GND	C/BE [6]#	GND
3	GND	CLK4	GND	GNT3#	REQ#4	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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CompactPCI J3 Pin Assignment

Pin	Z	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND	GND
18	GND	LPA_DA+	LPA_DA-	GND	LPA_DC+	LPA_DC-	GND
17	GND	LPA_DB+	LPA_DB-	GND	LPA_DD+	LPA_DD-	GND
16	GND	LPB_DA+	LPB_DA-	GND	LPB_DC+	LPB_DC-	GND
15	GND	LPB_DB+	LPB_DB-	GND	LPB_DD+	LPB_DD-	GND
14	GND	GND	GND	2.5V	GND	GND	GND
13	GND	LANA_1G#	LANA_100#	ACTA#	LINKA#	LANB_1G#	GND
12	GND	LINKB#	LANB_100#	ACTB#	5V(1)	5V(1)	GND
11	GND	IYAM0	IYAM1	IYAM2	IYAM3	ICLKAM	GND
10	GND	IYAP0	IYAP1	IYAP2	IYAP3	ICLKAP	GND
9	GND	IYBM0	IYBM1	IYBM2	IYBM3	ICLKBM	GND
8	GND	IYBP0	IYBP1	IYBP2	IYBP3	ICLKBP	GND
7	GND	CTS#	DSR#	RTS#	DTR#	NC	GND
6	GND	HSYNC	VSYNC	SIN	SOUT	DCD#	GND
5	GND	RED	GREEN	BLUE	DDCDATA	DDCCLK	GND
4	GND	TMDS1_TX1N	TMDS1_TX2N	TMDS1_TX3N	TMDS1_TXCN	TMDS_I2CC	GND
3	GND	TMDS1_TX1P	TMDS1_TX2P	TMDS1_TX3P	TMDS1_TXCP	TMDS_I2CD	GND
2	GND	LVDS_VDDEN	LVDS_TEN	LVDS_TCTL	NC	HTPLG	GND
1	GND	KBCLK	KBDATA	MSCLK	MSDATA	3.3V(1)	GND

2.3 Switch and Jumper Setting

The following table lists the switch and jumpers on the cPCI-3840.

Switch	Function
SW1	Reset
CN5	CF Master/Slave
JP2	Clear CMOS Content

Table 2-3: Switches and Jumpers

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Reset Button (SW1)

SW1 is a push-button on the front panel. Pressing SW1 generates a hard reset.

CF Master/Slave Setting (CN5)

CN5 is 3-pin jumper that can select CF device to be IDE master/slave (see Figure 1b above for its location on the carrier board).

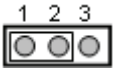
Status	CN5
Slave (Default)	
Master	

Table 2-4: CN5 CF Master/Slave Setting

Clear CMOS (JP2)

JP2 is 3-pin jumper that can be used to clear the CMOS memory (see Figure above for its location on the carrier board). The CMOS RAM stores the real time clock (RTC) information, BIOS configuration, and default BIOS setting. The CMOS is powered by the button cell battery when the system is powered off.

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Please follow the following steps to erase the CMOS RAM data:

1. Remove the cPCI-3840 CPU Module from chassis.
2. Short pins 2 and 3 of JP2, then reinstall the jumper to normal location.
3. Insert the CPU Module back into the chassis.

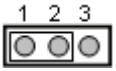
Status	JP2
Normal operation (Default)	
Clear CMOS	

Table 2-5: JP2 Clear CMOS

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2.4 cPCI-R3840 RTM Board Outline

The cPCI-R3840 is a rear transition module designed for the cPCI-3840. It comes with one LAN port, one USB port, one DVI connector, and one DB-9 serial port.

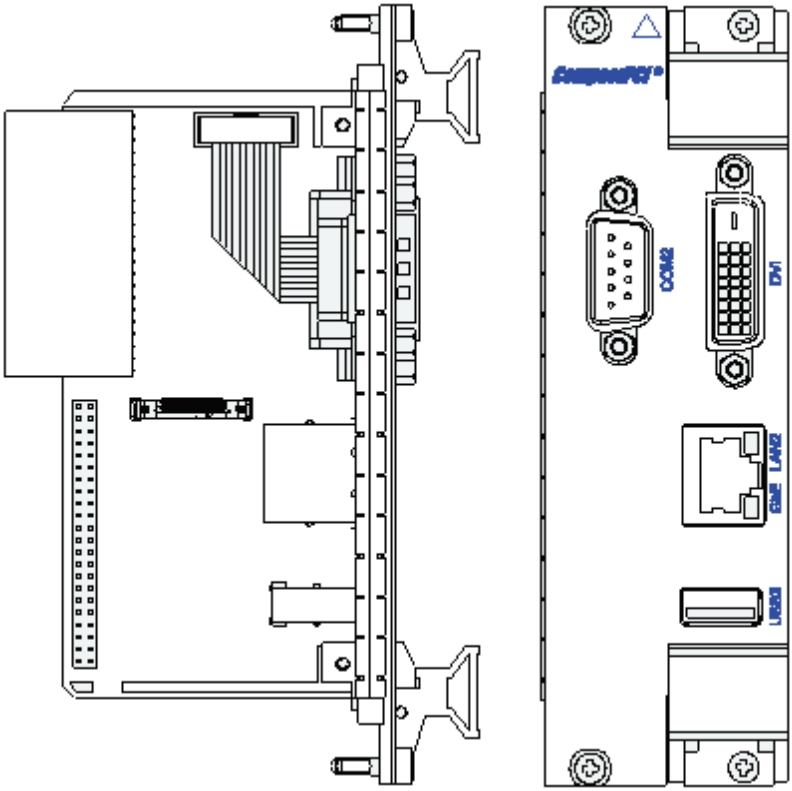


Figure 2-3: cPCI-R3840 Front View and Top View

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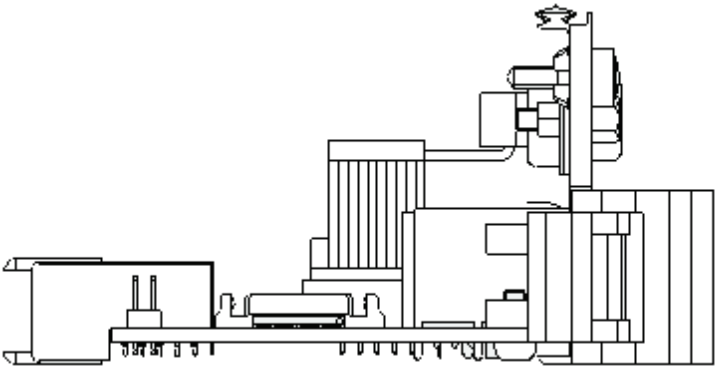


Figure 2-4: Side View of cPCI-R3840

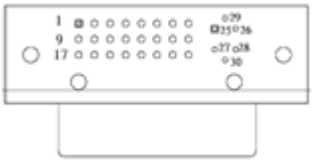
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2.5 cPCI-R3840 RTM Connector Pin Assignments

The connector pin assignments of the cPCI-R3840 Rear Transition Module's RJ-45 GbE port, USB port, and DB-9 serial port COM2 are identical to those of the cPCI-3840 CPU Module. Please refer to Section 2.2.

The pin assignments for the DVI connector and RJ2 connector are as follows:

DVI Connector



Pin	Signal	Pin	Signal
1	TX2-	16	HTPLG
2	TX2+	17	TX0-
3	GND	18	TX0+
4	NC	19	GND
5	NC	20	NC
6	I2CCLK	21	NC
7	I2CDATA	22	GND
8	VSYNC	23	TXC+
9	TX1-	24	TXC-
10	TX1+	25	RED
11	GND	26	GREEN
12	NC	27	BLUE
13	NC	28	HSYNC
14	+5V	29	GND
15	GND	30	GND

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cPCI-R3840 RJ2 Pin Assignment

Pin	A	B	C	D	E	F
RJ2-22	GA4	GA3	GA2	GA1	GA0	GND
RJ2-21	CLK6	GND	ICLKAP	1000LEDJ	IYAP3	GND
RJ2-20	CLK5	GND	ICLKAM	GND	IYAM3	GND
RJ2-19	GND	GND	SMBDATA	SMBCLK	SMBALERT	GND
RJ2-18	IYAP1	IYAP2	IYAM2	GND	100LEDJ	GND
RJ2-17	IYAM1	GND	PRST#	REQ6#	GNT6#	GND
RJ2-16	IYAP0	ACLEDJ	DEG#	GND	LILEDJ	GND
RJ2-15	IYAM0	GND	FAL#	REQ5#	GNT5#	GND
RJ2-14	COM2_RIJ	COM2_TXD	COM2_DTRJ	GND	GL_MDIB2-	GND
RJ2-13	COM2_RXD2	GND	VIO	GL_MDIB3-	GL_MDIB2+	GND
RJ2-12	COM2_CTSJ	COM2_DCDJ	COM2_DSRJ	GND	GL_MDIB3+	GND
RJ2-11	COM2_RTSJ	GND	VIO	GL_MDIB0+	GL_MDIB0-	GND
RJ2-10	TMDS_TXCP	TMDS_TXCN	RESERVE	GND	GL_MDIB1+	GND
RJ2-9	TMDS_HPDET	GND	VIO	NC	GL_MDIB1-	GND
RJ2-8	TMDS_TX3P	TMDS_TX3N	PANEL_I2CD	GND	USB_OCJ3	GND
RJ2-7	PANEL_I2CC	GND	VIO	USBP3+	USBP3-	GND
RJ2-6	TMDS_TX2N	TMDS_TX1P	TMDS_TX1N	GND	R_GB_+2.5V	GND
RJ2-5	TMDS_TX2P	GND	VIO	NC	PAR64	GND
RJ2-4	VIO	BRSV	R_+3.3V	GND	R_+5V	GND
RJ2-3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
RJ2-2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
RJ2-1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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3 Getting Started

This chapter provides information on how to install necessary components for the cPCI-3840 and cPCI-R3840 RTM, including:

- CPU installation
- Memory module installation
- CF installation
- CPU Core Module removal and installation
- Heat sink and 2.5” HDD installation
- cPCI-3840 CPU Module installation
- cPCI-3840 RTM installation

Depending on the options selected for your cPCI-3840, installation of the CPU, RAM, heat sink, and HDD may or may not be required. Please skip over any unnecessary steps.

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3.1 Installing the CPU

The cPCI-3840 supports the Intel® Pentium® M and Celeron® M processors. The CPU socket is located in the middle of the CPU Core Module as shown in Figure 4 below.

Remove the CPU from its packaging and place it carefully in the CPU socket as shown in Figure 4 below. Be sure to align the gold triangle on the corner of the chip with the corner of the socket that is missing a pin. Press down gently on the chip to ensure that it is securely in place, and then use a small flathead screwdriver to lock the CPU into position.

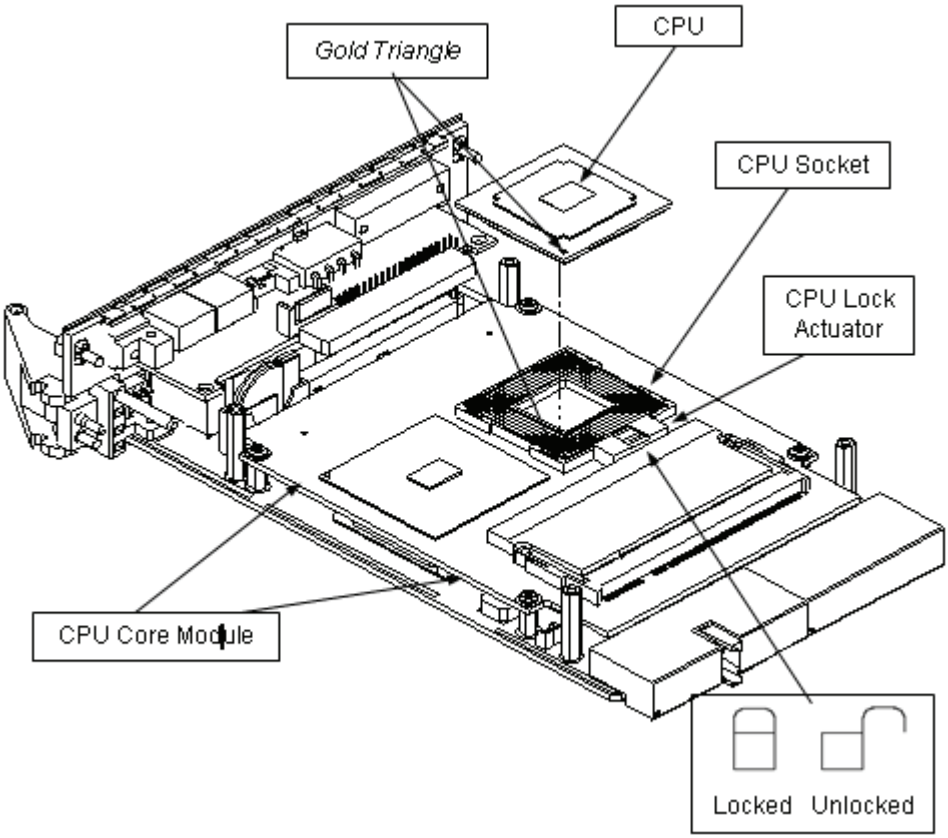


Figure 3-1: CPU Installation.

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3.2 Memory Module Installation

The cPCI-3840 CPU Module supports 144-bit wide PC2100/ PC2700 registered/unregistered ECC DDR DIMM up to 2GB maximum. Two memory sockets are located on the CPU Core Module (one on each side). If memory modules are pre-installed when the package is received, this section may be skipped.

Installing the First Memory Module

Please refer to the figure below to install the first memory module. Insert the module at a 30 degree angle and push the module firmly but gently into the slot until the security latches on the sockets have locked into place on each side of the module. (Note: There is a middle alignment key on 144 pin memory module which should help users with installation.)

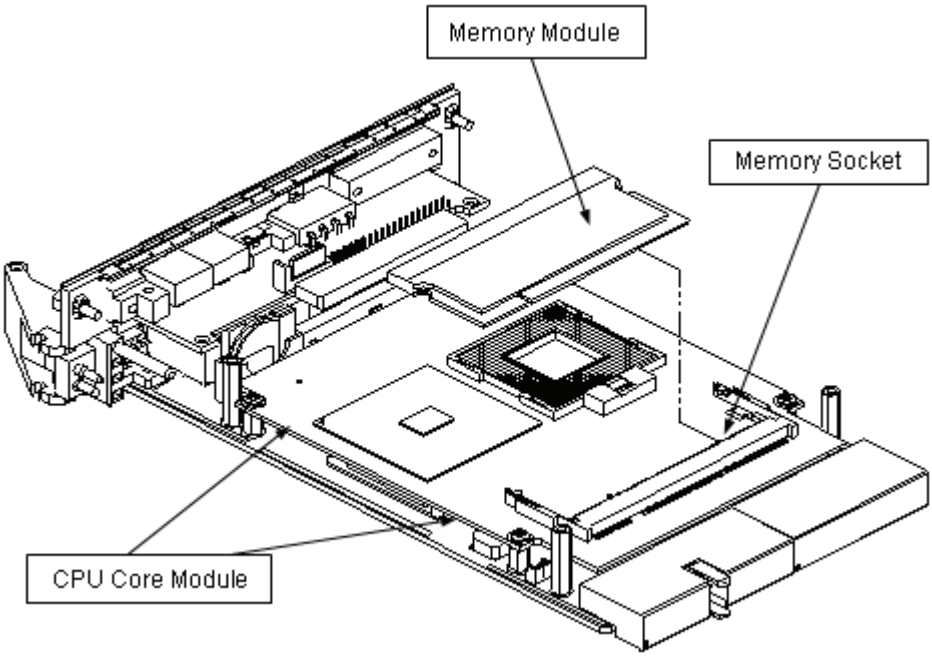


Figure 3-2: Memory Module Installation, Pt 1.

Note: Second memory socket is on underside of CPU Core Module – see below.

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Removing the CPU Core Module

The second memory socket is located on the underside of the CPU Core Module. If installation of a second memory socket is necessary, first remove the CPU Core Module by loosening the 4 screws that attach it to the carrier board. Then carefully lift it upwards by grasping it with thumb and forefinger at the points marked **GRIP HERE** shown in Figure 5b. This will prevent damage to the connector attaching the CPU Core Module to the carrier board.

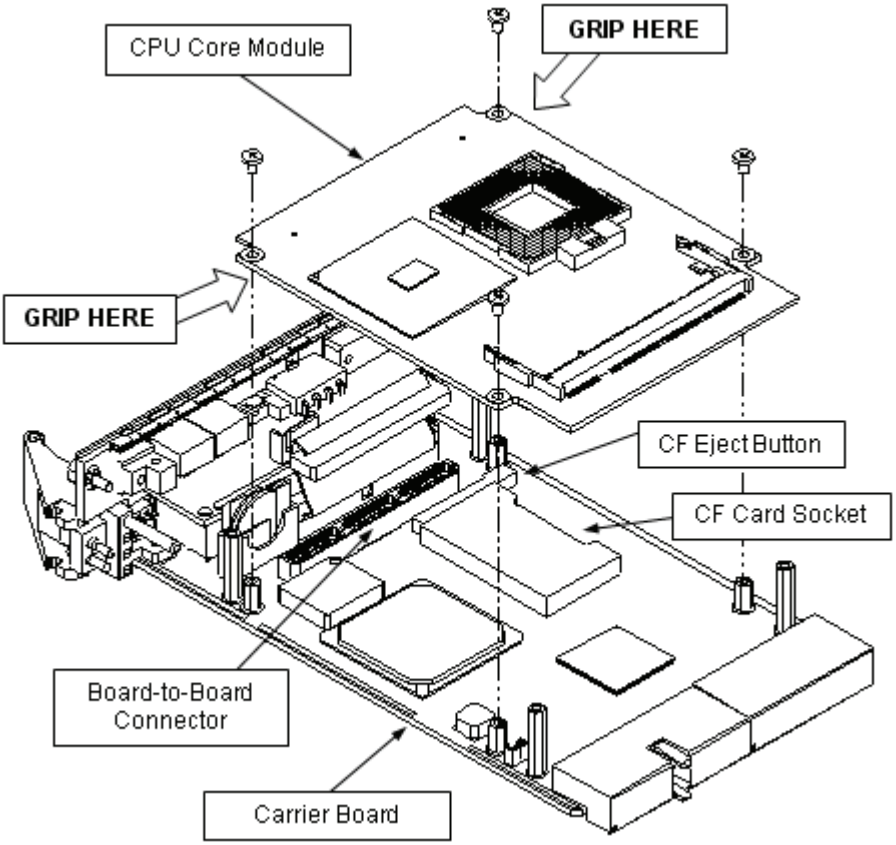


Figure 3-3: CPU Core Module Removal.

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Installing the Second Memory Module

Insert the second memory module into the slot shown in the figure below using the same procedure as described above for installation of the first memory module.

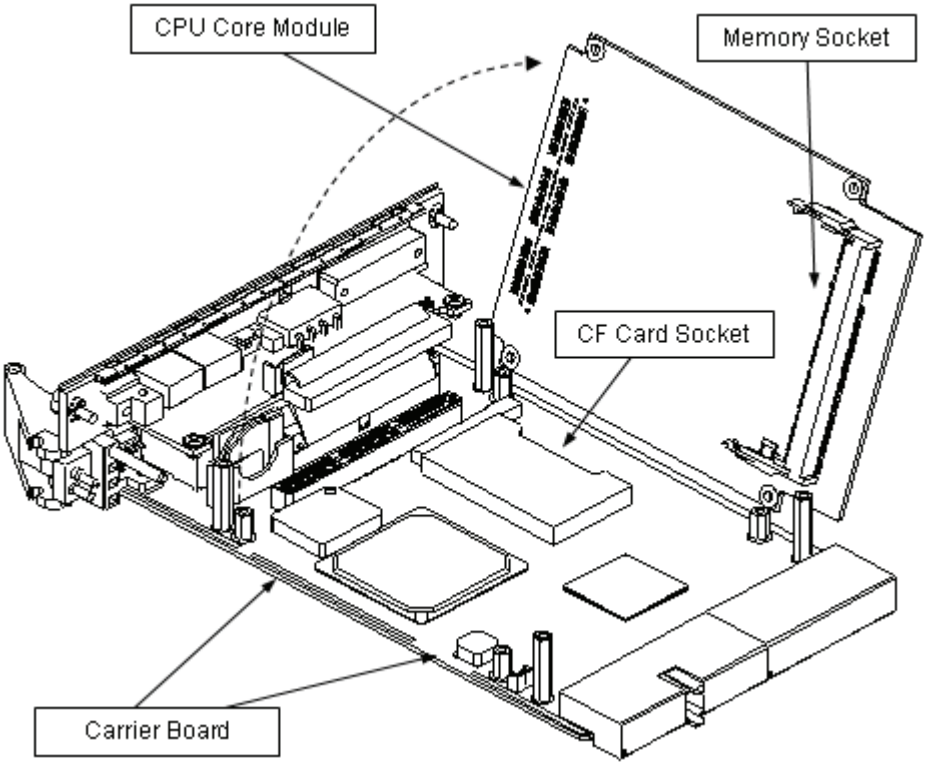


Figure 3-4: Memory Module Installation, Pt. 2.

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3.3 CF Card Installation

The CF card slot is located on the carrier board of the cPCI-3840. The CF card can be inserted and ejected with the CPU Core Module in place. However, if you are installing a second memory module, it is easier to install the CF card when the CPU Core Module has been removed.

3.4 CPU Core Module Installation

If you have removed the CPU Core Module to install a second memory module, you must reattach it to the carrier board. Align the 4 screw holes as shown in the figure above so that the board-to-board connector sockets of the CPU Core Module and carrier board meet properly. Then gently press down on the CPU Core Module at the points marked GRIP HERE shown in Figure 5b until it is firmly seated on the carrier board. Do not replace the screws until after you have installed the heat sink as described in Section 3.5 below.

3.5 Heat Sink Installation

In order to properly dissipate heat from the CPU, a heat sink is provided and must be installed before using the cPCI-3840 CPU Module. First, remove the transparent Mylar film from the white side of the thermal pad provided, and apply to the CPU as shown in the figure below. Then remove the Mylar film from the pink side of the thermal pad. (If you haven't removed the screws attaching the CPU Core Module to the carrier board, do so now – Section 3.2, Figure 5b.)

Next, remove the Mylar film from the raised block on the underside of the heat sink, being careful to leave the gray thermal pad in place. Place the heat sink over the CPU Core Module, being sure to align it so that the raised block is over the 855GME north bridge. Note that the cut-outs on the cooling fins are facing the front panel of the cPCI-3840 CPU Module. Attach the screws as shown.

Reserve the Heat Sink Paste for future use if the thermal pads should deteriorate after repeated removal and reinstallation of the heat sink.

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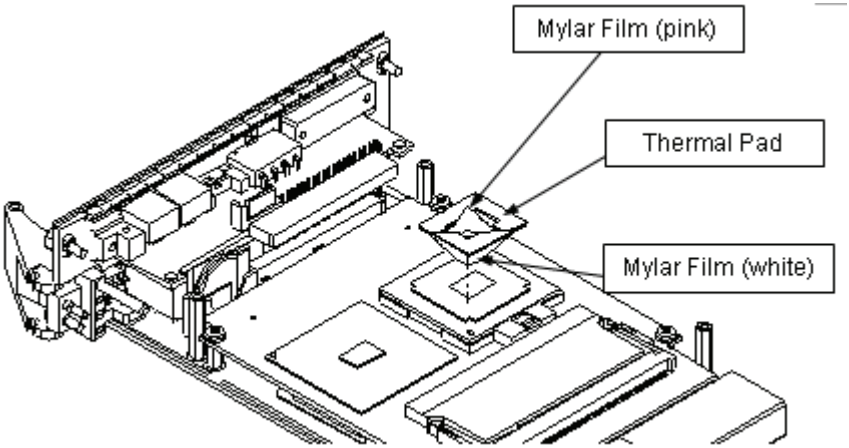


Figure 3-5: Thermal Pad

Apply the thermal pad to the CPU (white side down) and remove the Mylar film from the top (pink) side of the thermal pad.

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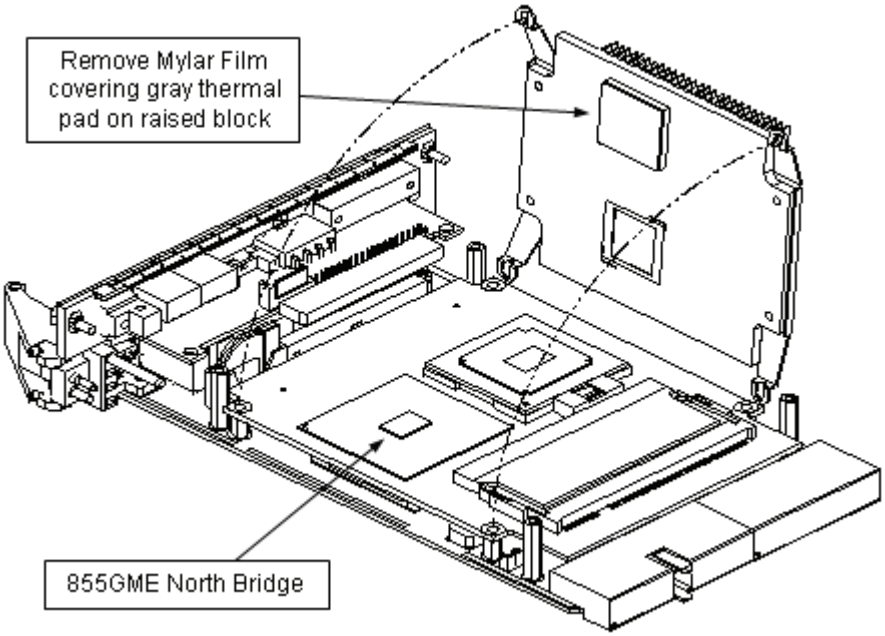


Figure 3-6: Heat Sink Fitting

Remove the Mylar Film covering the gray thermal pad on raised block. (Note orientation of heat sink to 855GME North Bridge.)

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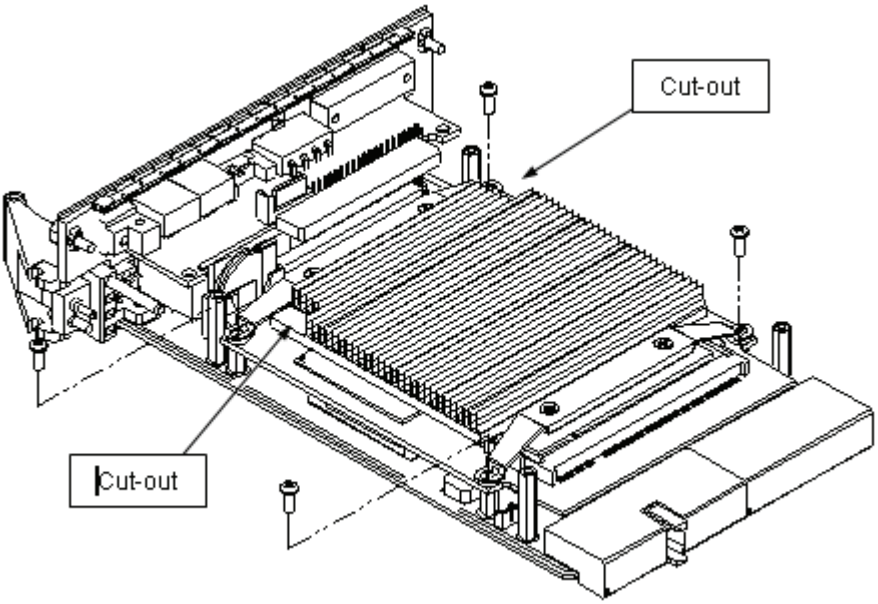


Figure 3-7: Heat Sink Screws

Remove the Mylar Film covering the gray thermal pad on raised block. (Note orientation of heat sink to 855GME North Bridge.)

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3.6 2.5” HDD Installation

To install a 2.5” hard drive, it is first necessary to install the mounting brackets. Follow the figure below for the installation procedure.

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Then attach the IDE connector.

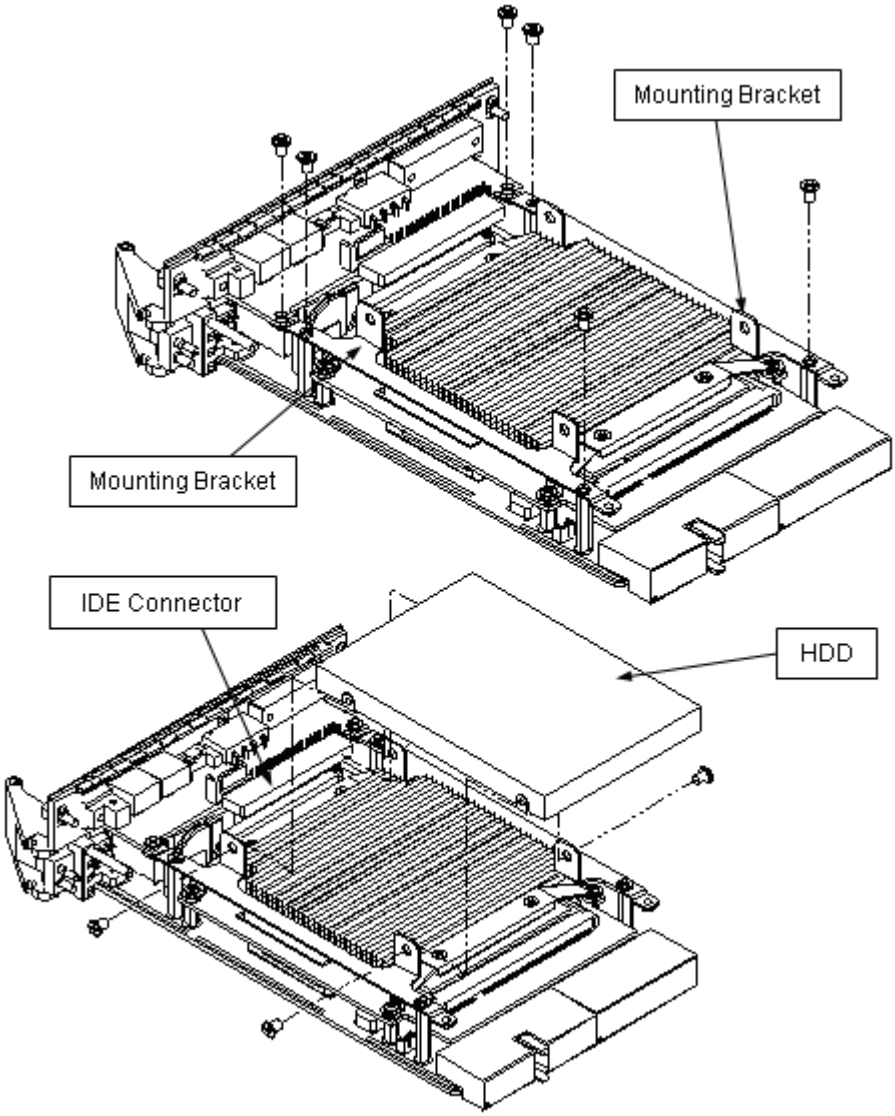


Figure 3-8: HDD and Mounting Bracket Installation

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3.7 cPCI-3840 CPU Module Installation

Use the following procedure to install the cPCI-3840 CPU Module to its CompactPCI chassis.

1. Refer to the relevant chassis user manual for pre-preparation of the chassis before installing the main board. Users need to assign a slot to the board. Be sure to select the correct slot (system or peripheral) depending on the operational purpose of the board. Turn off system power at both front and rear of the chassis.
2. Remove the blank face panel from the slot.
3. Align the top and bottom edges of the board with the card guides on the chassis then slide the board into the chassis until resistance is felt.
4. Move the locking handle in an inward direction until it is fully latched. Note that slight resistance will be felt while inserting the board. If this resistance is more than under normal conditions, check to ensure that there are no bent pins on the backplane and that the board's connector pins are aligned properly with the connectors on the backplane.
5. Verify that the board is seated properly. Secure the two screws hidden behind the upper and lower ejector; connect the proper cables to the board. The system can now be powered on.

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3.8 RTM Installation

The installation and removal procedures for a RTM are the same as those for CompactPCI boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-3840 series and related RTMs, make sure the RTM is the correct matching model.

Note: Use the correct RTM to enable functions (I/O interfaces) on rear side. The RTM or system board can be damaged if the incorrect RTM is used.

Some I/O ports are supported on both the front board and the RTM, including Keyboard, Mouse, VGA and USB. These I/O ports can be connected either via the front or rear modules but DO NOT access these ports on both front and rear simultaneously.

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4 Windows Driver Installation

The following sections show the driver installation procedures for Windows 2000, Windows XP and Windows Server 2003. When installing the Windows drivers, we recommend the following steps:

1. Fully install Windows properly before installing any driver. Most of the standard I/O device drivers are included in Windows.
2. Install the chipset driver.
3. Install the graphics driver and utilities.
4. Install the LAN drivers.

It is recommended that the chipset, graphics, and LAN drivers provided on the ADLINK All-in-One CD be used to ensure compatibility. Please contact ADLINK for support for Linux drivers and VxWorks BSP.

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4.1 Chipset Drivers Installation

1. Ensure Windows 2000/XP/Server 2003 is fully installed and running prior to executing the “Intel Chipset Software Installation Utility”.
2. Close any running applications.
3. The files are stored in an integrated application setup program. This program is designed for Windows 2000, XP and Server 2003.
4. Locate the directory X:\cPCI\cPCI-3840\Chipset in the CD-ROM, and then run Intel-Inf-v5111002.exe.
5. Click 'Next' on the Welcome screen to read and agree to the license agreement. Click Yes if you agree to continue. NOTE: If you click No, the program will terminate.
6. Click ‘Next’ on the Readme Information screen to install INF files.
7. Click 'Finish' to restart the system when prompted to do so.
8. Follow the screen instructions and use the default settings to complete setup when Windows 2000/XP/Server 2003 re-starts. Upon re-start, Windows may display that it has found new hardware and is installing drivers for them. Select Yes, if prompted to re-start Windows 2000/XP/Server 2003.

4.2 VGA Driver Installation

1. Run win2k_xp142.exe located in the following directory: X:\cPCI\cPCI-3840\VGA.
2. Click ‘Next’ on the Welcome screen. Select ‘Typical’ on the setup type screen and click Next’.
3. Use the default program folders on Select Program Folder screen. Click ‘Next’ to install driver.
4. Finally, click 'Finish' to restart.

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4.3 LAN Driver Installation

This section describes the LAN driver installation for the Intel® 82546EB onboard Ethernet controllers.

1. Run pro2kxp.exe located in the following directory: X:\cPCI\cPCI-3840\LAN.
2. Read the license agreement. Click 'I accept the terms in the license agreement' if you agree to continue.
3. Location to Save Files, click Next to save files in folder.
4. Intel® PRO Network Connections. Click Install Software to install drivers and Intel® PROSet.

4.4 Audio Codec Driver Installation

This section describes the LAN driver installation for the Intel® 82546EB onboard Ethernet controllers.

1. The driver is included in the driver CD. Run wdm_a357.exe located in the following directory: X:\cPCI\cPCI-3840\Audio.
2. Click 'Next' on the Welcome audio setup screen to install driver..
3. Finally, click 'Finish' to re-start.

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5 Utilities

5.1 Watchdog Timer

This section explains the operation of the cPCI-3840's watchdog timer. It provides an overview of watchdog operation and features, as well as a sample code to help you learn how the watchdog timer works.

WDT Overview

The primary function of the watchdog timer is to monitor the cPCI-3840's operation and to generate IRQs or reset the system if the software fails to function as programmed. The major features of the watchdog timer are:

- Enabled and disabled through software control
- Armed and strobed through software control

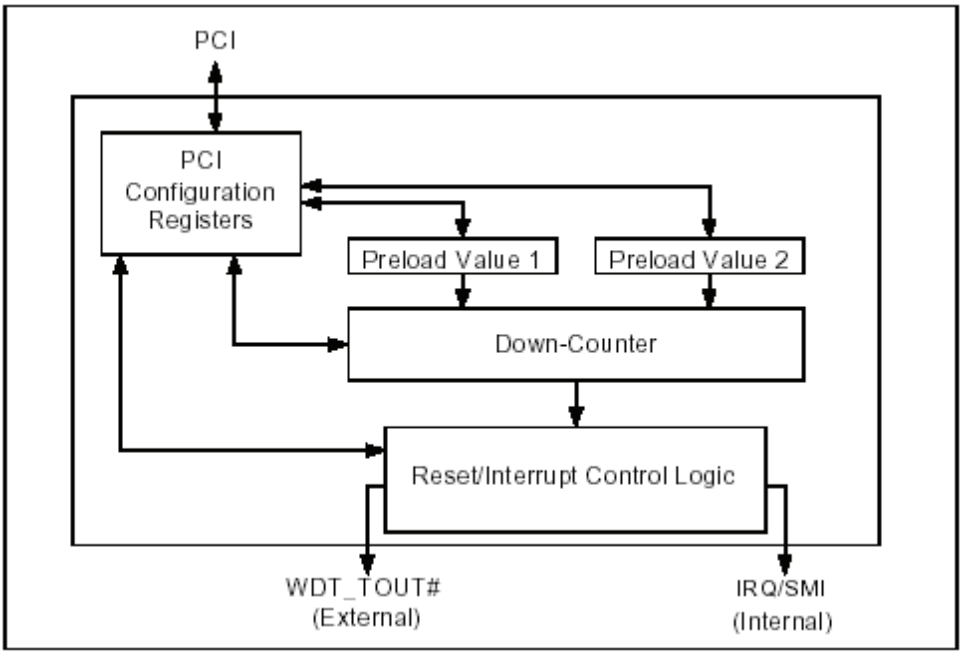


Figure 5-1: WDT Overview

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The cPCI-3840's custom watchdog timer circuit is integrated into the south bridge 6300ESB.

The Intel® 6300ESB ICH includes a two-stage Watchdog Timer (WDT) that provides a resolution ranging from one micro second to ten minutes. The timer uses a 35-bit Down-Counter. The counter is loaded with the value from the first Preload register. The timer is then enabled and it starts counting down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low. The WDT_TOUT# pin is held low until the system is reset.

The WDT of 6300ESB also supports multiple modes: WDT and free-running. Free-running mode is a one stage timer and it will toggle WDT_TOUT# after programmable time. WDT mode is a two stage timer and its operation is described as above.

Configuration Registers

The Intel® 6300ESB ICH WDT, appears to BIOS as PCI Bus 0, Device 29, Function 4, and has the standard set of PCI Configuration register. The configuration registers is described below.

Offset 10H: Base Address Register (BAR)

This register determines the memory base for WDT down-counter setting. It will be used to set Preload value 1 register, Preload value 2 register, General Interrupt Status register and Reload register.

Preload Value 1 & 2 registers

These two registers are used to hold the preload value for the WDT timer. Its value will be automatically transferred into the down-counter every time the WDT enters the first stage and second stage. Preload Value 1 register locates at Base + 00H and Preload Value 2 register locates at Base + 04H. Only bit [19:0] are settable.

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The register unlocking sequence is necessary when writing to the Preload registers. The following is the procedure of how to write a value into preload value 1 and 2 register.

1. Write 80H to offset BAR + 0CH.
2. Write 86H to offset BAR + 0CH.
3. Write desired value to preload register. (BAR + 00H or BAR + 04H)

General Interrupt Status Register

This register is at Base + 08H. Bit 0 is set when the first stage of down-counter reaches zero.

- Bit 0 = 0 – No Interrupt
- Bit 1 = 1 – Interrupt Active

Note: This bit is not set in free running mode.

Reload Register

This register is at Base + 0CH. Write 1 to bit 8 will reload the down-counter's value. Following is the procedure of how to prevent a timeout.

1. Write 80H to offset BAR + 0CH
2. Write 86H to offset BAR + 0CH
3. Write a '1' to RELOAD[8] of the reload register

Offset 60 – 61H: WDT Configuration Register

Bit 5 indicates whether or not the WDT will toggle the WDT_TOUT# pin when WDT times out. (0 = Enabled, 1 = Disabled)

Bit 2 provides two options for prescaling the main down-counter. (0 = 1ms – 10min, 1 = 1us – 1sec)

Bit [1:0] allows the user to choose the type of interrupt desired when the WDT reached the end of the first stage without being reset. (00 = IRQ, 01 = reserved, 10 = SMI, 11 = Disabled)

Note: Now, the WDT does not support SMI. IRQ uses APIC 1, INT 10 and it is active low, level triggered.

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Offset 68H: WDT Lock Register

Bit 2 is used to choose the functionality of the timer. (0 = Watchdog Timer mode, 1 = Free running mode) The free running mode ignores the first stage and only uses Preload Value 2. In free running mode it is not necessary to reload the timer as it is done automatically every time the down counter reaches zero.

Bit 1 enables or disables the WDT. (0 = Disabled, 1 = Enabled)

Bit 0 will lock the values of this register until a hard reset occurs or power is cycled. (0 = unlocked, 1 = locked) The default is Unlocked.

GPIO Control Registers

There are three GPIOs on the cPCI-3840 related to the watchdog timer. They are listed as follows. The GPIO control base port is 480H.

WDT_TOUT# pin selection

The WDT_TOUT# signal is multiplexed with GPIO32. When using WDT, this signal must be switched to WDT_TOUT# function. It uses bit 0 of GPIOBASE + 30H to set WDT_TOUT function. (0 = WDT_TOUT#, 1 = GPIO32)

RESET hardware circuit selection

GPO24 of the 6300ESB is designed to control the reset circuit. When GPO24 is low, the system will reset according to the level of the WDT_TOUT# signal. When GPO24 is high, the system will not be reset by WDT_TOUT#. Set bit 24 of GPIOBASE + 04H to 0 for output use. Bit 24 of GPIOBASE + 0CH determines the level of GPO24. (0 = Low, 1 = High) There already exists a setting in BIOS setup menu. (Integrated Peripherals page) The user can set this item before programming WDT.

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WDT LED Control

GPO25 of the 6300ESB is designed to control WDT LED. Two features of the WDT LED are supported on cPCI-3840. WDT LED lights or blinks.

- WDT LED lights: Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 0CH determines the state of WDT LED. (0=light, 1=dark)
- WDT LED blinks: Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 18H enables WDT LED blinking function. (0=function normally, 1=enable blinking) The high and low times have approximately 0.5 seconds each.

WDT Programming Procedure

1. Set BIOS Setting in Integrated Peripherals\Onboard Device Page Watch Dog Timer Item to “Enabled”.
2. Make sure WDT_TOUT# signal is functional. (Not GPIO32 function).
3. Set WDT output enable, presecaler and interrupt type into WDT configuration register.
4. Obtain control base from Base Address register.
5. Program Preload register’s value according to unlocking sequence.
6. Set WDT timer mode into WDT Lock Register.
7. Enable WDT from WDT Lock register and program the functionality of WDT LED.

To prevent the timer from causing an interrupt or driving WDT_TOUT#, the timer must be reloaded periodically. The frequency of reloads required is dependent on the value of the preload values. To reload the down-counter, the register unlocking sequence must be performed.

If the user wishes to disable WDT, set bit 1 of WDT Lock Register to 0.

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Utilities

ADLINK provide a demo DOS utility, HRWDT.EXE. It is included in the driver CD. Run “hrwdt /?” in the following directory for a more detailed description: X:\CHIPDRV\WDT\HRWDT

The user can also download the Intel® WDT demo windows application from the Intel® driver download center.

5.2 Intel® Preboot Execution Environment (PXE)

The cPCI-3840 series supports Intel® Preboot Execution Environment (PXE), which provides the capability of boot up or executing an OS installation through the Ethernet ports. There should be a DHCP server in the network with one or more servers running PXE and MTFTP services. It could be a Windows NT or Windows 2000 server running DHCP, PXE and MTFTP service or a dedicated DHCP server with one or more additional server running PXE and MTFTP service. This section describes the major items required for building a network environment with PXE support.

1. Setup a DHCP server with PXE tag configuration.
2. Install the PXE and MTFTP services
3. Make boot image file on PXE server (that is the boot server).
4. Enable the PXE boot function on the client computer.

For further details, please refer to the pdkrel30.pdf in the directory X:\Utility\PXE_PDK.

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   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
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   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.
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   - This warranty is not transferable or extendible.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

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