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ACL-7130

Isolated Digital I/O Card

User's Guide

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How to Use This Manual

This manual is designed to help you use the ACL-7130. The manual describes how to modify various settings on the ACL-7130 card to meet your requirements. It is divided into five chapters:

- **Chapter 1,** "Introduction," gives an overview of the product features, applications, and specifications.
- **Chapter 2,** "Installation," describes how to install the ACL-7130. The layout of ACL-7130 is shown, the DIP switch setting for base address, and jumpers setting for interrupt trigger, and trigger mode are specified.
- **Chapter 3,** "Register Format", describes the register format and how to program the ACL-7130 for digital I/O and timer/counter.
- **Chapter 4,** "Digital I/O Operation Theorem," describes how to connect the external signal with ACL-7130's isolated and non-isolated digital.

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1

Introduction

The ACL-7130 is an isolated digital I/O card with a bus. The card provides 16 isolated digital input and 16 isolated digital output channels. The isolated channels are suitable for applications in the industry environment. There are another 16 non-isolated digital input and output channels. It lets users to use the card more flexible.

The card provides dual interrupt lines. One is generated by the external digital signals and the other is generated from the 8254 timer. The dual interrupt lines are very usable in industrial applications of watchdog and trigger signal monitoring.

This card provides one 8254 chips on board. Two 8254 counters are cascaded to provide a timer interrupt source. Users can freely use the another counter.

The I/O signals are via a 37 pin D-type connector that project through the computer case at the rear of the board. Another two non-isolated digital I/O connectors are on-board, which can connect with the daughter board - ACLD-9182 and ACLD-9185 directly.

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1.1 Features

The ACL-7130 Isolated D/I Card provides the following advanced features:

- 16 isolated digital input and output channels
- 16 non-isolated digital input and output channels
- One 8254 chip on board which provide a set of cascaded timers and one independent counter
- Dual interrupt channels, one is for external interrupt and the other is for on board timer interrupt
- Use 37-pin D-type female connector
- AT-Bus and Compact / Half size PCB

1.2 Applications

- Laboratory and Industrial automation
- Programmable Logic Controller
- Watchdog timer
- Event counter

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1.3 Specifications

- **Isolated Digital Output**
- **Number of channels:** 16 channels
- **Electricity characteristics:** Open collector transistor
- **Output Voltage:** open collector 5V (min) to 40 VDC (max)
- **Sink Current:**

  Max. 500mA/ch for only one of the TD62003 transistor is ON

  347mA/ch for all of the TD62003 transistors are ON @ 10% duty
- **Isolation Voltage:** 2,500 VDC
- **Max. Throughput:** 10KHz
- **Isolated Digital Input**
- **Number of channels:** 16 channels
- **Electricity characteristics:** Non-polarity photo-coupler
- **Input Voltage:** 0 - 24VDC or –24VDC - 0

  Logic H: 3~24V or –24~ -3V

  Logic L: 0~2.4V or –2.4V~0
- **Input Resistance:** 1.2K Ohm @ 1W (470Ohm for special version)
- **Isolation Voltage:** 2,500 VDC
- **Max. Throughput:** 10KHz
- **Non-isolated Digital Input**
- **Number of channels:** 16 channels
- **Input logic low voltage:** Min. -0.5V; Max. 0.8V
- **Input logic high voltage:** Min. 2.0V; Max. 5.0V
- **Input loading current:** Max. 0.2 mA at 0.4V
- **Non-isolated Digital Output**
- **Number of channels:** 16 channels
- **Input logic low voltage (Sink):** Max. 0.5V at 24mA;
- **Input logic high voltage (Source):** Max. 0.4V at 12mA
- **Driving Capacity:**All inputs and outputs are TTL/DTL compatible
- **Programmable Counter:**

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- **Chips:** 8254 include 3 counters
- **Counter resolution:** 16-bit counters (counter0 ~ counter 2)
- **Counter usage**: counter 0 is free for users; counter 1 and counter 2 are cascaded together for timer pacer generation. Base frequency of Counter 2: 2MHz
- **Usable pins:** CLK and GATE for counter 0 (JP5)
- **General Specification**
- **Bus:** ISA bus
- **I/O port address:** Hex 200 ~ Hex 3F8 (8 bytes)
- **Connector:** One DB-37 for Isolated DIO
- Two 20-pin flat-cable for TTL DIO
- **Interrupt IRQ**: IRQ 3,4,5,6,7 for external digital interrupt
- IRQ 9,10,11,12,15 for internal timer interrupt
- **Operating Temperature:** 0 ~ 60 °C
- **Storage Temperature:** -20 ~ 80 °C
- **Humidity:** 5 to 95% non-condensing
- **Power Consumption:**
- 5V @ 360mA typical
- **Dimension:** 163 mm x 123 mm

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1.4 Software Supporting

The ACL-7130 is programmed using simple 8-bit I/O port commands. Users can use high level language, such as BASIC, C, or PASCAL, or low- level language, such as assembly to program the board. For the programming under Windows or LabView, please contact your dealer to purchase ACLS-DLL1 or ACLD-LVIEW.

ACLS-DLL1

For easily program the board under Windows environment, we also provide **ACLS-DLL1**, which include the DLL for Windows 95/98/NT. With ACLS-DLL1, you can use compilers such as VB, VC/C++, or Delphi.

ACLS-LVIEW

For easily link the ACL-7122 with LabView of National Instrument. ACLS-LVIEW includes the Vis of the ACL-7122 under for Windows 3.1/95/98 and NT.

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2

Installation

This chapter describes how to install the ACL-7130. The following procedures show the installation procedures:

- Check what you have
- Check the PCB and check the location of jumper and switch
- Setup the jumpers according to the operation theorem
- Installation the DOS software library if necessary

2.1 What You Have

In addition to this manual, the package includes the following items:

- ACL-7130 Isolated Digital I/O Card
- ADLINK CD

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future. The default setting of ACL-7130 is shown at the end of this chapter.

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2.2 Unpacking

Your ACL-7130 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be done on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat. Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handing damages on the module before processing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface component side up.

Again inspect the module for damage. Press down on the entire socket IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your ACL-7130.

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2.3 PCB Layout

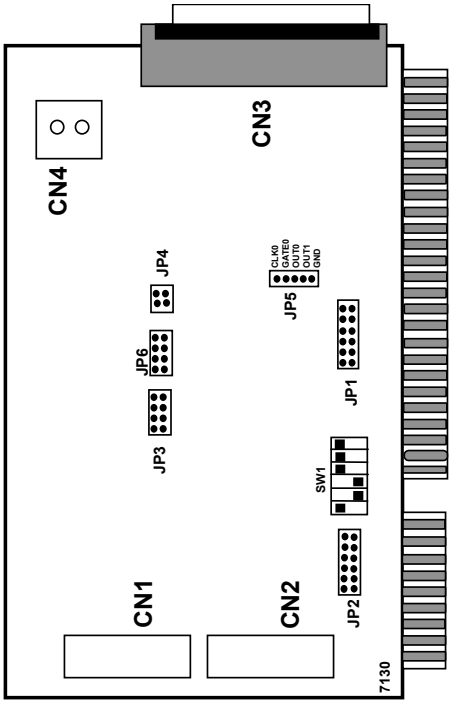


Figure 2.1 PCB Layout

Note: CN4 is for Rev A only, JP6 is for Rev B only.

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2.4 Jumper and DIP Switch Description

You can change the ACL-7130's channels and base address by setting jumpers and DIP switches on the card. The card's jumpers and switches are preset at the factory. Under normal circumstances, you should not need to change the jumper settings.

A jumper switch is closed (sometimes referred to as "shorted") with the plastic cap inserted over two pins of the jumper. A jumper is open with the plastic cap inserted over one or no pin(s) of the jumper.

2.5 Base Address Setting

The ACL-7130 requires 8 consecutive address locations in the I/O address space. The base address of the ACL-7130 is restricted by the following conditions.

1. The base address must be within the range *Hex 200* to *Hex 3FF*.

2. The base address should not conflict with any PC reserved I/O address.

3. The base address must not conflict with any add-on card on your own PC. Please check your PC before installing the ACL-7130.

The ACL-7130's base address of registers is selected by an 6 position DIP switch SW1. The default setting of base address is set to be ***HEX 300.*** All possible base address combinations are listed as Table 2.2. You may modify the base address if the address *HEX 300* has been occupied by another add-on card.

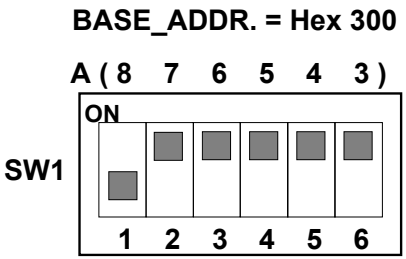


Figure 2.2 Default Base Address Setting

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I/O port Address(Hex)	1 A8	2 A7	3 A6	4 A5	5 A4	6 A3
200-207	ON (0)	ON (0)	ON (0)	ON (0)	ON (0)	ON (0)
208-20F	ON (0)	ON (0)	ON (0)	ON (0)	ON (0)	OFF (1)
210-217	ON (0)	ON (0)	ON (0)	ON (0)	OFF (1)	ON (0)
218-21F	ON (0)	ON (0)	ON (0)	ON (0)	OFF (1)	OFF (1)
:	:	:	:	:	:	:
2F8-2FF	ON (0)	OFF (1)	OFF (1)	OFF (1)	OFF (1)	OFF (1)
300-307 (default)	OFF (1)	ON (0)	ON (o)	ON (0)	ON (0)	ON (0)
308-30F	OFF (1)	ON (0)	ON (0)	ON (0)	ON (0)	OFF (1)
:	:	:	:	:	:	:
3F0-3F7	OFF (1)	OFF (1)	OFF (1)	OFF (1)	OFF (1)	ON (0)
3F8-3FF	OFF (1)	OFF (1)	OFF (1)	OFF (1)	OFF (1)	OFF (1)

* A3, ..., A8 is corresponding to PC Bus address lines

Table 2.1 Possible Base Address Combinations

How to define the base address for the ACL-7130 ?

The DIP1 to DIP6 in the switch SW1 are one to one corresponding to the PC bus address line A8 to A4. A9 is always 1 and A0~A3 are always 0. If you want to change the base address, you can only change the values of A8 to A4 (the shadow area of below table). The following table is an example, which shows you how to define the base address as ***Hex 300***

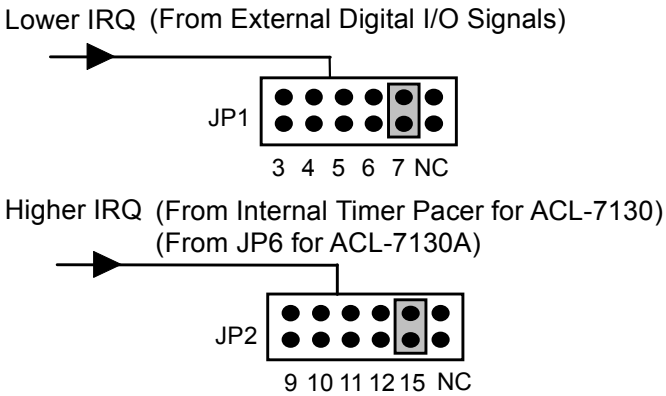
Base Address: ***Hex 300***

3		***0***				***0***			
1	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

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2.6 Interrupt Setting

The ACL-7130 offers AT Bus interrupt levels (IRQ3 ~ IRQ15), also a dual interrupt lines are supported. One is generated by the external digital signals and the other is generated from the 8254 timer on board.



The lower interrupt IRQ can be set as IRQ3~IRQ7 by Jumper JP1. It is illustrated as figure 2.3. The second interrupt IRQ can be set as IRQ9~IRQ15 by jumper JP2. It is illustrated as figure 2.4. Both of lower and higher IRQ can generate interrupt simultaneously.

The external digital signals can trigger the interrupt through lower interrupt setting. There are four different digital I/O signals can be used as interrupt trigger sources, also the trigger mode is either fall-edge or rising-edge trigger.

Note : Both lower and higher IRQ can be set simultaneously. And, two different IRQ can be generated by using ACL-7130. Be aware that there is no other add-on card shares the same interrupt level at the same system.

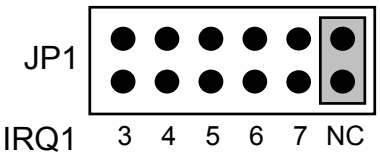


Figure 2.3 JP1 setting for lower IRQ

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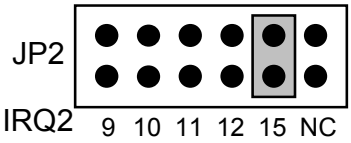


Figure 2.4 JP2 setting for higher IRQ

2.7 Setting of IRQ Signal Source

The lower Interrupt IRQ source (JP3) can be set as either

IDI_0:Isolated Digital Input channel 0, or

IDI_1:Isolated Digital Input channel 1, or

DI_0:Digital Input 0, or

DI_1:Digital Input 1.

The jumper JP4 is used for signal source selection.

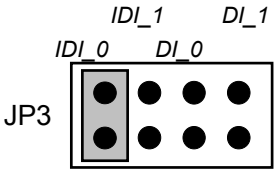


Figure 2.5-1 Jumper JP3 setting

The higher IRQ source (JP6) can be set as either

OUT1:Timer Pacer Output
IDI_0: Isolated Digital Input channel 0, or
IDI_1: Isolated Digital Input 1, or
DI_1: Digital Input 1.

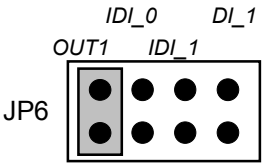


Figure 2.5-2 Jumper JP6 setting

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2.8 Setting of Lower IRQ Signal Polarity (JP4)

The Interrupt signal can be selected as Fall Edge trigger or Rise Edge trigger. It can be set as jumper JP4.

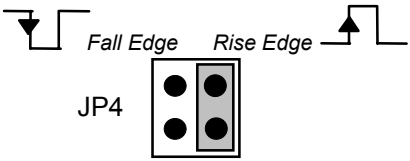


Figure 2.6 Jumper JP4 setting

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2.9 Pin Assignments

There are three DIO connectors. The pin assignments of the 37 pins D-type connector CN3, which is an isolated DIO signal connector, is shown in Figure 2.7. The definitions of the non-isolated DIO signal connectors CN1 and CN2 are shown is Figure 2.8 and Figure 2.9 respectively.

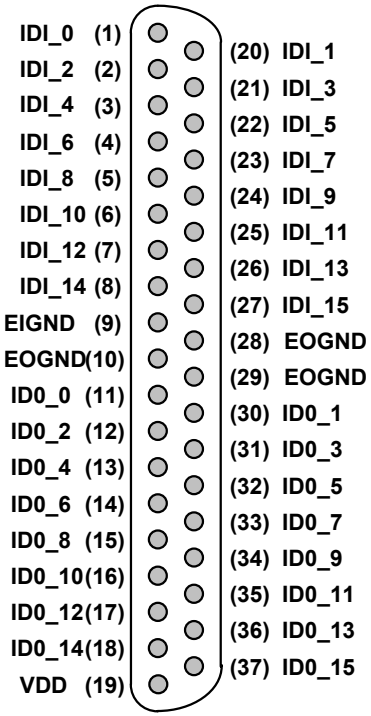


Figure 2.7 Pin assignment of Connector CN3

Legend:
IDI_n: Isolated digital input channel #n
IDO_n: Isolated digital output channel #n
EIGND: Ground return path of isolated input channels
EOGND: Ground return path of isolated output channels
VDD: Power supply of isolated output channels

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- CN 2: Digital Signal Input (DI 0 - 15)

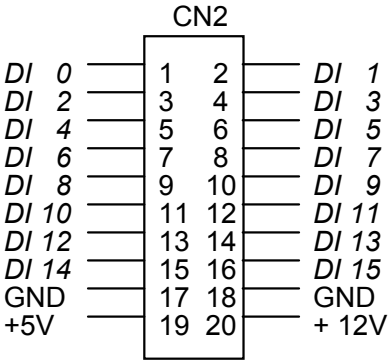


Figure 2.8 Pin assignment of Connector CN2

- CN 1: Digital Signal Output (DO 0 - 15)

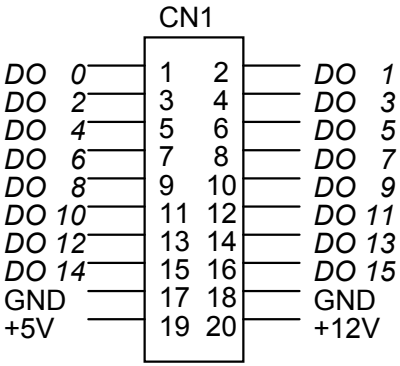
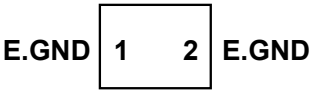


Figure 2.9 Pin assignment of Connector CN1

CN 4 : Isolated Output GND Terminal



Legend:

DO n: Digital output signal channel *n*
DI n: Digital input signal channel *n*
GND: Digital ground
E.GND: External Ground for Isolated Input

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2.10 Counter Signals Connector (JP5)

There is an internal programmable timer/counter 8254 chip on the ACL-7130. The counter1 and counter 2 are cascaded together for timer pacer generation. The reminder counter 0 is available for flexible usage. Refer figure 2.11. The jumper JP5 is connector for counter 0 and its pin assignment is illustrated as figure 2.10.

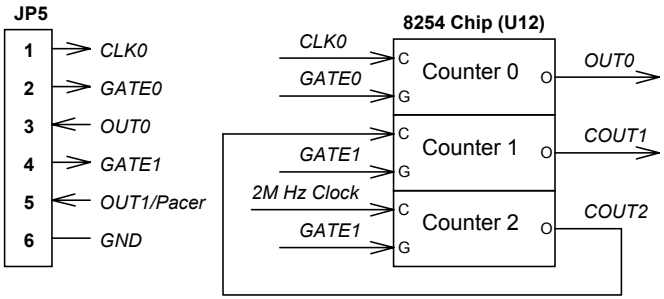


Figure 2.10 Pin Assignment of JP5

The pacer rate of above configuration is determined by the formula:

Pacer rate = 2 MHz / (C1 * C2)

The maximum pacer signal rate is 2MHz/1=2MHz. The minimum signal rate is 2MHz/65535/65535, which is a very slow frequency that user may never use it. For example, if you wish to get a pacer rate 2.5 kHz, you can set C1 = 40 and C2 = 20. That is 2.5KHz = 2MHz / (40 x 20)

2.11 Software Library Installation

To install the DOS library software and utilities, please follow the following installation procedures:

1. Put *ADLINK CD* into the appropriate CD-ROM drive.

2. Type the following commands to change to the card's directory (*X* indicates the CD-ROM drive):

   X:\>**CD \NuDAQISA\7130**

3. Execute the setup batch program to install the software:

   X:\NuDAQISA\7130>**SETUP**

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3

Registers Format

3.1 I/O Registers Map

The ACL-7130 requires 8 consecutive addresses in the PC I/O address space. The I/O address map is compatible with PCL-730 but which one more timer / counter chip. Table 3.1 shows the I/O address of each register with respect to the base address.

Address	Write	Read
Base + 0	Isolated DO low byte	Isolated DI low byte
Base + 1	Isolated DO high byte	Isolated DI high byte
Base + 2	DO low byte	DI low byte
Base + 3	DO high byte	DI high byte
Base + 4	8254 Counter #0	
Base + 5	8254 Counter #1	
Base + 6	8254 Counter #2	
Base + 7	8254 mode control	8254 counter status

Table 3.1 I/O Address Map of ACL-7130

DO -- Digital Output
DI -- Digital Input

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3.2 Digital Input Registers

There are total 32 digital input channels on the ACL-7130, including 16 isolated DI channels and 16 non-isolated channels. Each bit is corresponding to a signal on the connectors.

Address: BASE + 0 ~ BASE + 3

Attribute: read only

Data Format:

Bit	7	6	5	4	3	2	1	0
Base + 0	IDI_7	IDI_6	IDI_5	IDI_4	IDI_3	IDI_2	IDI_1	IDI_0
Base + 1	IDI_15	IDI_14	IDI_13	IDI_12	IDI_11	IDI_10	IDI_9	IDI_8
Base + 2	DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0
Base + 3	DI_15	DI_14	DI_13	DI_12	DI_11	DI_10	DI_9	DI_8

IDI_N : Isolated Digital Input CH *N*
DI_N : Non-isolated Digital Input CH *N*

3.3 Digital Output Registers

There are total 32 digital output channels on the ACL-7130; including 16 isolated DO channels and 16 non-isolated channels. Each bit is corresponding to a signal on the connector.

Address: BASE + 0 ~ BASE + 3

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
Base + 0	IDO_7	IDO_6	IDO_5	IDO_4	IDO_3	IDO_2	IDO_1	IDO_0
Base + 1	IDO_15	IDO_14	IDO_13	IDO_12	IDO_11	IDO_10	IDO_9	IDO_8
Base + 2	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0
Base + 3	DO_15	DO_14	DO_13	DO_12	DO_11	DO_10	DO_9	DO_8

IDO_N : Isolated Digital Output CH *N*
DO_N : Digital Output CH *N*

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3.4 Timer/Counter Registers

The 8254 occupy 4 I/O address locations in the ACL-7130 as shown blow. Users can refer to NEC's or Intel's data sheet for a full description of the 8254 features; condensed information is specified in Section 3.6.

Address: BASE + 4 ~ BASE + 7

Attribute: read / write

Data Format:

Base + 4	Counter 0 Register (R/W)
Base + 5	Counter 1 Register (R/W)
Base + 6	Counter 2 Register (R/W)
Base + 7	8254 Mode Control Register

3.5 Low-level Programming

To manipulate the ACL-7130, users may understand how to write a hardware dependent low-level program. The low-level programming can be carried out by using either assembly or high-level language such as BASIC or C language. The following gives examples to show how to use programming language to access a DAS card or any add-on I/O card.

Getting Start

Before programming, the add-on card should be correctly installed. After installing the card, the users should already understand how much system (PC) resources are used by this card, such as I/O address, IRQ channels, etc..

The second step is to study the register format and the operation theorem of the card. Then users can try to write low-level programs to operate it. Although the high-level program library is available, the low-level programming can improve the efficiency and perform functions which the library does not support. The low-level programming is not difficult and may be necessary to understand.

Programming Language

The programming language to be used is dependent on users' familiarity and the system requirement. No matter what kind of language is used, the user must understand the syntax of the I/O instructions to access the I/O card. The following sections introduce the syntax of the often-used programming languages. In each section, the write (output) port instruction and the read (input) port instruction are shown. In the examples, the base address of the

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I/O card is assumed as *HEX 300* and the port of the register to be access is BASE+2.

Assembly

To write an output port:

```
out300h,value
out300h,register
```

To read an input port

```
in300h
```

BASIC language

To write an output port:

```
10BASE=&H300
20 VALUE% = &H2F
30OUT (BASE+2), VALUE %
or
10OUT (&H302), &H2F
```

To read an input port

```
10BASE=&H300
20VALUE=INP (BASE+2)
or
10VALUE=INP (&H302 )
```

C language (Borland C++)

To write an output port:

```
#define BASE0x300
unsigned int Value=0x2F;
outportb (BASE+2 , Value);
or
outportb (0x302, 0x2F);
```

To read an input port

```
#define BASE0x300
unsigned intValue;
Value = inpportb (BASE+2);
or
Value = inportb (0x302);
```

C language (MicroSoft C)

To write an output port:

```
#define BASE0x300
unsigned intValue=0x2F;
outp (BASE+2 ,  Value) ;
or
outp (0x302 ,  0x2F);
```

To read an input port

```
#define BASE0x300
unsigned intValue;
Value = inp (BASE+2);
or
```


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```
Value = inp (0x302);
```

Perform Functions

Users should study the operation theorem and the relative data sheet to understand how to operate this card, then use the low-level programming to perform those functions. Generally, the DIO control can be easily performed by only a few instructions, it is very suitable to use the low level programming.

Digital Input Operation (Read):

The digital input states are read as a single byte from the port at address BASE+N (N= 0,1,2,3). Each of the 8 bits within the byte corresponding to particular digital input, a high bit (1) signifies the input is energized, a low bit (0) signifies the input is de-energized.

For example: (In BASIC)

```
05   BASE=&H300
10   VALUE1 = INP(BASE + 0)   'Read DO0 ~ DI 7
20   VALUE2 = INP (BASE + 2)   'Read DO16 ~ DI 23
```

Write operation :

The digital output states are written as 1 single byte to the port at address BASE+N (N=0,1,2,3). Data is written to all 8 bits as a single byte.

For example: (In BASIC)

```
05   BASE=&H300
06   VALUE1% = &H3F
07   VALUE2% = &HF3
10   OUT (BASE + 0), VALUE1% ' the digital outputs (DO0-
DO7)  will be (00111111 )
20   OUT (BASE + 2), VALUE2% ' the digital outputs
(DO16-DO23)  ' will be ( 11110011)
```


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3.6 Programmable Interval Timer

Note : The material of this section is adopted from

“Intel Microprocessor and Peripheral Handbook Vol. II --Peripheral”

3.6.1 The Intel (NEC) 8254

The Intel(NEC) 8254 contains three independent, programmable, multi-mode 16 bit counter/timers. The three independent 16 bit counters can be clocked at rates from DC to 5 MHz. Each counter can be individually programmed with 6 different operating modes by appropriately formatted control words. The most commonly uses for the 8254 in microprocessor based system are:

- programmable baud rate generator
- event counter
- binary rate multiplier
- real-time clock
- digital one-shot
- motor control

For more information about the 8254 , please refer to the NEC Microprocessors and peripherals or Intel Microprocessor and Peripheral Handbook.

3.6.2 The Control Byte

The 8254 occupies 8 I/O address locations in the ACL-7130 I/O map. As shown below.

Base + 4	LSB OR MSB OF COUNTER 0
Base + 5	LSB OR MSB OF COUNTER 1
Base + 6	LSB OR MSB OF COUNTER 2
Base + 7	CONTROL BYTE for Chip 0

Before loading or reading any of these individual counters, the **control byte** (Base + 7**)** must be loaded first. The format of control byte is :

Control Byte : (Base + 7)

Bit	7	6	5	4	3	2	1	0
	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

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- SC1 & SC1 - Select Counter (Bit7 & Bit 6)

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	ILLEGAL

- RL1 & RL0 - Select Read/Load Operation (Bit 5 & Bit 4)

RL1	RL0	OPERATION
0	0	COUNTER LATCH
0	1	READ/LOAD LSB
1	0	READ/LOAD MSB
1	1	READ/LOAD LSB FIRST, THEN MSB

- M2, M1 & M0 - Select Operating Mode (Bit 3, Bit 2, & Bit 1)

M2	M1	M0	MODE
0	0	0	0
0	0	1	1
x	1	0	2
x	1	1	3
1	0	0	4
1	0	1	5

- BCD - Select Binary/BCD Counting (Bit 0)

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4 DECADES)

NOTE:

1. The count of the binary counter is from 0 up to 65,535.

2. The count of the BCD counter is from 0 up to 99,999.

3.6.3 Mode definition

In 8254, there are six different operating modes can be selected. The they are :

- **Mode 0 :** interrupt on terminal count

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high

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and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1)Write 1st byte stops the current counting.

(2)Write 2nd byte starts the new count.

- **Mode 1 :** Programmable One-Shot

The output will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at anytime without affecting the one-shot pulse.

The one-shot is re-triggerable, hence the output will remain low for the full count after any rising edge of the gate input.

- **Mode 2 :** Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input when low would force the output high. When the gate input goes high, the counter will start form the initial count. Thus, the gate input can be used to synchronize by software.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

- **Mode 3 :** Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (or even numbers) and go low for the other half of the count. This is accomplished by decrement the counters by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2 after time-out, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until time-out. Then

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the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

In Modes 2 and 3, if a CLK source other then the system clock is used, GATE should be pulsed immediately following Way Rate of a new count value.

- **Mode 4** : Software Triggered Strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

- **Mode 5** : Hardware Triggered Strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is re-triggerable. The output will not go low until the full count after the rising edge of any trigger.

The detailed description of the mode of 8254, please refers the Intel Microsystem Components Handbook.

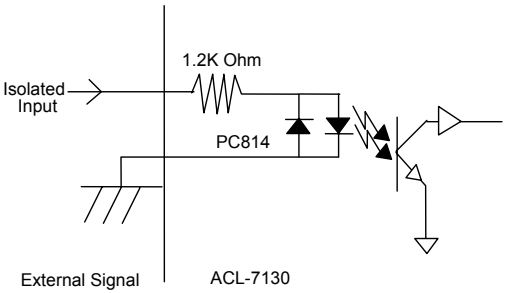
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4

Signal Connections

4.1 Isolated Digital Input Channels

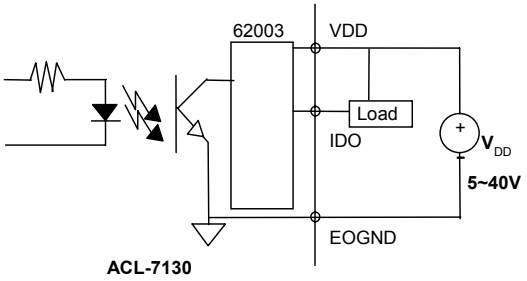
The isolated digital output is an open collector transistor output. The input accepts voltage form 5V to 24V and input resister is 1.2K Ω. The connection between outside signal and ACL-7130 is shown below.



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4.2 Isolated Digital Output Channels

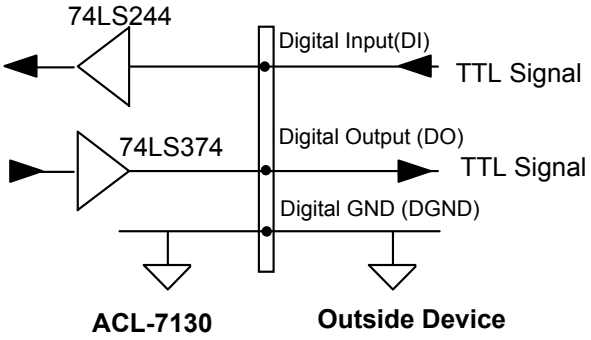
The connection of isolated-digital output is shown as following diagram. An external voltage source (5~40VDC) is necessary to power the internal isolated circuits, and it is connected with pin-19 of CN3. When the isolated digital output goes to high, the sink current will be from VDD.



4.3 Digital I/O Channels

The ACL-7130 provides 16 digital input and 16 digital output channels through the connector CN1 and CN2 on board. The digital I/O signal are fully TTL/DTL compatible. Please refer to section 1.3 for the detailed digital I/O (DIO) signal specification, and section 2.9 for the DIO connectors, and section 3.2 for the registers format.

To program digital I/O operation is fairly straight forward. The digital input operation is just to read data from its corresponding registers, and output operation is to write data to registers.



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   - Damage caused by carelessness on the user's part during product transportation.
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