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PCIe-7350

32-CH High-speed DIO Board

User's Manual

Manual Rev. 2.00

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1 Introduction

ADLINK's PCIe-7350 is a high-speed digital I/O board with 32-channel bi-direction parallel I/O lines. The data rate can achieve up to 200 MB/s through the x1 PCI Express® interface. The clock rate can support up to 50 MHz internal clock or 100 MHz external clock, which is ideal for the applications of high-speed and large-scale digital data acquisition or exchange, such as digital image capture, video playback and IC testing.

1.1 Features

The PCIe-7350 comes with the following advanced features:

- x1 lane PCI Express® Interface
- Maximum 50 MHz clock rate from internal timer or 100 MHz from external clock
- 200 MB/s maximum throughput
- Software selectable voltage level of 1.8 V, 2.5 V, and 3.3 V (5 V compatible)
- 16-steps phase shift in external clock mode
- Per group (8-bit) input/output direction selectable
- Supports I^2C and SPI programmable serial interfaces for external device communication
- Scatter-gather DMA support
- Flexible handshaking and external digital trigger modes
- 8-channel auxiliary programmable I/O support

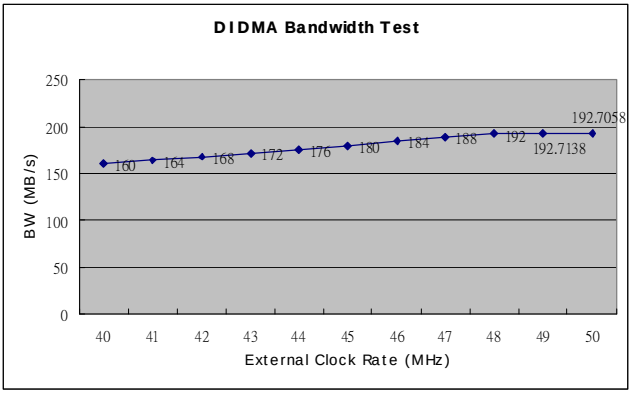
1.2 Applications

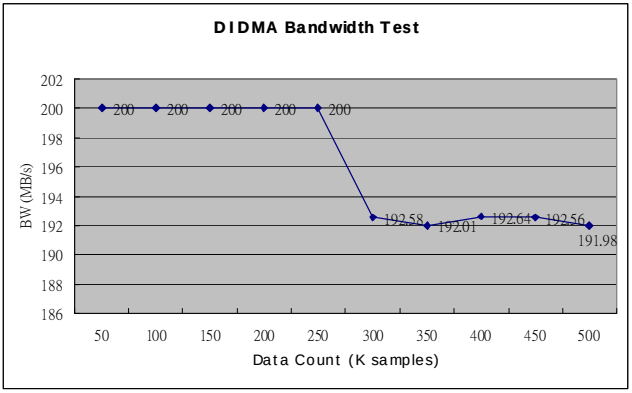
- High-speed digital data exchange
- Digital pattern generation and acquisition
- IC testing
- Interface to external high-speed A/D and D/A converter
- ATE

1.3 Specifications

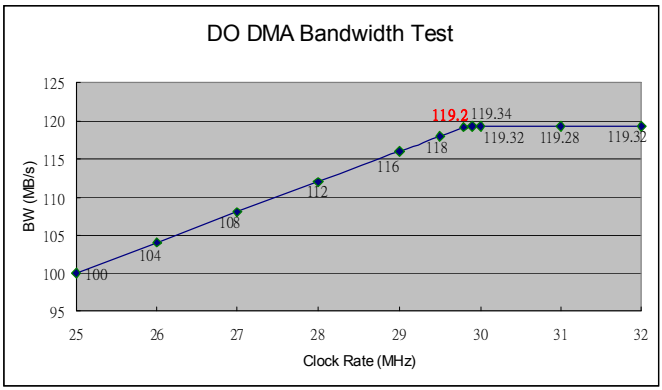
Digital I/O Specifications				
Number of Channels		32		
Direction (programmable)		Input or output, per group (8 channel) basis		
Logic Level (programmable)		1.8 V	2.5 V	3.3 V (5 V compatible)
Input Voltage	**Min. V_{IH}**	1.2 V	1.6 V	2 V
	Max. V_{IL}	0.63 V	0.7 V	0.8 V
Output Voltage	**Min. V_{OH}**	1.6 V	2.3 V	3.1 V
	Max. V_{OL}	0.2 V	0.2 V	0.2 V
Driving capacity(max.)		±8 mA	±16 mA	±32 mA
Throughput		Digital Input: Maximum: 200 MByte/s (32-bits input @ 50 MHz) (data size≤250k samples) Sustained: 192 MByte/s (data size>250k samples) (Note*) Digital Output: Maximum: 200 MByte/s (32-bit output @ 50 MHz) (FIFO load mode, max. 8k samples) Sustained: 119.2 MByte/s (Note**)		
FIFO Size		Digital Input: 8k samples Digital Output: 8k samples		
Data Transfer		Software Polling Bus-mastering DMA with Scatter-Gather		
Clocking Modes		Internal clock: max. 50 MHz External clock: max. 100 MHz Handshaking Burst handshaking		
Trigger Source		Software External Digital signal Pattern match		
Trigger Modes		Post trigger with re-trigger Gate trigger		
Input impedance		10 KΩ		
Input protection range		-1 to 6 V		
Output impedance		50 Ω		
Power-up initial state		Tri-State / All digital inputs		
Output protection range		-0.5 V to 3.8 V		
Dimensions		168 mm x 112 mm (not including connectors)		
Connectors		68-pin VHDCI female x1 SMB x2		
Operating Temp.		0 to 55° C		
Storage Temp.		-20 to 70° C		
Relative Humidity		5 to 95%, non-condensing		

Note*: DI DMA throughput





Note**: DO DMA throughput



If you want to have DO throughput to be up to 200M Byte/s, the data size is limited to less than the 8K FIFO size by the following steps:

Step1: Read 8K DO data from system memory into DO FIFO by DMA before writing 8K DO data from DO FIFO to the external device

Step2: After 8K DO data are all stored into DO FIFO, and then start writing these 8K DO data to the external device with 50MHz DO sample clock rate and 32-bit data width.

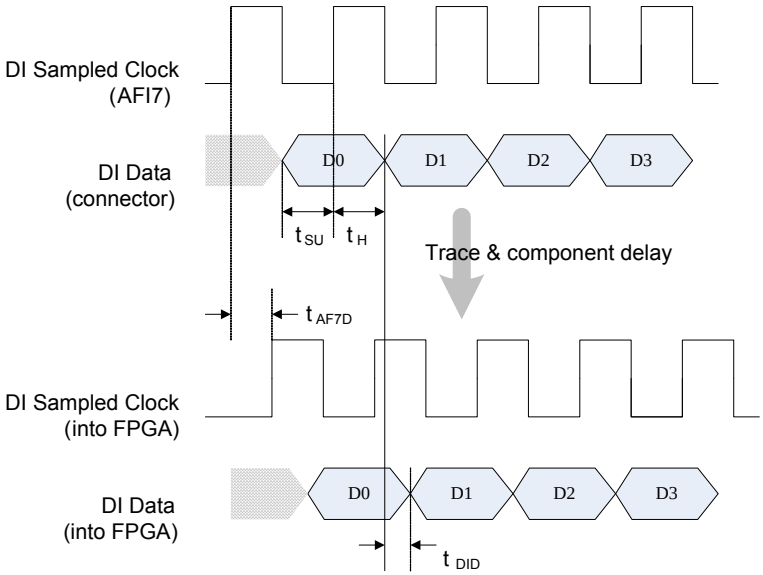
External clock rate can be up to 100 MHz, but only support 8 or 16-bit data width because the DI data throughput can't exceed 200 MB/s

Application Function I/O (AFI)				
Number of channels		8		
Direction (programmable)		Input or output, per channel basis		
Logic Levels (programmable)		1.8 V	2.5 V	3.3 V (5 V Compatible)
Input Voltage	**Min. V_{IH}**	1.2 V	1.6 V	2 V
	Max. V_{IL}	0.63 V	0.7 V	0.8 V
Output Voltage	**Min. V_{OH}**	1.6 V	2.3 V	3.1 V
	Max. V_{OL}	0.2 V	0.2 V	0.2 V
Driving capacity (max.)		±8 mA	±16 mA	±32 mA
Input impedance		10 KΩ		
Input protection range		-1 to 6 V		
Output impedance		50 Ω		
Power-up initial state		Tri-State / All digital inputs		
Output protection range		-0.5V to 3.8V		
Supported Mode (programmable)		I^2C master SPI master Handshaking External trigger in/out DI/DO sample clock in/out		

Timing Specifications	
Sample Clock	
Clock Sources	Internal clock: on-board 100MHz with 16-bit divider External clock: 1. AFI6 (for DO) 2. AFI7 (for DI) 3. SMB CLK in
Internal Clock Rate (programmable)	1526 Hz – 50 MHz (100 MHz/ N; 2≤N≤65,535)
Ext. frequency range	0 - 100 MHz (no phase shift) 2 MHz - 50MHz (phase shift enabled)*
Phase shift	Internal clock: N/A External clock: 16 steps; 1 step = 22.5°
Sample Clock Exporting	
Destination	1. AFI6 (only for DO) 2. AFI7 (only for DI) 3. SMB CLK out
Frequency range	0 ~ 50 MHz (no phase shift) 2 MHz ~ 50MHz (phase shift enabled) (note3)
Clock jitter	Period jitter: 160 ps
Clock duty cycle	50%
Phase shift resolution	1/16 of external sampled clock period (16 steps; 1 step = 22.5°)

When you enable phase shift, the clock must be continuous and free-running

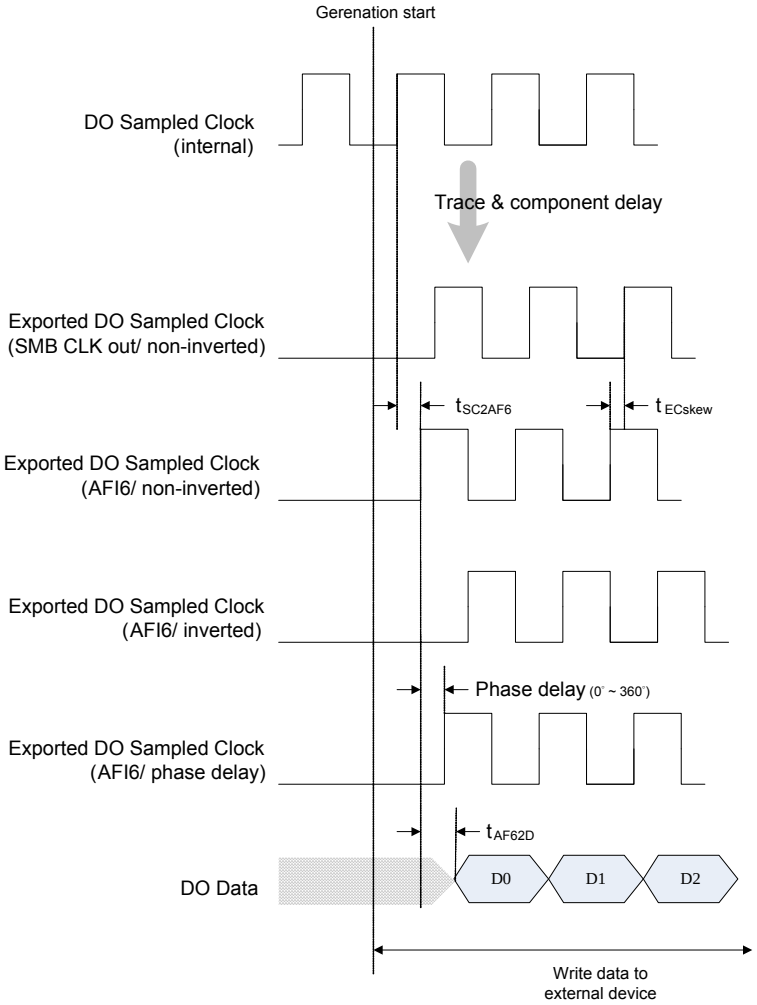
Timing Accuracy	
Acquisition Timing	
Channel-to-Channel skew	±1.08 ns
Setup time to sampled clock (t_{SU})	2 ns
Hold time to sampled clock (t_H)	2 ns
Time delay of external sampled clock from AFI7 to internal (t_{AF7D})	7.22 ns
Time delay of external sampled clock from SMB CLK in to internal (t_{SMBID})	8.02 ns
Time delay of DI data from VHDCI connector to internal (t_{DID})	3.26 ns - 4.34 ns
Generation Timing	
Exported Clock SkewAFI6 -to- SMB CLK out(t_{ECskew})	3.24 ns
Exported Clock (AFI6) -to- DO Data Delay (t_{AF62D})	600 ps - 5 ns



t_{AF7D} = Time delay of external sampled clock from AFI7 to internal

t_{DID} = Time delay of DI data from VHDCI connector to internal

Figure 1-1: Acquisition Timing Diagram



t_{SC2AF6} = Time delay from sampled clock (internal) to exported sampled clock (AFI6)

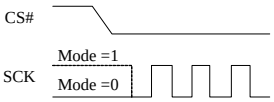
t_{ECskew} = Time delay from exported clock (AFI6) to exported clock (SMB CLK out)

t_{AF62D} = Time delay from exported sampled clock (AFI6) to do data

Figure 1-2: Generation Timing Diagram

External Clock I/O Specification		
CLK IN (SMB Jack Connector)		
Destination	DI or DO sample clock	
Input coupling	AC	
Input Impedance	50 Ω	
Minimum detectable pulse width	8 ns	
External sampled clock range	Square Wave	
	Voltage	0.2 Vpp to 5 Vpp
	Frequency	100 KHz - 50 MHz
	Duty cycle	40% - 60%
	Sine Wave	
	Voltage	0.2 Vpp to 5 Vpp
	Frequency	100 KHz – 50 MHz
CLK OUT (SMB Jack Connector)		
Sources	DI or DO sample clock	
Source impedance	50 Ω	
Logic Levels (programmable)	The same logic level of AFI I/O (1.8 V, 2.5 V, or 3.3 V)	
Driving Capacity (Max.)	±8 mA at 1.8 V ±16 mA at 2.5 V ±32 mA at 3.3 V	

I^2C Master Specification				
Signal			Direction	Pin
		SCL	O	AFI0
		SDA	I/O	AFI1
Supported clock rate (programmable)		1.9 kHz -244.14 kHz; 488.28125 kHz / (n + 1); 1 ≤ n ≤ 255		
Transfer size of Data		0 - 4 Bytes		
Transfer size of Cmd/ Addr		0 - 4 Bytes		
Logic families (programmable)		1.8 V	2.5 V	3.3 V
Input Voltage	**Min. V_{IH}**	1.2 V	1.6 V	2.0 V
	Max. V_{IL}	0.63 V	0.7 V	0.8 V
Output Voltage	**Min. V_{OH}**	1.6 V	2.3 V	3.1 V
	Max. V_{OL}	0.2 V	0.2 V	0.2 V

SPI Master Specification				
Signal			Direction	Pin
		SCK	O	AFI0
		SDO	O	AFI1
		SDI	I	AFI2
		CS_0	O	AFI3
		CS_1	O	AFI4
		CS_2	O	AFI5
Supported clock rate (programmable)		244.14 kHz -62.5 MHz, 62.5 MHz / (n + 1); 0 ≤ n ≤ 255		
Clock mode				
The first bit be transferred		MSB/ LSB (Default: MSB)		
Transfer size of Data		0 - 32 bits		
Transfer size of Cmd/ Addr		0 - 32 bits		
Dummy size		0 - 15 bits		
SPI Slave selection		Max. 3 slave devices (selected by CS_0 / CS_1 / CS_2		
Logic families (programmable)		1.8 V	2.5 V	3.3 V
Input Voltage	**Min. V_{IH}**	1.2 V	1.6 V	2 V
	Max. V_{IL}	0.63 V	0.7 V	0.8 V
Output Voltage	**Min. V_{OH}**	1.6 V	2.3 V	3.1 V
	Max. V_{OL}	0.2 V	0.2 V	0.2 V

General Specification			
Interface	x1 PCI Express interface		
Connector	1. SMB Jack Connector x2 (CLK IN & OUT) 2. 68-pin SCSI-VHDCI x1 (32-bit Data Lines & 8-ch AFI)		
Operation Temperature	0°C - 45°C		
Storage Temperature	-20°C - 70°C		
Humidity	5 - 95%, non-condensing		
Dimension	168 mm (L) x 112 mm (H), not including connectors		
Power Consumption		Typical	Maximum
	+3.3 VDC	450 mA	780 mA
	+12V VDC	625 mA	680 mA
	Total Power	9 W	10.8 W

1.4 Software Support

ADLINK provides versatile software drivers and packages for users' different approach to building up a system. ADLINK not only provides programming libraries such as DLL for most Windows based systems, but also provide drivers for other software packages such as LabVIEW®.

All software options are included in the ADLINK CD. Non-free software drivers are protected with licensing codes. Without the software code, you can install and run the demo version for two hours for trial/demonstration purposes. Please contact ADLINK dealers to purchase the formal license.

1.4.1 Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

- **PCIS-DASK:** Include device drivers and DLL for **Windows 98/NT/2000/XP/Vista**. DLL is binary compatible across Windows 98/NT/2000/XP/Vista. This means all applications developed with PCIS-DASK are compatible across Windows 98/NT/2000/XP/Vista. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of PCIS-DASK are in the CD.
  (\\Manual\Software Package\PCIS-DASK)

2 Hardware Information

This chapter provides information on the PCIe-7350 layout, connectors, and pin assignments.

2.1 Card Layout

Figure 2-1 shows the PCIe-7350 board layout and dimensions.

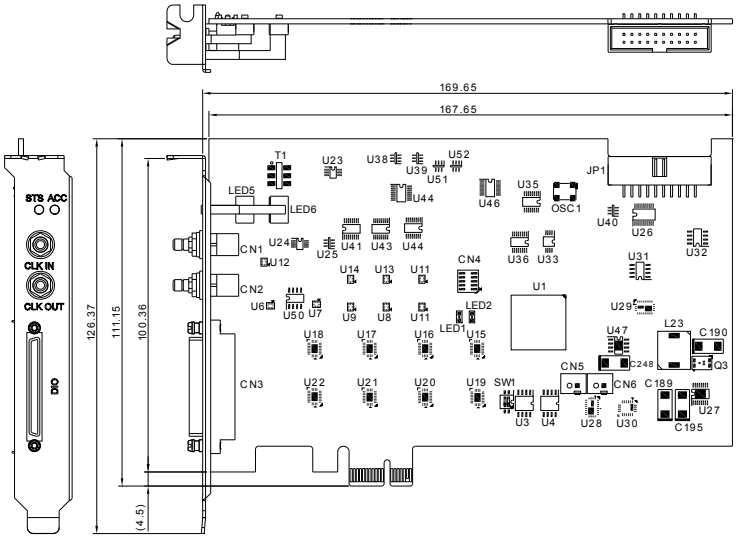
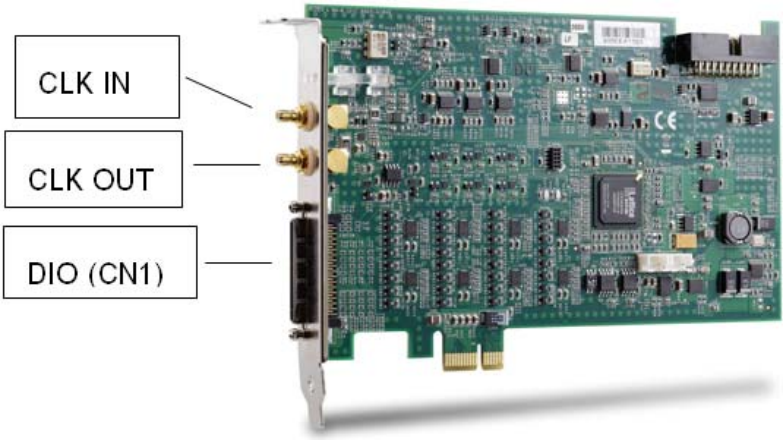


Figure 2-1: PCB Layout and Mechanical Drawing of the PCIe-7350

2.2 Connector Pin Assignment

The PCIe-7350 card is equipped with one 68-pin SCSI-VHDCI connector and two SMB connectors. The SCSI-VHDCI connector is for high-speed digital I/O and programmable function I/O, while the SMB connectors are for sample clock input or exporting.



	Pin #	Pin #	
GND	68	34	GND
(DI CLK) AFI7	67	33	AFI6 (DO CLK)
GND	66	32	GND
D0	65	31	D1
AFI5	64	30	AFI4
D2	63	29	D3
GND	62	28	GND
D4	61	27	D5
AFI3	60	26	AFI2
D6	59	25	D7
GND	58	24	GND
D8	57	23	D9
GND	56	22	GND
D10	55	21	D11
GND	54	20	GND
D12	53	19	D13
AFI1	52	18	GND
D14	51	17	D15
GND	50	16	GND
D16	49	15	D17
GND	48	14	GND
D18	47	13	D19
GND	46	12	GND
D20	45	11	D21
GND	44	10	GND
D22	43	9	D23
GND	42	8	AFI0
D24	41	7	D25
GND	40	6	GND
D26	39	5	D27
GND	38	4	GND
D28	37	3	D29
GND	36	2	GND
D30	35	1	D31

Table 2-1: Connector CN1 Pin Assignment

Signal Descriptions

Below are the signal descriptions for the SCSI-VHDCI and SMB connectors:

Pin Number	Signal Name	Signal Type	Direction	Description
25, 27, 29, 31, 59, 61, 63, 65	D0 – D7	Data	I/O	Port_A bi-directional digital data lines
17, 19, 21, 23, 51, 53, 55, 57	D8 – D15	Data	I/O	Port_B bi-directional digital data lines
9, 11, 13, 15, 43, 45, 47, 49	D16 – D23	Data	I/O	Port_C bi-directional digital data lines
1, 3, 5, 7, 35, 37, 39, 41	D24 – D31	Data	I/O	Port_D bi-directional digital data lines
8, 26, 30, 52, 60, 64	AFI0 – AFI5	Control /Data	I/O	Application Function I/O, can be configured as the following control signals: ▶ I^2C/ SPI ▶ Handshaking signal ▶ External trigger in/out ▶ Event out
33	AFI6	Control /Data	I/O	Application Function I/O, can be configured as the following control signals: ▶ Handshaking signal ▶ External trigger in/out ▶ Event out ▶ DO sampled clock in/out
67	AFI7	Control /Data	I/O	Application Function I/O, can be configured as the following control signals: ▶ Handshaking signal ▶ External trigger in/out ▶ Event out ▶ DI sampled clock in/out
2, 4,6, 10, 12, 14, 16, 18,20, 22, 24, 28, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 54, 56, 58, 62, 66, 68	GND	Ground	--------	Ground reference for Data I/O and AFI I/O

Table 2-2: I/O Signal Descriptions

SMB Jack Connector Signal Description

Signal Name	Signal Type	Direction	Description
CLK IN	Clock	I	External clock input for DI/DO sampled clock from external device to the PCIe-7350
CLK OUT	Clock	O	DI/DO sampled clock exporting from the PCIe-7350 to an external device

Table 2-3: SMB Jack Connector Signal Descriptions

2.3 LED indicator

There are two LEDs on the bracket which display the I2C & SPI communication and digital I/O status of the PCIe-7350.



LED	Color	Mode
STS (Status)	Red	I^2C mode enabled
	Yellow	SPI mode enabled
ACC (Access)	Red	DI DMA operation
	Yellow	DO DMA operation
	Amber	DI & DO DMA operation

Table 2-4: LED indicator

2.4 Installing the Card

IMPORTANT Install the card driver before you install the card into your computer system. Refer to section 1.5 for driver support information.

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCI Express slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.
6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system.

Configuration

The card configuration is done on a card-by-card basis for all PCI/PCI Express cards on your system. Because configuration is controlled by the system and the software, there is no jumper setting required for base address, DMA, and interrupt IRQ. The configuration is subject to change with every boot of the system as new PCI/PCI Express® cards are added or removed.

Troubleshooting

If your system fails to boot or if you experience erratic operation with your PCI/PCI Express card in place, this is likely caused by an interrupt conflict (such as when the BIOS Setup is incorrectly configured). Refer to the BIOS documentation that came with the system for details.

2.5 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK. Check if the following items are included in the package.

- PCIe-7350 high-speed DIO card
- ADLINK All-in-One CD
- User's manual

If any of the items is damaged or missing, contact your dealer immediately.

CAUTION The card must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the card. Wear a grounded wrist strap when servicing.

2.6 Cables and Termination board

The PCIe-7350 is a high-speed digital I/O card. The impedance matching is very important to the high-speed application for eliminate the signal reflection generated by the cable or PCB trace. The following cable and termination board is recommended to improve the signal quality during high-speed signal transfer.

DIN-68H – Termination board with one 68-pin SCSI-VHDCI connector and user selectable impedance. Refer to Appendix A for more information.

ACL-10279 – 68-pin SCSI-VHDCI cable with 50Ω impedance

SMB-SMB-1M – SMB to SMB cable, 1 M, for sample clock in/out

SMB-BNC-1M – SMB to BNC cable, 1 M, for sample clock in/out

3 Function Block and Operation Theory

The operation theory of the PCIe-7350 card is described in this chapter. These functions include high-speed digital pattern acquisition, digital pattern generation, application function I/O, and etc. The operation theory can help you understand how to configure and operate the PCIe-7350 card.

3.1 Block Diagram

There are 32-channel bi-direction high-speed digital I/O lines, 8-channel AFI (Application Function I/O) lines, and two sample clock input/output channels available on the PCIe-7350 card. All the 32-channel high-speed digital I/O lines are connected to level shifter, Fairchild FXL4245 and can be programmed as 1.8 V, 2.5 V, or 3.3 V (5 V compatible) logic levels. These channels can be also programmed as input channels for digital pattern acquisition or output channels for digital pattern generation.

The 8-channel application function I/O lines are connected to level shifter, Fairchild FXL2T245, too. These application function I/O can be programmed as I2C or SPI serial interface, handshaking interface, external digital trigger input, event output and external clock input/output with 1.8 V or 2.5 V or 3.3 V (5 compatible) logic levels by direction and logic level control of level shifter and by AFI controller implemented in FPGA.

The digital pattern acquisition/generation and corresponding flexible sample timing are controlled by ADLINK Smart Control Engine implemented by FPGA. Please refer to Figure 3-1 PCIe-7350 block diagram.

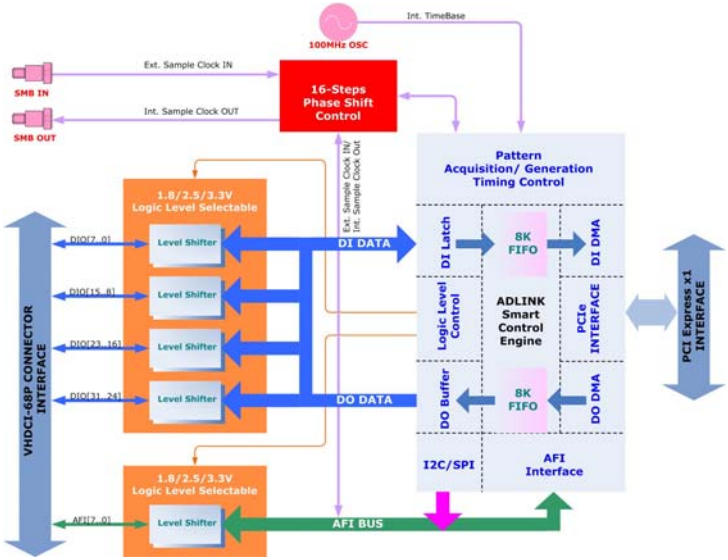


Figure 3-1: PCIe-7350 Block Diagram

3.2 Programmable Logic Level

To interface different logic level applications, the PCIe-7350 supports three software selectable logic levels of 1.8 V, 2.5 V, or 3.3 V (5 V compatible) for all digital I/O lines, sample clocks, I^2C, SPI, triggers, and events. When you choose one of these three logic levels, all the I/O lines will be at the same logic level you choose. Below are the definition and high/low range for different logic levels. When connecting PCIe-7350 to a device under test (DUT), you must ensure that the interface voltage levels are compatible.

- V_{IH}: The digital input voltage at logic high; senses a binary one (1)
- V_{IL}: The digital input voltage at logic low; senses a binary zero (0)
- V_{OH}: The digital output voltage at logic high; generates a binary one (1)
- V_{OL}: The digital output voltage at logic low; generate a binary zero (0)

Logic Levels		1.8 V	2.5 V	3.3 V (5 V compatible)
Digital Input	Min. VIH	1.2 V	1.6 V	2 V
	Max. VIL	0.63 V	0.7 V	0.8 V
Digital Output	Min. VOH	1.6 V	2.3 V	3.1 V
	Max. VOL	0.2 V	0.2 V	0.2 V

Table 3-1: PCIe-7350 Logic Levels

3.3 Digital I/O Configuration

The 32-channel high-speed digital I/O lines are bi-direction and divided into four groups. Each group contains 8 channels and can be configured as input port or output port individually. At power-up status, all the I/O lines are preset to input ports. When configuring to digital output mode, the initial status of digital outputs are in tri-state. The possible configuration modes are as follows:

Port	Channel	Power-up status	Direction
Port A	D0 ~ D7	Input	Input or output
Port B	D8 ~ D15	Input	Input or output
Port C	D16 ~ D23	Input	Input or output
Port D	D24 ~ D31	Input	Input or output

Table 3-2: PCIe-7350 High-Speed Digital I/O Configuration

3.3.1 DI Row Data Mapping

For digital pattern acquisition, the data width can be configured to 8-bit, 16-bit, 24-bit, or 32-bit and the data transfer is based on 32-bit data width. Below is the mapping table for different DI port combination.

Data Width	Input Ports				Row Data Mapping
8 bits	D	C	B	**A**	Refer to Figure 3-2
	D	C	**B**	A	Refer to Figure 3-2
	D	**C**	B	A	Refer to Figure 3-2
	D	C	B	A	Refer to Figure 3-2
16 bits	D	C	**B**	**A**	Refer to Figure 3-3
	D	**C**	B	**A**	Refer to Figure 3-3
	D	C	B	**A**	Refer to Figure 3-3
	D	**C**	**B**	A	Refer to Figure 3-3
	D	C	**B**	A	Refer to Figure 3-3
	D	**C**	B	A	Refer to Figure 3-3
24 bits	D	**C**	**B**	**A**	Refer to Figure 3-4
	D	C	**B**	**A**	Refer to Figure 3-4
	D	**C**	B	**A**	Refer to Figure 3-4
	D	**C**	**B**	A	Refer to Figure 3-4
32 bits	**D**	**C**	**B**	**A**	Refer to Figure 3-5

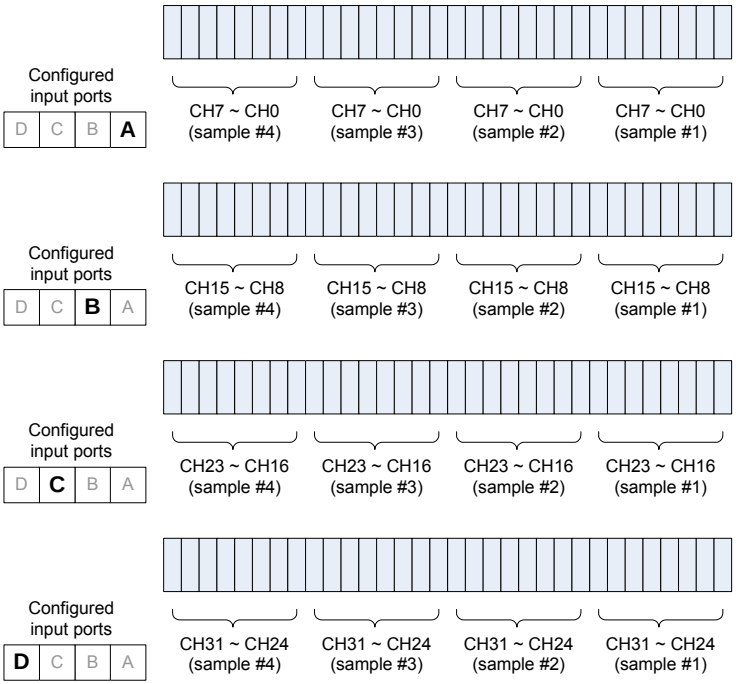


Figure 3-2: DI Row Data Mapping for 8 Bits Data Width

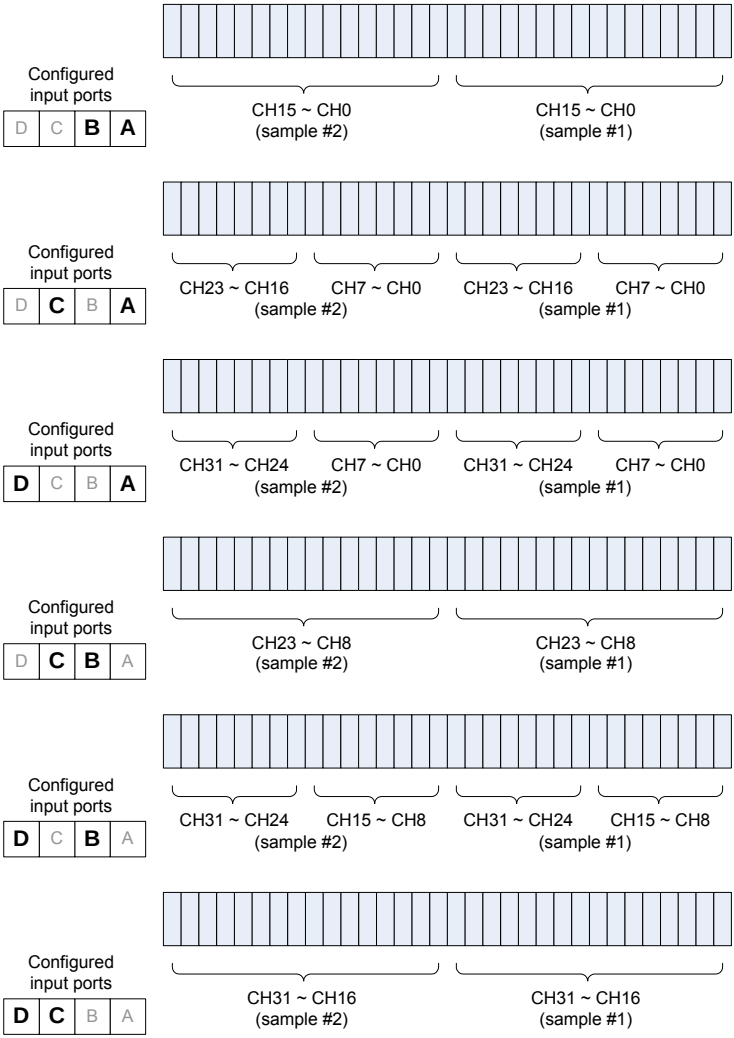


Figure 3-3: DI Row Data Mapping for 16 Bits Data Width

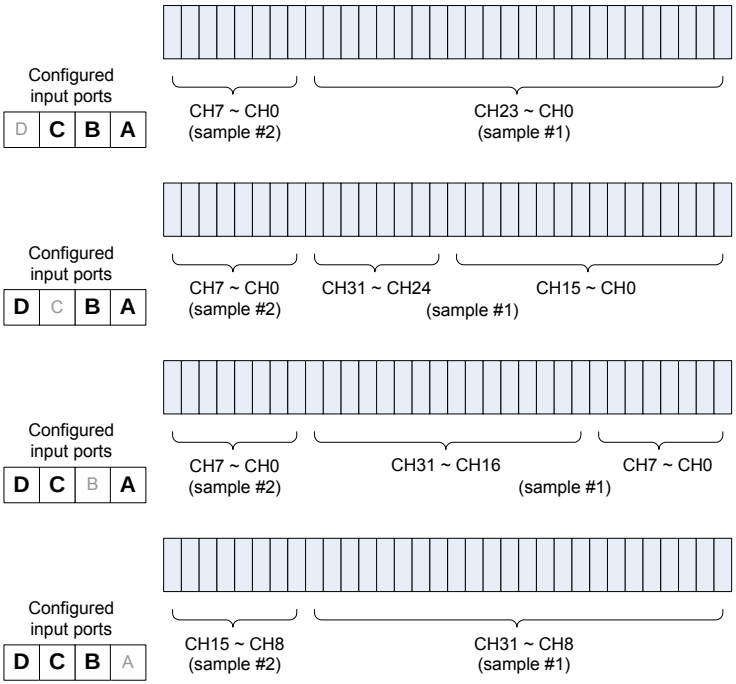


Figure 3-4: DI Row Data Mapping for 24 bits Data Width

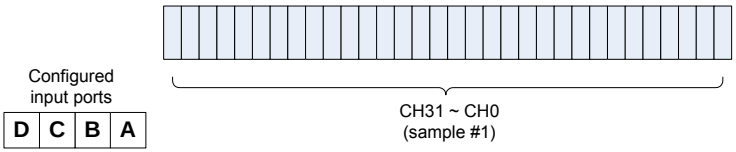


Figure 3-5: DI Row Data Mapping for 32 Bits Data Width

3.4 Phase Shift of Sample Clock

PCIe-7350 features phase shift of sample clock (on SMB connector or AFI6 & AFI7 of SCSI-VHDCI connector). The sample clock can be from external DUT or can be the exporting clock generated from internal time base. The resolution of phase shift is 4-bit (16 steps) implemented by Phase-Locked Loop (PLL) function of FPGA. In other words, the phase shift of sample clock is 22.5° x N, where N is any integer from 1 to 15. Furthermore, in phase shifting mode, the supported clock frequency is from 2 MHz to 50 MHz. This function can optimize the timing of digital pattern acquisition or generation to avoid sampling/exporting the data from/to DUT at transition state. Therefore, for digital input, the data can be sampled in clean and valid timing instead of transition timing. For digital output, it can fine tune the exporting clock to avoid the sampling of DUT at setup time or hold time instead of aligning the data.

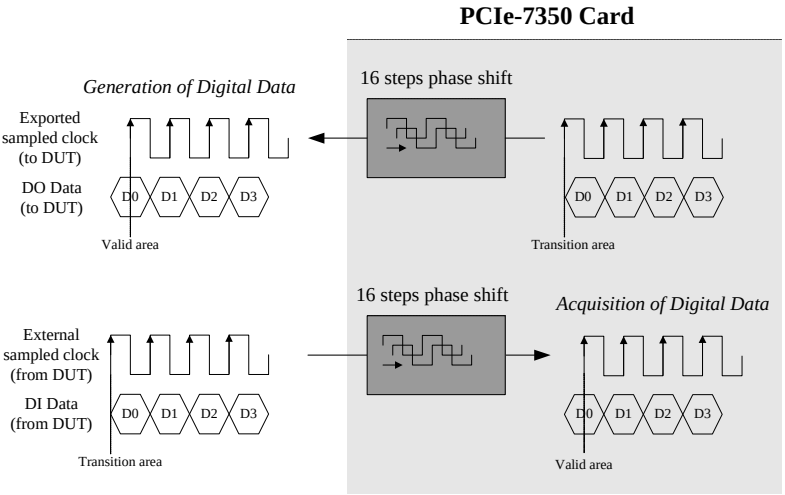


Figure 3-6: Phase Shift of Sample Clock

	Value
Revolution	16 steps (1 step = 22.5°)
Supported Frequency Range	2MHz ~ 50MHz
Supported CLK	User can shift the clock phase ofthe following clock: External DI sample clock (from SMB CLK IN or AFI7) External DO sample clock (from SMB CLK IN or AFI6) Exported DI sample clock (from SMB CLK IN or AFI7) Exported DO sample clock (from SMB CLK IN or AFI6)

Table 3-3: Phase Shift Configuration of PCIe-7350

3.5 Bus-mastering DMA Data Transfer

Digital I/O data transfer between PCIe-7350 and PC's system memory is through bus mastering DMA, which is controlled by PCIe IP Core.

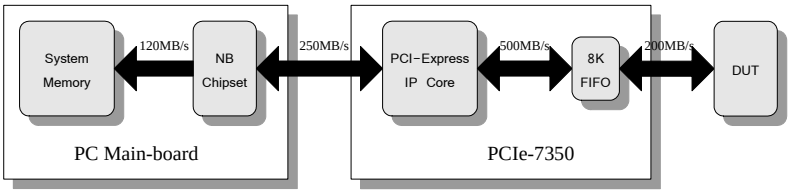


Figure 3-7: Maximum Data Throughput of the PCIe-7350

The bus-mastering controller controls the PCI/PCIe bus when it becomes the master of the bus. Bus mastering reduces the size of the on-board memory and reduces the CPU loading because data is directly transferred to the computer's memory without host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on PCI-bus. Once the analog/digital input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the on-board Data FIFO and then transfers the data to a user-defined DMA buffer memory in the computer. Please note that even when the acquired data length is less than the Data FIFO, the data will not be kept in the Data FIFO but directly transferred into host memory by the bus-mastering DMA.

The DMA transfer mode is very complex to program. We recommend using a high-level program library provided by our driver to configure this card. By using a high-level programming library for high speed DMA data acquisition, users simply need to assign the sampling period and the number of conversion into their specified counters. After the trigger condition is matched, the data will be transferred to the system memory by the bus-mastering DMA.

The PCI/PCIe controller also supports the function of scatter/gather bus mastering DMA, which helps the users to transfer large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multi-tasking OS, like Microsoft Windows, Linux, and so on, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI/PCIe controller provides the function of scatter -gather or chaining mode DMA to link the non-continuous memory blocks into a linked list so that users can transfer very large amounts of data without being limited by the fragment of small size memory. Users can configure the linked list for the input DMA channel or the output DMA channel. Figure 4.7 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI/PCIe address, PCI/PCIe dual address, a transfer size, and the pointer to the next descriptor. PCI/PCIe address and PCI/PCIe dual address support 64-bit addresses which can be mapped into more than 4GB of the address space. Users can allocate many small size memory blocks and chain their associative DMA descriptors altogether by their application programs. The software driver provides simple settings of the scatter-gather function, and some sample programs are also provided within the ADLINK all-in-one CD.

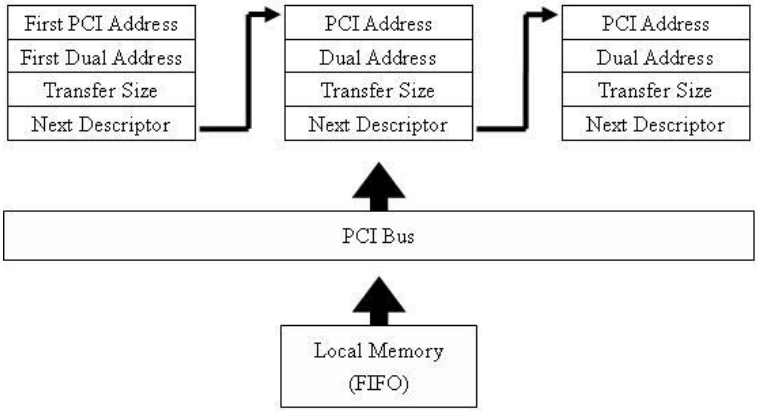


Figure 3-8: Scatter-Gather DMA for Data Transfer

Choose Finite or Continuous Operation

You can transfer data continuously to or from computer memory (continuous operation), or you can specify the number of samples you want to transfer (one-shot operation). In either case, the PCIe-7350 transfers the data using direct memory access (DMA) without occupying CPU resources.

3.6 Sample Clock

The sample clock controls the data rate of digital pattern acquisition and generation. For PCIe-7350, the sample clock can be configured from internal timer pacer or external clock through the SMB connectors or SCSI-VHDCI connector.

3.6.1 Digital Input (DI) Sample Clock

For the operation of digital pattern acquisition in continuous mode or burst handshaking mode, the PCIe-7350 card can acquire digital data from external devices at a specific sampling rate (DI sample clock). DI sample clock can be selected as the following two clock sources:

- Internal DI sample clock – the PCIe-7350 can internally generate the sample clock signal for digital data acquisition. With an internal base clock source of 100 MHz, the PCIe-7350 can generate any clock frequency of 100 MHz/n, where n is any integer from 2 to 65535.
- External DI sample clock – the PCIe-7350 can receive external clock signal from AFI7 or SMB CLK as the DI sample clock for synchronization applications.

In addition, the PCIe-7350 can also export DI sample clock to external devices through AFI7 pin or SMB CLK connector.

3.6.2 Digital Output (DO) Sample Clock

For the operation of digital pattern generation in continuous mode or burst handshaking mode, PCIe-7350 card can generate digital data to external devices at a specific update rate (DO sample clock). DO sample clock can be selected as the following two clock sources:

- Internal DO sample clock – the PCIe-7350 can internally generate the sample clock signal for digital data generation. With an internal clock source of 100MHz, the PCIe-7350 can generate any clock frequency of 100 MHz/n, where n is any integer from 2 to 65535.
- External DO sample clock – the PCIe-7350 can receive an external sample clock signal from AFI6 or SMB CLK connector as the DO sample clock for synchronization applications.

In addition, the PCIe-7350 can also export DO sample clock to external devices through AFI6 pin or SMB CLK connector. Figure 3-8 shows the DI/DO sample clock architecture of PCIe-7350.

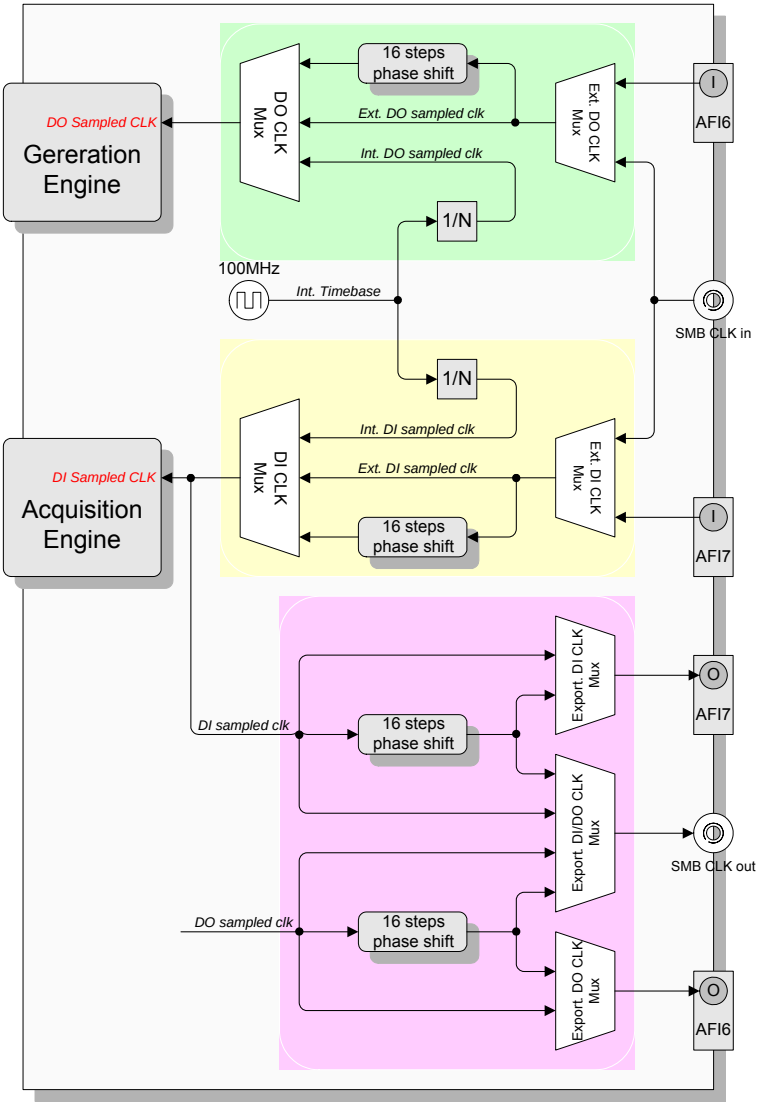


Figure 3-9: DI/DO Sample Clock Architecture

		DI Sample CLK	DO Sample CLK
Internal clock	Source	On-board 100 MHz oscillator	On-board 100 MHz oscillator
	Freq.	100 MHz/n (n = 2~65535)	100 MHz/n (n = 2~ 65535)
External clock	Source	AFI7 SMB CLK in	AFI6 SMB CLK in
	Freq.	0 – 100 MHz	0 – 100 MHz
	Freq. (phase shift)	2 MHz – 50 MHz	2 MHz – 50 MHz
Sample clock exporting	Destination	AFI7 SMB CLK out	AFI6 SMB CLK out
	Freq.	0 – 50 MHz	0 – 50 MHz
	Freq. (phase shift)	2 MHz – 50 MHz	2 MHz – 50 MHz

Table 3-4: DI/DO Sample Clock Configuration of the PCIe-7350

3.7 Operation Mode

The PCIe-7350 supports four different modes for acquisition and generation operation, including software polling, continuous, handshaking, and burst handshaking mode..

3.7.1 Polling Mode (Single Read/Write)

The PCIe-7350 supports a software polling mode to read or write a single chunk of data via a software command. That is, the 32-bit high-speed I/O lines can be used as a static I/O. The data width can be 8-bit, 16-bit, 24bit, or 32-bit.

3.7.2 DI DMA in Continuous Mode

For the DI pattern acquisition operation in continuous mode, PCIe-7350 card can acquire input data from external devices at a specific sampling clock rate (DI sampled clock). DI sample clock can be selected from internal or external clock source. The operation sequences are listed as follows:

Steps:

- Define DI port configuration (32/24/16/8-bits data width)
- Define DI logic level configuration (3.3/2.5/1.8 V)
- Define DI sample clock configuration (internal/external)
  - If choose internal sampled clock, you can define sampling clock rate to be 100MHz/n (n = 2~65535)
  - If choose external sampled clock, the phase shift function is available when external clock is a free-running clock (not a strobe signal) and external clock rate is from 2 MHz ~ 50 MHz.
- Define DI starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DI-Start) from AFI0 ~ AFI7.
- Define DI data count
- Execute DI DMA Read Command (continuous mode)

The operation architecture of DI DMA in continuous mode is shown as below:

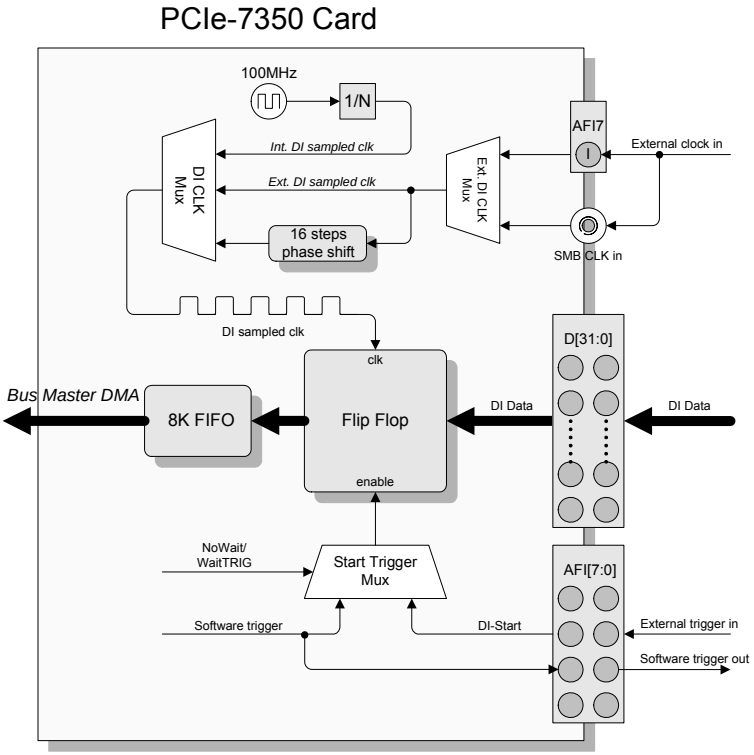
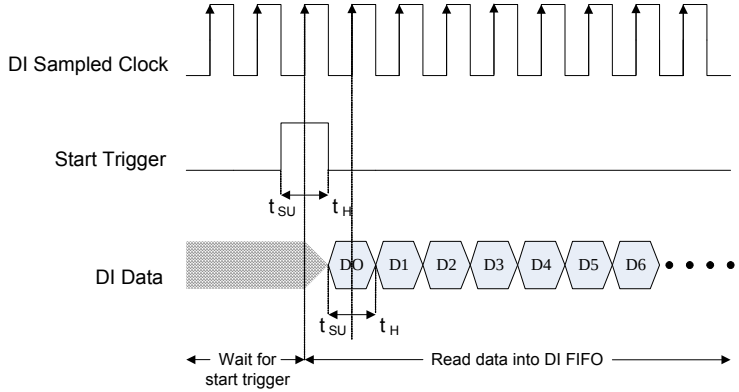


Figure 3-10: DI Continuous Mode Architecture

The timing diagram of DI DMA in continuous mode is shown as below:



t_{SU} = Maximum required setup time

t_H = Maximum required hold time

Figure 3-11: DI Timing Diagram

Note: In the continuous mode of DI pattern acquisition, the input data will be stored in the DI FIFO of the PCIe-7350. The data then transfer to system memory by bus mastering DMA if PCIe bus is available. If the speed of translation from external device to the DI FIFO on board is higher than that from DI FIFO to system memory or the PCIe bus is busy for a long time, the DI FIFO become full and the DI pattern acquisition controller will stop to write data into DI FIFO until the DI FIFO is not full. So the data will be lost when the DI FIFO is full.

3.7.3 DO DMA in Continuous Mode

For the DO pattern generation operation in continuous mode, PCIe-7350 card can generate digital data to external devices at a specific update clock rate (DO sample clock). DO sample clock can be selected from internal or external clock source. The operation sequences are listed as follows:

Steps:

- Define DO port configuration (32/24/16/8-bits data width)
- Define DO logic level configuration (3.3/2.5/1.8 V)
- Define DO sample clock configuration (internal/external)
  - If choose internal sample clock, you can define sampling clock rate to be 100MHz/n (n = 2~65535)
  - If choose external sample clock, the phase shift function is available when external clock rate is 2MHz ~ 50MHz.
- Define DO exporting sample clock configuration (AFI6/SMB CLK out)
  - PCIe-7350 can also export DO sample clock to external devices. The destination of DO sample clock exporting can be AFI6 or SMB CLK out connector.
  - The phase shift function is available when exported clock is a free-running clock and the clock rate is 2MHz ~ 50MHz.
- Define DO starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DO-Start) from AFI0 ~ AFI7.
- Define DO data count.
- Execute DO DMA Write Command (continuous mode)

The operation architecture of DO DMA in continuous mode is shown as below:

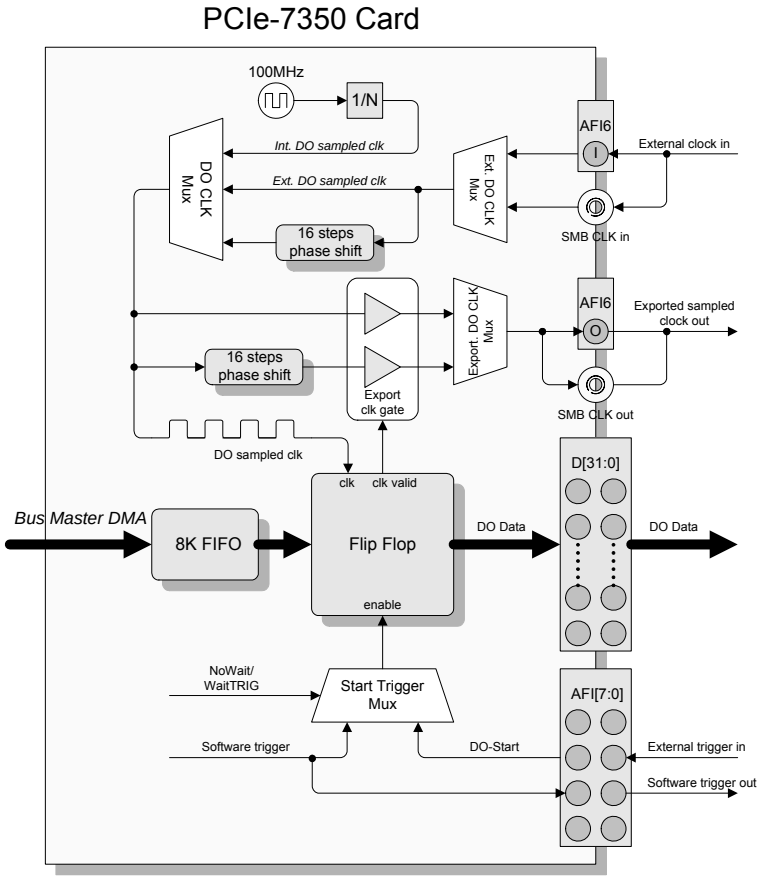
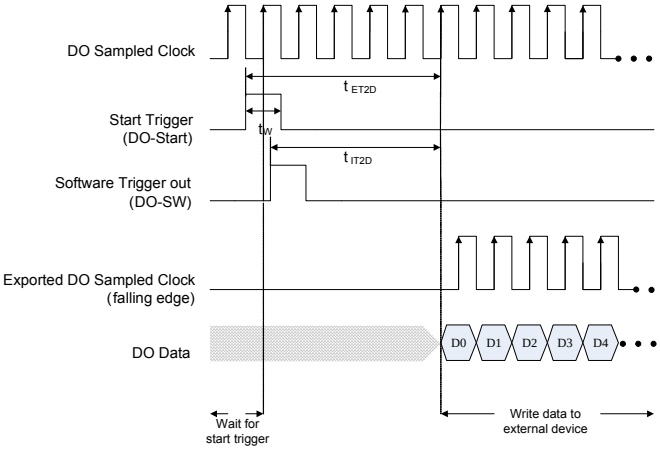


Figure 3-12: DO Continuous Mode Architecture

The timing diagram of DO DMA in continuous mode is shown as below:



t_W = Minimum detectable trigger width

t_{ET2D} = Delay from external trigger to do data out (about 5 cycle)

t_{IT2D} = Delay from software trigger out to do data out (about 4 cycle)

Figure 3-13: DO Timing Diagram

3.7.4 DI DMA in Handshaking Mode

For the DI pattern acquisition operation in handshaking mode, PCIe-7350 card can acquire input data from external devices by handshaking data transfer through DI-REQ input signal and DI-ACK output signal of AFI interface. The operation sequences are listed as follows:

Step1: Configuration

- Define DI port configuration (32/24/16/8-bits data width)
- Define DI logic level configuration (3.3/2.5/1.8V)
- Define DI-REQ and DI-ACK signal (AFI0 ~ AFI7)
  - For example: if configure AFI3 as DI-REQ and AFI4 as DI-ACK, and then you must connect the handshaking signal (DI-REQ and DI-ACK) of external device to the AFI3 and AFI4.
- Define DI starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DI-Start or DI-TRIG) from AFI0 ~ AFI7.
- Define DI data count

Step2: Execute DI DMA Read Command (handshaking mode)

- After DI data is ready on device side, the peripheral device strobe data into the PCIe-7350 by asserting a DI-REQ signal. (action_1)
- The DI-REQ signal caused the PCIe-7350 to latch DI data and store it into DI FIFO. (action_2)
- The PCIe-7350 asserts a DI-ACK signal when it is ready for another input. (action_3)
  - The action_1 to action_3 is repeated in handshaking mode.
- The DI data in the DI FIFO will be transferred into system memory directly and automatically by bus mastering DMA.

The operation architecture of DI DMA in handshaking mode is shown as below:

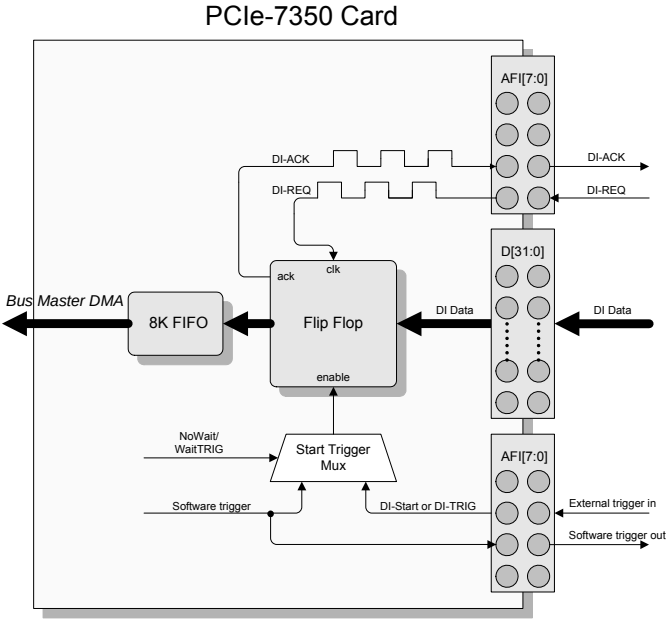
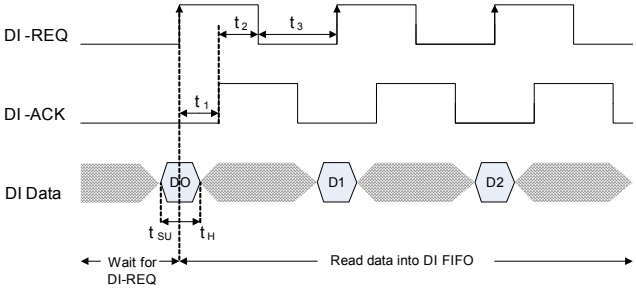


Figure 3-14: DI Handshaking Mode Architecture

The timing diagram of DI DMA in handshaking mode is shown as below:



t_{SU} = Maximum required setup time

t_H = Maximum required hold time

t_1 ≥ 20 ns

t_2 ≥ 10 ns

t_3 ≥ 50 ns

Figure 3-15: DI Handshaking Timing Diagram

3.7.5 DO DMA in Handshaking Mode

For the DO pattern generation operation in handshaking mode, PCIe-7350 card can generate output data to external devices by handshaking data transfer through DO-REQ output signal and DO-ACK input signal of AFI interface. The operation sequences are listed as follows:

Step1: Configuration

- Define DO port configuration (32/24/16/8-bits data width)
- Define DO logic level configuration (3.3/2.5/1.8V)
- Define DO-REQ and DO-ACK signal (AFI0 ~ AFI7)
  - For example: if configure AFI3 as DO-REQ and AFI4 as DO-ACK, and then you must connect the handshaking signal (DO-REQ and DO-ACK) of external device to the AFI3 and AFI4.
- Define DO starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DO-Start or DO-TRIG) from AFI0 ~ AFI7.
- Define DO write count

Step2: Execute DO DMA Write Command (handshaking mode)

- The DO data saved in the system memory will be transferred to DO FIFO directly and automatically by bus mastering DMA.
- After DO data are ready, DO-REQ signal is generated and DO data are sent to the external device. (action_1)
- After DO-ACK signal from external device is gotten (action_2)
  - The action_1 to action_2 is repeated in handshaking mode.

The operation architecture of DO DMA in handshaking mode is shown as below:

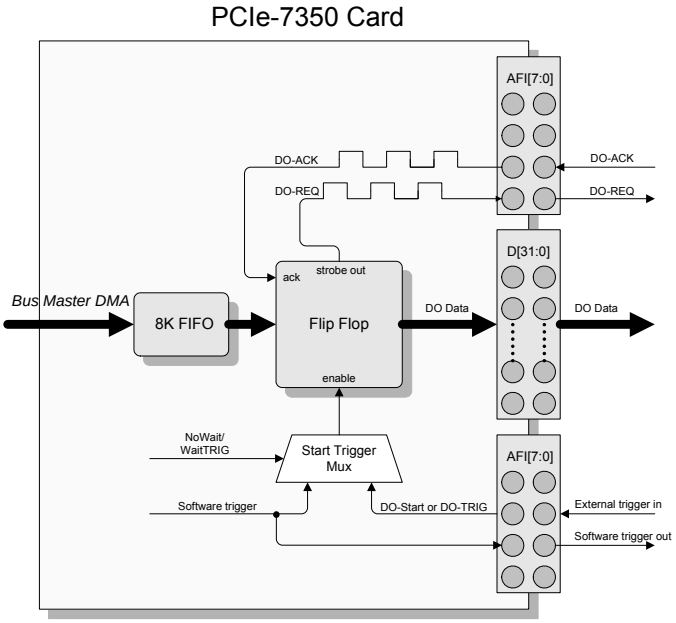
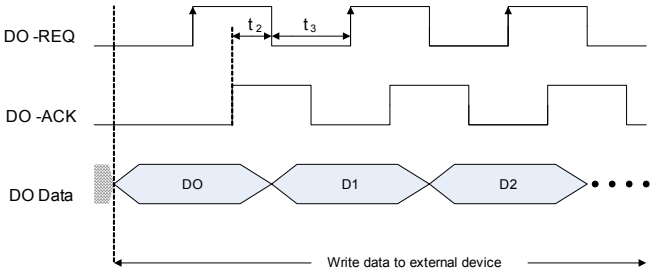


Figure 3-16: DO Handshaking Mode Architecture

The timing diagram of DO DMA in handshaking mode is shown as below:



t_2 ≥ 40 ns

t_3 ≥ 50 ns

Figure 3-17: DO Handshaking Timing Diagram

3.7.6 DI DMA in Burst Handshaking Mode

The burst handshaking mode is a fast and reliable data transfer protocol. It has both advantage of handshaking mode and continuous mode.

In DI burst handshaking mode, DI-REQ signal will be active by external device when it is ready to send DI data and sample clock. And then DI-ACK signal will be generated by PCIe-7350 when it is ready to receive DI data from external device.

External device should start to send DI data after it detect DI-ACK signal is active. DI data transfer between PCIe-7350 and external device should be continued when both DI-REQ and DI-ACK are active. When DI FIFO of PCIe-7350 becomes almost full, DI-ACK signal will be inactive. External device should stop to send DI data and sample clock after it detects DI-ACK signal inactive. The operation sequences are listed as follows:

Step1: Configuration

- Define DI port configuration (32/24/16/8-bits data width)
- Define DI logic level configuration (3.3/2.5/1.8 V)
- Define DI sample clock configuration (only external)
  - The phase shift function is available when external clock is a free-running clock (not a strobe signal) and external clock rate is from 2 MHz – 50 MHz.
- Define DI-REQ and DI-ACK signal (AFI0 ~ AFI7)
  - For example: if configure AFI3 as DI-REQ and AFI4 as DI-ACK, and then you must connect the handshaking signal (DI-REQ and DI-ACK) of external device to the AFI3 and AFI4.
- Define DI starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DI-Start or DI-TRIG) from AFI0 ~ AFI7.
- Define DI data count

Step2: Execute DI DMA Read Command (burst handshaking mode)

- PCIe-7350 will generate DI-ACK signal when it is ready to receive DI data after DI-REQ signal is active.
- External device starts to send DI data and DI sample clock after DI-ACK signal is active.
- PCIe-7350 starts to receive DI data and DI sample clock from external device when DI-REQ and DI-ACK are all active.
- The DI data in the DI FIFO will be transferred into system memory directly and automatically by bus mastering DMA.

The operation architecture of DI DMA in burst handshaking mode is shown as below:

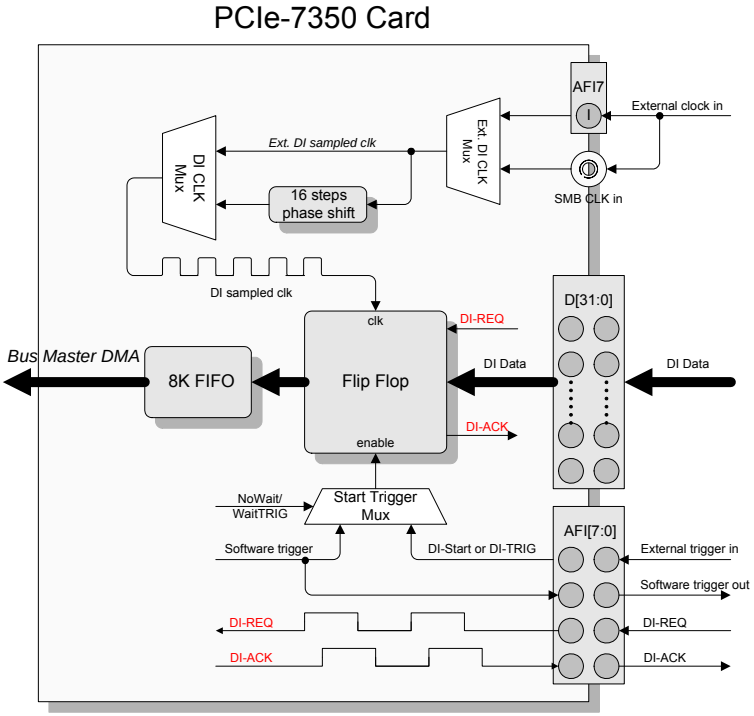


Figure 3-18: DI Burst Handshaking Mode Architecture

The timing diagram of DI DMA in burst handshaking mode is shown as below:

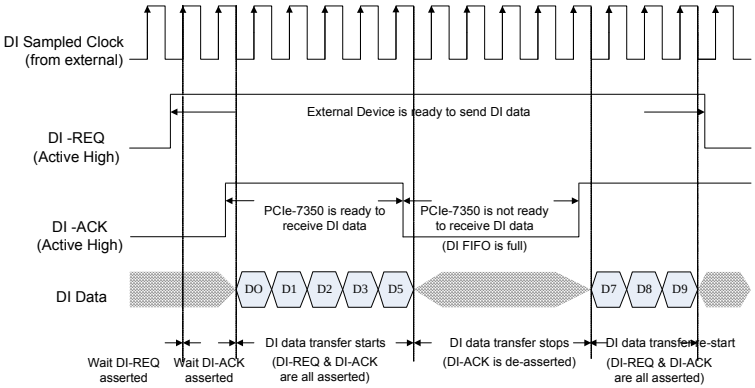


Figure 3-19: DI Burst Handshaking Timing Diagram

3.7.7 DO DMA in Burst Handshaking Mode

In DO burst handshaking mode, DO-REQ signal will be active by PCIe-7350 when it is ready to send out DO data. And then DO-ACK signal should be generated by external device when it is ready to receive DO data. Once DO-ACK is active, external device has to keep DO-ACK active until its input buffer is almost full. The operation sequences are listed as follows:

Step1: Configuration

- Define DO port configuration (32/24/16/8-bits data width)
- Define DO logic level configuration (3.3/2.5/1.8 V)
- Define DO sample clock configuration (internal/external)
  - If choose internal sampled clock, you can define sampling clock rate to be 100 MHz/n (n = 2-65535)
  - If choose external sampled clock, the phase shift function is available when external clock rate is from 2 MHz - 50 MHz.
- Define DO exporting sample clock configuration (AFI6/SMB CLK out)
  - The PCIe-7350 can also export DO sampled clock to external devices. The destination of the exported DO sampled clock can be AFI6 or SMB CLK out connector.
  - The phase shift function is available when exported clock rate is from 2 MHz – 50 MHz.
- Define DO-REQ and DO-ACK signal (AFI0 - AFI7)
  - For example: if configure AFI3 as DO-REQ and AFI4 as DO-ACK, and then you must connect the handshaking signal (DO-REQ and DO-ACK) of external device to the AFI3 and AFI4.
- Define DO starting mode configuration (NoWait or WaitTRIG)
  - If choose WaitTRIG, you can define start trigger source to be software trigger or external trigger (DO-Start or DO-TRIG) from AFI0 - AFI7.
- Define DO data count

Step2: Execute DO DMA Write Command (burst handshaking mode)

- The DO data saved in the system memory will be transferred to DO FIFO directly and automatically by bus mastering DMA.
- After DO data are ready, DO-REQ signal is asserted.
- PCIe-7350 start to send DO data and DO sampled clock to external device after DO-ACK signal is asserted.
- If input buffer of external device has no much space for new DO data, DO-ACK signal will be inactive and PCIe-7350 will be only allowed to send 4 more data to the receiver.
- If DO data are not ready (DO FIFO is empty), DO-REQ signal will be inactive and PCIe-7350 stops to send DO data and DO sample clock until DO data are ready again.

The operation architecture of DO DMA in burst handshaking mode is shown as below:

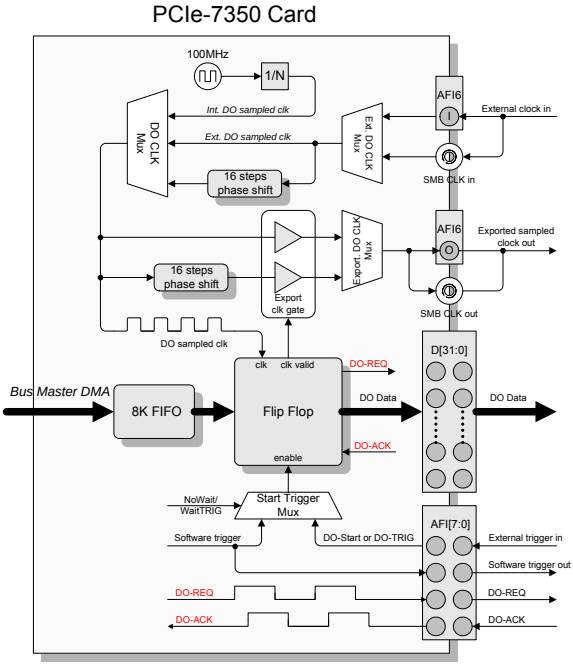


Figure 3-20: DO Burst Handshaking Mode Architecture

The timing diagram of DO DMA in burst handshaking mode is shown as below:

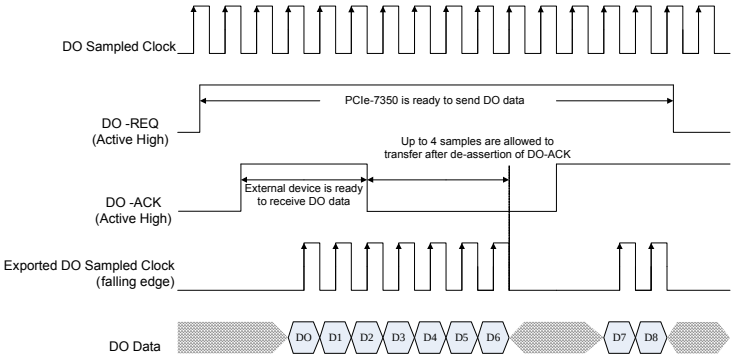


Figure 3-21: DO Burst Handshaking Timing Diagram

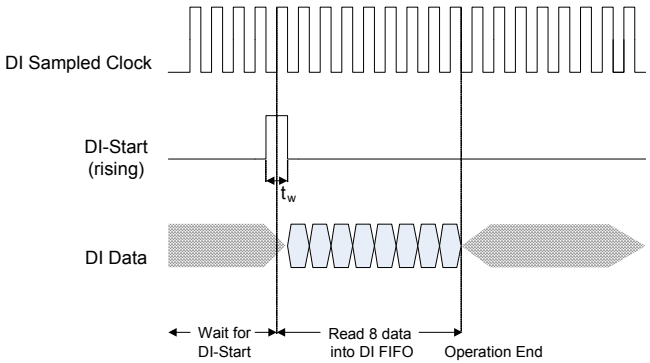
3.8 Trigger Source and Trigger Mode

The PCIe-7350 supports 2 trigger sources, software command trigger and external digital trigger, to start or pause the DI or DO operation. In addition, the PCIe-7350 supports 3 trigger modes, including post trigger, gated trigger, and post trigger with re-trigger. In post trigger mode and post trigger with re-trigger mode, the polarity of digital trigger signal can be configured to rising edge or falling edge. In gated trigger mode, the level of trigger signal will start or pause the operation of digital pattern acquisition or generation. Below are the examples of these trigger conditions.

[Example 1] External digital trigger with post trigger mode

DI data Count: 8 samples

Trigger Event: DI-Start (rising edge)



t_w = Minimum required pulse width time

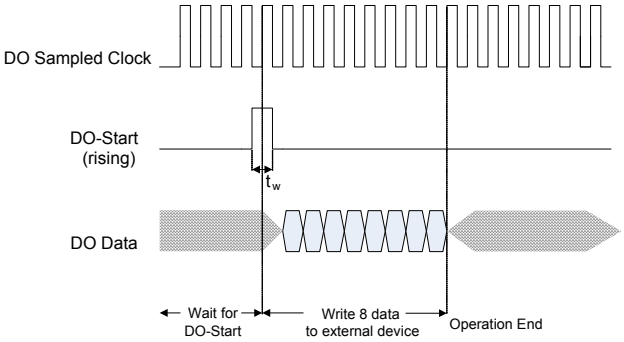
Figure 3-22: DI Post Trigger

[Example 2] External digital trigger with post trigger

DO data Count: 8 samples

Trigger Event: DO-Start (rising edge)

Re-Trigger Count: 3



t_w = Minimum required pulse width time

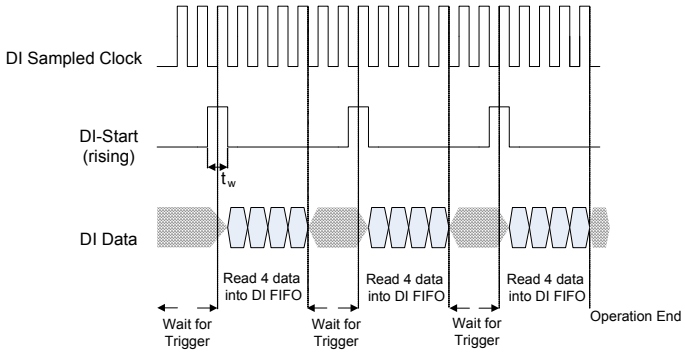
Figure 3-23: DO Post Trigger

[Example 3] External digital trigger with post trigger and re-trigger

DI data Count: 4 samples per trigger

Trigger Event: DI-Start (rising edge)

Re-Trigger Count: 3



t_w = Minimum required pulse width time

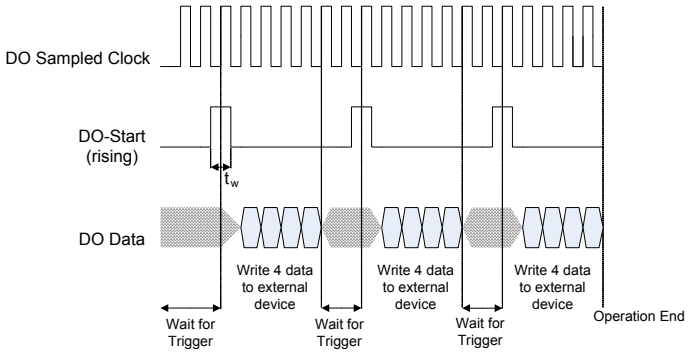
Figure 3-24: DI Post Trigger with Re-trigger

[Example 4] External digital trigger with post trigger and re-trigger

DO data Count: 4 samples per trigger

Trigger Event: DO-Start (rising edge)

Re-Trigger Count: 3



t_w = Minimum required pulse width time

Figure 3-25: DO Post Trigger with Re-Trigger

[Example 5] External digital trigger with gated trigger

DI data Count: 12 samples

Trigger Event: DI-Pause (logic high)

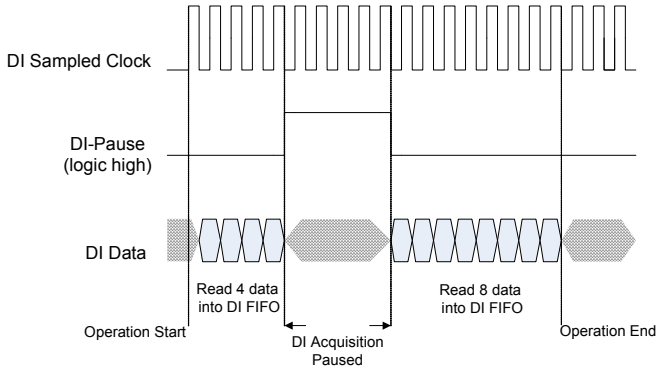


Figure 3-26: DI Gated Trigger

[Example 6] External digital trigger with gated trigger

DO data Count: 12 samples

Trigger Event: DO-Pause (logic high)

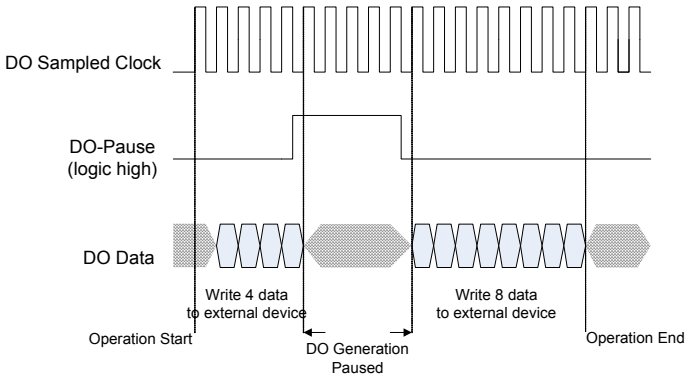


Figure 3-27: DO Gated Trigger

3.9 Application Function I/O

PCIe-7350 features eight AFI (Application Function I/O) lines. These bi-direction digital I/O lines allow you to route I2C, SPI, trigger, event, handshaking, and clock signals to/from the SCSI-VHDCI I/O connector. The following table lists the supporting functions of AFI lines and the corresponding pin out.

Function	Signal	I/O	AFI0	AFI1	AFI2	AFI3	AFI4	AFI5	AFI6	AFI7
I^2C Master	SCL	O	●							
	SDA	I/O		●						
SPI Master	SCLK	O	●							
	SDO	O		●						
	SDI	I			●					
	CS_0	O				●				
	CS_1	O					●			
	CS_2	O						●		
External Trigger in	DI-Start	I	●	●	●	●	●	●	●	●
	DO-Start	I	●	●	●	●	●	●	●	●
	DI-Pause	I	●	●	●	●	●	●	●	●
	DO-Pause	I	●	●	●	●	●	●	●	●
Trigger out	DI_SW	O	●	●	●	●	●	●	●	●
	DO_SW	O	●	●	●	●	●	●	●	●
Event	PM	O	●	●	●	●	●	●	●	●
	COS	O	●	●	●	●	●	●	●	●
Handshake	DI-REQ	I	●	●	●	●	●	●	●	●
	DI-ACK	O	●	●	●	●	●	●	●	●
	DI-TRIG	I	●	●	●	●	●	●	●	●
	DO-REQ	O	●	●	●	●	●	●	●	●
	DO-ACK	I	●	●	●	●	●	●	●	●
	DO-TRIG	I	●	●	●	●	●	●	●	●
Clock	DO-SCLK	I/O							●	
	DI-SCLK	I/O								●

Table 3-5: PCIe-7350 AFI I/O Configuration

Function	Signal	I/O	Description
I^2C Master	**SCL**	**O**	**I^2C Clock**– I^2C clock signal to slave device capable of clock rate up to 1953.125KHz.
	SDA	**I/O**	**I^2C Serial Data**– Data signal for I^2C read/ write communication.
SPI Master	**SCK**	**O**	**SPI Clock**– SPI clock signal to slave device capable of clock rate up to 62.5MHz.
	SDI	**I**	**Master Input Slave Output**– Data signal for SPI read communication.
	SDO	**O**	**Master Output Slave Input**– Data signal for SPI write communication.
	CS_0	**O**	**Chip Select of Slave Device 0**– Output signal to select the desired SPI slave device 0.
	CS_1	**O**	**Chip Select of Slave Device 1**– Output signal to select the desired SPI slave device 1.
	CS_2	**O**	**Chip Select of Slave Device 2**– Output signal to select the desired SPI slave device 2.
External Trigger in	**DI-Start**	**I**	**DI Start Trigger in**– External digital trigger signal to begin an acquisition operation.
	DO-Start	**I**	**DO Start Trigger in**– External digital trigger signal to begin a generation operation.
	DI-Pause	**I**	**DI Gate Trigger in**– External digital signal to start/pause an acquisition operation.
	DO-Pause	**I**	**DO Gate Trigger in**– External digital signal to start/pause a generation operation.
Trigger out	**DI_SW**	**O**	**DI Trigger out**– A pulse signal output generated by PCIe-7350 when receiving a software start command of DI.
	DO_SW	**O**	**DO Trigger out**– A pulse signal output generated by PCIe-7350 when receiving a software start command of DO.

Table 3-6: PCIe-7350 AFI Signal Description

Function	Signal	I/O	Description
Event	PM	O	**Pattern Match Event**– A pulse signal output to indicate the event of pattern match of user-defined data lines.
	COS	O	**Change Detection Event**– A pulse signal output to indicate the change detection of any user-defined data lines.
Handshake	DI-REQ	I	**Digital Input Reques**– In handshaking mode for DI pattern acquisition, DI-REQ carries handshaking control information from DUT to PCIe-7350.
	DI-ACK	O	**Digital Input Acknowledge**– In handshaking mode for DI pattern acquisition, DI-ACK carries handshaking status information from PCIe-7350 to DUT.
	DI-TRIG	I	**Digital Input Trigger**– In handshaking mode for DI pattern acquisition, DI-TRIG can be used to start the operation.
	DO-REQ	O	**Digital Output Request**– In handshaking mode for DO pattern generation, DO-REQ carries handshaking control information from PCIe-7350 to DUT.
	DO-ACK	I	**Digital Output Acknowledge**– In handshaking mode for DO pattern generation, DO-ACK carries handshaking status information from DUT to PCIe-7350.
	DO-TRIG	I	**Digital Output Trigger**– In handshaking mode for DO pattern generation, DO-TRIG can be used to start the operation.

Table 3-6: PCIe-7350 AFI Signal Description

Function	Signal	I/O	Description
Clock	DI-SCLK	I/O	**External DI Sampled Clock in**– In free-running mode or burst handshaking mode, PCIe-7350 can receive external sampled clock from DUT for acquisition by DI-SCLK. **Export DI Sampled Clock out**– In free-running mode or burst handshaking mode, PCIe-7350 can export sampled clock of acquisition to DUT by DI-SCLK.
	DO-SCLK	I/O	**External DO Sample Clock in**– In continuous mode or burst handshaking mode, PCIe-7350 can receive external sampled clock from DUT for generation by DO-SCLK. **Export DO Sample Clock out**– In continuous mode or burst handshaking mode, PCIe-7350 can export sample clock of generation to DUT by DO-SCLK.

Table 3-6: PCIe-7350 AFI Signal Description

3.9.1 I²C Master

PCIe-7350's application function I/O (AFI) can be configured as I2C node for communicating with peripheral devices through PCIe-7350's built-in I²C master protocol and provided Windows API directly. Along with I²C master of PCIe-7350, users can easily communicate with ADC/ Microcontroller/ EEPROM/ image sensor for initializing and programming.

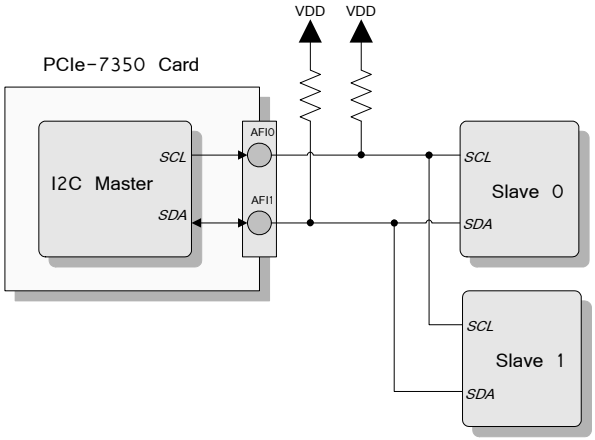


Figure 3-28: I2C Master of PCIe-7350

The I²C master of the PCIe-7350 provides at most 8 bytes data width -- 4 bytes address/ command and 4 bytes data. A basic I²C command is consisted of at least two parts: slave address (with Read/Write bit) and one or more types of data bytes (Command, Address or Data). Figure 3-29 shows the data transfer on the I²C bus.

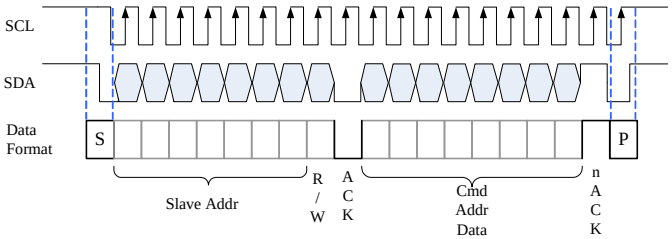
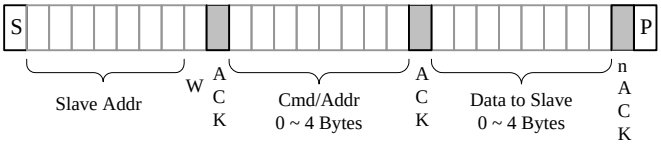


Figure 3-29: Data Transfer on the I²C Bus

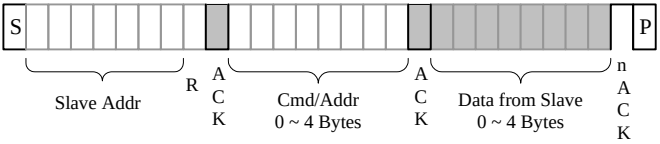
I²C master of PCIe-7350 supports the clock range from 1.9 kHz to 244.14 kHz. After issuing command to I²C slave device, the clock rate might be changed according the request from I²C slave. The below formula is to calculate the I²C clock rate.

F_{scl} = 488.28 / (Clk Pre-scale + 1) (kHz),
where Clk Pre-scale = 1~255

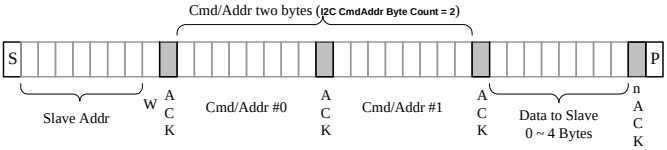
I²C Write Command: the content of Cmd/Addr and Data are stored in registers I²C_A_CA and I²C_A_DAT and their byte counts are indicated by I²C CmdAddr Byte Count and Access Byte Count, respectively.



I²C Read Command: the format of Read command is similar with a write command except that the data part is derived by slave device.



I²C Cmd/Addr Count is less than 4 byte:



I²C Data Count is less than 4 byte:

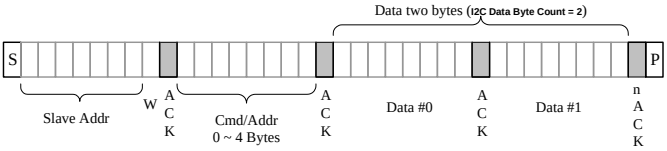


Figure 3-30: I²C Data Format

3.9.2 SPI Master

PCIe-7350's application function I/O (AFI) can be configured as SPI node for user to communicate with peripheral devices through PCIe-7350's built-in SPI master protocol and provided API directly. Along with SPI master of PCIe-7350, user can easily communicate with ADC/ Microcontroller/ EEPROM/ image sensor for initializing and programming.

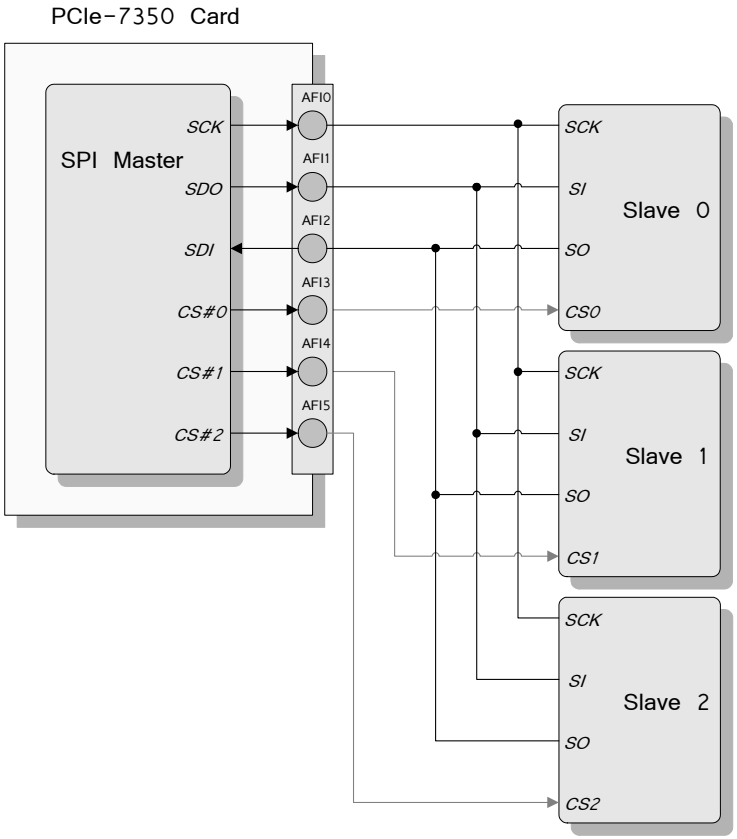


Figure 3-31: SPI Master of PCIe-7350

SPI master of PCIe-7350 provide at most 64 bits -- 32 bits address/ command and 32 bits data. SPI master of PCIe-7350 supports only three slave devices. Figure 3-32 shows the data transfer on SPI bus.

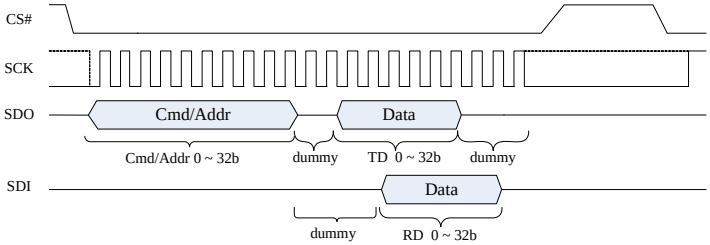


Figure 3-32: Data Transfer on SPI Bus

SPI master of PCIe-7350 supports clock frequency range from 244.14 kHz to 62.5 MHz. After issuing command to SPI slave device, the clock rate might be changed according the request from SPI slave. The below formula is to calculate the SPI clock rate.

Fscl = 62.5 / (Clk Pre-scale + 1) (MHz),
where Clk Pre-scale=0~255

SPI master of PCIe-7350 supports two different modes of SCK. Figure 3-11 shows the clock mode 0 and clock mode 1 of SCK.

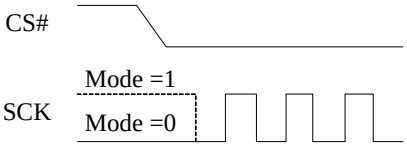


Figure 3-33: Clock Mode of SCK

3.9.3 External Digital Trigger

PCIe-7350 supports external digital trigger mode to start or pause an acquisition or generation operation. PCIe-7350 supports two trigger sources, internal software trigger and external digital trigger. The digital pattern acquisition or generation will start upon a software command or an external digital trigger signal to start or pause the process. The PCIe-7350's Application Function I/O (AFI) can be configured as the external digital trigger source.

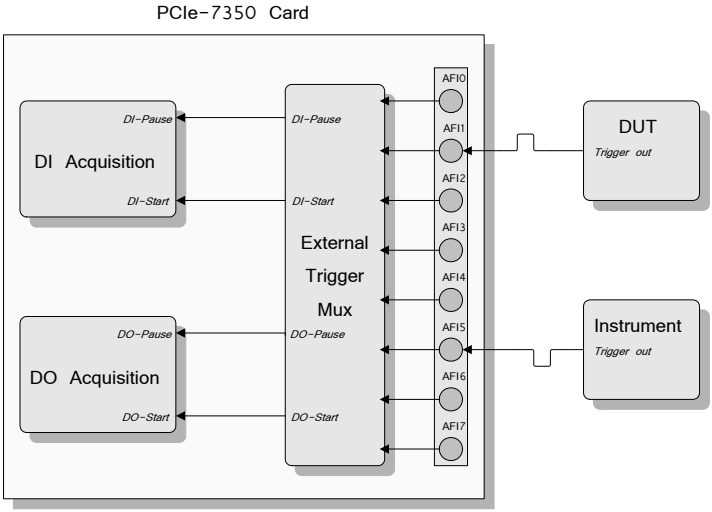


Figure 3-34: External Digital Trigger Input Configuration

3.9.4 Trigger Out

PCIe-7350's Application Function I/O (AFI) can be configured as trigger output when receiving a software start command of digital pattern acquisition or generation. The trigger out signal can synchronize the operation between PCIe-7350 and DUT.

The pulse width of trigger out signal can be configured from 8ns to 34.359738368 sec. (8 ns x N, where N is from 1 to 2^{32}-1)

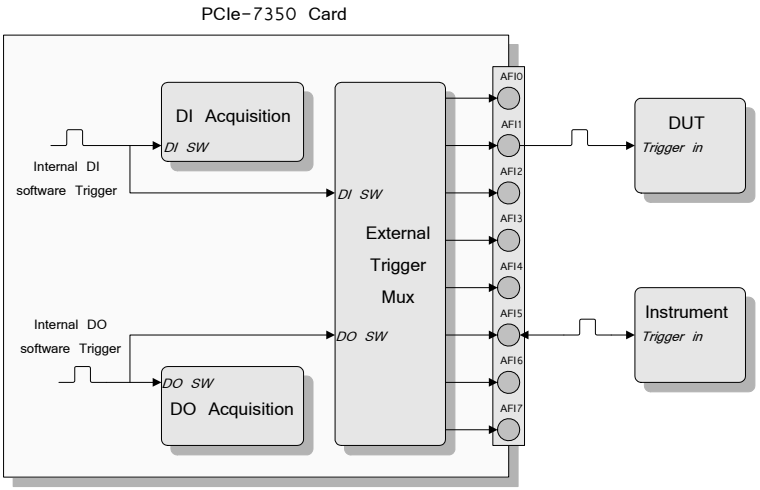


Figure 3-35: Configured AFI as Internal Software Trigger Output

3.9.5 Event Out

PCIe-7350's Application Function I/O (AFI) can be configured as event output of pattern match or COS (Change of State).

Pattern Match event is a pulse signal generated while the PCIe-7350's digital data input lines matching the pre-defined pattern. COS (Change of State) event is a pulse signal generated while the PCIe-7350 detects a change on the pre-defined data input line. The pulse width of Event Out signal can be configured from 8ns to 34.359738368 sec. (8 ns x N, where N is from 1 to 2^{32}-1)

You can export this event out signal to trigger external devices for synchronization purpose or inform external device.

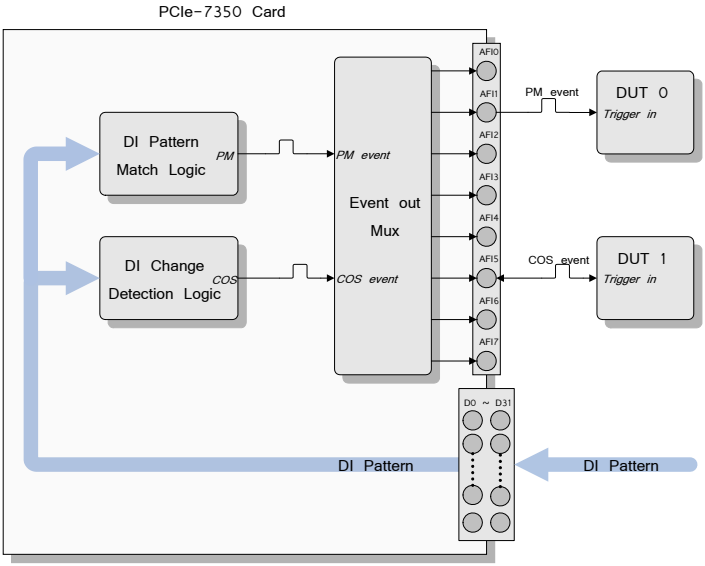


Figure 3-36: Pattern Match and COS Event Configuration

3.9.6 Handshaking

PCIe-7350's Application Function I/O (AFI) can be configured as handshaking mode (DI-REQ/DI-ACK/DI-TRIG/DO-REQ/DO-ACK/DO-TRIG) to communicate with an external device using an acknowledge signals to request and acknowledge each data transfer. The handshaking mode can ensure the data transfer without loss.

For the digital pattern acquisition using handshaking, through DI-REQ input signal from external device and DI-ACK output signal to the external device, the digital input can have simple handshaking data transfer. (Refer to section 3.7.3 to 3.7.6 for more information)

For the digital pattern generation using handshaking, through DO-REQ output signal to the external device and DO-ACK input signal from external device, the digital output can have simple handshaking data transfer.

Note: For the PCIe-7350 to communicate with peripheral devices using handshaking, verify that the DUT and the PCIe-7350 have compatible timing.

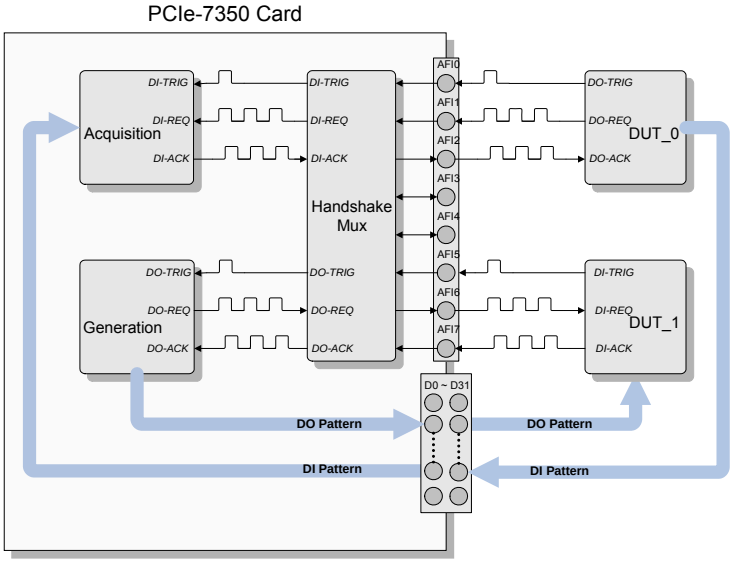


Figure 3-37: Configured AFI as Handshaking Interface

3.9.7 Sample Clock In/Out

The AFI of PCIe-7350 can be configured to sample clock in/out pin. More details, please refer to section 3.6.

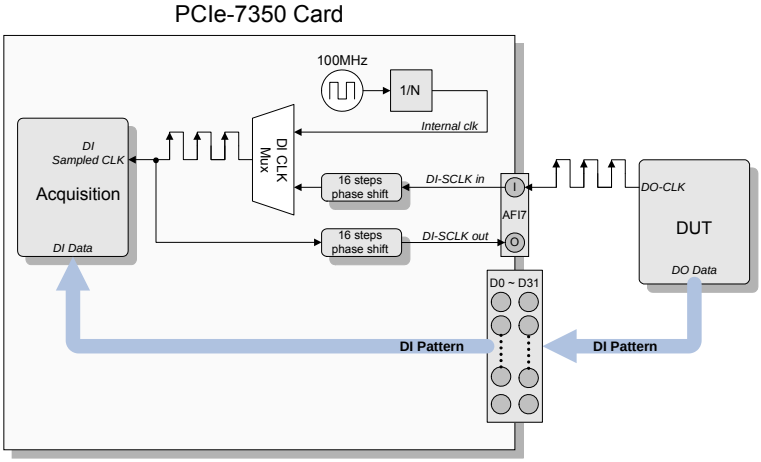


Figure 3-38: Configured AFI7 as DI Sampled Clock In/Out

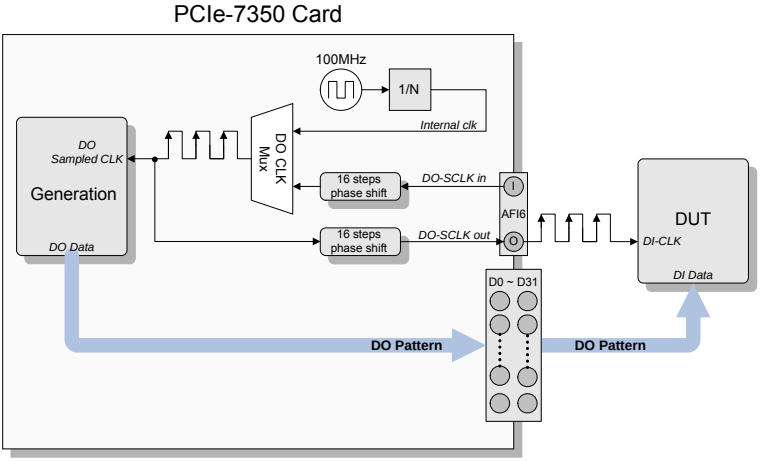


Figure 3-39: Configured AFI6 as DO Sampled Clock In/Out

3.10 Pattern Match

PCIe-7350 supports pattern match function to monitor the data input lines that conform to the user-defined pattern (for example, 10101110). When the data lines conform to the user-defined pattern, PCIe-7350 will generate a pulse signal of pattern match event to the AFI pin and generate the pattern match interrupt to host PC as well.

Below are the conditions of pattern match. The pattern match can be a single change of specific data line or a combination of different data lines.

Logic State	Description
0	Match on a logic low level at the input channel
1	Match on a logic high level at the input channel
R	Match on rising edge at the input channel
F	Match on falling edge at the input channel
X	Ignore the input channel

Table 3-7: Logic States of Pattern Match

Figure 3-39 is an example of 9 channel (CH0 – CH8) pattern match operation. All of the enabled DI channel's signal logic states will be compared with the user-defined pattern "1100RRFFX". The pattern match event and interrupt will be generated while the following conditions are all matched:

- CH0 and CH1 are logic high
- CH2 and CH3 are logic low
- CH4 and CH5 are rising edge
- CH6 and CH7 are falling edge
- CH8 is ignored

Note: For PCIe-7350, the edge detection (rising or falling) compare the currently sampled data with the previously sampled data.

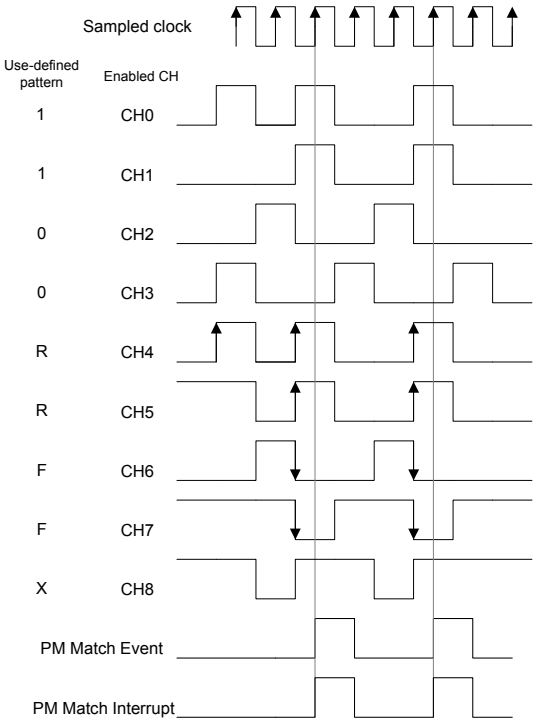


Figure 3-40: Example of Pattern Match

3.11 COS (Change of State) Event

PCIe-7350 supports COS (Change of State) Event to monitor if there is any change on the user-defined or any data lines.

When PCIe-7350 detects the change (either the input state changes from low to high or from high to low) of data input lines, PCIe-7350 will have the following response:

- Generate a pulse signal of change detection event to AFI
- Generate the change detection interrupt to host PC
- Latch the corresponding DI data into change detection latch register

In COS mode, the DI data are sampled by 125 MHz clock rate. Therefore, the pulse width of the DI data should be longer than 8ns. Otherwise, the change detection latch register won't latch the correct input data.

Figure 4-15 is an example of 8 channel change detection operation. Any level change of the enabled DI data lines will be detected and then generate the event and interrupt. The corresponding DI data will be latched into change detection register.

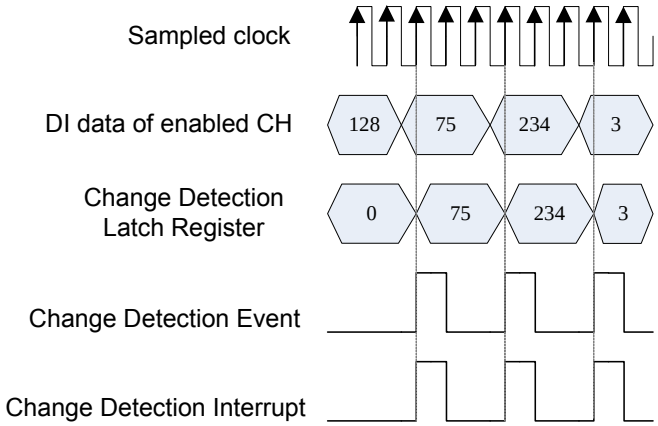


Figure 3-41: Example of Pattern Match

3.12 Termination

Proper termination is very important for applications using high-speed digital data transfer to eliminate the signal reflection caused by cables, wiring, connectors, or PCB traces and improve signal quality.

The output impedance (source impedance) of the PCIe-7350 is 50 Ω and the characteristic impedance of the SCSI-VHDCI cable is also 50 Ω. When you connect to a DUT with 50 Ω input impedance, the best impedance matching will be achieved, but the voltage level sensed by the DUT will be half of the PCI-7350's output voltage due to voltage-divider principles. You can also connect to a DUT with a high impedance (at least 1 - 100 KΩ) if precision timing and excellent signal integrity is not so critical. The voltage level sensed by the DUT will be almost the same as the output voltage of the PCIe-7350.

The input impedance of the PCIe-7350 is 10 K Ω, which is a high impedance. So with a high impedance 10 KΩ load termination, the external source impedance of DUT should match the characteristic impedance (50 Ω) of the SCSI-VHDCI cable to achieve better signal integrity and avoid signal reflection.

Appendix A ADLINK DIN-68H

The DIN-68H is a terminal board designed for PCIe-7350 to provide the easier wiring for test circuit or measure signal. Below is the layout and pin-to-pin reference table of DIN-68H:

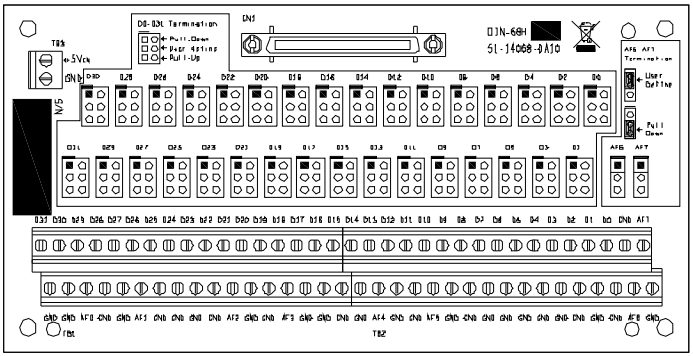


Figure A-1: DIN-68H Layout

PCIe-7350	DIO0	DIO1	DIO2	DIO3	DIO4	DIO5	DIO6	DIO7
DIN-68H	D0	D1	D2	D3	D4	D5	D6	D7

PCIe-7350	DIO8	DIO9	DIO10	DIO11	DIO12	DIO13	DIO14	DIO15
DIN-68H	D8	D9	D10	D11	D12	D13	D14	D15

PCIe-7350	DIO16	DIO17	DIO18	DIO19	DIO20	DIO21	DIO22	DIO23
DIN-68H	D16	D17	D18	D19	D20	D21	D22	D23

PCIe-7350	DIO24	DIO25	DIO26	DIO27	DIO28	DIO29	DIO30	DIO31
DIN-68H	D24	D25	D26	D27	D28	D29	D30	D31

PCIe-7350	AFI6	AFI7
DIN-68H	AF6	AF7

Table A-1: DIN-68H Pin Assignment

All jumpers on DIN-68H are used for the setting of pull-up or pull-down resistor termination. The proper termination setting can reduce signal refection during high-speed data transfer. The below diagram is the schematic of AF6, AF7, and D0 to D31. The default jumper setting of DIN-68H is set to 50Ω pull-down termination. When you change the jumper setting to 5V pull-up termination, you have to apply +5V power to $+5V_{IN}$ connector. If you don't want to set termination on specific channels, just remove the corresponding jumpers on the DIN-68H..

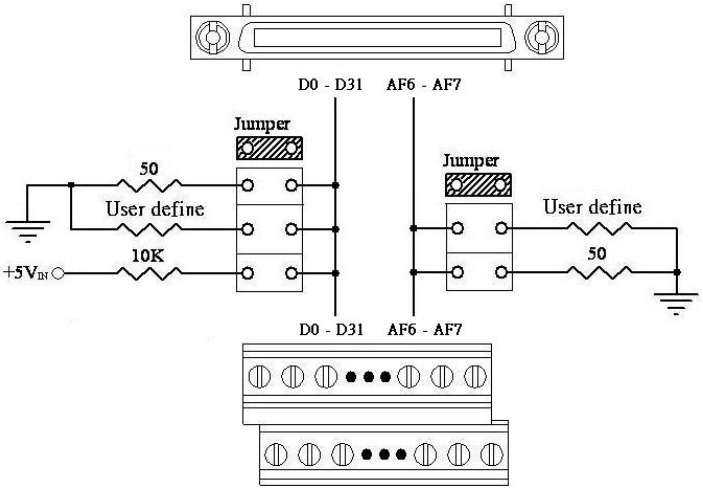


Figure A-2: Resistor Termination Schematic

The DIN-68H also provides the option of user define pull-up resistor termination. Please note that the pad position of the resistor is on the back side of PCB and the resistor footprint is 1206 packaging. Below is the layout of the back side PCB and reference table of user-defined resistor termination.

Channel	D0	D1	D2	D3	D4	D5	D6	D7
Resistor	R71	R72	R79	R80	R87	R88	R97	R98

PCIe-7350	D8	D9	D10	D11	D12	D13	D14	D15
DIN-68H	R73	R74	R81	R82	R89	R90	R99	R100

PCIe-7350	D16	D17	D18	D19	D20	D21	D22	D23
DIN-68H	R75	R76	R83	R84	R91	R92	R101	R102

PCIe-7350	D24	D25	D26	D27	D28	D29	D30	D31
DIN-68H	R77	R78	R85	R86	R93	R94	R103	R104

PCIe-7350	AF6	AF7
DIN-68H	R95	R96

Table A-2: Pad Position of User-Defined Resistor Termination

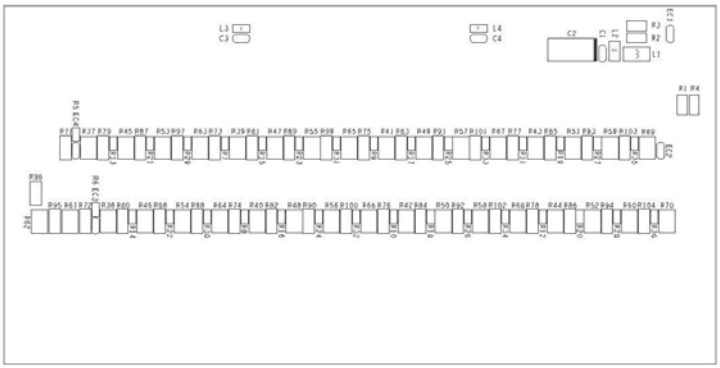


Figure A-3: DIN-68H Layout (Back Side)

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