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PCI-1760U

Isolated Relay Actuator and Digital Input Card

User's Manual

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1 x PCI-1760U card

1 x Companion CD-ROM (DLL driver included)

1 x User Manual (this manual)

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CHAPTER 1

General Information

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1.1 Introduction

The most common method of interfacing a microcomputer system, such as the PC with an industrial process, is by using programmable digital input and output registers. The computer can write data into digital output registers, treating them as I/O ports. The output from these registers can then be wired to an interface device, such as a relay. Thus, by sending data to an output register, it is possible to activate and deactivate a relay. The relay could, in turn, control, for example, an electric motor.

Similarly, a digital input register can be considered as an I/O port that has wires attached to individual bit locations. When read, the data reflects the states of signals on the wires. Digital input registers can be used to monitor incoming signals. For example, to determine whether a switch is open or closed, the switch can be wired to the input of a digital input register.

The PCI-1760U Relay Actuator & Isolated Digital Input Card is a PC add-on card for the PCI bus, which was designed with this idea in mind. This card offers the user 8 opto-isolated digital inputs with isolation protection of 2500 V_{DC} for collecting digital signals under noisy environment, 8 relay actuators for serving as ON/OFF control devices or small power switches, and 2 isolated PWM (Pulse Width Modulation) outputs for user's specific applications.

Each isolated digital input supports both dry contact and wet contact, designated by jumper settings, so that it can easily interface with other devices. Additionally, for easy monitoring, each relay is equipped with one red LED to reflect its ON/OFF status.

Digital filter eliminates unexpected input noise

The PCI-1760U includes a programmable digital filter on each digital input channel to eliminate the unexpected signal or noise from the card's inputs. When the digital filter is enabled, the state of the corresponding input channel will not update immediately until one high/low signal has lasted for a period which is programmed by the user.

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Interrupt function ensures faster system response

The PCI-1760U provides a “Pattern Match” interrupt function for the digital input channels. The card monitors the state of some or all of the input channels and compares it with a pre-set pattern. When the received state matches the pre-set pattern, the card generates an interrupt signal to the system.

The “Change of Input State” interrupt function also monitors the state of the input channels. When any input changes its state, the card interrupts the system to handle this event.

Up event counter for each DI

Each isolated digital input channel is connected to a 16-bit UP event counter. A counter will increment by 1 whenever it reads either a rising-edge (low to high) or a falling-edge (high to low) input signal with the maximum frequency of 500 Hz. When the counter overflows or reaches a pre-set value (programmed by software), it generates an interrupt signal to the PC.

1.2 Features

- 8 opto-isolated digital input channels
- 8 relay actuator output channels
- 2 opto-isolated PWM outputs
- Universal PCI card, adapt 3.3V and 5V PCI slot
- LED indicators to show activated relays
- Jumper selectable dry contact/wet contact input signals
- 16-bit Up counter function for each DI
- Programmable digital filter function for each DI
- Pattern match interrupt function for each DI
- Change of input state interrupt function for each DI
- Board ID set by DIP switch

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1.3 Applications

- Digital signal and contact status monitoring
- Industrial On/Off control
- Signal switching
- External relay driving

1.4 Specifications

Isolated Digital Input

- **Channels**: 8
- **Opto-isolator**: PC354
- **Input voltage**: 5 ~ 12 V

  High: > 4.5 V

  Low: < 1.0 V

  Uncertain: 1.0V ≤ Vin ≤ 4.5V
- **Input resistance**: 1k Ω @ 1/4 W
- **Isolation voltage**: 2500 V_{DC}
- **Digital Filter:**

  Minimum effective High input period ≥ [(2 ~ 65535) x 5 ms] + 5 ms

  Minimum effective Low input period ≥ [(2 ~ 65535) x 5 ms] + 5 ms
- **16-bit UP counter:**

  Maximum effective input frequency: 500Hz

  Minimum High period ≥ 1 ms

  Minimum Low period ≥ 1 ms

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Relay Output

- **Channels**: 8
- **Relay type**: single-pole double-throw (SPDT, Form C),
  but RE2 ~ RE7 are hooked up as single-pole single-throw (SPST)
- **Output type**: RE0 and RE1: NC and NO outputs
  RE2 ~ RE7: NC or NO outputs (selected by jumper)
- **Rating contact load**: 120 VAC @ 0.5 A or 30 VDC @ 1 A
- **Contact resistance**: less than 100 mΩ initially
- **Dielectric strength**:

  Coil to contacts (deenergized): 1500 Vrms (1 minute)

  Between open contacts (deenergized & energized):
  1000 Vrms (1 minute)
- **Life expectancy**:
  200,000 operations @ 0.5 A 120 VAC

  500,000 operations @ 1.0 A 30 VDC
- **Operating & Releasing time**:

  Operating time: 5 ms max.

  Releasing time: 5 ms max.

Isolated PWM output

- **Channels**: 2
- **Isolation voltage**: 2500 VDC
- **Scaling resolution**: 16 bits (100 µs for each step)

  High period = [(1 ~ 65535) x 100 µs] ± 50 µs (max.)

  Low period = [(1 ~ 65535) x 100 µs] ± 50 µs (max.)
- **Output level:**

  High: (5 ± 0.5) V

  Low: < 0.8 V

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General

- **Power consumption**: +5V @ 450 mA (typical), 850 mA (max.)
- **Operating temperature:** 0 ~ +60° C (32 ~ 140° F)

  (refer to IEC 68 - 2 - 1, 2)
- **Storage temperature:** -20 ~ +70° C (-4 ~ 158° F)
- **Operating humidity:** 5 ~ 95%RH non-condensing

  (refer to IEC 68-2-3)
- **MTBF:** over 117,317 hrs @ 25°C, grounded, fixed environment

Physical

- **Connector:** One 37-pin D-type connector
- **Dimensions:** 175 x 100 mm (6.9" x 3.9")

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1.5 Pin Assignments

Description of pin use:

IGND: Isolated Ground for PWM outputs and dry contact wiring of IDI

IDIn+(n = 0 ~ 7):

Isolated digital input+

IDIn- (n = 0 ~ 7):

Isolated digital input-

PWMn (n = 0, 1):

Isolated PWM output

Rn_OUT (n = 2 ~ 7):

Normally Open/Closed pin of Relay output

Rn_NO (n = 0 ~ 1):

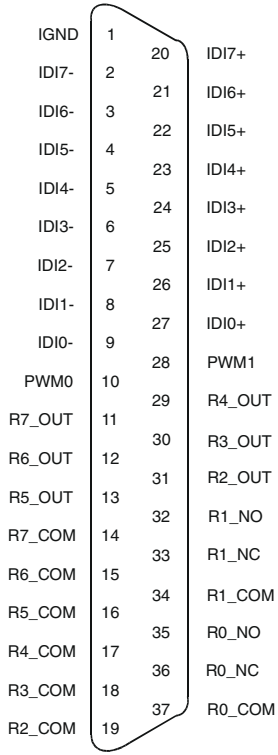
Normally Open pin of Relay output

Rn_NC (n = 0 ~ 1):

Normally Closed pin of Relay output

Rn_COM (n = 0 ~ 7):

Common pin of Relay output



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1.6 Block Diagram

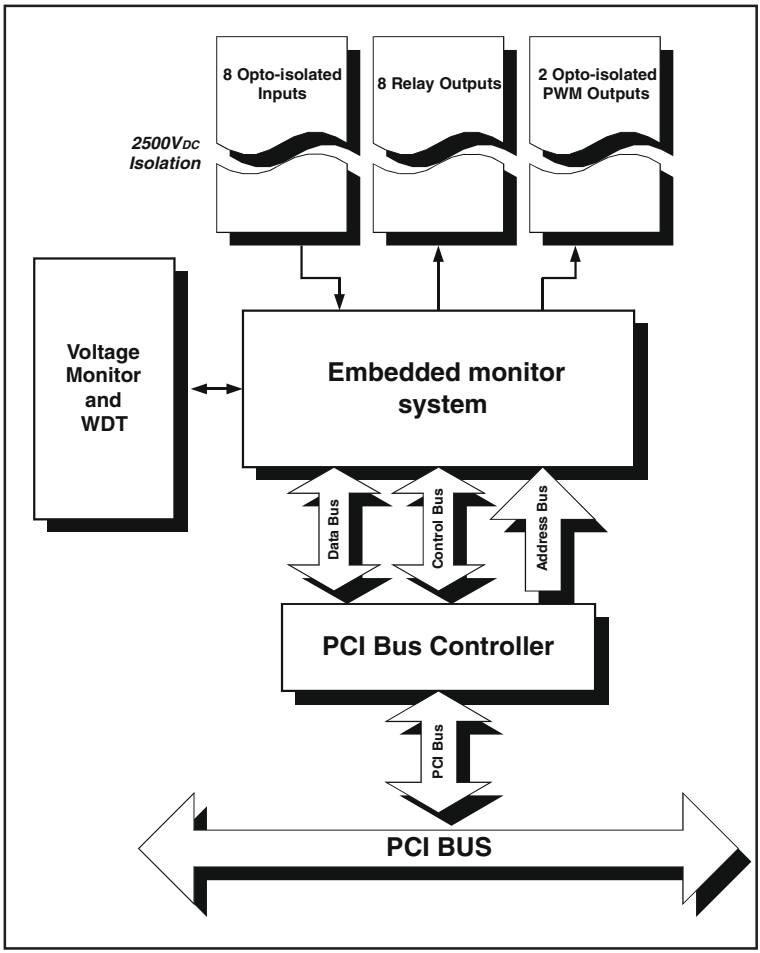


Figure 1.1 PCI-1760U Block Diagram

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CHAPTER 2

Installation

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2.1 Initial Inspection

Before installing the PCI-1760U, check the card for visible damage. We have carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order upon receipt.

As you unpack the PCI-1760U, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or fails to meet specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

2.2 Unpacking

The PCI-1760U contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCI-1760U card from its protective packaging by grasping the card's rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, protect the card by storing it in this package.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Check the product contents inside the packing. There should be one card, one CD-ROM, and this manual. Make sure nothing is missing.

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2.3 Jumper Settings

We designed the PCI-1760U with ease-of-use in mind. It is a "plug and play" card, i.e. the system BIOS assigns the system resources such as base address and interrupt automatically. There are only three functions with 15 jumpers to be set by the user (see Figure 2.1 and Table 2-1). You may refer to the figure below for help in identifying card components.

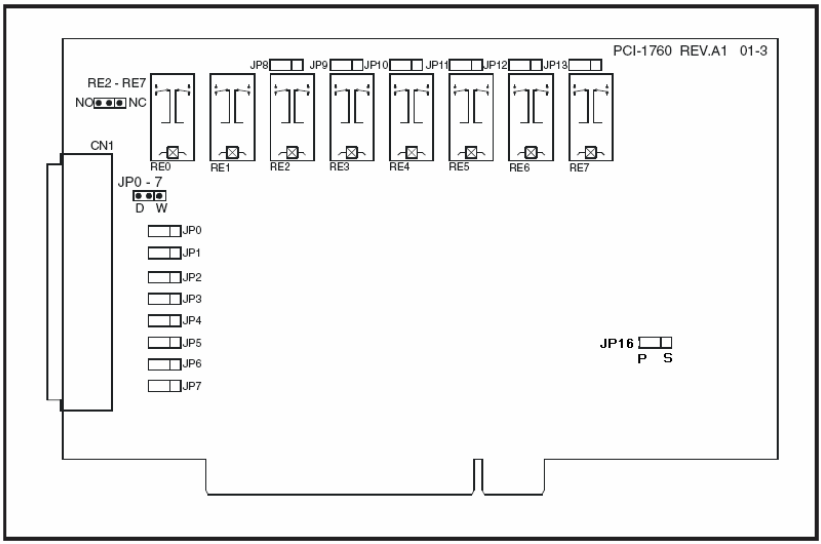
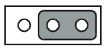


Figure 2.1 Location of jumpers and relays

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Table 2.1: Summary of jumper settings

Names of Jumpers	Function description	
JP0 ~ 7		Supports dry contact for digital input (default)
		Supports wet contact for digital input
JP8 ~ 13		Sets relay output to be normally open (default)
		Sets relay output to be normally closed
JP14		Clears relay outputs to "OFF" when the system (or PC) issues a reset signal on the PCI bus.
		Clears relay outputs to "OFF" only when system powers-on.

Setting dry/wet contact connection for each DI

Each of the 8 isolated digital input channels accepts either dry contact or 5 ~ 12 V_{DC} wet contact inputs according to the corresponding jumper settings (see Table 2.2). The default setting for each IDI is dry contact. For detailed information, please refer to **Chapter 3**.

Setting relay outputs to be NC/NO

6 relay outputs, RE2 ~ RE7, are single-pole single-throw (SPST), which can be jumper set as either nornally open (NO) or normally close (NC) (see Table 2.3). The default settings for RE2 ~ RE7 are normally open. For detailed information, please refer to **Chapter 4**.

Note!: *RE0 and RE1 are Form C relays*

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Table 2.2: IDI and corresponding jumper

Isolated Digital Input Channel	Corresponding Jumper
IDI0	JP0
IDI1	JP1
IDI2	JP2
IDI3	JP3
IDI4	JP4
IDI5	JP5
IDI6	JP6
IDI7	JP7

Table 2.3: Relay output and corresponding jumper

Relay Output Channel	Corresponding Jumper
RE2	JP8
RE3	JP9
RE4	JP10
RE5	JP11
RE6	JP12
RE7	JP13

Setting the time to reset the relay outputs

Some users will want the capability of clearing each relay output when the system (or PC) issues a reset signal on the PCI bus. Some users will want to clear their relays only as part of system power-on. The PCI-1760U satisfies both these needs by providing jumper JP14. Depending on the application, this capability may allow relay outputs to be "OFF" without requiring a complete shutdown of processes controlled by the card.

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Complete loss of power to the chip clears the chip memory. Thus, no matter how JP14 is set, if the power to the PCI-1760U is disconnected, the relay initial power-on state will be "OFF" (NC or NO, depending on the user's settings).

Setting the Broad ID (SW1)

Use Read Board ID Command (0x0D) to get the board ID. The PCI-1760U has a built-in DIP switch (SW1), which is used to define each card's board ID. You can determine the board ID on the register as shown in Table 2.4. When there are multiple cards on the same chassis, this board ID setting function is useful for identifying each card's device number through board ID. We set the PCI-1760U board ID as 0 at the factory. If you need to adjust it to other board ID, set the SW1 by referring to DIP switch setting.

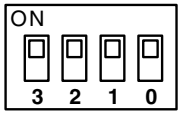


Figure 2.2 Board ID Switch

Table 2.4 Board ID Settings

SW1	Position 1	Position 2	Position 3	Position 4
Board ID	ID3	ID2	ID1	ID0
15	OFF	OFF	OFF	OFF
14	OFF	OFF	OFF	ON
13	OFF	OFF	ON	ON
:	:	:	:	:
1	ON	ON	ON	OFF
0*	ON	ON	ON	ON

* Default setting is 0

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2.4 Installation Instructions

The PCI-1760U can be installed in any PCI slot in a computer. However, to avoid any mistakes or dangerous conditions, please refer to your computer user's manual before you follow the installation procedure below:

1. Turn off your computer and any accessories connected to the computer.

Warning! *TURN OFF your computer power supply whenever you install or remove any card, or connect and disconnect cables.*



2. Disconnect the power cord and any other cables from the back of the computer.
3. Remove the cover of the computer.
4. Select an empty 5 V PCI slot. Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.
5. Carefully grasp the upper edge of the PCI-1760U. Align the hole in the retaining bracket with the hole on the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the card into the socket gently but firmly. Make sure the card fits the slot tightly.
6. Secure the PCI-1760U by screwing the mounting bracket to the back panel of the computer.
7. Attach any accessories (37-pin D type cable, wiring terminal board, etc.) to the card.
8. Replace the cover of your computer. Connect the cables you removed in step 2.
9. Turn the computer power on.

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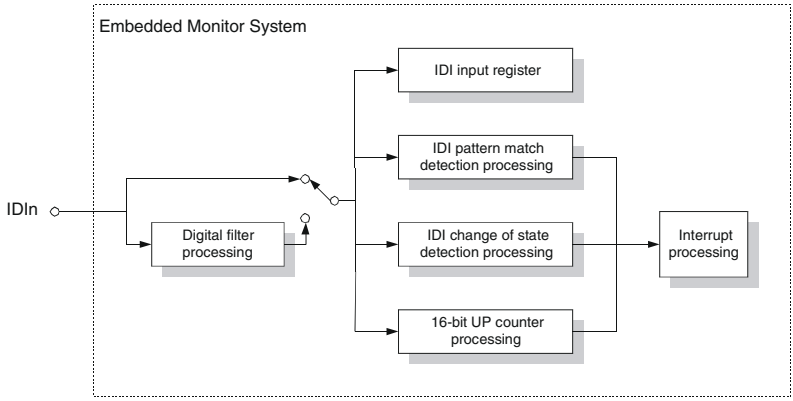
CHAPTER 3

Digital Input Programming

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3.1 Overview

The PCI-1760U provides 8 opto-isolated digital input channels with 2500V_{DC} isolation. In addition to supporting both dry and wet contacts, this card provides "Digital Filter", "Pattern Match", "Change of State" and 16-bit UP counter functions for each digital input channel. All these functions are optional. Users can enable/disable each function to fit their applications. Figure 3.1 is a simplified function logic block diagram for the PCI-1760's digital inputs. The following sections will introduce these useful functions.



IDIn : Isolated digital input (n = 0 ~ 7)

Figure 3.1: PCI-1760U function logic block diagram

3.2 Dry Contact Support for Each IDI

Each of the 8 isolated digital input channels accepts either dry contact or 5 ~ 12 V_{DC} wet contact inputs as determined by the corresponding jumper settings (see Table 2.1 and Table 2.2). Dry contact capability allows an input channel to respond to changes in an external circuit (e.g., the closing of a switch in the external circuit) when no voltage is present in the external circuit. Figure 3.2 shows the internal and external circuitry, with both wet and dry contact components connected as an input source for one of the PCI-1760's isolated digital input channels.

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Note!: *The default settings of jumpers JP0 ~ JP7 are dry contact, just as shown in Figure 3.2.*

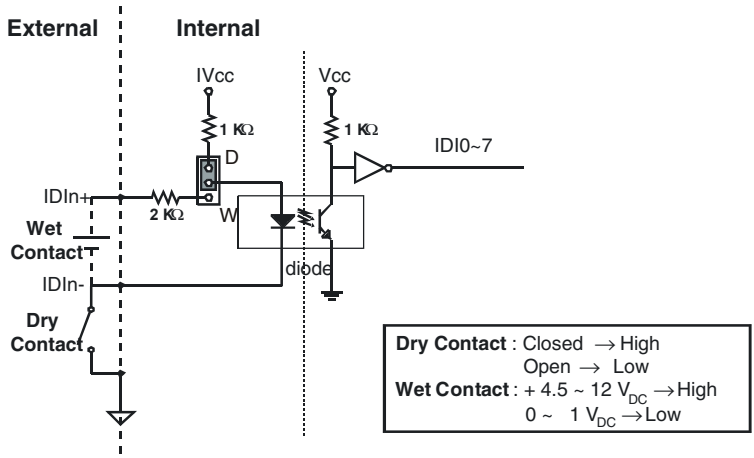


Figure 3.2: Dry and wet contacts

3.3 Digital Filter

Each digital input channel has a programmable digital filter for eliminating unexpected signals and noise from the card circuitry. The user can set different digital filtering parameters for each input channel in different applications. The following is a functional description of the digital filter.

1. When a digital filter is enabled, the PCI-1760U will sample the signals at the enabled input channel at a 5 ms sampling rate.
2. When a high or low signal is present at a digital input channel whose digital filter function is enabled, the signal will be filtered out as noise unless it lasts for an effective period.
3. The effective period is determined by multiplying the sampling rate (5 ms) by the sampling number (2 ~ 65535) chosen by the user, i.e.

Effective period = Sampling number x 5 ms.

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Note!: *The sampling numbers for High and Low signals can be different. For example, assuming that the sampling numbers are 10 for a High signal and 15 for a Low signal, the state of the digital input channel will update if a high signal lasts for 50 ms or more, or a low signal lasts for 75 ms or more.*

Note!: *For digital input channels whose digital filter functions are not enabled, the PCI-1760U samples the signals at these input channels at a 100 ms sampling rate and immediately updates the state of these input channels when the signal changes.*

3.4 Pattern Match

The PCI-1760U provides a pattern match interrupt function on its digital input channels. It monitors the status of the enabled input channels, and compares these with a pre-set pattern. When the actual state matches the pre-set pattern, the PCI-1760U delivers an interrupt signal to the system. This function releases the CPU from the burden of polling all the I/O points, enabling a PC to handle more I/O points with higher performance. An example follows:

Example 3.1 Assume that the pattern match function is enabled for the isolated digital input channels IDI1, IDI2, IDI6 and IDI7 (i.e. IDI0, IDI3, IDI4, and IDI5 are ignored during the pattern match process). Then the user can set the pattern match values for the enabled input channels. The table below shows one possibility.

Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0
Pattern match status	1	0	X	X	X	1	1	X

In thes example, when IDI1, IDI2 and IDI7 are high and IDI6 is low, an interrupt signal will be generated. No matter what the status of IDI0, IDI3, IDI4 and IDI5 are, these will not affect the result.

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3.5 Change of Input State

The PCI-1760U also provides a change of state interrupt function on each digital input channel allowing users to monitor the status of the enabled digital input channels more efficiently. When one of the enabled channels changes its state, the PCI-1760U delivers an interrupt signal to the system to handle this event. The function can be set to generate an interrupt for a rising edge signal, a falling edge signal, or a signal with both edges, depending on user application requirements. The following is an example.

Example 3.2 Assume that the change of input state function for the isolated digital input channels IDI1, IDI2, IDI6 and IDI7 is enabled (i.e. the signals at IDI0, IDI3, IDI4 and IDI5 are ignored by the change of state function). When a change of state occurs in IDI1, IDI2, IDI6 or IDI7, an interrupt signal is sent to the system.

3.6 Counter

Each digital input channel is connected to a 16-bit UP event counter with a maximum frequency of 500 Hz. Each counter is enabled or disabled by software. The following describes its major functions:

1. Counter reset value

Each counter has its own reset value. When most cards are powered on, the start-up value of a counter is zero, but in the PCI-1760U, users are allowed to set the reset value to a number between 0 and 65535. This is a very useful feature when one of the counters needs to be started from a non-zero number.

2. Counter value match interrupt

All eight counters also have a counter value match interrupt function. When this interrupt function is enabled, an interrupt signal will be generated if the counter value reaches a pre-set counter match value. The counter will continue to count until an overflow occurs, then it will go back to its reset value and continue the counting process.

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3. Overflow

An overflow will occur when the counter reaches its maximum value, 65535, and an interrupt signal will be generated when this function is enabled.

4. Count edge

A user can set each individual channel's counter to count either falling edge (high-to-low) or rising edge (low-to-high) signals. The appropriate setting depends on the initial state of the input signals; if they are low, a rising edge setting would be appropriate.

The following figure illustrates counter operation. Counting starts from the counter reset value and continues until it reaches its match value. At that time, an interrupt will also be generated. Afterwards, the counter continues to count until it reaches the maximum capacity of 65535, at which time an overflow interrupt is generated and the counter is reset to its reset value, and continues to count.

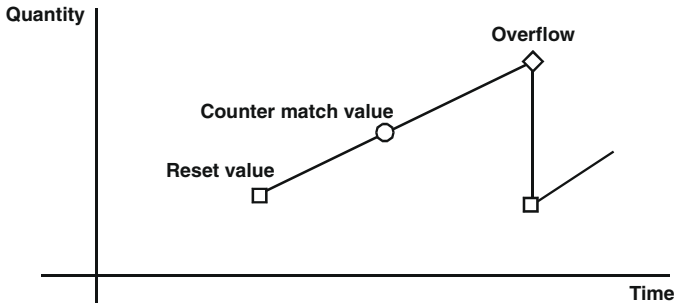


Figure 3.3: Example for counter operation

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CHAPTER 4

Relay Output

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4.1 Relay Output

The PCI-1760U provides 8 relay outputs to serve as On/Off control devices. The user can enable and disable each relay output using software commands. For easy monitoring, each relay output is equipped with one red LED to show its On/Off status.

Note!: *Please refer to* ***Appendix B*** *for more information about relay output software programming.*

Of these eight relays, two relays (RE0 and RE1) are single-pole double-throw (SPDT, Form C) and six (RE2 ~ RE7) are single-pole single-throw (SPST), which can be set as either normally open (NO) or normally closed (NC) via jumper settings. The following figure illustrates the structures and connections of the relay outputs.

Note!*: The default setting for RE2 ~ RE7 is normally open (NO). Please refer to* ***Chapter 2*** *for detailed information concerning the setting of jumpers.*

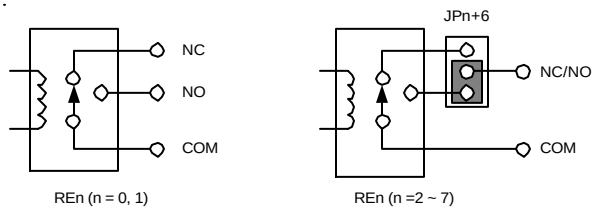


Figure 4.1: Relay structures and connections

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CHAPTER 5

Pulse-Width Modulation

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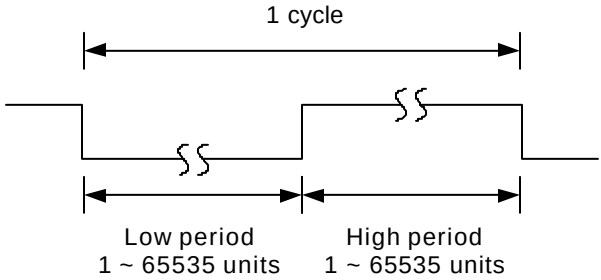
5.1 Overview

The PCI-1760U also provides two PWM (Pulse-Width Modulation) outputs with 2500 V_{DC} isolation. Each PWM output can be independently enabled or disabled using software commands.

5.2 Introduction to PWM

A pulse-width modulated waveform is created when the High and Low periods of a periodic rectangular signal are varied. In the PCI-1760U, the user can individually set each channel's High and Low periods for from 1 to 65535 units (1 unit = 100μs), depending on his needs.

The user can also define the "burst count", the number of cycles



generated in each PWM channel. It can be a specific number of cycles or a non-stop cycle. If not a non-stop cycle, the predefined number of cycles must be between 1 and 65535.

When the user enables a PWM output, the PCI-1760U will check the PWM burst count value first. If the burst count value is zero, the PWM output will be non-stop. If the burst count value is non-zero, the PWM will output the number of cycles which equals the burst count value, then stop. If the user wants to output another pulse chain, he has to set a new burst count value, then enable the PWM again.

Note!: *Please refer to* ***Appendix B*** *for more information about PWM software programming.*

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APPENDIX A

Register Structure and Format

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A.1 Overview

The PCI-1760U is delivered with an easy-to-use 32-bit DLL driver for user programming under the Windows 95/98/NT operating system. To program the PCI-1760U, users are advised to use the 32-bit DLL driver provided by Advantech to avoid the complexity of low-level programming by register.

When it is necessary to program the PCI-1760U at a register level, the most important consideration is to understand the function of the card's registers. The PCI-1760U occupies 128 bytes in the PC's I/O space. In general operations, it only requires 8 I/O spaces, 4 for writing commands and 4 for reading commands. To enable/disable the interrupt function, the PCI-1760U requires another 4 I/O spaces to read/write. The address of each register is specified as an offset from the card's base address.

A.2 OMB0 ~ 3: Outgoing Mailbox Bytes

Write	OMB3	OMB2	OMB1	OMB0
Address (Hex.)	Base + 0x0F	Base + 0x0E	Base + 0x0D	Base + 0x0C

OMB3: This byte is not currently used. It is reserved for future use. Its value must be 0x00 unless 16 or 32-bit command codes are used.

OMB2: Writes a command code (0x00 ~ 0xFF) to the PCI-1760U. For detailed descriptions of the command codes, please refer to **Appendix B**.

OMB1: The High byte of the parameter for the command in OMB2

OMB0: The Low byte of the parameter for the command in OMB2

Note!: *If a command needs one parameter, users should write the parameter (OMB1 and/or OMB0) first, then write the command code to OMB2.*

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A.3 IMB0 ~ 3: Incoming Mailbox Bytes

Read	IMB3	IMB2	IMB1	IMB0
Address (Hex.)	Base + 0x1F	Base + 0x1E	Base + 0x1D	Base + 0x1C

IMB3: This byte shows IDI (Isolated Digital Inputs) current values. This status will be updated every 100μs by the PCI-1760's on-board monitor system.

IMB2: This byte shows the current command status. When the user writes a command code in OMB2, IMB2's status will be updated to match OMB2 if the command code is successfully received by the PCI-1760U.

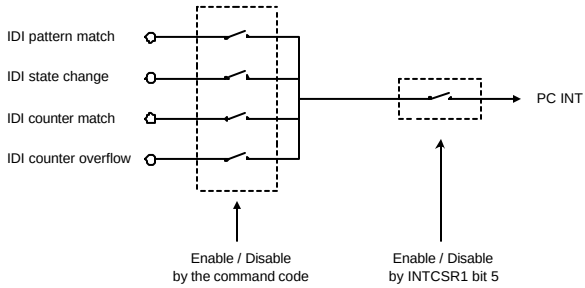
IMB1: The High byte of the feedback data for the command in OMB2

IMB0: The Low byte of the feedback data for the command in OMB2

A.4 INTCSR0 ~ 3: Interrupt Control/Status Register

There are 4 interrupt sources (IDI pattern match, IDI state change, IDI counter value match and IDI counter overflow) provided by the PCI-1760U. To enable/disable the interrupt function, the PCI-1760U requires another 4 I/O spaces to read/write.

INTCSR3: Must be 0 unless 16 or 32-bit command codes are used



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Read/Write	INTCSR3	INTCSR2	INTCSR1	INTCSR0
Address (Hex.)	Base + 0x3B	Base + 0x3A	Base + 0x39	Base + 0x38

INTCSR2: This byte shows the interrupt status (read only)

bit 0: Outgoing mailbox Interrupt (not available now)

bit 1: Incoming mailbox Interrupt (not available now)

bit 2 ~ 5: Must be 0

bit 6: On-board interrupt status

bit 7: Interrupt asserted

INTCSR1: To enable/disable the interrupt function

bit 0 ~ 4: Must be 0

bit 5: To enable/disable the on-board interrupt function

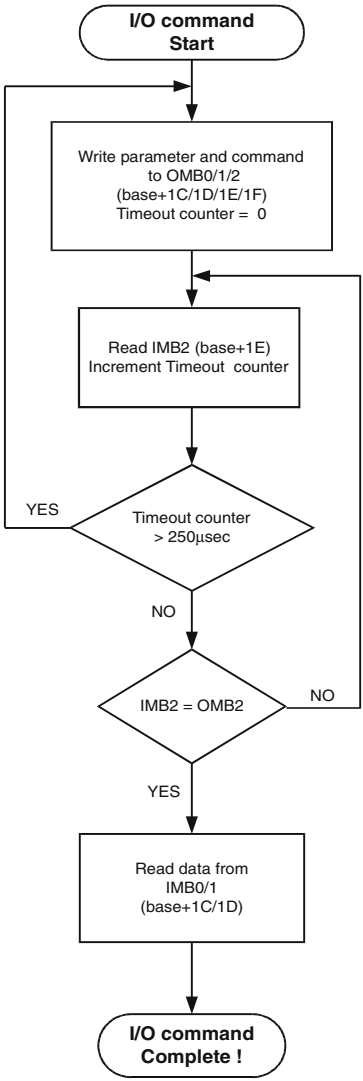
bit 6 ~ 7: Must be 0

INTCSR0: Must be 0 unless 16 or 32-bit command codes are used

A.5 Flow Chart

To write a command or confirm the command status, please follow the flow chart below.

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APPENDIX B

Description of Command Codes

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COMMAND CODE: 00

PURPOSE: Clears IMB2's Contents to 0

OMB3	OMB2	OMB1	OMB0
0x00	0x00	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x00	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to clear IMB2's contents by echoing the command code "00" from OMB2. Users can detect when a command has been executed by reading its echo in IMB2. When a given command is executed twice in a very short period, it can be very difficult to identify the two separate commands just by reading the command code in IMB2. A simple solution to this problem is to write a command code "00" between the two identical commands in OMB2. The command code "00" clears the first command code in IMB2 and lets the user clearly recognize execution of the second command. Of course, if a user does not need to distinguish each separately executed command, the insertion of the command code "00" between the two identical commands is not necessary.

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COMMAND CODE: 01

PURPOSE: Enable/Disable Relay Outputs

OMB3	OMB2	OMB1	OMB0
0x00	0x01	N/A	0x00 ~ 0xFF

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x01	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to enable/disable the 8 relay outputs of the PCI-1760U. Users may input the relay configuration parameters in OMB0, either “1” or “0”, in each of the 8 data bits, to enable or disable the corresponding relay output. The value "1" enables the channel and the value "0" disables it. The first bit of OMB0, bit 0, corresponds to the relay output channel 0, RE0; the second bit, bit 1, corresponds to RE1, and so forth. The following table shows this correspondence.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Relay channel	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

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COMMAND CODE: 02

PURPOSE: Read the Relay Status

OMB3	OMB2	OMB1	OMB0
0x00	0x02	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x02	XX	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB0: Current states of relays REO ~ RE7

The purpose of this command is to read the current status of each relay. The states can be read in register IMB0. The first bit of IMB0, bit 0, corresponds to RE0, the second bit, bit 1, corresponds to RE1, and so forth. The following table shows this correspondence.

Data in IMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Relay channel	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

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COMMAND CODE: 07

PURPOSE: Read the Current Status

OMB3	OMB2	OMB1	OMB0
0x00	0x07	N/A	0x00 ~ 00xFF

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x07	0x00 ~ 0xFF	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to read the value or state at one specific address of the register. The parameter input in OMB0 is the address of the function. It is the command code that is normally entered into OMB2 to execute a command. Once the command "07" is executed, the value or data associated with the function input in OMB0 will be shown in IMB0 and/or IMB1.

For example, a user may enable the digital filter function of the first isolated digital input channel IDI0 by using command code 20 with the parameter 01. The command's result may be read by executing a command code 07 in OMB2 with the parameter 20 to display the current status of the digital filter function. The following is an illustration.

A) Enable the digital filter function of IDI0.

OMB3	OMB2	OMB1	OMB0
0x00	0x20	N/A	0x01

OMB2: Command code

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If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x20	XX	XX

IMB3: IDI current values

IMB2: Command code echo

B) Read the current status of the digital filter function

OMB3	OMB2	OMB1	OMB0
0x00	0x07	N/A	0x20

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x07	N/A	0x01

IMB3: IDI current values

IMB2: Command code echo

IMB0: Current digital filter function state. (In this case, the filter function at IDI0 is enabled and the filter functions at IDI1~IDI7 are disabled)

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COMMAND CODE: 0D

PURPOSE: Read Board ID

OMB3	OMB2	OMB1	OMB0
0x00	0x0D	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x0 D	XX	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB0: Current Board ID Value, the format of IMB0 is as below,

Bit#	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	ID3	ID2	ID1	ID0

ID0: the least significant bit (LSB) of Board ID

ID3: the most significant bit (MSB) of Board ID

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COMMAND CODE: 0E, 0F

PURPOSE: Reads PCI-1760U's Firmware/Hardware Version

OMB3	OMB2	OMB1	OMB0
0x00	0x0E, 0x0F	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x0E, 0x0F	0x00 ~ 0xFF	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB1: The High byte of PCI-1760U's firmware/hardware version

IMB0: The Low byte of PCI-1760U's firmware/hardware version

The purpose of this command is to read the firmware/hardware version of the PCI-1760U. The command code 0E is to read the firmware version, and 0F, the hardware version. The version number will be displayed at IMB0 and IMB1 once the command code has been executed.

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COMMAND CODE: 10, 11, 12, 13

PURPOSE: Sets the “High” and “Low” Period Value of the PWMn

OMB3	OMB2	OMB1	OMB0
0x00	0x10 ~ 0x13	0x00 ~ 0xFF	0x00 ~ 0xFF

OMB2: Command code

OMB1: The High byte of the High/Low period value

OMB0: The Low byte of the High/Low period value

The High/Low period value of the PWMn = 256 * OMB1 + OMB0

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x10 ~ 0x13	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set the high and low period values of the two PWMs, PWM0 and PWM1. The wavelength is the sum of both high and low period values and its maximum value is 2 x 65535 units (one unit is equal to 100 μs).

Both OMB0 and OMB1 are used in this command. OMB0 and OMB1 respectively represent the low and high byte values. The following gives the descriptions of command codes 10 ~ 13.

Command Code (Hex.) OMB2	Purpose
10	Sets the “High” period value of PWM0
11	Sets the “Low” period value of PWM0
12	Sets the “High” period value of PWM1
13	Sets the “Low” period value of PWM1

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COMMAND CODE: 14, 15

PURPOSE: Sets PWMn's Burst Count

OMB3	OMB2	OMB1	OMB0
0x00	0x14, 0x15	0x00 ~ 0xFF	0x00 ~ 0xFF

OMB2: Command code

OMB1: The High byte of the burst count value

OMB0: The Low byte of the burst count value

The burst count value of the PWMn = 256 * OMB1 + OMB0

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x14, 0x15	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set the number of cycles generated in each PWM channel. Command code 14 sets the burst count for PWM0 and command code 15 sets the burst count for PWM1. When the parameter is “0”, there will be a non-stop cycle generated. If not a non-stop cycle, the maximum number of predefined cycles is 65535. Both OMB0 and OMB1 are used in this command.

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COMMAND CODE: 1F

PURPOSE: Enables/Disables PWM Outputs

OMB3	OMB2	OMB1	OMB0
0x00	0x1F	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: Bit 0: "1" enables the PWM0 output and "0" disables it

Bit 1: "1" enables PWM1 output and "0" disables it

Bit 2 ~ 7 must be 0

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x1F	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control both of the PWM output channels by using the first 2 bits in OMB0. Bit 0 controls the output of PWM0 and bit 1, the output of PWM1. The values of bit 2 to bit 7 in OMB0 must be 0 and OMB1 is not used.

Note: *When the PCI-1760U receives this command, it checks the burst count value(s) of the enabled PWM output channel(s) first. If the value(s) is zero, the PWM output(s) will be a non-stop cycle. Conversely, if the burst count value(s) is nonzero, the PCI-1760U will output as many cycles as the burst count value(s), then disable the PWM channel(s)*

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COMMAND CODE: 20

PURPOSE: Enables/Disables the Digital Filter Function of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x20	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to enable the digital filter function at IDIn; "0" means to disable the fuction of IDIn (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x20	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control the operation of the digital filter function at each isolated digital input channel. The first bit of OMB0, bit 0, controls the digital filter function of IDI0, the second bit, bit 1, controls IDI1, and so forth. The following table illustrates how the two hexadecimal bytes in OMB0 enable/ disable different combinations of IDI channels 0 ~ 7.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IDI channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0
Case A: 0x01	0	0	0	0	0	0	0	1
Case B: 0x11	0	0	0	1	0	0	0	1

In case A, the input value is 0x01, so the digital filter function at IDI0 is enabled. In case B, the input value is 0x11, so the digital filter functions at IDI0 and IDI4 are enabled.

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COMMAND CODE: 21

PURPOSE: Enables/Disables the Pattern Match Function of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x21	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to enable the pattern match function for IDIn; "0" means to disable the fuction for IDIn (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x21	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control the pattern match function of each isolated digital input channel. The first bit of OMB0, bit 0, controls the pattern match function of IDI0, the second bit, bit 1, controls IDI1, and so forth. The following table illustrates how the 8 bits of OMB0 control enabling/disabling the pattern match function for IDI channels 0 ~ 7.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0
Case A: 0x01	0	0	0	0	0	0	0	1
Case B: 0x11	0	0	0	1	0	0	0	1

In case A, the input value is 0x01, so the pattern match function at IDI0 is enabled. In case B, the input value is 0x11, so the pattern match functions at IDI0 and IDI4 are enabled.

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COMMAND CODE: 22
PURPOSE: Sets the Pattern Match Value of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x22	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: The preset pattern match value. Bit 0 corresponds to IDI0; bit 1 corresponds to IDI1, and so forth.

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x22	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set the pattern match value of each isolated input channel. The input for a channel will not be relevant unless the channel has been enabled by command code 21. In the other words, whatever the input value is, the system will ignore the channel if it is not an enabled pattern match channel. The following table illustrates how the pattern-match-enabled channels are relevant to the operations of the pattern match function and the pattern-match-disabled channels are irrelevant to the pattern match function.

Command code	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0
21	0	0	1	1	1	0	1	0
22	-	-				-		-

The pattern match function of IDI1, IDI3, IDI4 and IDI5 is enabled by using command code 21. The pattern match value is only relevant in these channels and is ignored in IDI0, IDI2, IDI6 and IDI7.

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COMMAND CODE: 23, 24

PURPOSE: Enables/Disables the Rising/Falling Edge Detection Function of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x23, 0x24	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to enable the rising/falling edge detection function for IDIn; "0" means to disable the function for IDIn (n = 0 ~ 7).

Command code (Hex.) OMB2	Purpose
23	Enables/Disables the rising edge detection function of IDI
24	Enables/Disables the falling edge detection function of IDI

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x23,0x24	XX	XX

IMB3: IDI current values

IMB2: Command code echo

These commands enable/disable the detection of the changes of digital input signals and the generation of interrupt signals to the system following detections. The command code 23 enables/disables the detection of a “low-to-high” state change at each digital input channel. The command code 24 enables/disables the detection of a “high-to-low” state change at each digital input channel.

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COMMAND CODE: 28

PURPOSE: Enables/Disables the UP Counter Function of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x28	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to enable the UP counter function for IDIn; "0" means to disable the function for IDIn (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x28	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control the UP counter function for each isolated digital input channel. The first bit of OMB0, bit 0, controls the UP counter function of IDI0, the second bit, bit 1, controls IDI1, and so forth. The following table shows this correspondence of bit number in OMB0 to the channel number of IDI.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0

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COMMAND CODE: 29

PURPOSE: Resets the UP Counter of IDIn to Its Reset Value

OMB3	OMB2	OMB1	OMB0
0x00	0x29	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to reset the UP counter of IDIn to its reset value; "0" means to retain the current count value at IDIn (n = 0~7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x29	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to reset the UP counter of each isolated digital input channel to its reset value. The first bit of OMB0, bit 0, controls the counter for channel IDI0, the second bit, bit 1 controls IDI1, and so forth. The following table shows the correspondence of bit number in OMB0 to IDI channel number.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0

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COMMAND CODE: 2A

PURPOSE: Enables/Disables the UP Counter Overflow Interrupt Function of IDIn

OMB3	OMB2	OMB1	OMB0
0x00	0x2A	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to enable the overflow interrupt function of IDIn's UP counter; "0" means to disable the function of IDIn's UP counter (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x2A	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control the overflow interrupt function of IDIn's UP counter. If the setting is “1”, the overflow interrupt function will be enabled and will generate an interrupt signal to the system when the counter overflows. If it is “0”, no interrupt will be generated for a counter overflow. The first bit of OMB0, bit 0, controls the overflow interrupt function of ID0's UP counter, the second bit, bit 1, controls IDI1's UP counter, and so forth. The following table shows the correspondence of bit number in OMB0 to IDI channel number.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0

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COMMAND CODE: 2B

PURPOSE: Enables/Disables the UP Counter Value Match Interrupt function of IDI

OMB3	OMB2	OMB1	OMB0
0x00	0x2B	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means to emable the counter value match interrupt function of IDIn's UP counter; "0" means to disable the function of IDIn's UP counter (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x2B	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control the value match interrupt function of IDIn's UP counter. The first bit of OMB0, bit 0, controls the value match interrupt function of IDI0's UP counter, the second bit, bit 1, controls IDI1's UP counter, and so forth. A value of "1" in a given bit enables the corresponding channel's UP counter value match interrupt function. A value of "0" disables it. The following table shows the correspondence of bit number in OMB0 to IDI channel number.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0

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COMMAND CODE: 2C

PURPOSE: Sets the Count Edge of IDI's UP Counter

OMB3	OMB2	OMB1	OMB0
0x00	0x2C	N/A	0x00 ~ 0xFF

OMB2: Command code

OMB0: In bit n, "1" means IDIn's UP counter will add 1 when there is a falling edge at IDIn; "0" means IDIn's UP counter will add 1 when there is a rising edge (n = 0 ~ 7).

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x2C	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to control IDIn's UP counter to count a signal having either a falling or a rising edge. The first bit of OMB0, bit 0, controls the count edge of IDI0's UP counter, the second bit, bit 1, controls IDI1's UP counter, and so forth. For instance, if the parameter in OMB0 is 11, then the counters at IDI0 and IDI4 will count each signal with a falling edge, and the counters at IDI1, IDI2, IDI3, IDI5, IDI6 and IDI7 will count each signal with a rising edge. The following table shows the correspondence of bit number in OMB0 to IDI channel number.

Parameters in OMB0								
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Channel	IDI7	IDI6	IDI5	IDI4	IDI3	IDI2	IDI1	IDI0

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COMMAND CODE: 2F

PURPOSE: Reads IDIn's UP Counter Current Value

OMB3	OMB2	OMB1	OMB0
0x00	0x2F	N/A	0x00 ~ 0x07

OMB2: Command code

OMB0: Bit 0 ~ 2: the IDI channel n (n = 0 ~ 7) whose current UP counter count value the user wants to read

Bit 3 ~ 7: must be zero

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x2F	0x00 ~ 0xFF	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB1: The High byte of the assigned counter's current value

IMB0: The Low byte of the assigned counter's current value

IDIn's UP counter current value = 256 * IMB1 + IMB0

The purpose of this command is to read the current count value in a specified IDI channel's UP counter. The IDI channel n is specified by writing the channel number in binary code in bits 0 ~ 2 of OMB0. For example, OMB0 = 00000011 specifies IDI channel 3; OMB0 = 00000100 specifies IDI channel 4.

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COMMAND CODE : 30~3F

PURPOSE : Sets the Sampling Number for the Effective "High/Low" Period of IDIn

OMB3	OMB2	OMB1	OMB0
0x00	0x30 ~ 0x3F	0x00 ~ 0xFF	0x00 ~ 0xFF

OMB2: Command code

OMB1: The High byte of the sampling number for the effective High/Low period of IDI channel n (n = 0 ~ 7)

OMB0: The Low byte of the sampling number for the effective High/Low period of IDI channel n (n = 0 ~ 7)

Effective High/Low period = Sampling number * 5ms

Sampling number = 256 * OMB1 + OMB0

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x30 ~ 0x3F	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set the sampling number for the effective "High/Low" period of each isolated digital input channel. The sampling numbers for the effective High and Low periods of IDI channel n are set separately. The parameter in OMB0 represents the low byte of the sampling number and OMB1 represents the high byte. The following table summarizes the correspondence of the command code in OMB2 to IDI channel number and High/Low period setting.

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Command code (Hex.) OMB2	Purpose
30	Sets the sampling number for the effective “High” period of IDI 0
31	Sets the sampling number for the effective “High” period of IDI 1
32	Sets the sampling number for the effective “High” period of IDI 2
33	Sets the sampling number for the effective “High” period of IDI 3
34	Sets the sampling number for the effective “High” period of IDI 4
35	Sets the sampling number for the effective “High” period of IDI 5
36	Sets the sampling number for the effective “High” period of IDI 6
37	Sets the sampling number for the effective “High” period of IDI 7
38	Sets the sampling number for the effective “Low” period of IDI 0
39	Sets the sampling number for the effective “Low” period of IDI 1
3A	Sets the sampling number for the effective “Low” period of IDI 2
3B	Sets the sampling number for the effective “Low” period of IDI 3
3C	Sets the sampling number for the effective “Low” period of IDI 4
3D	Sets the sampling number for the effective “Low” period of IDI 5
3E	Sets the sampling number for the effective “Low” period of IDI 6
3F	Sets the sampling number for the effective “Low” period of IDI 7

When a signal is shorter than the effective period, the PCI-1760U will ignore this signal and treat it as noise.

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COMMAND CODE : 40~47

PURPOSE : Sets IDIn's UP Counter Reset Value

OMB3	OMB2	OMB1	OMB0
0x00	0x40 ~ 0x47	0x00 ~ 0xFF	0x00 ~ 0xFF

OMB2: Command code

OMB1: The High byte of IDIn's UP counter reset value

OMB0: The Low byte of IDIn's UP counter reset value

IDIn's UP counter reset value = 256 * OMB1 + OMB0

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x40 ~ 0x47	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set IDIn's UP counter reset value. The reset value is the starting value of the counter. It might be 0 or any value within the range of 0 ~ 65535. Every IDIn's UP counter may have its own unique reset value. The parameter in OMB0 represents the low byte of the reset value and OMB1 represents the high byte. The following table shows the correspondence of the command code and the IDI channel number whose UP counter reset value is being set.

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Command Code (Hex.) OMB2	Purpose
40	Sets IDI0's counter reset value
41	Sets IDI1's counter reset value
42	Sets IDI2's counter reset value
43	Sets IDI3's counter reset value
44	Sets IDI4's counter reset value
45	Sets IDI5's counter reset value
46	Sets IDI6's counter reset value
47	Sets IDI7's counter reset value

This command has no effect on a given IDI channel unless the UP counter function for that channel has been enabled.

COMMAND CODE: 48~4F

PURPOSE: Sets IDIn's UP Counter Match Value

OMB3	OMB2	OMB1	OMB0
0x00	0x48 ~ 0x4F	0x00 ~ 0xFF	0x00 ~ 0xFF

OMB2: Command code

OMB1: The High byte of IDIn's UP counter match value

OMB0: The Low byte of IDIn's UP counter match value

IDIn's UP counter match value = 256 * OMB1 + OMB0

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If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x48 ~ 0x4F	XX	XX

IMB3: IDI current values

IMB2: Command code echo

The purpose of this command is to set each UP counter's match value. When the counter value match interrupt function is enabled by calling command code 2B, an interrupt signal will be generated to the system when the enabled counter value equals its match value. Each counter's match value is set individually using command codes ranging from 48 to 4F as shown in the following table. The parameter in OMB0 represents the low byte of the counter match value and that in OMB1 represents the high byte.

Command Code (Hex.) OMB2	Purpose
48	Set IDI0's counter match value
49	Set IDI1's counter match value
4A	Set IDI2's counter match value
4B	Set IDI3's counter match value
4C	Set IDI4's counter match value
4D	Set IDI5's counter match value
4E	Set IDI6's counter match value
4F	Set IDI7's counter match value

This command has no effect on a given IDI channel unless the UP counter function for that channel has been enabled.

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COMMAND CODE : 60

PURPOSE : Reads Interrupt Flags

OMB3	OMB2	OMB1	OMB0
0x00	0x60	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x60	XX	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB0: Bit 0: "1" means an IDI pattern match interrupt occurred.

Bit 1: "1" means an IDI change of state interrupt occurred.

Bit 2: "1" means an IDI's counter overflow or counter value match interrupt occurred.

The purpose of this command is to read the interrupt status of the PCI-1760U card. The interrupt status includes:

1. IDI pattern match interrupt status displayed in bit 0 of IMB0.
2. IDI change of state interrupt status displsyed in bit 1 of IMB0.
3. IDI's counter overflow or counter value match interrupt status displayed in bit 2 of IMB0.

When a high signal appears in bit 0, bit 1 or bit 2, one or more than one interrupt signal has been generated to the system. A user might find the sources of the interrupts by using related commands.

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COMMAND CODE: 61

PURPOSE: Reads IDI Edge Change Flags

OMB3	OMB2	OMB1	OMB0
0x00	0x61	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x61	0x00 ~ 0xFF	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB1: In bit n: “1” means the last signal change at IDI channel n was from a high to a low signal; "0" means the last signal change was not from high to low (n = 1 ~ 7).

IMB0: In bit n: “1” means the last signal change at IDI channel n was from a low to a high signal; "0" means the last signal change was not from low to high (n = 1 ~ 7).

The purpose of this command is to check whether the last change of state at IDI channel n (n = 0 ~ 7) was from low to high or from high to low. If the reading in any bit of IMB0 or IMB1 is “1”, a change of input state has occurred. The first bit of IMB0/IMB1, bit 0, is represented IDI0, the second bit, bit 1, is represented IDI1 and so forth.

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COMMAND CODE: 62

PURPOSE: Reads the IDI's Counter Overflow/Value Match Flags

OMB3	OMB2	OMB1	OMB0
0x00	0x62	N/A	N/A

OMB2: Command code

If successful

IMB3	IMB2	IMB1	IMB0
0x00 ~ 0xFF	0x62	0x00 ~ 0xFF	0x00 ~ 0xFF

IMB3: IDI current values

IMB2: Command code echo

IMB1: In bit n, "1" means IDIn's UP counter overflowed and "0" means IDIn's UP counter did not overflow (n = 0 ~ 7).

IMB0: In bit n, "1" means IDIn's UP counter value matched the preset value and "0" means no match value occurred (n = 0 ~ 7).

The purpose of this command is to read IDIn's UP counter overflow/ value match flag. If the returned value is "1", it means there was an overflow or value match flag signal from the PCI-1760U. The overflow status is displayed in IMB1 and the match value status is displayed in IMB0. The first bit of IMB0/IMB1, bit 0, displays the flag for IDI0, the second bit, bit 1, displays the flag for IDI1, and so forth.

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APPENDIX C

PCI-1760U Command Codes Quick Reference

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PCI-1760U Command Code Quick Reference

RB	Command Code (Hex.)	Description
	0x00	Clears IMB2's contents to 0
	0x01	Enables/disables relay outputs
	0x02	Reads the relay status
	0x07	Reads the current status
	0x0E	Reads PCI-1760's firmware version
	0x0F	Reads PCI-1760's hardware version
V	0x10	Sets the High period value of PWM0
V	0x11	Sets the Low period value of PWM0
V	0x12	Sets the High period value of PWM1
V	0x13	Sets the Low period value of PWM1
V	0x14	Sets PWM0's burst count value
V	0x15	Sets PWM1's burst count value
V	0x1F	Enables/disables PWM outputs
V	0x20	Enables/disables the digital filter function of IDI
V	0x21	Enables/disables the pattern match function of IDI
V	0x22	Sets the pattern match value of IDI
V	0x23	Enables/disables the rising edge function of IDI
V	0x24	Enables/disables the falling edge function of IDI
V	0x28	Enables/disables the UP counter function of IDI
	0x29	Resets the UP counter of IDIn to its reset value
V	0x2A	Enables/disables the UP counter overflow interrupt function of IDI
V	0x2B	Enables/disables the UP counter value match interrupt function of IDI
V	0x2C	Sets the count edge of IDI's UP counter
	0x2F	Reads IDIn's UP counter current value
V	0x30	Sets the sampling number of the effective High period of IDI0
V	0x31	Sets the sampling number of the effective High period of IDI1
V	0x32	Sets the sampling number of the effective High period of IDI2
V	0x33	Sets the sampling number of the effective High period of IDI3
V	0x34	Sets the sampling number of the effective High period of IDI4
V	0x35	Sets the sampling number of the effective High period of IDI5
V	0x36	Sets the sampling number of the effective High period of IDI6
V	0x37	Sets the sampling number of the effective High period of IDI7

RB : Register can be read back

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RB	Command Code (Hex.)	Description
V	0x38	Sets the sampling number of the effective Low period of IDI0
V	0x39	Sets the sampling number of the effective Low period of IDI1
V	0x3A	Sets the sampling number of the effective Low period of IDI2
V	0x3B	Sets the sampling number of the effective Low period of IDI3
V	0x3C	Sets the sampling number of the effective Low period of IDI4
V	0x3D	Sets the sampling number of the effective Low period of IDI5
V	0x3E	Sets the sampling number of the effective Low period of IDI6
V	0x3F	Sets the sampling number of the effective Low period of IDI7
V	0x40	Sets IDI0's counter reset value
V	0x41	Sets IDI1's counter reset value
V	0x42	Sets IDI2's counter reset value
V	0x43	Sets IDI3's counter reset value
V	0x44	Sets IDI4's counter reset value
V	0x45	Sets IDI5's counter reset value
V	0x46	Sets IDI6's counter reset value
V	0x47	Sets IDI7's counter reset value
V	0x48	Sets IDI0's counter match value
V	0x49	Sets IDI1's counter match value
V	0x4A	Sets IDI2's counter match value
V	0x4B	Sets IDI3's counter match value
V	0x4C	Sets IDI4's counter match value
V	0x4D	Sets IDI5's counter match value
V	0x4E	Sets IDI6's counter match value
V	0x4F	Sets IDI7's counter match value
	0x60	Reads interrupt flags
	0x61	Reads IDI edge change flags
	0x62	Reads the IDI's counter overflow/value match flags

RB : Register can be read back

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