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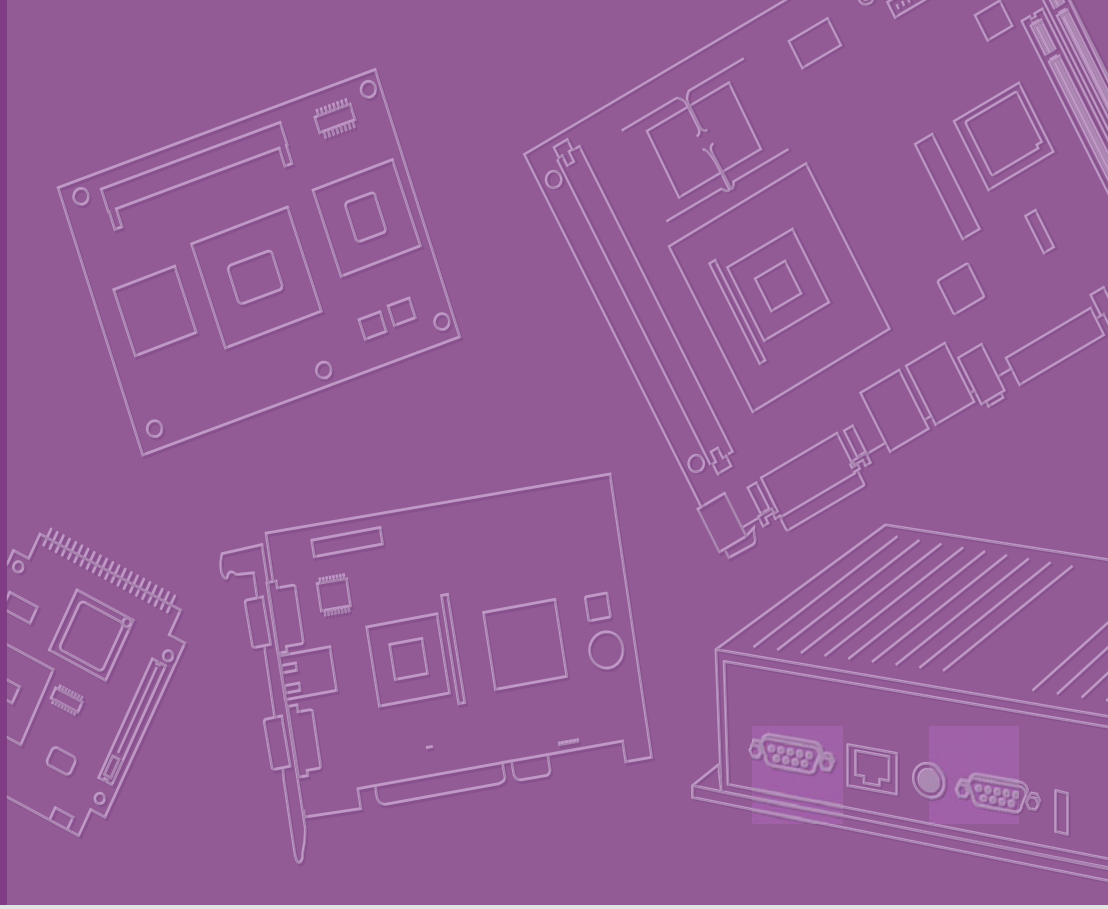
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User Manual

PCM-3353

PC/104+ SBC w/AMD LX800/ LX600, VGA, LCD, LAN, USB2.0 and CF

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ADVANTECH

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This manual is for the PCM-3353.

Part No. 2006335312 Edition 3

Printed in China September 2010

Declaration of Conformity

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommendedby the manufacturer. Discard used batteries according to the manufacturer's instructions.*



Technical Support and Assistance

1. Visit the Advantech web site at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x PCM-3353 SBC
- 1 x Power cable
- 1 x Audio cable (p/n:1700000918)
- 1 x COM cable (p/n: 1703040157)
- 1 x Four COM cable (p/n:1701400181)
- 1 x Keyboard/Mouse cable (p/n:1703060053)
- 1 x Y cable (for KB/MS extention) (p/n:1700060202)
- 1 x Ethernet RJ-45 Conn.conversion cable . (p/n:1701100202)
- 1 x LPT port cable (p/n:1700260250)
- 1 x IDE cable (p/n:1701440350)
- 1 x VGA cable (p/n:1700000898)
- 2 x USB cable (bracket type with two USB ports) (p/n:1703100121)
- 1 x Startup manual
- 1 x CD-ROM (Manual, Driver, Utility)

Model No. List	Description
PCM-3353F-L0A2E	PC/104+ SBC w/AMD LX800, VGA, LVDS, LAN, USB and CF
PCM-3353F-J0A2E	PC/1-4+ SBC w/AMD LX600, VGA, LVDS, LAN, USB and CF
PCM-3353Z-512A2E	PCM-3353F-L0A2E w/ phoenix gold package
PCM-3353Z2-512A2E	PCM-3353F-L0A2E w/ phoenix platinum package

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Chapter 1

General Information

This chapter gives background information on the PCM-3353.

1.1 Introduction

The PCM-3353 is a fanless, best-cost, performance PC/104+ SBC (Single Board Computer) geared to satisfy the needs for various industrial computing equipment. PCM-3353 is ideal for communication, gaming and medical applications that require flat panel support using digital displays with TTL and LVDS interfaces and single Ethernet ports.

For those who want superior performance for various low-power embedded applications, PCM-3353 uses an AMD LX-800 processor clocked at 500 MHz, in conjunction with onboard DDR333 system memory.

PCM-3353 offers convenient connector layout, easy assembly, multiple I/O, and includes single 10/100Mbps Ethernet, four USB (Universal Serial Bus) 2.0 and four serial ports for easy system expansibility.

1.2 Features

- AMD low power LX800 500MHz/LX600 366MHz Processor
- Supports DDR memory
- Supports 24-bit TFT LCD interface
- Supports 18-bit LVDS interface (supports 24-bit JEIDA LVDS)
- Supports 1 x 100Base-T Fast Ethernet
- Supports Four USB2.0 ports
- Supports Four COM ports
- PC/104+ expansion interface

1.3 Specifications

1.3.1 Standard PC/104 Biscuit SBC Functions

- **CPU:** AMD Geode® LX800/LX600 processor, up to 500 MHz
- **System memory:** Support SO-DIMM DDR 333/400 MHz, up to 1 GB
- **2nd cache memory:** 128 KB on the processor
- **System chipset:** AMD Geode LX800/LX600
- **BIOS:** AWARD 4Mbit Flash BIOS
- **Watchdog timer:** 255 levels timer interval
- **Expansion interface:** PC/104+
- **Battery:** Lithium 3V/196 mAH
- **Enhanced IDE interface:** One channel supports up to two EIDE devices. BIOS auto-detect, PIO Mode 3 or Mode 4, supports UDMA 33/66 mode
- **Serial ports:** Four serial RS-232 ports in one 40 pin connector (CN30: COM1/2/3/4). RS-422 and RS-485 in one pinheader (CN20) and can be configured via CN39 connector.
- **Parallel port:** One parallel port, supports SPP/EPP/ECP mode
- **Keyboard/mouse connector:** Supports one standard PC/AT keyboard and a PS/2 mouse
- **Audio:** Supports AC97 Audio stereo sound
- **USB:** Four USB 2.0 ports compliant universal serial bus ports
- **CF:** Solid State Disk (SSD) supports one 50-pin socket for CFC type I (type II optional)

1.3.2 VGA/LVDS Interface

- **Chipset:** AMD Geode LX800/LX600
- **Memory Size:** Optimized Shared Memory Architecture, supports 64 MB frame buffer using system memory
- **Resolution:** CRT resolution: up to 1600 x 1200 x 16 bpp at 100 Hz and up to 1024 x 768 x 32 bpp at 60 Hz for TFT LCD
- **LCD interface:** Supports up to 24-bit TFT LCD (TTL signal)
  Supports 18-bit LVDS LCD (supports 24-bit JEIDA LVDS)
- **Dual simultaneous display:** CRT + LCD, CRT + LVDS

1.3.3 Ethernet Interface

- **Chipset supports:** 1 x 10/100 Mbps - Intel 82541PI
- **Interface:** 1 x internal box header
- Standard IEEE 802.3u (100 BASE-T) protocol compatible

1.3.4 Audio Function

- **Audio controller:** Realtek ALC 203 chipset, supports AC97 3D Audio stereo sound
- **Audio interface:** Microphone in, Line in, Line out

1.3.5 OS support

- This board supports Win XP, Win CE and Win XPe.
- For further information about OS support in your PCM-3353, visit the following web resource Advantech: website: www.advantech.com or please contact technical support center

1.3.6 Mechanical and Environmental

- **Dimensions:** 96 x 115 mm (3.77"x 4.05"), Mechanical Drawing (dxf file) is available.
- **Power supply type:** AT
- **Power requirement:** +5 V ± 5%, +12 V ± 5% (Optional), (5V only, 12V optional for PC104 add on card and LCD inverter)
- **Power consumption:** (Geode LX800, 256 MB DDR333)
  - Max: +5 V @ 1.51 A, +12 V @ 0.1 A
  - Typical: +5 V @ 1.35 A, +12 V @ 0.1A
- **Operating temperature:** 0 ~ 60° C (32 ~ 140° F)
- **Operating humidity:** 10% ~ 90% relative humidity, non-condensing
- **Weight:** 0.85 kg (reference weight of total package)

1.4 Board Layout: Dimensions

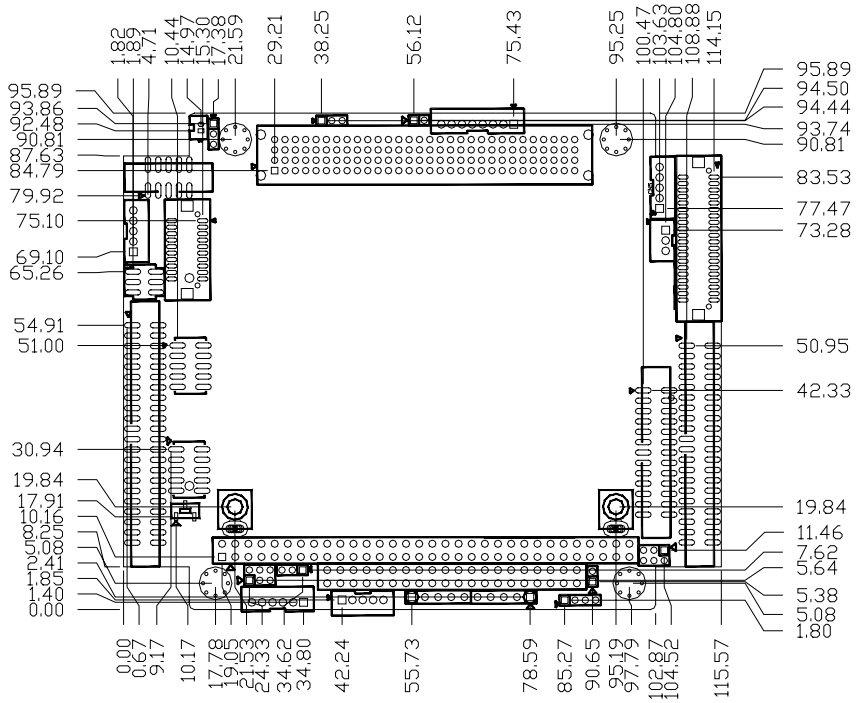


Figure 1.1 Board layout: dimensions (component side)

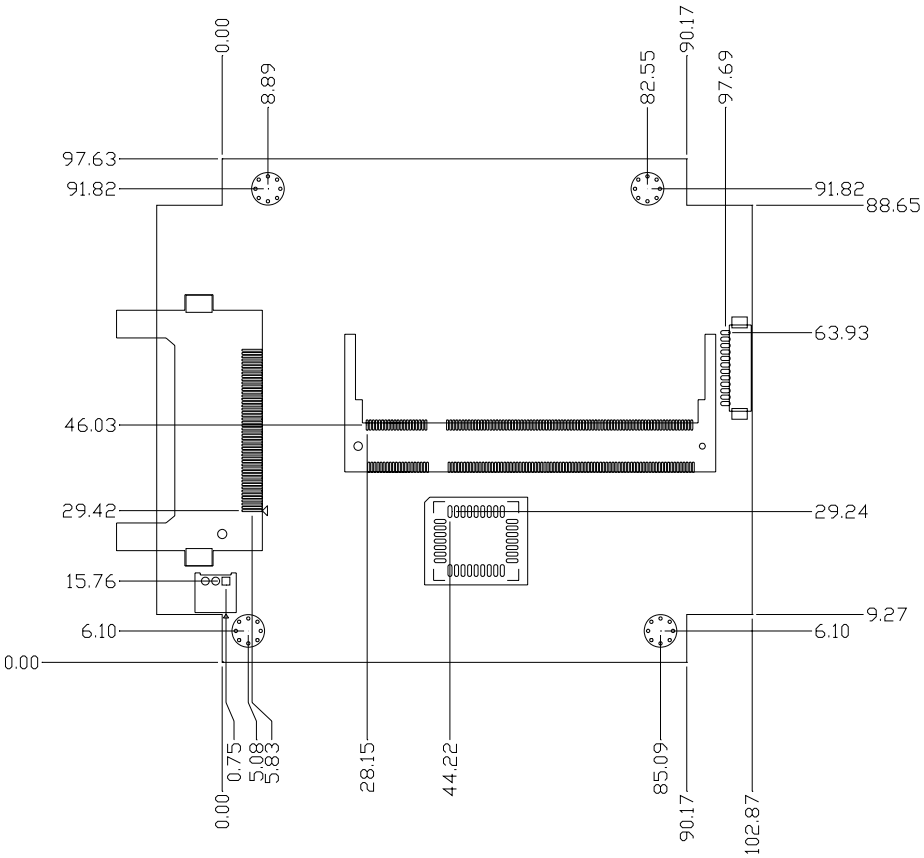


Figure 1.2 Board layout: dimensions (solder side)

Chapter 2

Installation

This chapter explains the setup procedures of the PCM-3353 hardware, including instructions on setting jumpers and connecting peripherals, switches and indicators. Be sure to read all safety precautions before you begin the installation procedure.

2.1 Jumpers

The PCM-3353 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

Table 2.1: Jumper/Switch Setting	
J3	Clear CMOS
J5	PCI VI/O Power Selector
CN39	COM2 Setting
SW1	CF Master / Slave Selector
J6	LVDS Power Selector

2.2 Connectors

Onboard connectors link the PCM-3353 to external devices such as hard disk drives, a keyboard, or floppy drives. The table below lists the function of each of the board's connectors.

Table 2.2: Connector Table	
CN4	TFT LCD I/F
CN5	Inverter Power
CN6	SMBus
CN11	IDE
CN15	USB1/2 / CN17 USB 3/4
CN18	KB/MS
CN19	Print Port
CN20	RS422/485
CN23	ISA -5 V & -12 V Input
CN26	LAN
CN27	CRT
CN30	COM1/2/3/4
CN32	Reset / Buzzer pin header
CN33	Battery Connector
CN35	AUDIO-OUT / CN34 AUDIO-IN
CN36	GPIO1
CN37	GPIO2
CN38	Power Input
CN40	DDR RAM Socket
CN41	CF Socket
CN42	LVDS LCD I/F
CN43	Inverter Power (LVDS)

2.3 Locating Connectors

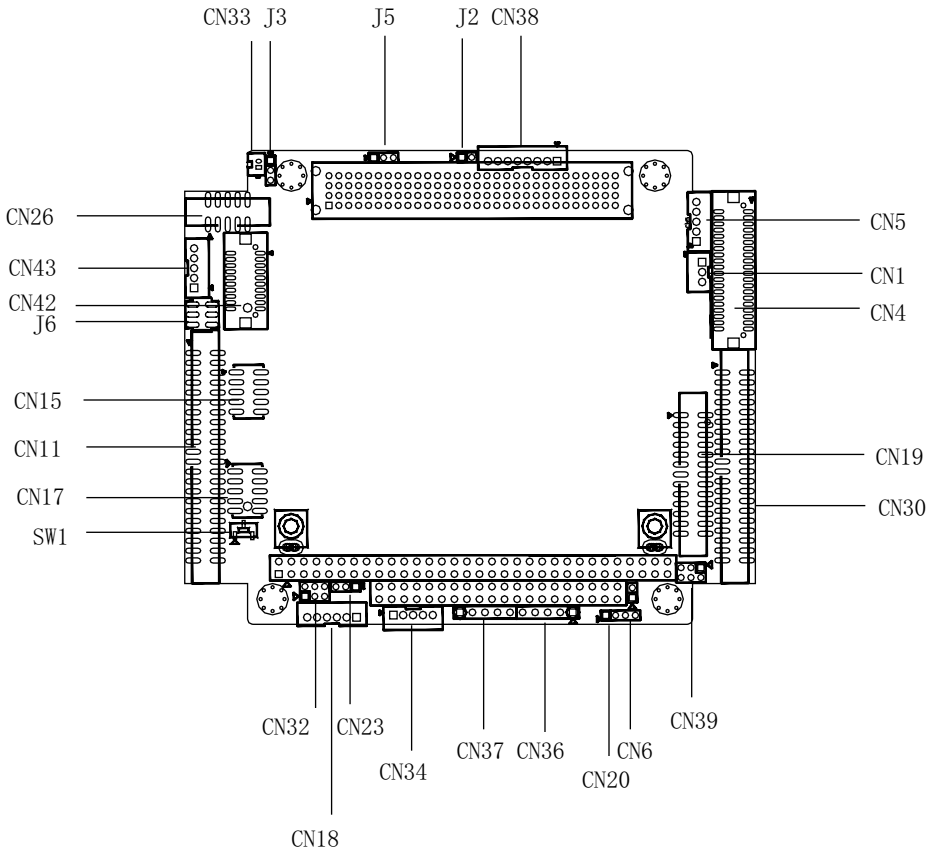


Figure 2.1 Connectors (component side)

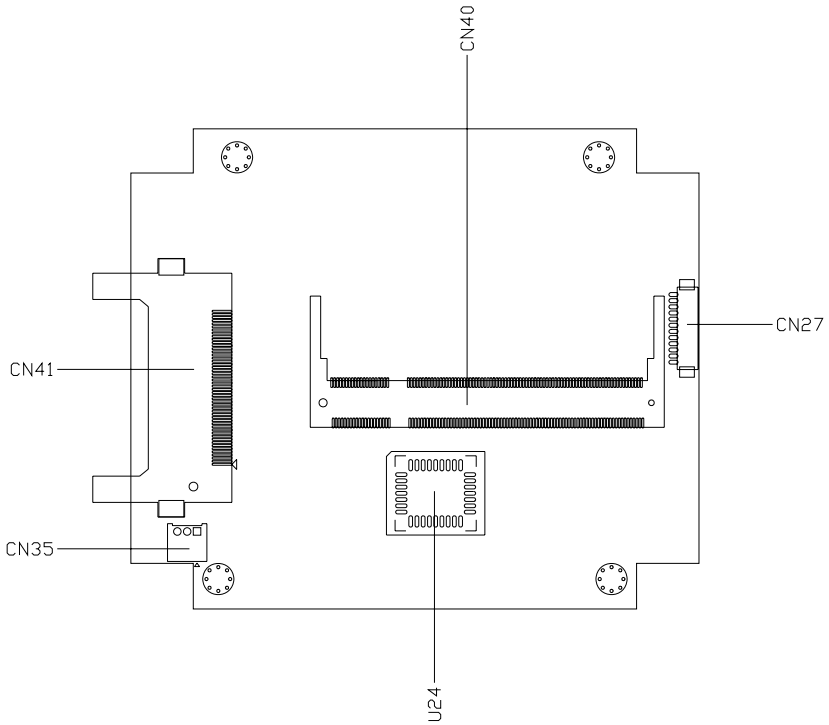
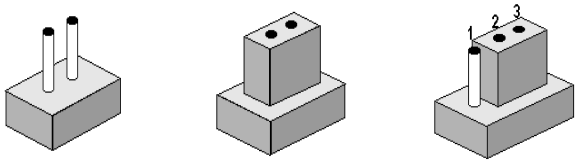


Figure 2.2 Connectors (solder side)

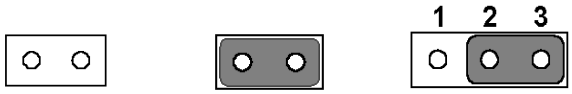
2.4 Setting Jumpers

You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper, you connect the pins with the clip. To “open” a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



open closed closed 2-3

The jumper settings are schematically depicted in this manual as follows:.



open closed closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

2.5 Installing SO-DIMMs

The procedures for installing SODIMMs are described below. Please follow these steps carefully. You can install SDRAM memory modules using 200-pin SODIMMs (Small Outline Dual In-line Memory Modules).

1. Ensure that all power supplies to the system are switched off.
2. Tilt the SODIMM card just above the board and slide it into the housing card slot.
3. Push the module into the socket until the module gently snaps in. There should only be a slight insertion force to engage the module into the contacts. Make sure that the module and the housing are aligned and locked in place.

2.6 IDE, CDROM Hard Drive Connector (CN11)

The board provides 1 IDE channel which you can attach up to two Enhanced Integrated Drive Electronics hard disk drives or CDROM to the board's internal controller. Its IDE controller uses a PCI interface. This advanced IDE controller supports faster data transfer, PIO mode 3, mode 4 and up to UDMA 33/66.

2.6.1 Connecting the Hard Drive

Connecting drives is done in a daisy-chain fashion. This package includes One 44 PIN IDE cable that can connect to 1.8" and 2.5" drives.

1. Connect one end of the cable to Hard Drive connector. Make sure that the red (or blue) wire corresponds to pin 1 on the connector, which is labeled on the board (on the right side).
2. Plug the other end of the cable into the Enhanced IDE hard drive, with pin 1 on the cable corresponding to pin 1 on the hard drive. (See your hard drive's documentation for the location of the connector.)

If desired, connect a second drive as described above.

Unlike floppy drives, IDE hard drives can connect to either end of the cable. If you install two drives, you will need to set one as the master and one as the slave by using jumpers on the drives. If you install only one drive, set it as the master.

2.7 Solid State Disk

The board provides a CompactFlash card type I socket and type II for optional kit.

2.7.1 Compact Flash (CN41)

The CompactFlash card shares a secondary IDE channel which can be enabled/disabled via the BIOS settings.

2.8 Parallel Port Connector (CN19)

Normally, the parallel port is used to connect the cable to a printer. The board includes a multi-mode (ECP/EPP) parallel port accessed via CN19 and a 26-pin flat-cable connector. You will need an adapter cable if you use a traditional DB-25 connector. The adapter cable has a 26-pin connector on one end, and a DB-25 connector on the other.

The parallel port is designated as LPT1, and can be disabled or changed to LPT2 or LPT3 in the system BIOS setup.

The parallel port interrupt channel is designated to be IRQ7.

You can select ECP/EPP/ECP DMA channel via BIOS setup.

2.9 Keyboard and PS/2 Mouse Connector (CN18)

The board provides a keyboard connector that supports both a keyboard and a PS/2 style mouse. In most cases, especially in embedded applications, a keyboard is not used. If the keyboard is not present, the standard PC/AT BIOS will report an error or fail during power-on self-test (POST) after a reset. The PCM 3353's BIOS standard setup menu allows you to select "All, But Keyboard" under the "Halt On" selection. This allows no-keyboard operation in embedded system applications, without the system halting under POST.

2.10 Power Connectors (CN38)

2.10.1 Main Power Connector, +5 V, +12 V (CN38)

Supplies main power +5 V to the PCM-3353, and to devices that require +12 V.

2.10.2 Power Reset Button

Momentarily pressing the reset button will activate a reset. The switch should be rated for 10 mA, 5 V.

2.11 Audio Interfaces (CN34/35)

2.11.1 Audio Connector Audio-out(CN35), Audio-in(CN34)

The board provides all major audio signals on a 8-pin cable connector, These audio signals include Microphone in (mono), Line in (stereo) and Line out (stereo).

2.12 COM Port Connector (CN20,CN30)

The board provides four serial ports: Four serial RS-232 ports in one 40 pin connector (CN30: COM1/2/3/4). It provides connections for serial devices or a communication network. You can find the pin assignments for the COM port connector in Appendix C.

2.12.1 Serial Port RS-422/485 (CN20)

Serial port can be configured to operate in RS-422 and RS-485 mode. RS-422 and RS-485 in one pinheader (CN20) and can be configured via CN39 connector.

Table 2.3: Serial Port RS-422/485 (CN39)

Setting	Function
1-2 (default)	RS-232
3-4	RS-485
5-6	RS-422

2.13 VGA/LCD Interface Connections

The board's PCI SVGA interface can drive conventional CRT displays and is capable of driving a wide range of flat panel displays.

2.13.1 CRT Display Connector (CN27)

The CRT display connector is a 15-pin D-SUB connector used for conventional CRT displays.

2.13.2 TTL TFT LCD Connector (CN4)

For PCM-3353 series, CN4 consists of a 40-pin connector which can support up to 24-bit LCD panel. It is Hirose's product no. DF13A-40DP-1.25 V

2.13.3 LVDS TFT LCD Connector (CN42)

Four PCM-3353 series, the board supports 1 channel 18-bit LVDS LCD panel displays.

2.14 Ethernet Configuration

The board is equipped with one high performance 32-bit PCI-bus Ethernet interface which are fully compliant with IEEE 802.3U 10/100Mbps standards. They are supported by all major network operating systems.

2.14.1 100Base-T Connector (CN26)

100Base-T connections are made via one internal 10-pin box header.

2.15 Watchdog Timer Configuration

An onboard watchdog timer reduces the chance of disruptions which EMP (electromagnetic pulse) interference can cause. This is an invaluable protective device for standalone or unmanned applications. Setup involves one jumper and running the control software (refer to Appendix A).

2.16 USB Connectors (CN15,CN17)

The board provides up to four USB (Universal Serial Bus) ports using Plug and Play. The USB interfaces comply with High Speed USB specification Rev. 2.0 which supports 480 Mbps transfer rate, and are fuse protected.

The USB interface is accessed through two 5 x 2-pin flat-cable connectors. You will need an adapter cable if you use a standard USB connector. The adapter cable has a 5 x 2-pin connector on one end and a USB connector on the other.

The USB interfaces can be disabled in the system BIOS setup.

2.17 GPIO (General Purpose Input Output) (CN36/CN37)

The board supports 8-bit GPIO through GPIO connector. The 8 digital inputs and outputs can be programmed to read or control devices, with each input or output defined. The default setting is 8 bits input.

Chapter 3

Award BIOS Setup

3.1 Introduction

Award's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed memory (CMOS RAM) so that it retains the setup information when the power is turned off.

3.1.1 CMOS RAM Auto-backup and Restore

The CMOS RAM is powered by an onboard button cell battery. When you finish BIOS setup, the data in CMOS RAM will be automatically backed up to Flash ROM. If operation in harsh industrial environments causes a software error, the BIOS will recheck the data in CMOS RAM and automatically restore the original data in Flash ROM to CMOS RAM for booting.

3.2 Entering Setup

Turn on the computer and check for the ìpatch codeî. If there is a number assigned to the patch code, it means that the BIOS supports your CPU.

If there is no number assigned to the patch code, please contact Advantechís applications engineer to obtain an up-to-date patch code file. This will ensure that your CPUís system status is valid. After ensuring that you have a number assigned to the patch code, press <Del> to enter the setup.

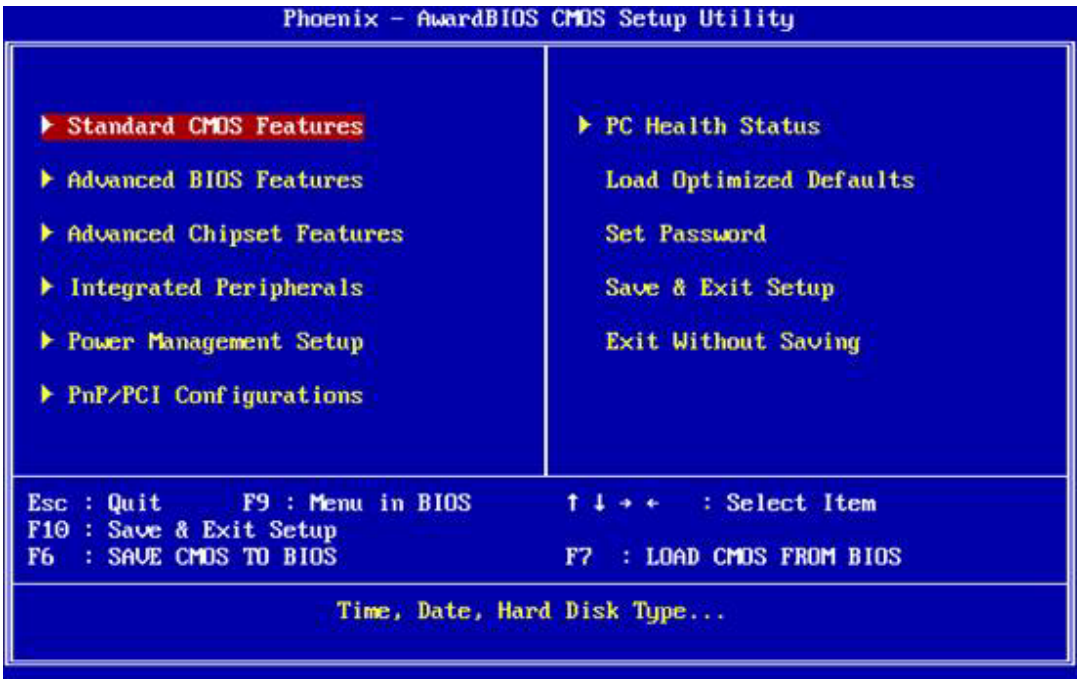


Figure 3.1 Award BIOS setup initial screen

Note! *If you intend to change the CMOS setting without restoring the previous backup, you have to click on "DEL" within two seconds of the "CMOS checksum error..." display screen message appearing. Then enter the "Setup" screen to modify the data. If the "CMOS checksum error..." message appears again and again, please check to see if you need to replace the battery in your system.*

3.3 Standard CMOS Setup

Choose the “Standard CMOS Features” option from the “Initial Setup Screen” menu, and the screen below will be displayed. This menu allows users to configure system components such as date, time, hard disk drive, video, Halt On, display, and memory.

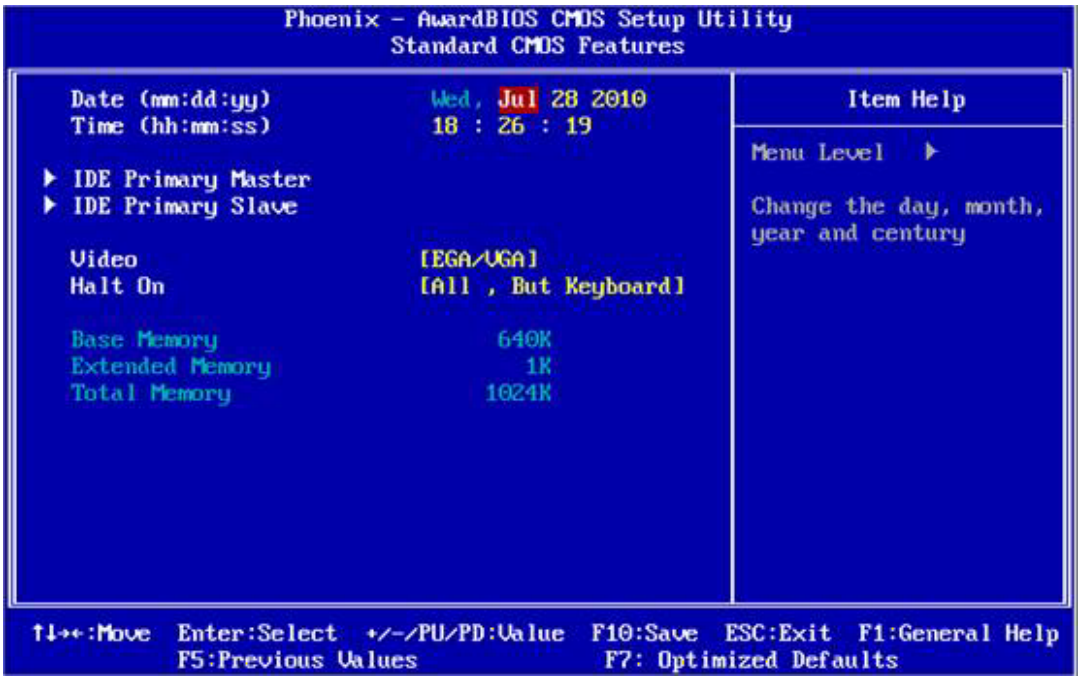


Figure 3.2 Standard CMOS setup screen

- **Date**
  The date format is <Weekday>, <Month>, <Day>, <Year>.
- **Time**
  The time format is in <hours> : <minutes> : <seconds>, based on 24-hour time.
- **IDE Primary Master/Slave**
  IDE HDD Auto-Detection. Press "Enter" for automatic device detection.
- **Halt on**
  The item determines whether the computer will stop if an error is detected during power up.
- **Base Memory**
  The BIOS POST displays the amount of base (or conventional) memory installed in the system.
- **Extended Memory**
  The BIOS POST displays the amount of extended memory (above 1 MB in the CPU’s memory address map) installed in the system.
- **Total Memory**
  This item displays the total system memory size.

No Errors	The system boot will not stop for any error.
All Errors	Whenever the BIOS detects a non-fatal error the system will be stopped.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors. (Default value)

3.4 Advanced BIOS Features

The “Advanced BIOS Features” screen appears when choosing the “Advanced BIOS Features” item from the ìInitial Setup Screenî menu. It allows the user to configure the board according to his particular requirements. Below are some major items that are provided in the Advanced BIOS Features screen. A quick booting function is provided for your convenience. Simply enable the Quick Booting item to save yourself valuable time.

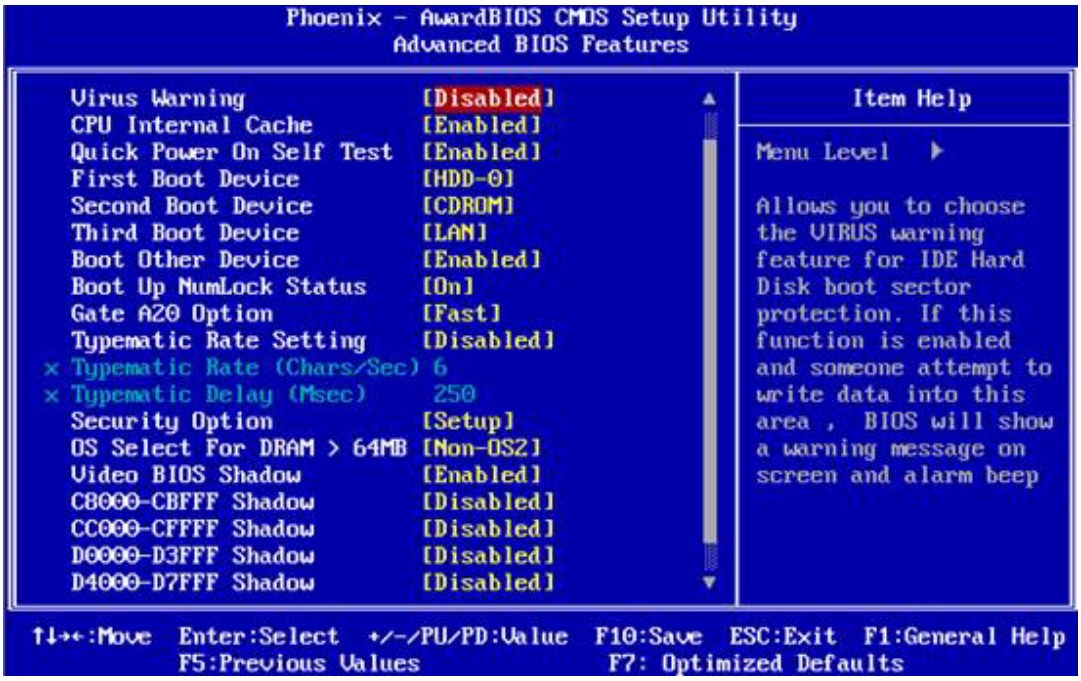


Figure 3.3 Advanced BIOS features screen

- **Virus Warning**

  If enabled, a warning message and alarm beep activates if someone attempts to write here. The commands are ìEnabledî or ìDisabled.î

- **CPU Internal Cache**

  This item allows user to enable CPU internal cache. (Disable is sometimes useful for troubleshooting.)

- **Quick Power On Self Test**

  This BIOS feature allows you to decrease the time it takes to boot up the computer by shortening or skipping certain standard booting procedures.

  If enabled, the BIOS will shorten the booting process by skipping some tests and shortening others. If disabled, the BIOS will run the whole gamut of boot-up tests

- **First/Second/Third/Other Boot Device**

Floppy	Assign this boot device priority to Floppy.
HDD	Assign this boot device priority to Hard Disk.
CDROM	Assign this boot device priority to CDROM.
USB-FDD	Assign this boot device priority to USB-FDD.
USB-CDROM	Assign this boot device priority to USB-CDROM.
USB-HDD	Assign this boot device priority to USB-HDD.
LAN	Assign this boot device priority to LAN.

Disabled Do not assign this boot priority.

- **Boot Up NumLock Status [On]**
  When enabled, the keyboard keypad boots up in number mode. When disabled, the keypad boots up in cursor control mode (arrow mode).
- **Gate A20 Option [Fast]**
  This item enables users to switch A20 control by port 92 or not.
- **Typematic Rate Setting [Disabled]**
  This item enables users to enable or disable typematic action. When enabled, they can set the two typematic controls items, controlling the speeds of:
  - Typematic Rate (Chars/Sec)
    This item controls the speed at which the system registers repeated key-strokes.The eight settings are 6, 8, 10, 12, 15, 20, 24 and 30 characters/second.
  - Typematic Delay (Msec)
    This item sets the keypress delay before typematic repetition kicks in. The four delay options are 250, 500, 750 and 1000 milliseconds.

Note! *These typematic settings apply to systems that communicate with the keyboard via BIOS. For Windows systems, typematic settings are controlled by keyboard driver settings in Windows Control Panel.*

- **Security Option [Setup]**
  System System can not boot and can not access to Setup page if the correct password is not entered at the prompt.
  Setup System will boot, but access to Setup is denied if the correct password is not entered at the prompt. (Default value)

Note! *To disable security, select PASSWORD SETTING in the main menu. Then you will be asked to enter a password. Simply press <Enter> to disable security. When security is disabled, the system will boot and you can enter Setup freely.*

- **OS Select For DRAM > 64M [Non-OS2]**
  Select OS2 only if system is running OS/2 operating system with greater than 64 MB of RAM on the system.
- **Video BIOS Shadow [Enabled]**
  For copying of video BIOS to shadow RAM--sometimes improves performance.
  - C8000-CBFFF Shadow [Disabled]
    Control copying of this block to shadow RAM.
  - CC000-CFFFF Shadow [Disabled]
    Control copying of this block to shadow RAM.
  - D0000-D3FFF Shadow [Disabled]
    Control copying of this block to shadow RAM.
  - D4000-D7FFF Shadow [Disabled]
    Control copying of this block to shadow RAM.
  - D8000-DBFFF Shadow [Disabled]
    Control copying of this block to shadow RAM.
  - DC000-DFFFF Shadow [Disabled]
    Control copying of this block to shadow RAM.

- **Small Logo (EPA) Show [Disabled]**
  Show EPA logo during system post stage.
- **Cyrix 6X86/MII CPUID [Enabled]**
  This item allows user to control BIOS enabled or disabled CPUID for CPU Cyrix/MII.

3.5 Advanced Chipset Features

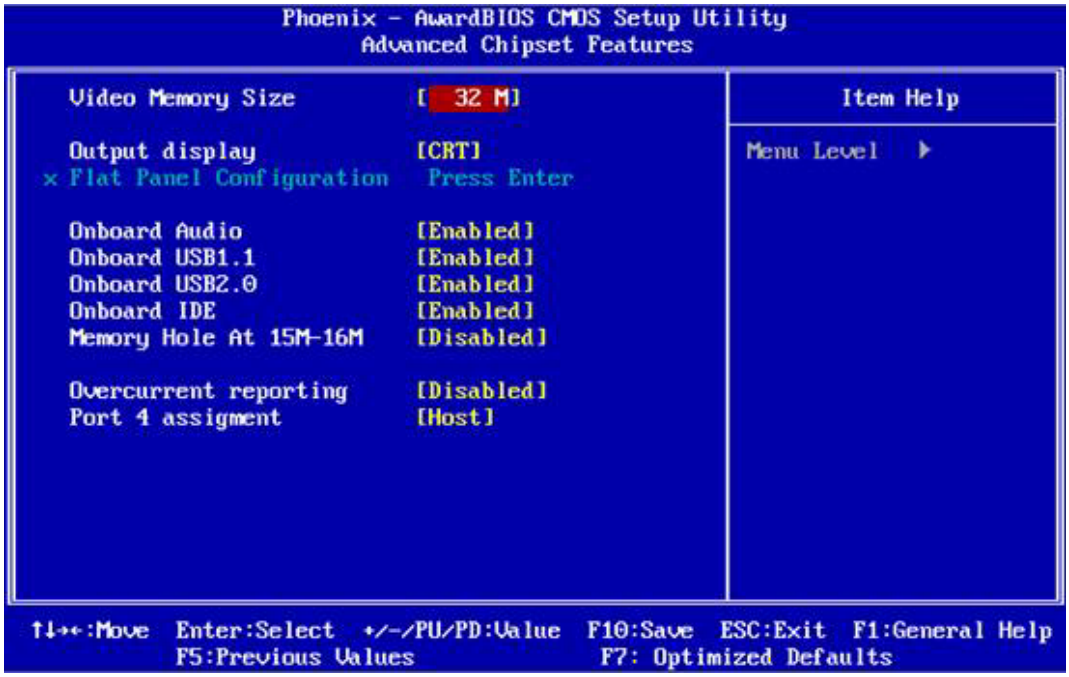


Figure 3.4 Advanced chipset features screen

Note! *This Advanced Chipset Features screen controls the configuration of the board's chipset for fine-tuning system performance. Screen options depend on the specific chipset. It is strongly recommended that only technical users make changes to the default settings.*

- **Video Memory Size [32 M]**
  This item allows user to adjust VGA shared memory size.
- **Output Display [CRT]**
  This item allows the user to choose screen display type: "Flat Panel", "CRT" and "Panel & CRT". BIOS default value is set to "CRT".
- **Flat Panel Configuration [Press Enter] (Show Only)**
  This item provides flat panel adjustments.
- **Onboard USB1.1 [Enabled]**
  This item enables or disables motherboard USB1.1 device.
- **Onboard USB2.0 [Enabled]**
  This item enables or disables motherboard USB2.0 device.
- **Onboard IDE [Enabled]**
  This item enables or disables motherboard IDE device.

- **Memory Hole At 15 M-16 M [Disabled]**
  This item reserves 15 MB-16 MB memory address space to ISA expansion cards that specifically require the setting. Memory from 15 MB-16 MB will be unavailable to the system because only expansion cards can access memory in this area.
- **Overcurrent Reporting [Disabled]**
  This item enables or disables USB overcurrent reporting function. Suggest leaving on default setting (Disabled).
- **Port 4 assignment [Host]**
  This item allows user to change mode of USB port 4. The selections are "Host", "Device", or "Not Used".

3.6 Integrated Peripherals

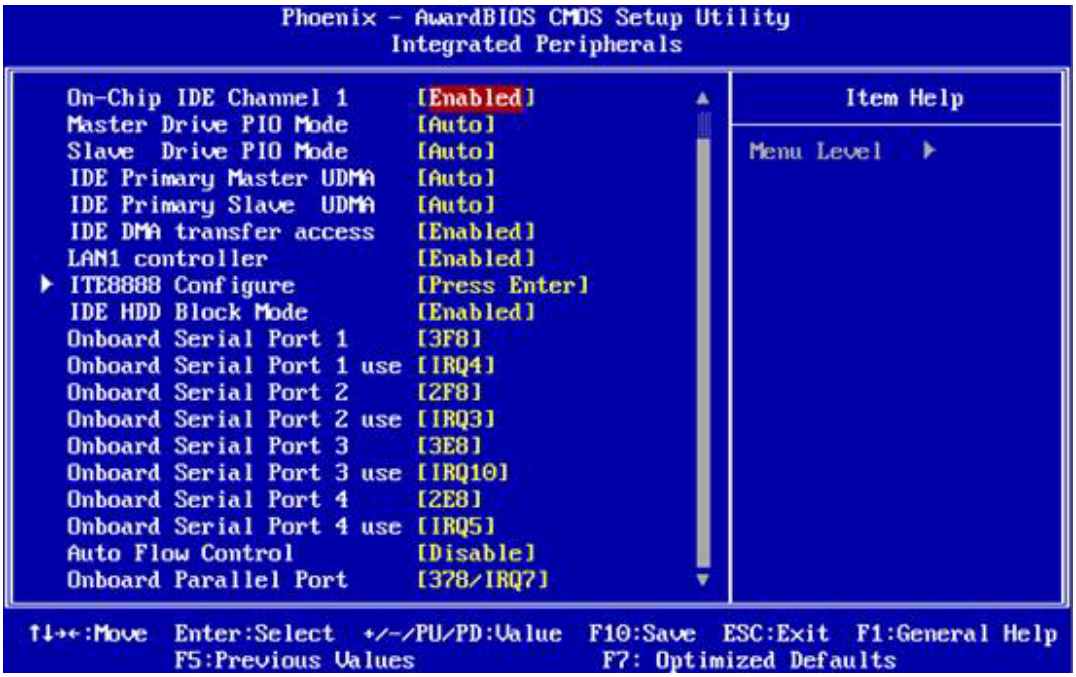


Figure 3.5 Integrated peripherals screen

- **IDE Master/Slave PIO/UDMA Mode,**
  IDE Master/Slave PIO/UDMA Mode (Auto) has a master and a slave, making two IDE devices possible. Because each IDE device may have a different Mode timing (0, 1, 2, 3, 4), it is necessary for these to be independent. The default setting “Auto” will allow auto detection to ensure optimal performance.
- **Master Drive PIO Mode [Auto]**
  This item allows user to adjust master IDE mode of type for modification purpose. Suggested BIOS default value is "Auto".
- **Slave Drive PIO Mode [Auto]**
  This item allows user to adjust slave IDE mode of type for modification purpose. Suggested BIOS default value is "Auto".
- **IDE Primary Master UDMA [Auto]**
  This item allows user to adjust primary master IDE mode of type for modification purpose. Suggested BIOS default value is "Auto".

- **IDE Primary Slave UDMA [Auto]**
  This item allows adjustment of primary slave IDE mode or type for modification purposes. Suggested BIOS default value is "Auto".
- **IDE DMA transfer access [Enabled]**
  This item allows adjustment of IDE DMA mode. Enabling increases IDE Data transfer speed. Suggested BIOS default value is "Enabled".
- **LAN1 controller [Enabled]**
  This item enables/disables the onboard LAN switch.
- **ITE8888 Configure [Press Enter]**
  This item allows user to make detailed ITE8888 adjustments.
- **IDE HDD Block Mode [Enabled]**
  This item allows enabling or disabling IDE block data transfer mode. When enabled, it will speed up HDD data transfer of efficiency. Suggested BIOS default value is "Enabled".
- **LPT/FDC switch: [Disabled]**
  This item enables/disables the LPT/FDC port switch. When enabled, it will change from LPT to FDC port. Suggested BIOS default value is "Disabled".
- **Onboard Serial Port 1 [3F8]**
  This item allows user to change COM 1 address. Suggested BIOS default value is "3F8".
- **Onboard Serial Port 1 use [IRQ4]**
  This item allows user to change COM 1 IRQ. Suggested BIOS default value is "IRQ4".
- **Onboard Serial Port 2 [2F8]**
  This item allows user to change COM 2 address. Suggested BIOS default value is "2F8".
- **Onboard Serial Port 2 use [IRQ3]**
  This item allows user to change COM 2 IRQ. Suggested BIOS default value is "IRQ3".
- **Onboard Serial Port 3 [3E8]**
  This item allows user to change COM 3 address. Suggested BIOS default value is "3E8".
- **Onboard Serial Port 3 use [IRQ10]**
  This item allows user to change COM 3 IRQ. Suggested BIOS default value is "IRQ10".
- **Onboard Serial Port 4 [2E8]**
  This item allows user to change COM 4 address. Suggested BIOS default value is "3E8".
- **Onboard Serial Port 4 use [IRQ5]**
  This item allows user to change COM 4 IRQ. Suggested BIOS default value is "IRQ5".
- **Auto Flow Control [Disabled]**
  This item allows user to control COM port auto flow transfer. Suggested BIOS default value is "Disabled".
- **Onboard Parallel Port [378/IRQ7]**
  This item allows user to change parallel port address. Suggested BIOS default value is "378/IRQ7".

- **Parallel Port Mode [Standard]**
  This item allows user to change parallel port mode. User can choose "SPP", "EPP", "ECP" and "ECP+EPP". SPP (Standard Parallel Port). ECP (Extended Capabilities Port). EPP (Enhanced Parallel Port). Suggested BIOS default value is "Normal".
- **ECP Mode Use DMA [3]**
  This selection is available only if you select ìECPî or ìECP + EPPî in the Parallel Port Mode field. In ECP Mode Use DMA, you can select DMA channel 1, DMA channel 3, or Disable. Leave this field on the default setting.

3.7 Power Management Setup

The power management setup controls the CPU cardís ìgreenî features to save power. The following screen shows the manufacturerís defaults:

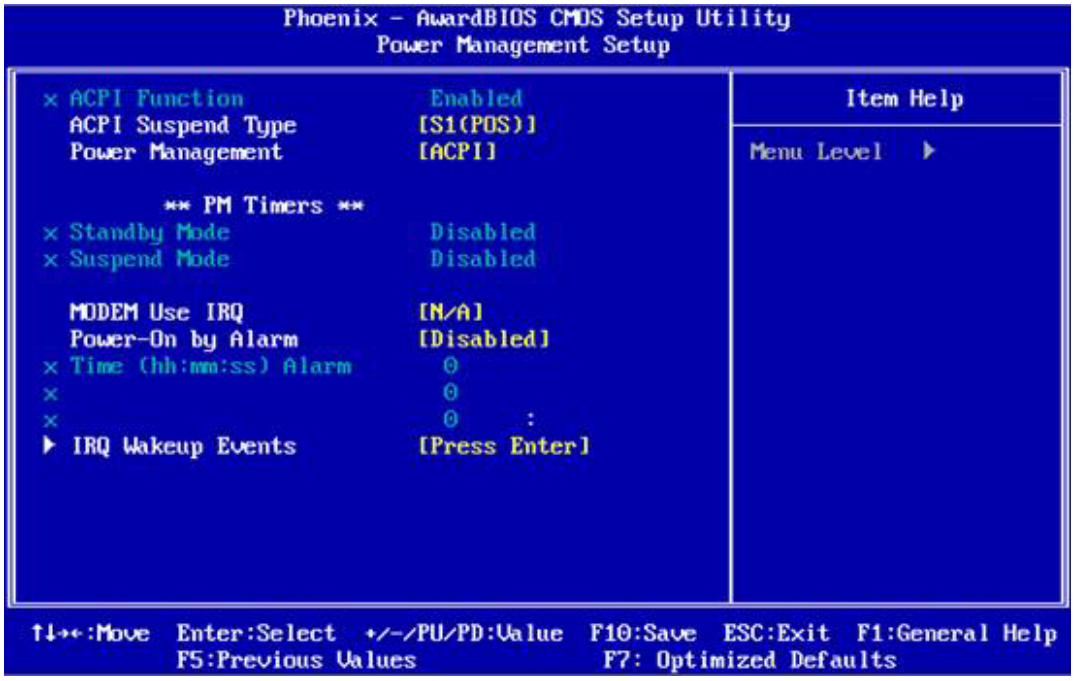


Figure 3.6 Power management setup screen

- **ACPI function**
  The choices: Enabled, Disabled.
- **ACPI Suspend Type**
  This item only support S1 function.
- **Power Management**
  This category allows you to select the type (or degree) of power saving and is directly related to the following modes:
  1. HDD Power Down
  2. Suspend Mode

  There are four selections for Power Management, three of which have fixed mode.

  Settings

  This item determines delay time for the watchdog timer.

  Min. Power Saving Minimum power management., Suspend Mode = 1 hr., and HDD Power Down = 15 min.

Max. Power Saving Maximum power management., Suspend Mode = 1 min., and HDD Power Down = 1 min.

User Defined (Default) Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

- **Modem Use IRQ**

  This determines the IRQ which the MODEM can use. The choices: 3, 4, 5, 7, 9, 10, 11, NA.

- **Power-On by Alarm [Disabled]**

  This item allows users to power on the system at a specified date and time.

  Disabled Disables this function.

  Enabled Enables alarm function to power on system Day (of the month) Alarm 1-31 Time (HH:MM:SS) Alarm (0-23): (0-59): 0-59)

- **IRQ Wakeup Events [Press Enter]**

  This item allows user to control wakeup from an IRQ event.

3.8 PnP/PCI Configurations

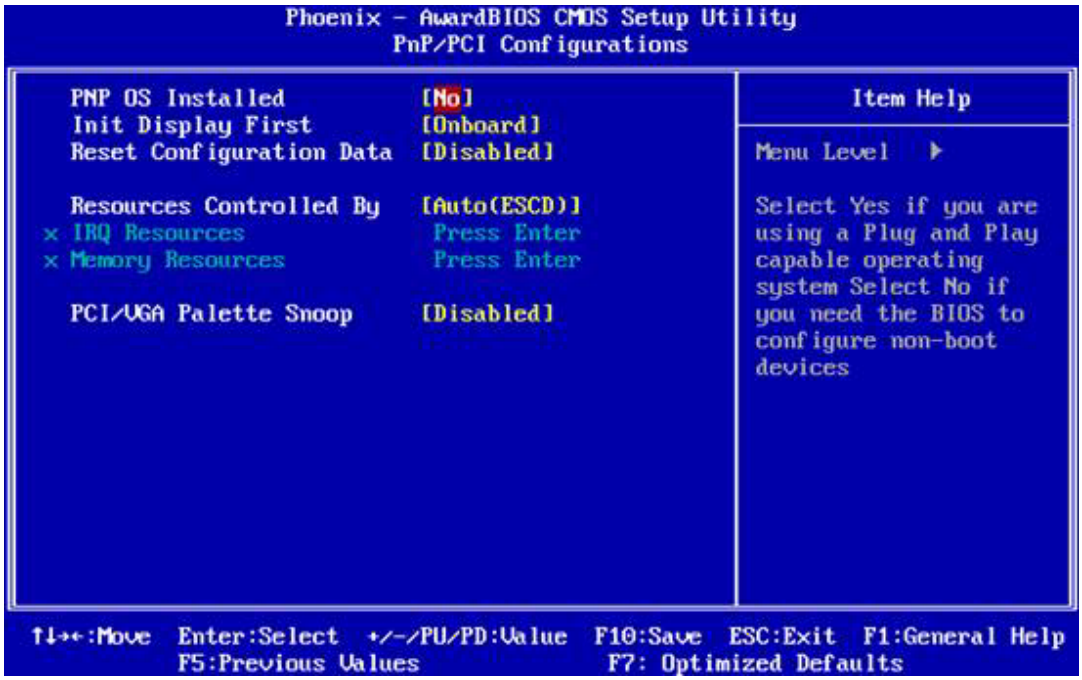


Figure 3.7 PnP/PCI configurations screen

- **PnP OS Installed**

  Select Yes if you are using a plug and play capable operating system. Select No if you need the BIOS to configure non-boot device.

- **Init Display First [Onboard]**

  This item allows user to change boot display sequence.

- **PNP OS Installed [No]**

  Usually best set to No. Some rare cases may need to set to Yes.

- **Reset Configuration Data [Disabled]**

  This item allows user to clear any PnP configuration data stored in the BIOS.

- **Resources Controlled By [Auto (ESCD)]**
  - IRQ Resources
    This item allows you respectively to assign interrupt types for IRQ-3, 4, 5, 7, 9,10, 11,12, 14, and 15.
  - Memory Resources
    This item allows you respectively to assign memory blocks from N/A to DC00.
- **PCI VGA Palette Snoop [Disabled]**
  The item is designed to solve problems caused by some non-standard VGA cards. A built-in VGA system does not need this function.

3.9 PC Health Status

This is to check the PC health, e.g.: current CPU temperature.

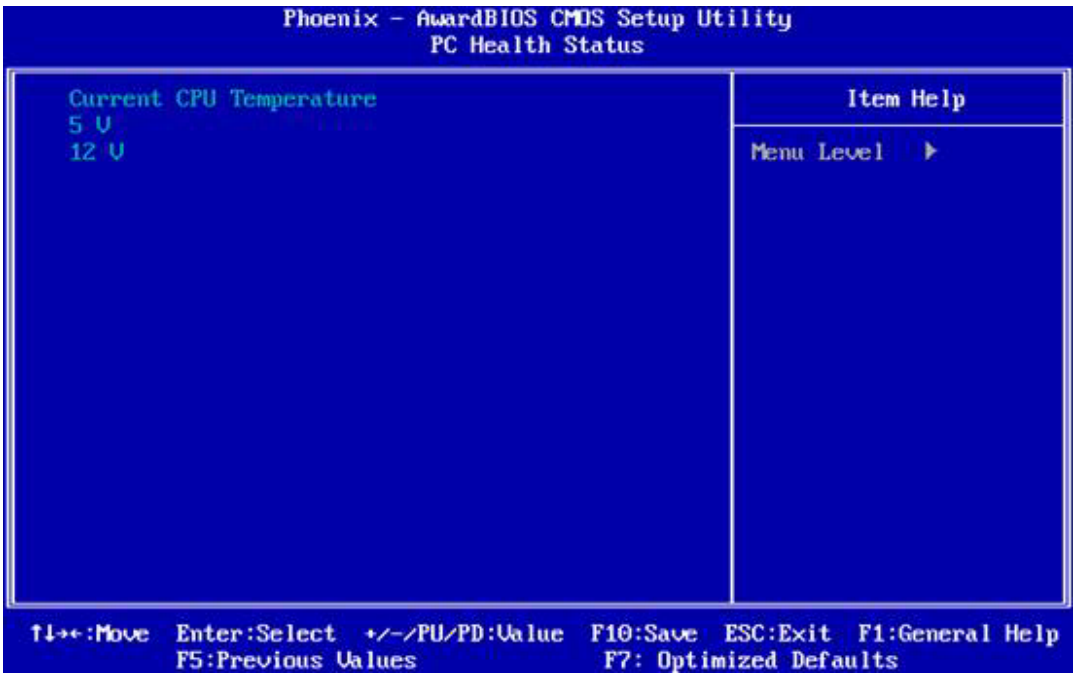


Figure 3.8 PC health status screen

- **Current CPU Temp [Show Only]**
  This item displays current system and CPU temperature.
- **5 V / 12 V [Show Only]**
  This item displays current CPU and system Voltage.

3.10 Load Optimized Defaults

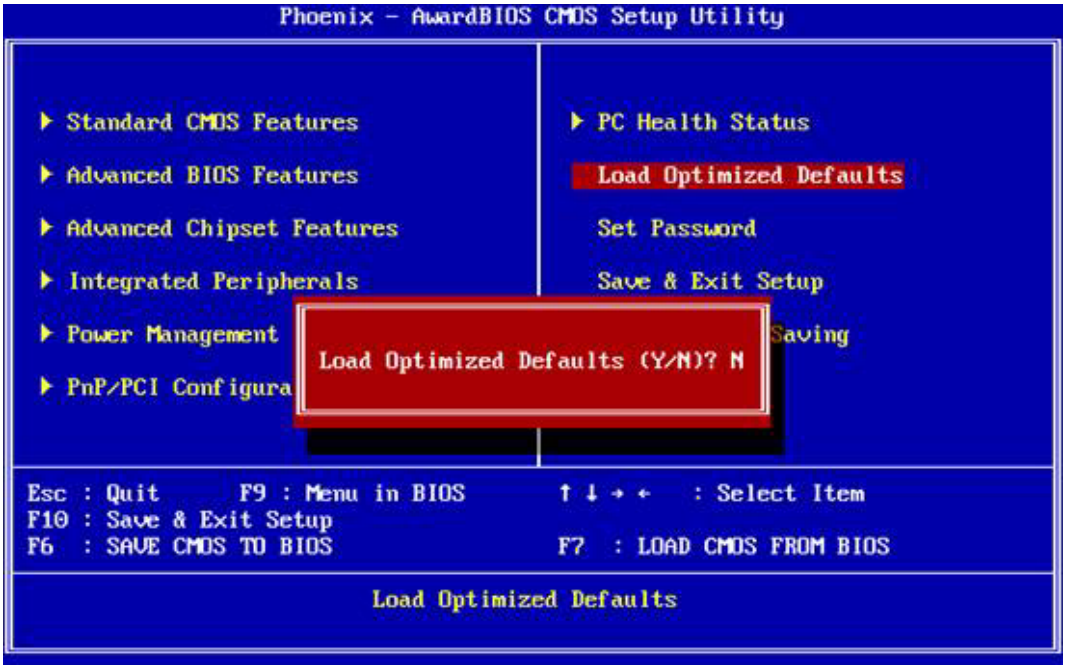


Figure 3.9 Load optimized defaults screen

The PCM-3353 automatically configures all setup items to optimal settings when you select this option. Optimal Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Defaults if your computer is experiencing system configuration problems. Select Load Optimal Defaults from the Exit menu and press <Enter>.

3.11 Password Setting

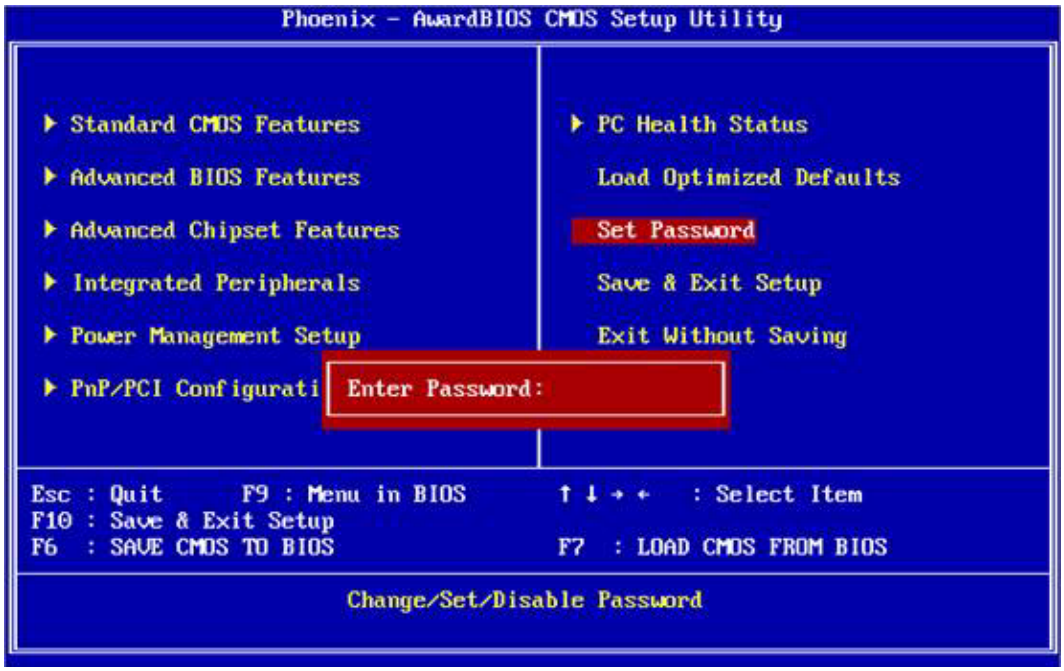


Figure 3.10 Password setting screen

To change the password:

1. Choose the “Set Password” option from the “Initial Setup Screen” menu and press <Enter>.

   The screen will display the following message.

   Press <Enter>.

2. If the CMOS is good or if this option has been used to change the default password, the user is asked for the password stored in the CMOS. The screen will display the following message:

   Enter the current password and press <Enter>.

3. After pressing <Enter> (ROM password) or the current password (user-defined), you can change the password stored in the CMOS. The password must be no longer than eight (8) characters.

   Remember, to enable the password setting feature, you must first select either “Setup” or “System” from the ”Advanced BIOS Features” menu.

3.12 Save & Exit Setup

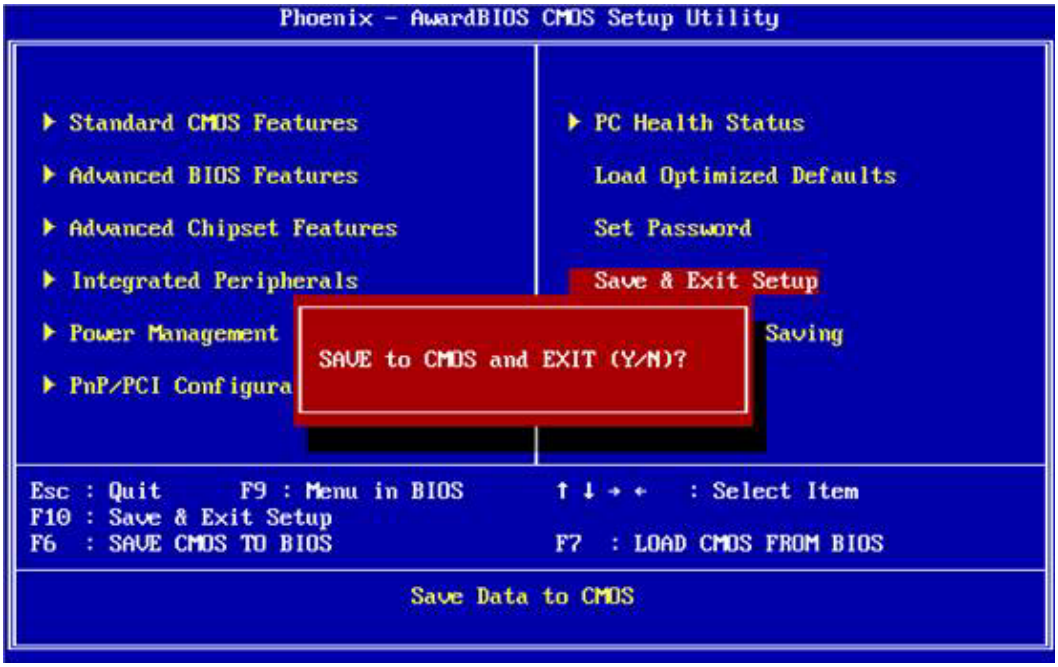


Figure 3.11 Save & exit setup screen

If you select this and press <Enter>, the values entered in the setup utilities will be recorded in the CMOS memory of the chipset. The microprocessor checks this every time you turn your system on and compares this to what it finds as it checks the system.

This record is required for the system to operate.

3.13 Exit without Saving

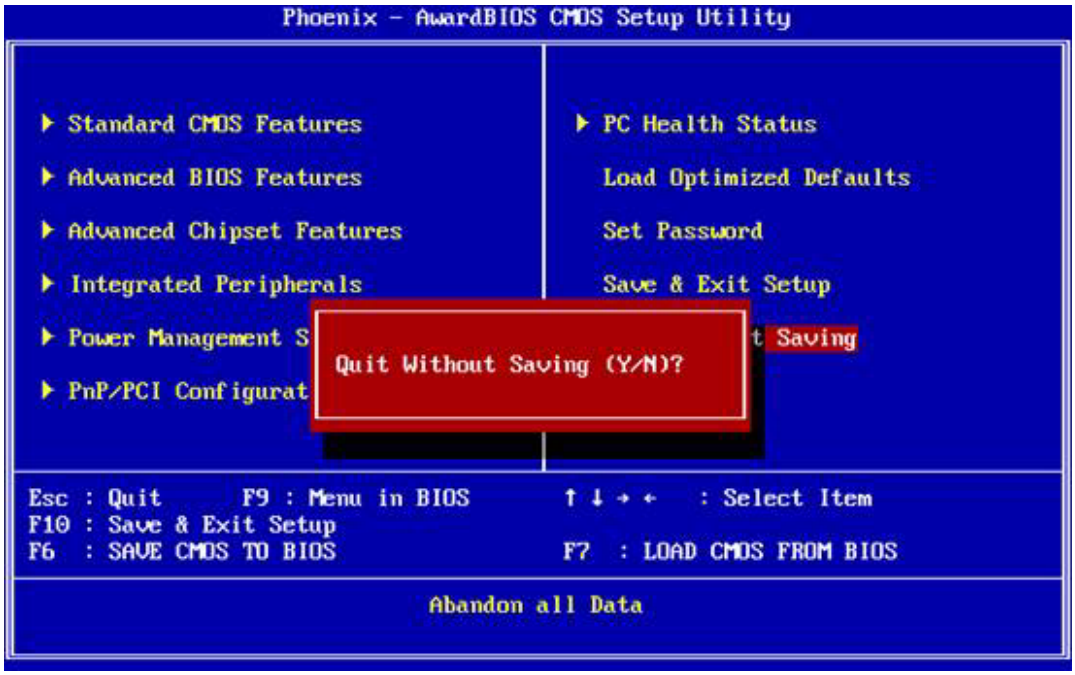


Figure 3.12 Exit without saving screen

Selecting this option and pressing <Enter> lets you exit the setup program without recording any new values or changing old ones.

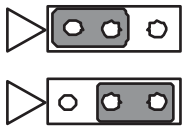
Appendix A

Pin Assignments

This appendix contains information of a detailed or specialized nature.

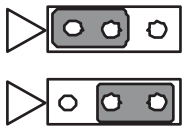
A.1 Jumper and Connector Tables

Table A.1: SW1, CF Master / Slave Selector



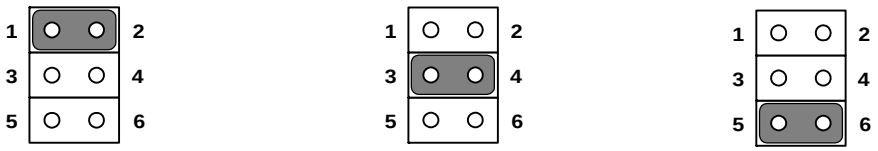
Part Number	1600000071
Footprint	JH2X1V-2M
Description	PIN HEADER 2*1P 180D (M)SQUARE 2.0mm
Setting	Function
(1 - 2)	Master (default)
(2 - 3)	Slave

Table A.2: J3, Clear CMOS



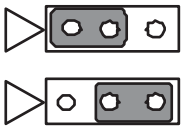
Part Number	1653003101
Footprint	JH3X1V-2M
Description	PIN HEADER 3*1P 180D (M)SQUARE 2.0mm
Setting	Function
(1 - 2)	BAT (default)
(2 - 3)	Clear-CMOS

Table A.3: CN39, COM2 Setting



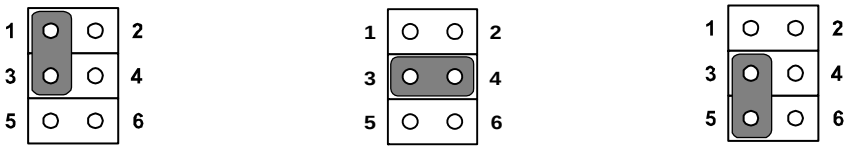
Part Number	1653003201
Footprint	JH3X2S-2M
Description	PIN HEADER 3*2P 180D SMDMALE SQUARE PIN 2.0mm
Setting	Function
(1 - 2)	RS232 (defualt)
(3 - 4)	RS485
(5 - 6)	RS422

Table A.4: J5, PCI VI/O POWER



Part Number	1653003101
Footprint	JH3X1V-2M
Description	PIN HEADER 3*1P 180D (M)SQUARE 2.0mm
Setting	Function
(1 - 2)	With +5 V
(2 - 3)	With +3.3 V (defualt)

Table A.5: J6, LVDS Power Selector



Part Number	1653003260
Footprint	HD_3x2P_79
Description	PIN HEADER 3*2P 180D (M) 2.0mm SMD SQUARE PIN
Setting	Function
(1 - 3)	+3.3 V (default)
(3 - 4)	+12 V
(3 - 5)	+5 V

Table A.6: CN42, LVDS LCD I/F

Part Number	1653910261		
Footprint	SPH10x2		
Description	*CONN. DF13-20DP-1.25V		
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	GND	GND	
3	D0+	I/O	
4	NONE		
5	D0-	I/O	
6	NONE		
7	D1+	I/O	
8	NONE		
9	D1-	I/O	
10	NONE		
11	D2+	I/O	

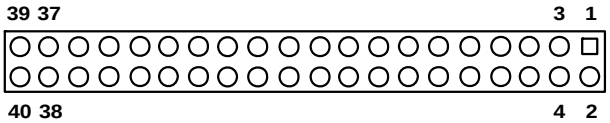
12	NONE		
13	D2-	I/O	
14	NONE		
15	CLK+	I/O	
16	D3+		
17	CLK-	I/O	
18	D3-		
19	+12 V/+5 V/+3.3 V	PWR	+12 V/+5 V/+3.3 V
20	+12 V/+5 V/+3.3 V	PWR	+12 V/+5 V/+3.3 V

Table A.7: CN38, Power Input



Part Number	1655308020		
Footprint	PWR-B4PV		
Description	PIN HEADER DIP 8*1P 180D(M) 2.00mm		
Pin	Pin Name	Signal Type	Signal Level
1	+5 V	PWR	+5 V
2	+5 V	PWR	+5 V
3	+5 V	PWR	+5 V
4	GND	GND	-
5	GND	GND	-
6	GND	GND	-
7	GND	GND	-
8	+12 V	PWR	+12 V

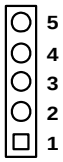
Table A.8: CN4, TFT LCD I/F



Part Number	1653920200		
Footprint	SPH20X2		
Description	*CONN. DF13-40DP-1.25V		
Pin	Pin Name	Signal Type	Signal Level
1	+5 V	PWR	+5 V
2	+5 V	PWR	+5 V
3	GND	GND	-
4	GND	GND	-
5	+3.3 V	PWR	+3.3 V

6	+3.3 V	PWR	+3.3 V
7	TV-CLK	CLK48M	+3.3 V
8	GND	GND	-
9	D0	I/O	+3.3 V
10	D1	I/O	+3.3 V
11	D2	I/O	+3.3 V
12	D3	I/O	+3.3 V
13	D4	I/O	+3.3 V
14	D5	I/O	+3.3 V
15	D6	I/O	+3.3 V
16	D7	I/O	+3.3 V
17	D8	I/O	+3.3 V
18	D9	I/O	+3.3 V
19	D10	I/O	+3.3 V
20	D11	I/O	+3.3 V
21	D12	I/O	+3.3 V
22	D13	I/O	+3.3 V
23	D14	I/O	+3.3 V
24	D15	I/O	+3.3 V
25	D16	I/O	+3.3 V
26	D17	I/O	+3.3 V
27	D18	I/O	+3.3 V
28	D19	I/O	+3.3 V
29	D20	I/O	+3.3 V
30	D21	I/O	+3.3 V
31	D22	I/O	+3.3 V
32	D23	I/O	+3.3 V
33	GND	GND	-
34	GND	GND	-
35	DOTCLK	CLK	+3.3 V
36	VS	OUT	+3.3 V
37	DE	I/O	+3.3 V
38	HS	OUT	+3.3 V
39	RST	OUT	+3.3 V
40	FP	OUT	+3.3 V

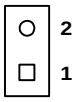
Table A.9: CN5, Inverter Power



Part Number	1655305020		
Footprint	WHL5V-2M		
Description	WAFER BOX 2.0mm 5P 180D MALE W/LOCK		
Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V

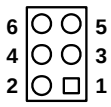
2	GND	GND	-
3	ENABKL	OUT	+3.3V
4	VBR	OD	+3.3V
5	+5V	PWR	+5V

Table A.10: CN6, SMBus



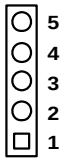
Part Number	1653002101		
Footprint	JH2X1V-2M		
Description	PIN HEADER 2*1P 180D (M)SQUARE 2.0mm		
Pin	Pin Name	Signal Type	Signal Level
1	SMB-CLK	CLK	+3 V
2	SMB-DAT	I/O	+3 V

Table A.11: CN32, Reset / Buzzer pin header



Part Number	1653002201		
Footprint	WHL2V-2M		
Description	PIN HEADER DIP 2*2P 180D(M) 2.00mm		
Pin	Pin Name	Signal Type	Signal Level
1	-	-	-
2	-	-	-
3	GND	GND	-
4	RST	IN	+3.3 V
5	Buzzer -	-	-
6	Buzzer +	-	-

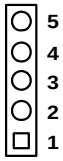
Table A.12: CN36, GPIO1



Part Number	1653010100		
Footprint	JH5X2S-2M		
Description	PIN HEADER SMD 5*1P 180D(M) 2.54mm		
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5 V

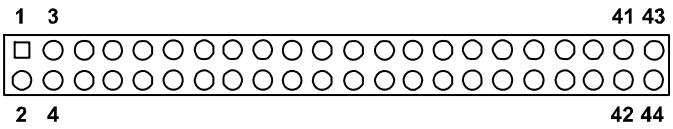
2	GPIO0	I/O	+5 V
3	GPIO1	I/O	+5 V
4	GPIO2	I/O	+5 V
5	GPIO3	I/O	+5 V

Table A.13: CN37, GPIO2



Part Number	1653010100		
Footprint	JH5X2S-2M		
Description	PIN HEADER SMD 5*1P 180D(M) 2.54mm		
Pin	Pin Name	Signal Type	Signal Level
1	GPIO4	I/O	+5 V
2	GPIO5	I/O	+5 V
3	GPIO6	I/O	+5 V
4	GPIO7	I/O	+5 V
5	GND	-	-

Table A.14: CN11, IDE



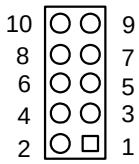
Part Number	1653222262		
Footprint	BH22X2SV		
Description	BOX HEADER SMD 22*2P 180D(M) 2.0mm IDIOT-PROOF		
Pin	Pin Name	Signal Type	Signal Level
1	RST#	Out	+5 V
2	GND	GND	-
3	D7	I/O	+5 V
4	D8	I/O	+5 V
5	D6	I/O	+5 V
6	D9	I/O	+5 V
7	D5	I/O	+5 V
8	D10	I/O	+5 V
9	D4	I/O	+5 V
10	D11	I/O	+5 V
11	D3	I/O	+5 V
12	D12	I/O	+5 V
13	D2	I/O	+5 V
14	D13	I/O	+5 V
15	D1	I/O	+5 V

16	D14	I/O	+5 V
17	D0	I/O	+5 V
18	D15	I/O	+5 V
19	GND	GND	-
21	DREQ	Out	+5 V
22	GND	GND	-
23	IOW#	Out	+5 V
24	GND	GND	-
25	IOR#	Out	+5 V
26	GND	GND	-
27	IORDY	Out	+5 V
28	CSEL#	Out	+5 V
29	DACK#	Out	+5 V
30	GND	GND	-
31	IRQ14	In	+5 V
32	NC	-	-
33	A1	In	+5 V
34	D66DET#	In	+5 V
35	A0	In	+5 V
36	A2	In	+5 V
37	CS#1	Out	+5 V
38	CS#3	Out	+5 V
39	ASP#	Out	+5 V
40	GND	GND	-
41	+5 V	PWR	+5 V
42	+5 V	PWR	+5 V
43	GND	GND	-
44	NC	-	-

Table A.15: CN27, CRT

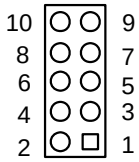
Part Number	1655912120		
Footprint	DBVGA-VF5M		
Description	CONN. 12P 90D(F) SMD 1.25mm		
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	-
2	R	OUT	Analog
3	G	OUT	Analog
4	B	OUT	Analog
5	GND	GND	-
6	+5 V	PWR	-
7	DDAT	OD I/O	+3.3 V
8	DCLK	OD I/O	+3.3 V
9	GND	GND	-
10	HSYNC	OUT	+3.3 V
11	VSYNC	OUT	+3.3 V
12	GND	-	-

Table A.16: CN15, USB1/2



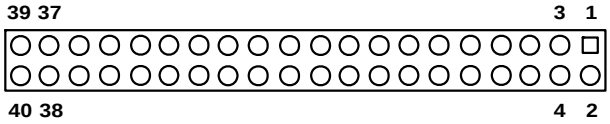
Part Number	1653005260		
Footprint	JH5X2S-2M		
Description	PIN HEADER 5*2P 180D(M) 2.0mm SMD IDIOT-PROOF		
Pin	Pin Name	Signal Type	Signal Level
1	+5 V	PWR	+5 V
2	+5 V	PWR	+5 V
3	P0-	I/O	USB
4	P1-	I/O	USB
5	P0+	I/O	USB
6	P1+	I/O	USB
7	GND	GND	-
8	GND	GND	-
9	GND	GND	-
10	NC	-	-

Table A.17: CN17, USB3/4



Part Number	1653005260		
Footprint	JH5X2S-2M		
Description	PIN HEADER 5*2P 180D(M) 2.0mm SMD IDIOT-PROOF		
Pin	Pin Name	Signal Type	Signal Level
1	+5 V	PWR	+5 V
2	+5 V	PWR	+5 V
3	P2-	I/O	USB
4	P3-	I/O	USB
5	P2+	I/O	USB
6	P3+	I/O	USB
7	GND	GND	-
8	GND	GND	-
9	GND	GND	-
10	NC	-	-

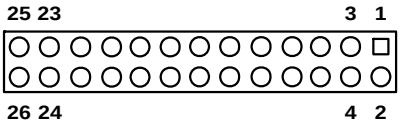
Table A.18: CN30, COM1/2/3/4



Part Number	1653220260		
Footprint	BH20X2SV-2.00mm		
Description			
Pin	Pin Name	Signal Type	Signal Level
1	DCD#1	IN	-3 ~ -12 V, +3 ~ +12 V
2	DSR#1	IN	-3 ~ -12 V, +3 ~ +12 V
3	RXD1	IN	-3 ~ -12 V, +3 ~ +12 V
4	RTS#1	I/O	-3 ~ -12 V, +3 ~ +12 V
5	TXD1	OUT	-3 ~ -12 V, +3 ~ +12 V
6	CTS#1	IN	-3 ~ -12 V, +3 ~ +12 V
7	DTR#1	I/O	-3 ~ -12 V, +3 ~ +12 V
8	RI#1	IN	-3 ~ -12 V, +3 ~ +12 V
9	GND	GND	-
10	GND	GND	-
11	DCD#2	In	-3~-12V, +3~+12V
12	DSR#2	In	-3~-12V, +3~+12V
13	RXD2	In	-3~-12V, +3~+12V
14	RTS#2	I/O	-3~-12V, +3~+12V
15	TXD2	Out	-3~-12V, +3~+12V
16	CTS#2	In	-3~-12V, +3~+12V
17	DTR#2	I/O	-3~-12V, +3~+12V
18	RI#2	In	-3~-12V, +3~+12V
19	GND	GND	-
20	GND	GND	-
21	DCD#3	In	-3 ~ -12 V, +3 ~ +12 V
22	DSR#3	In	-3 ~ -12 V, +3 ~ +12 V
23	RXD3	In	-3 ~ -12 V, +3 ~ +12 V
24	RTS#3	I/O	-3 ~ -12 V, +3 ~ +12 V
25	TXD3	Out	-3 ~ -12 V, +3 ~ +12 V
26	CTS#3	In	-3 ~ -12 V, +3 ~ +12 V
27	DTR#3	I/O	-3 ~ -12 V, +3 ~ +12 V
28	RI#3	In	-3 ~ -12 V, +3 ~ +12 V
29	GND	GND	-
30	GND	GND	-
31	DCD#4	In	-3 ~ -12 V, +3 ~ +12 V
32	DSR#4	In	-3 ~ -12 V, +3 ~ +12 V
33	RXD4	In	-3 ~ -12 V, +3 ~ +12 V
34	RTS#4	I/O	-3 ~ -12 V, +3 ~ +12 V
35	TXD4	Out	-3 ~ -12 V, +3 ~ +12 V
36	CTS#4	In	-3 ~ -12 V, +3 ~ +12 V
37	DTR#4	I/O	-3 ~ -12 V, +3 ~ +12 V
38	RI#4	In	-3 ~ -12 V, +3 ~ +12 V

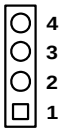
39	GND	GND	-
40	GND	-	-

Table A.19: CN19, Print Port



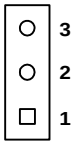
Part Number	1653213260		
Footprint	BH13x2SV-2.00		
Description	BOX HEADER SMD 13*2P 180D(M) 2.0mm		
Pin	Pin Name	Signal Type	Signal Level
1	STB#	Out	+5 V
2	AFD#	Out	+5 V
3	PD0	I/O	+5 V
4	ERR#	In	+5 V
5	PD1	I/O	+5 V
6	INIT#	Out	+5 V
7	PD2	I/O	+5 V
8	SLIN#	Out	+5 V
9	PD3	I/O	+5 V
10	GND	GND	-
11	PD4	I/O	+5 V
12	GND	GND	-
13	PD5	I/O	+5 V
14	GND	GND	-
15	PD6	I/O	+5 V
16	GND	GND	-
17	PD7	I/O	+5
18	GND	GND	-
19	ACK#	In	+5 V
20	GND	GND	-
21	BUSY	In	+5 V
22	GND	GND	-
23	PE	In	+5 V
24	GND	GND	-
25	SLCT	In	+5 V
26	NC	-	-

Table A.20: CN20, RS422/485



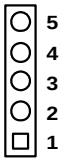
Part Number	1653004101		
Footprint	JH4X1V-2M		
Description	PIN HEADER 4*1P 180D(M) SQUARE 2.0mm		
Pin	Pin Name	Signal Type	Signal Level
1	422-RXD-	In	+5 V
2	422-RXD+	In	+5 V
3	485-422-TXD+	Out	+5 V
4	485-422-TXD-	Out	+5 V

Table A.21: CN35, AUDIO-OUT



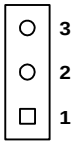
Part Number	1655303120		
Footprint	WHL3V-2M		
Description	WAFER BOX 2.0mm 3P 180D w/LOCK		
Pin	Pin Name	Signal Type	Signal Level
1	LIN-OUT-R	OUT	Analog
2	GND	GND	-
3	LIN-OUT-L	Out	Analog

Table A.22: CN34, AUDIO-IN



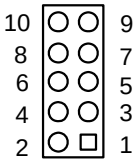
Part Number	1653005020		
Footprint	WHL3V-2M		
Description	WAFER BOX 2.0 mm 5P 180D w/LOCK		
Pin	Pin Name	Signal Type	Signal Level
1	LIN-IN-R	IN	Analog
2	GND	GND	-
3	LIN-IN-L	IN	Analog
4	GND	GND	-
5	MIC-IN	IN	Analog

Table A.23: CN23, ISA -5V & -12V Input



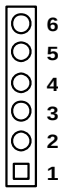
Part Number	1653003101		
Footprint	JH3X1V-2M		
Description	PIN HEADER 3*1P 180D (M)SQUARE 2.0 mm		
Pin	Pin Name	Signal Type	Signal Level
1	-12 V	PWR	-12 V
2	-5 V	PWR	-5 V
3	GND	GND	-

Table A.24: CN26, LAN1



Part Number	1653205260		
Footprint	BH5X2SV		
Description	BOX HEADER SMD 5*2 180D (M) 2.0 mm		
Pin	Pin Name	Signal Type	Signal Level
1	+3.3 V	PWR	+3.3 V
2	LAN2-ACTLED	IN	Analog
3	LAN2-RX+	IN	Analog
4	LAN2-RX-	IN	Analog
5	LAN2-LILED	IN	Analog
6	LAN2-LCT	I/O	Analog
7	N/A	-	-
8	LAN2-LCT	I/O	Analog
9	LAN2-TX+	OUT	Analog
10	LAN2-TX-	OUT	Analog

Table A.25: CN18, KB/MS



Part Number	1655306020		
Footprint	BH5X2SV		
Description	BOX HEADER DIP 6*1 180D (M) 2.0 mm		
Pin	Pin Name	Signal Type	Signal Level
1	KB-CLK	IN	+5 V
2	KB-DATA	IN	+5 V
3	MS-CLK	IN	+5 V
4	GND	PWR	-
5	+5 V	PWR	+5 V
6	MS-DATA	IN	+5 V

Table A.26: CN40, DDR RAM SOCKET

Part Number	1651000051
Footprint	
Description	SODIMM 200P DDR SMD

Table A.27: CN41, CF SOCKET

Part Number	1653025211
Footprint	JH5X2S-2M
Description	HEADER 50P 90D

Table A.28: CN33, Battery Connector

Part Number	1655902032		
Footprint	WHL2V-125		
Description	WAFER 2P 180D(M) 1.25 mm 53047-0210		
Pin	Pin Name	Signal Type	Signal Level
1	+VBAT	PWR	+3.3 V
2	GND	GND	+5 V

Appendix B

System Assignments

This appendix contains information of a detailed nature.

B.1 System I/O Ports

Table B.1: System I/O Ports

Addr. range (Hex)	Device
000-01F	DMA controller
020-021	Interrupt controller 1, master
040-05F	8254 timer
060-06F	8042 (keyboard controller)
070-07F	Real-time clock, non-maskable interrupt (NMI) mask
080-09F	DMA page register
0A0-0BF	Interrupt controller 2
0C0-0DF	DMA controller
0F0	Clear math co-processor
0F1	Reset math co-processor
0F8-0FF	Math co-processor
1F0-1F8	Fixed disk
200-207	Reserved (Game I/O)
278-27F	Reserved (Parallel port 2,LTP3)
2E8-2EF	Reserved (Series port 4)
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1 (LPT 2)
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and printer adapter (LPT1)
3C0-3CF	Reserved
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Reserved (Series port 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1

* PNP audio I/O map range from 220 ~ 250H (16 bytes)
  MPU-401 select from 300 ~ 330H (2 bytes)

B.2 1st MB Memory Map

Table B.2: 1st MB Memory Map

Addr. range (Hex)	Device
F0000h - FFFFFh	System ROM
*CC000h - EFFFFh	Unused (reserved for Ethernet ROM)
C0000h - CBFFFh	Expansion ROM (for VGA BIOS)
B8000h - BFFFFh	CGA/EGA/VGA text
B0000h - B7FFFh	Unused
A0000h - AFFFFh	EGA/VGA graphics
00000h - 9FFFFh	Base memory

Table B.2: 1st MB Memory Map	
Addr. range (Hex)	**Device**
* If Ethernet boot ROM is disabled (Ethernet ROM occupies about 16 KB)	
* E0000 - EFFFF is reserved for BIOS POST	

B.3 DMA Channel Assignments

Table B.3: DMA Channel Assignments	
Channel	**Function**
0	Available
1	Available (audio)
2	Floppy disk (8-bit transfer)
3	Available (parallel port)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available
* Audio DMA select 1, 3, or 5	
** Parallel port DMA select 1 (LPT2) or 3 (LPT1)	

B.4 Interrupt Assignments

Table B.4: Interrupt Assignments	
Interrupt#	**Interrupt source**
IRQ 0	Interval timer
IRQ 1	Keyboard
IRQ 2	Interrupt from controller 2 (cascade)
IRQ 3	COM2
IRQ 4	COM1
IRQ 5	Reserved (COM4)
IRQ 6	FDD
IRQ 7	LPT1
IRQ 8	RTC
IRQ 9	Reserved (audio)
IRQ 10	Reserved (COM3)
IRQ 11	Reserved for watchdog timer
IRQ 12	PS/2 mouse
IRQ 13	INT from co-processor
IRQ 14	Primary IDE
IRQ 15	Secondary IDE for CFC
* Ethernet interface IRQ select: 9, 11, 15 * PNP audio IRQ select: 9, 11, 15 * PNP USB IRQ select: 9, 11, 15 * PNP ACPI IRQ select: 9, 11, 15	

Appendix C

Watchdog Timer Sample Code

C.1 Watchdog Function

```
;The SCH3114 Runtime base I/O address is 800h
;Setting WatchDog time value location at offset 66h
;If set value "0", it is mean disable WatchDog function.
Superio_GPIO_Port = 800h
mov dx,Superio_GPIO_Port + 66h
mov al,00h
out dx,al
.model small
.486p
.stack 256
.data
SCH3114_IO EQU 800h
.code
org 100h
.STARTup
;================================================
;47H
;enable WDT function bit [0]=0Ch
;================================================
mov dx,SCH3114_IO + 47h
mov al,0Ch
out dx,al
;================================================
;65H
;bit [1:0]=Reserved
;bit [6:2]Reserve=00000
;bit [7] WDT time-out Value Units Select
;Minutes=0 (default) Seconds=1
;================================================
mov dx,SCH3114_IO + 65h ;
mov al,080h
out dx,al
;================================================
;66H
;WDT timer time-out value
;bit[7:0]=0~255
;================================================
mov dx,SCH3114_IO + 66h
mov al,01h
out dx,al
;================================================
;bit[0] status bit R/W
;WD timeout occurred =1
;WD timer counting = 0
```

```
;=================================================
mov dx,SCH3114_IO + 68h
mov al,01h
out dx,al
.exit
END
```

Appendix D

GPIO Sample Code

D.1 GPIO Sample Code

```
;=============================================================
===
    NEWIODELAY Macro
            out  0ebh,al
            ENDM
;=============================================================
====
            .model small
            .486p
            .stack 256
            .data
;=============================================================
====
;               Data Area
;=============================================================
====
     SMBus_Port       EQU6000h
     PCA9555_ID         EQU  4Eh
     Input_Reg          EQU  00h
     Output_Reg         EQU  01h
     Inversion_Reg      EQU  02h
     Configure_Reg      EQU  03h
     Advantech_Str      db  'Advantech Company Copyright (C) 2005 Design by Dun-
can',0AH,0Dh,'$'
     Advantech_Str      db  'Advantech Company Copyright (C) 2005 Design by Dun-
can, Modify by Steven',0AH,0Dh,'$'
     GX3_Fun_Str        db  'Check Philip GPIO function.',0Ah,0Dh,'$'
     Note1_Str          db  'Test Method: GPIO 0 connect to GPIO 1.',0Ah,0Dh,'$'
     Note2_Str          db  '             GPIO 2 connect to GPIO 3.',0Ah,0Dh,'$'
     Note3_Str          db  '             GPIO 4 connect to GPIO 5.',0Ah,0Dh,'$'
     Note4_Str          db  '             GPIO 6 connect to GPIO 7.',0Ah,0Dh,'$'
     Success1_Str       db  'First GPIO Chip Test success !!  ',0Ah,0Dh,'$'
     Success2_Str       db  'Second GPIO Chip Test success !! ',0Ah,0Dh,'$'
Success_lenght  EQU     ($ - offset Success1_Str) / 2
                    db  'Third GPIO Chip Test success !!  ',0Ah,0Dh,'$'
                    db  'Fouth GPIO Chip Test success !!  ',0Ah,0Dh,'$'
                    db  'Fifth GPIO Chip Test success !!  ',0Ah,0Dh,'$'
                    db  'Sixth GPIO Chip Test success !!  ',0Ah,0Dh,'$'
                    db  'Seventh GPIO Chip Test success !!',0Ah,0Dh,'$'
                    db  'Eighth GPIO Chip Test success !! ',0Ah,0Dh,'$'
     Fail_Str           db  'First GPIO Chip Test Fail !!  ',0Ah,0Dh,'$'
     Fail2_Str          db  'Second GPIO Chip Test Fail !! ',0Ah,0Dh,'$'
Fail_lenght     EQU     ($ - offset Fail_Str) / 2
                    db  'Third GPIO Chip Test Fail !!  ',0Ah,0Dh,'$'
                    db  'Fouth GPIO Chip Test Fail !!  ',0Ah,0Dh,'$'
```

```
                    db  'Fifth GPIO Chip Test Fail !!  ',0Ah,0Dh,'$'
                    db  'Sixth GPIO Chip Test Fail !!  ',0Ah,0Dh,'$'
                    db  'Seventh GPIO Chip Test Fail !!',0Ah,0Dh,'$'
                    db  'Eighth GPIO Chip Test Fail !! ',0Ah,0Dh,'$'
    Error_Str1      db  'Error !! The system has no GPIO Chip or no support INT15
hook! ',0Ah,0Dh,'$'

;================================================================
====
;           Main Program Start
;================================================================
====

.code
             org    100h
 .STARTup
            ;Clear Screen
             pusha
             lea    dx, Advantech_Str
             mov    ah,09h
             int    21h
             lea    dx, GX3_Fun_Str
             mov    ah,09h
             int    21h
             lea    dx, Note1_Str
             mov    ah,09h
             int    21h
             lea    dx, Note2_Str
             mov    ah,09h
             int    21h
             lea    dx, Note3_Str
             mov    ah,09h
             int    21h
             lea    dx, Note4_Str
             mov    ah,09h
             int    21h
;================================================================
====
;     Get Number of GPIO group
;     one group mean 8 gpio pins(one GPIO Chip)
; Input:
;     ax=5E87h
;     bh=00h
; output:
;     ax=5E78       ;function success, other value means function fail
;     cl= n group of gpio
```

```
;=============================================================
====

;=============================================================
====
;       Get GPIO Config
; Input:
;       ax=5E87h
;       bh=01h
;       cl= n ; n means which group of GPIO you want to get
; output:
;       ax=5E78         ;function success, other value means function fail
;       bl= the n group of gpio config
;          bit 0 = gpio 0 , 0 => output pin; 1 => input pin
;          bit 1 = gpio 1 , 0 => output pin; 1 => input pin
;              .....
;          bit 7 = gpio 7 , 0 => output pin; 1 => input pin
;=============================================================
====

;=============================================================
====
;       Set GPIO Config
; Input:
;       ax=5E87h
;       bh=02h
;       cl= n ; n means which group of GPIO you want to set
;       bl= the n group of gpio config
;          bit 0 = gpio 0 , 0 => output pin; 1 => input pin
;          bit 1 = gpio 1 , 0 => output pin; 1 => input pin
;              .....
;          bit 7 = gpio 7 , 0 => output pin; 1 => input pin
; output:
;       ax=5E78         ;function success, other value means function fail
;=============================================================
====

;=============================================================
====
;       Get GPIO status
; Input:
;       ax=5E87h
;       bh=03h
;       cl= n ; n means which group of GPIO you want to get
; output:
;       ax=5E78         ;function success, other value means function fail
```

```
;       bl= the n group of gpio status
;          bit 0 = gpio 0 , 0 => Low; 1 => High
;          bit 1 = gpio 1 , 0 => Low; 1 => High
;             .....
;          bit 7 = gpio 7 , 0 => Low; 1 => High
;================================================================
====

;================================================================
====
;       Set GPIO status
; Input:
;       ax=5E87h
;       bh=04h
;       cl= n ; n means which group of GPIO you want to set
;       bl= the n group of gpio status
;          bit 0 = gpio 0 , 0 => Low; 1 => High
;          bit 1 = gpio 1 , 0 => Low; 1 => High
;             .....
;          bit 7 = gpio 7 , 0 => Low; 1 => High
; output:
;       ax=5E78         ;function success, other value means function fail
;================================================================
================
              mov     ax,5e87h
              mov     bh,00h
              int     15h
              cmp     ax,5e78h
              je      next_test

              lea     dx, Error_Str1
              mov     ah,09h
              int     21h
              jmp     Finish_Test
next_test:
              xor     ch,ch
              push    cx              ;save NO. of GPIO chip
          ;1.Set GPIO 0,2,4,6 as output, GPI 1,3,5,7 as input
              mov     ax,5e87h
              mov     bx,02aah
              int     15h
          ;2. Set GPIO 0,2,4,6 Output Low
              pop     cx              ;restore  NO. of GPIO chip
              push    cx              ;save NO. of GPIO chip
              mov     ax,5e87h
              mov     bx,0400h
```

```
    int     15h
;3. Check GPI 1,3,5,7 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,03FFh
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,00
    jne     test_result


;4. Set GPIO 0,2,4,6 Output differential
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0411h
    int     15h
;5. Check GPI 1,3,5,7 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,03FFh
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,33h
    jne     test_result

    cmp     al,00h
```

```
    jne    test_fail
;4.Set GPIO 1,3,5,7 as output,GPIO 0,2,4,6 as input
    pop     cx
    push    cx
    mov     ax,5e87h
    mov     bx,0255h
    int     15h
;4. Set GPIO 1,3,5,7 Output High
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,04ffh
    int     15h
;6. Check GPIO 0,2,4,6 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0300h
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,0ffh
    jne     test_result


;4. Set GPIO 1,3,5,7 Output differential
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0422h
    int     15h
;5. Check GPI 0,2,4,6 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,03FFh
    int     15h
```

```
                pop     cx              ;restore  NO. of GPIO chip
                push    cx              ;save NO. of GPIO chip
                dec     cx

                mov     al,Fail_lenght
                mul     cl
                lea     dx, Fail_Str
                add     dx,ax
                cmp     bl,33h
                jne    test_result

                pop     cx              ;restore  NO. of GPIO chip
                push    cx              ;save NO. of GPIO chip
                dec     cx
                mov     al,Success_lenght
                mul     cl
                lea     dx, Success1_Str
                add     dx,ax

            ;Do Second PCA9554 test
            ;1.Set GPIO 0,2,4,6 as output, GPI 1,3,5,7 as input

test_result:
                mov     ah,09h
                int     21h
                pop     cx
                dec     cx
                jnz     next_test
    Finish_Test:
                popa
                .exit
;=============================================================
;Input     : CL - register index
;            CH - device ID
;Output : AL - Value read
;=============================================================
Ct_I2CReadByteProcNear

                    push  cx

                    mov   dx,SMBus_Port +04h
                    inc     ch
                    mov   al,ch                 ;ID cmd(read)
                    out     dx,al
                    NEWIODELAY
```

```
                NEWIODELAY

                call    CT_Chk_SMBus_Ready

                pop     ax
                mov     dl,03h
                out     dx,al           ;Index
                NEWIODELAY
                NEWIODELAY

                mov     dl,02h
                mov     al,48h
                out     dx,al           ;Read data
                NEWIODELAY
                NEWIODELAY

                mov     cx, 100h

        @@:
                newiodelay
                loop    short @B

                call    CT_Chk_SMBus_Ready

                mov     dl,05
                in      al,dx           ;Data0
                NEWIODELAY
                NEWIODELAY

                ret
Ct_I2CReadByteEndp
;============================================================
;Input : CL - register index
;        CH - device ID
;        AL - Value to write
;Output: none
;============================================================
Ct_I2CWriteByteProcNear

                push    ax
                push    cx

                mov     dx,SMBus_Port +04h
                mov     al,ch           ;ID cmd(Write)
                out     dx,al
```

```
                call    Delay5ms
                call    Delay5ms

                call    CT_Chk_SMBus_Ready

                pop     ax
                mov     dl,03h
                out     dx,al           ;Index
                call    Delay5ms
                call    Delay5ms

                pop     ax
                mov     dl,05
                out     dx,al           ;Data0
                call    Delay5ms
                call    Delay5ms

                mov     dl,02h
                mov     al,48h
                out     dx,al           ;write data
                call    Delay5ms
                call    Delay5ms

                mov     cx, 100h
        @@:
                newiodelay
                loop    short @B

                call    CT_Chk_SMBus_Ready

                ret
Ct_I2CWriteByteEndp
CT_Chk_SMBus_ReadyProcNear
                mov     dx,SMBus_Port + 0;status port
                clc
                mov     cx,0800h
Chk_I2c_OK:
                in      al,dx       ;get status
                NEWIODELAY
                out     dx,al       ;clear status
                NEWIODELAY

                test    al, 02H     ;termination of command ?
                jnz     short Clear_final
```

```
                and   al, NOT 40H;mask INUSE bit
                or    al,al         ;status OK ?
                jz    short Clear_final

                test  al,04h        ;device error
                jnz   short SMBus_Err

                loop  short Chk_I2c_OK
          ;SMbus error due to timeout
SMBus_Err:

                stc
                ret
Clear_final:
                clc
                ret
CT_Chk_SMBus_ReadyEndp


;;=============================================================
===
Delay5msprocnear
                push  cx
                mov   cx, 1000
          @@:
                NEWIODELAY
                loop  short @B
                pop   cx
                ret
Delay5ms       ENDP
Phoenix_debuger  proc near
             pushf
             push cx
             push offset PhdebugRetAddr
             push cs
             push cs
             db 0EAh
             dw 0013h
             dw 0DA00h
PhdebugRetAddr:
             popf
Phoenix_debuger  endp
;=============================================================
====
;          Program  END
```

```
;=============================================================================

        END
```

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